

January 1997

**NOT RECOMMENDED
FOR NEW DESIGNS**
Use CMOS Technology

BiCMOS FCT Interface Logic, Octal D Flip-Flop with Reset

Features

- Buffered Inputs
- Typical Propagation Delay: 5.3ns at $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50pF$
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at $V_{CC} = 5V$
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------|------------------|------------|----------|
| CD74FCT273E | 0 to 70 | 20 Ld PDIP | E20.3 |
| CD74FCT273M | 0 to 70 | 20 Ld SOIC | M20.3 |

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

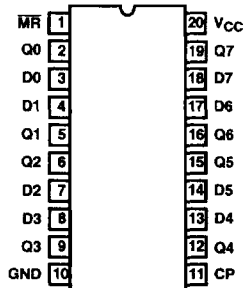
Description

The CD74FCT273 octal D flip-flop with reset uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC} . This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

Information at the D input of the CD74FCT273 is transferred to the Q output on the positive going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and common reset (\overline{MR}). Resetting is accomplished by a low voltage level independent of the clock.

Pinout

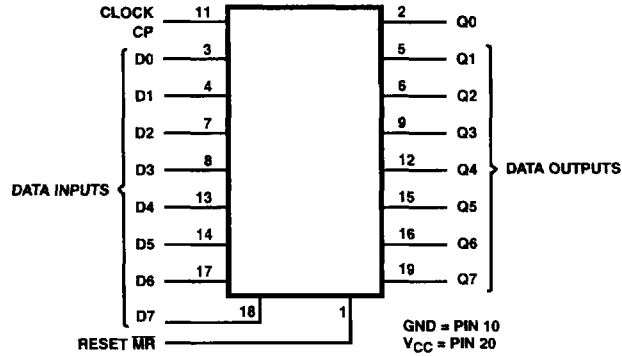
CD74FCT273
(PDIP, SOIC)
TOP VIEW



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BICMOS FCT
PRODUCTS

CD74FCT273

Functional Diagram



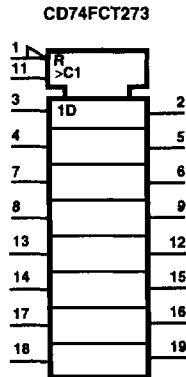
TRUTH TABLE (Note 1)

| INPUTS | | | OUTPUTS |
|----------|----------|---------|---------|
| RESET MR | CLOCK CP | DATA Dn | Qn |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | Q0 |

NOTE:

- H = HIGH Voltage Level (Steady State)
 L = LOW Voltage Level (Steady State)
 X = Irrelevant
 ↑ = Transition from low to high level.
 Q0 = The level of Q before the indicated steady state input conditions were established.

IEC Logic Symbol



CD74FCT273

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage (V_{CC}) | -0.5V to 6V |
| DC Input Diode Current, I_{IK} (For $V_I < -0.5V$) | -20mA |
| DC Output Diode Current, I_{OK} (for $V_O < -0.5V$) | -50mA |
| DC Output Sink Current per Output Pin, I_O | 70mA |
| DC Output Source Current per Output Pin, I_O | -30mA |
| DC V_{CC} Current (I_{CC}) | 140mA |
| DC Ground Current (I_{GND}) | 400mA |

Thermal Information

| | |
|--|------------------------------------|
| Thermal Resistance (Typical, Note 2) | θ_{JA} ($^{\circ}C/W$) |
| PDIP Package | 135 |
| SOIC Package | 125 |
| Maximum Junction Temperature | 150 $^{\circ}C$ |
| Maximum Storage Temperature Range | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$ |
| (SOIC-Lead Tips Only) | |

Operating Conditions

| | |
|--|---------------------------------|
| Operating Temperature Range (T_A) | 0 $^{\circ}C$ to 70 $^{\circ}C$ |
| Supply Voltage Range, V_{CC} | 4.75V to 5.25V |
| DC Input Voltage, V_I | 0 to V_{CC} |
| DC Output Voltage, V_O | 0 to $\leq V_{CC}$ |
| Input Rise and Fall Slew Rate, dt/dv | 0 to 10ns/V |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 5)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | AMBIENT TEMPERATURE (T_A) | | | | UNITS |
|--|-----------------|-------------------------|------------|--------------|-------------------------------|------|---------------------------------|------|---------|
| | | V_I (V) | I_O (mA) | | 25 $^{\circ}C$ | | 0 $^{\circ}C$ TO 70 $^{\circ}C$ | | |
| | | | | | MIN | MAX | MIN | MAX | |
| High Level Input Voltage | V_{IH} | | | 4.75 to 5.25 | 2 | - | 2 | - | V |
| Low Level Input Voltage | V_{IL} | | | 4.75 to 5.25 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage | V_{OH} | V_{IH} or V_{IL} | -15 | Min | 2.4 | - | 2.4 | - | V |
| Low Level Output Voltage | V_{OL} | V_{IH} or V_{IL} | 48 | Min | - | 0.55 | - | 0.55 | V |
| High Level Input Current | I_{IH} | V_{CC} | | Max | - | 0.1 | - | 1 | μA |
| Low Level Input Current | I_{IL} | GND | | Max | - | -0.1 | - | -1 | μA |
| Three State Leakage Current | I_{OZH} | V_{CC} | | Max | - | 0.5 | - | 10 | μA |
| | I_{OZL} | GND | | Max | - | -0.5 | - | -10 | μA |
| Input Clamp Voltage | V_{IK} | V_{CC} or GND | -18 | Min | - | -1.2 | - | -1.2 | V |
| Short Circuit Output Current (Note 3) | I_{OS} | $V_O = 0 V_{CC}$ or GND | | Max | -60 | - | -60 | - | mA |
| Quiescent Supply Current, MSI | I_{CC} | V_{CC} or GND | 0 | Max | - | 8 | - | 80 | μA |
| Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load | ΔI_{CC} | 3.4V (Note 4) | | Max | - | 1.6 | - | 1.6 | mA |

NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at V_{CC} or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. at 70 $^{\circ}C$.

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BICMOS FCT PRODUCTS

CD74FCT273

Switching Specifications Over Operating Range FCT Series $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L (Figure 4) (Note 6)

| PARAMETER | SYMBOL | V_{CC} (V) | 25°C | 0°C TO 70°C | | UNITS |
|-------------------------------|----------------------|--------------|------|-------------|-----|-------|
| | | | TYP | MIN | MAX | |
| Propagation Delays | | | | | | |
| CP to Qn | t_{PLH}, t_{PHL} | 5 | 7 | 2 | 13 | ns |
| \overline{MR} to Qn | t_{PLH}, t_{PHL} | 5 | 8 | 2 | 13 | ns |
| Power Dissipation Capacitance | C_{PD} (Note 7) | - | 36 | - | - | pF |
| Input Capacitance | C_I | - | - | - | 10 | pF |

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.

7. C_{PD} , measured per flip-flop, is used to determine the dynamic power consumption.

$$P_D \text{ (per package)} = V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_i C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D) \text{ where:}$$

V_{CC} = supply voltage

ΔI_{CC} = flow through current x unit load

C_L = output load capacitance

D = duty cycle of input high

f_O = output frequency

f_i = input frequency

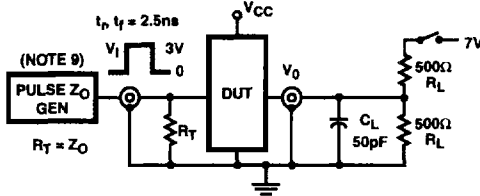
Prerequisite for Switching (Note 8)

| PARAMETER | SYMBOL | V_{CC} (V) | 25°C | 0°C TO 70°C | | UNITS |
|-------------------------------------|-----------|--------------|------|-------------|-----|-------|
| | | | TYP | MIN | MAX | |
| Data to CP Setup Time | t_{SU} | 5 | - | 3 | - | ns |
| Hold Time | t_H | 5 | - | 2 | - | ns |
| Removal Time, \overline{MR} to CP | t_{REM} | 5 | - | 4 | - | ns |
| \overline{MR} Pulse Width | t_W | 5 | - | 7 | - | ns |
| CP Pulse Width | t_W | 5 | - | 7 | - | ns |
| CP Frequency | f_{MAX} | 5 | - | 70 | - | MHz |

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

- 9. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$; $t_r, t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

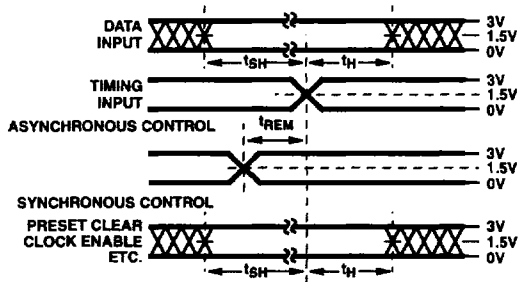


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

| SWITCH POSITION | |
|--------------------------------------|--------|
| TEST | SWITCH |
| t_{PLZ}, t_{PZL} , Open Drain | Closed |
| $t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$ | Open |

DEFINITIONS:

- C_L = Load capacitance, includes jig and probe capacitance.
- R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.
- $V_{IN} = 0\text{V}$ to 3V .
- Input: $t_r = t_f = 2.5\text{ns}$ (10% to 90%), unless otherwise specified

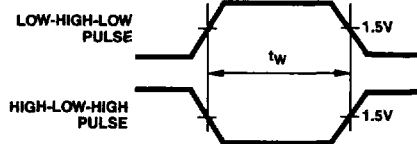


FIGURE 3. PULSE WIDTH

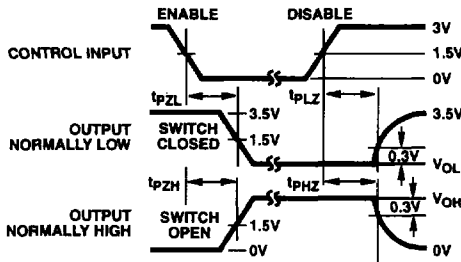


FIGURE 4. ENABLE AND DISABLE TIMING

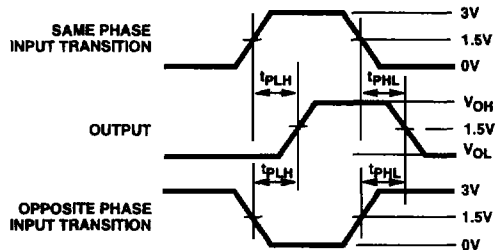
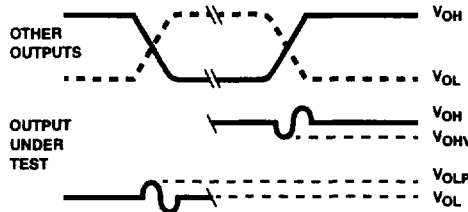


FIGURE 5. PROPAGATION DELAY



NOTES:

- 10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH} .
- 11. Input pulses have the following characteristics: $P_{RR} \leq 1\text{MHz}$, $t_r = 2.5\text{ns}$, $t_f = 2.5\text{ns}$, skew 1ns .
- 12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with $0.1\mu\text{F}$ capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

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