



# PSMN013-100BS

N-channel 100V 13.9mΩ standard level MOSFET in D2PAK

21 February 2014

Product data sheet

## 1. General description

Standard level N-channel MOSFET in D2PAK package qualified to 175°C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

## 3. Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

## 4. Quick reference data

Table 1. Quick reference data

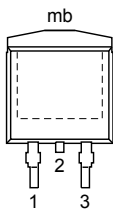
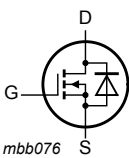
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	-	100	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 2</a>	[1]	-	-	68	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>		-	-	170	W
$T_j$	junction temperature			-55	-	175	°C
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 100\text{ °C};$ <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	19.4	25	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 13</a>		-	10.8	13.9	mΩ
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 50\text{ V};$ <a href="#">Fig. 15</a> ; <a href="#">Fig. 14</a>		-	17	23.8	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 50\text{ V};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	59	83	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 68\text{ A}$ ; $V_{\text{sup}} \leq 100\text{ V}$ ; unclamped; $R_{GS} = 50\text{ }\Omega$	-	-	127	mJ

[1] Continuous current is limited by package

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>D2PAK (SOT404)</b></p>	 <p>mbb076</p>
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN013-100BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN013-100BS	PSMN013-100BS

## 8. Limiting values

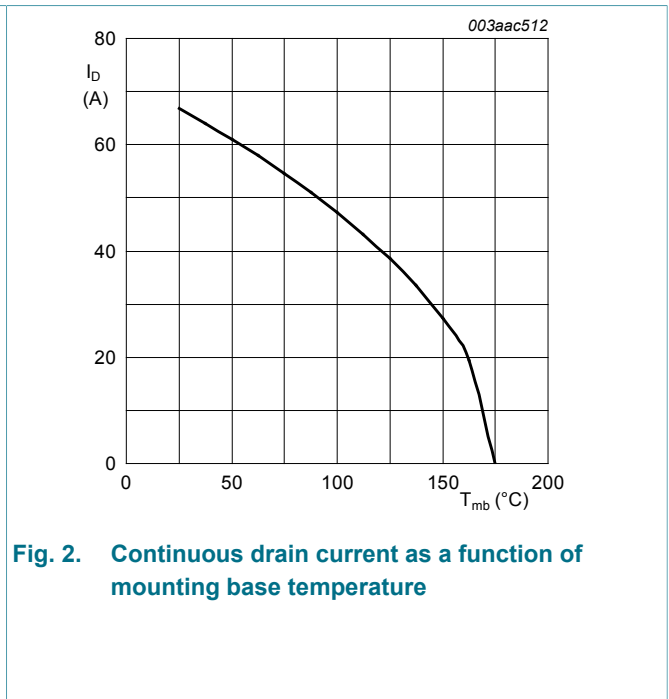
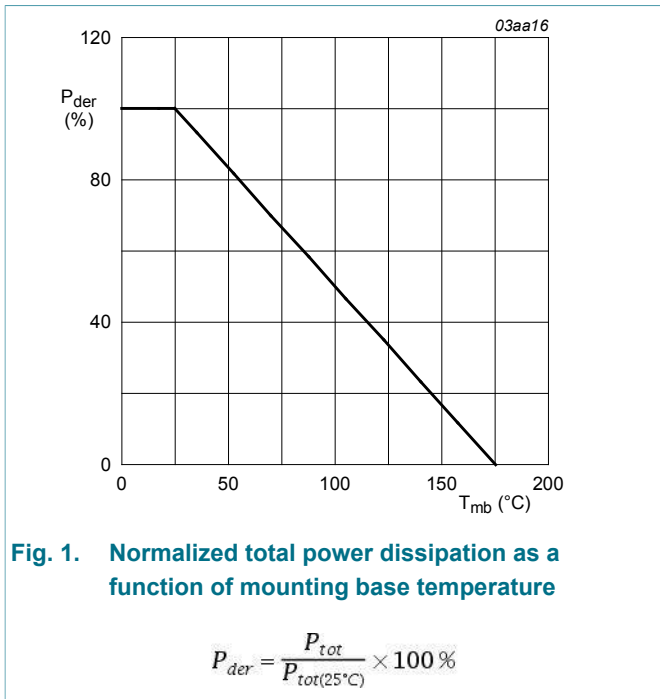
Table 5. Limiting values

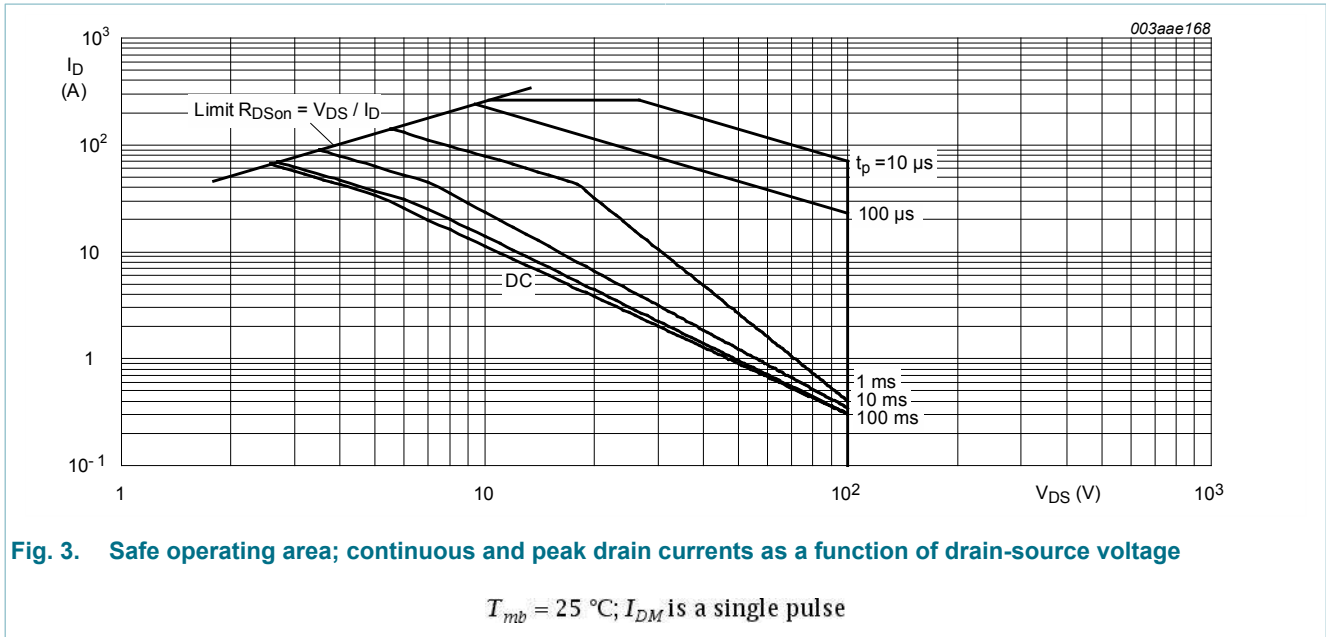
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$T_j \leq 175\text{ °C}$ ; $T_j \geq 25\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	100	V

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	170	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 2</a>	[1]	-	47	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	[1]	-	68	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 3</a>		-	272	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	68	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	272	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 68 A; V <sub>sup</sub> ≤ 100 V; unclamped; R <sub>GS</sub> = 50 Ω		-	127	mJ

[1] Continuous current is limited by package

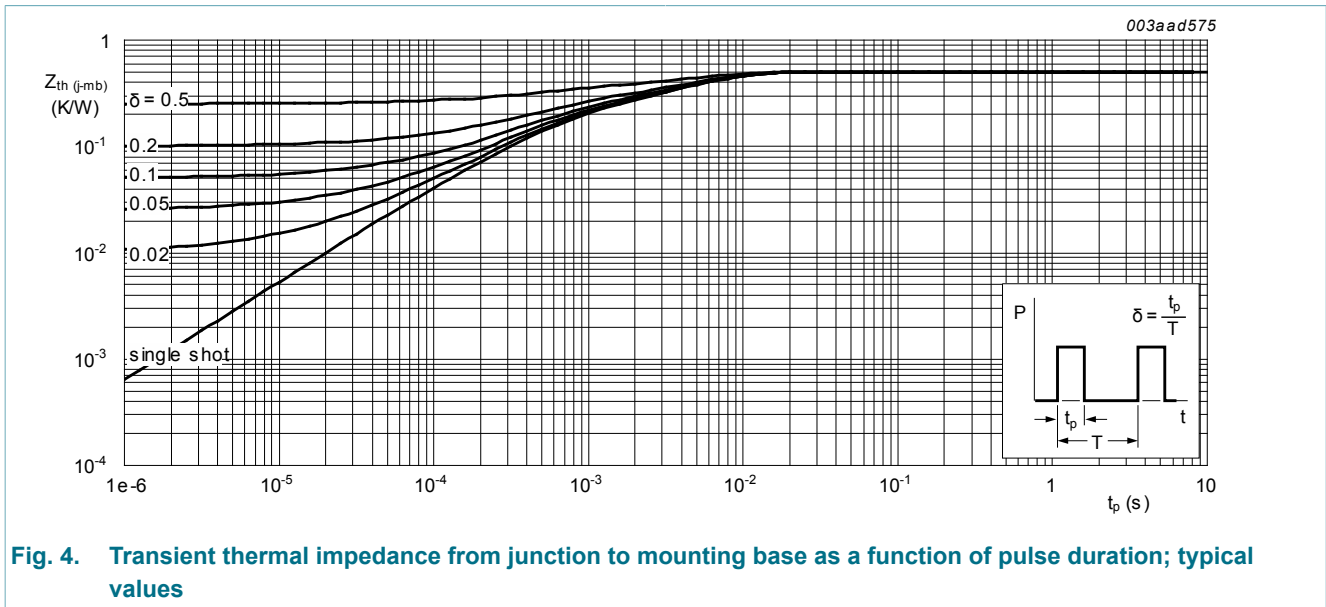




## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.5	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	50	-	K/W



## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	90	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 10; Fig. 11</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	-	4.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.06	2	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ <a href="#">Fig. 12; Fig. 13</a>	-	19.4	25	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 12; Fig. 13</a>	-	29.5	38.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13</a>	-	10.8	13.9	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	0.5	1	2	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 14; Fig. 15</a>	-	59	83	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	47.6	66.7	nC
$Q_{GS}$	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 14; Fig. 15</a>	-	13.8	19.4	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ <a href="#">Fig. 15; Fig. 14</a>	-	9.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.6	-	nC
$Q_{GD}$	gate-drain charge		-	17	23.8	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 50 \text{ V};$ <a href="#">Fig. 15; Fig. 14</a>	-	4.4	-	V
$C_{iss}$	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	3195	4315	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	221	300	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{rss}$	reverse transfer capacitance		-	136	191	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}; R_L = 2\ \Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 4.7\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	20.7	31.1	ns
$t_r$	rise time		-	25	37.5	ns
$t_{d(off)}$	turn-off delay time		-	52.5	78.8	ns
$t_f$	fall time		-	24	36	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; dI_S/dt = 100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	52	68	ns
$Q_r$	recovered charge	$V_{DS} = 50\text{ V}$	-	109	142	nC

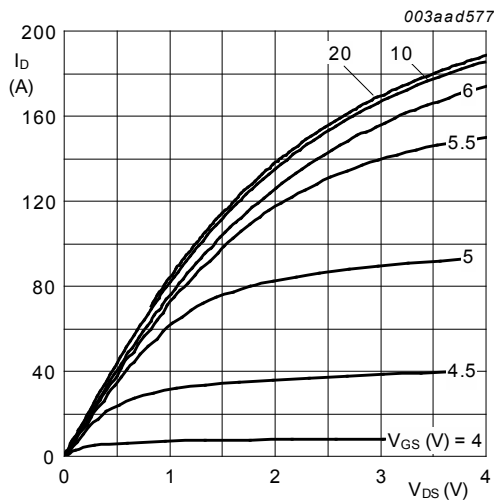


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

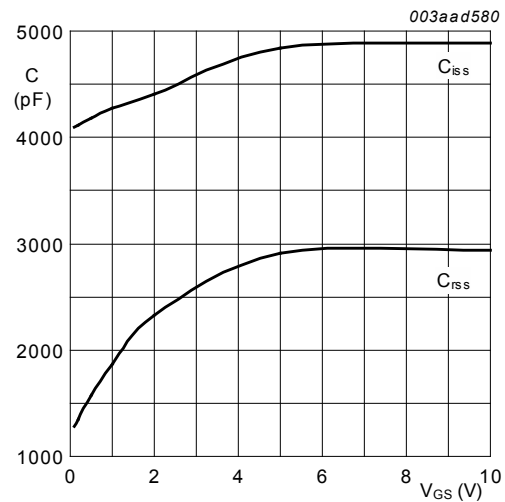


Fig. 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

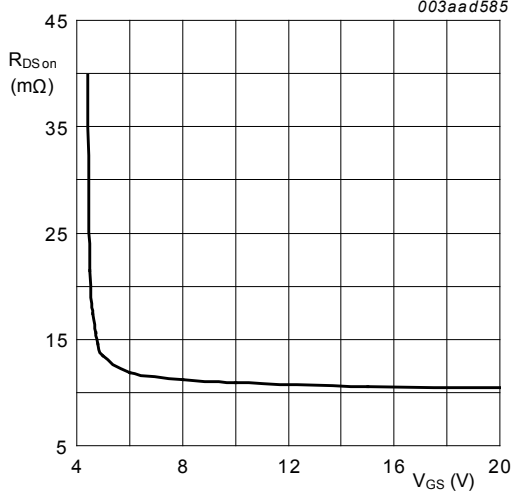


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_J = 25^\circ\text{C}$

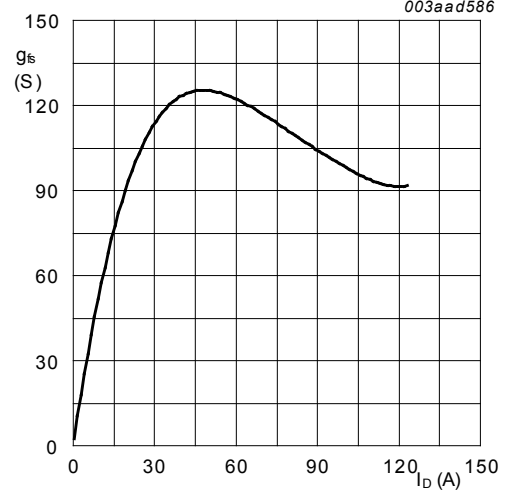


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_J = 25^\circ\text{C}; V_{DS} = 15\text{V}$

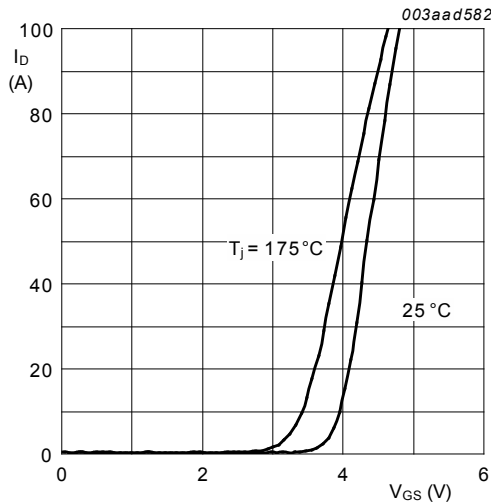


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DS(on)}$

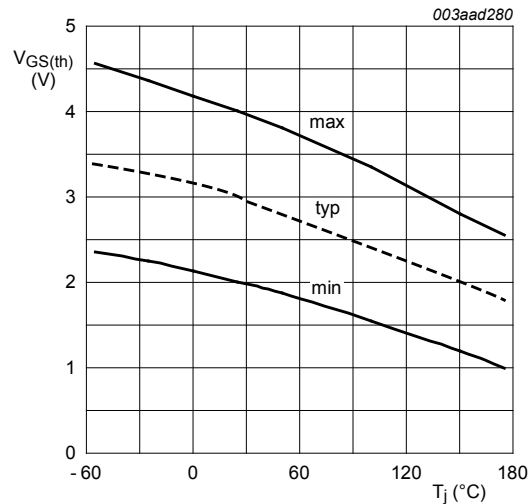
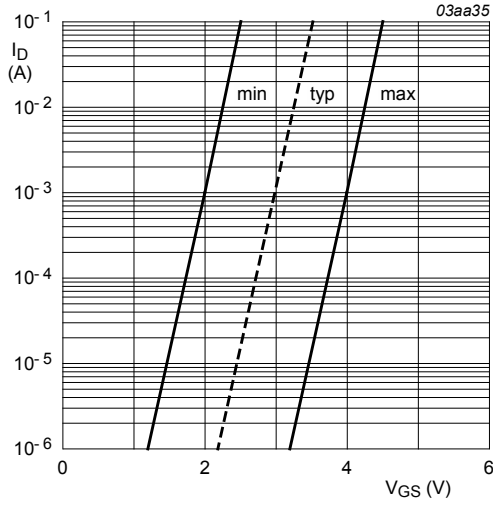


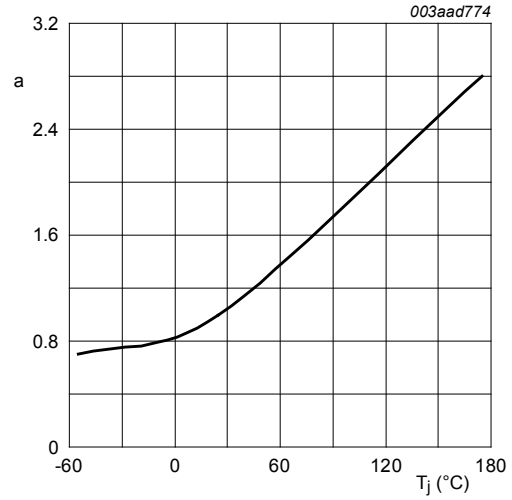
Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$



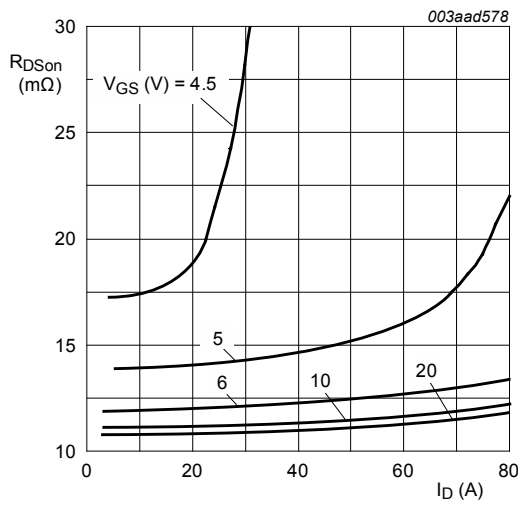
**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$



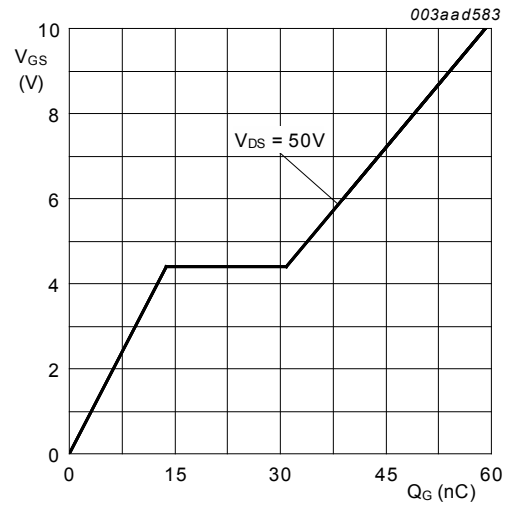
**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$



**Fig. 13. Drain-source on-state resistance as a function of drain current; typical values**

$$T_j = 25^\circ\text{C}$$



**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$



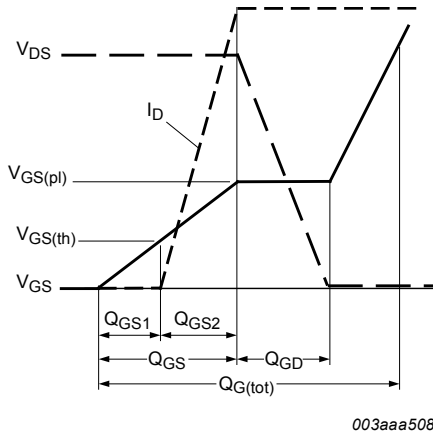


Fig. 15. Gate charge waveform definitions

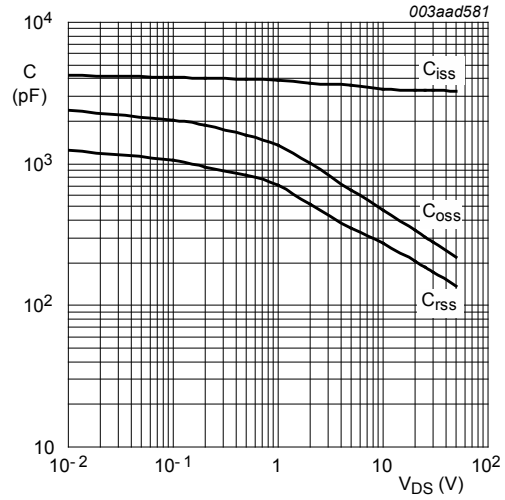


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

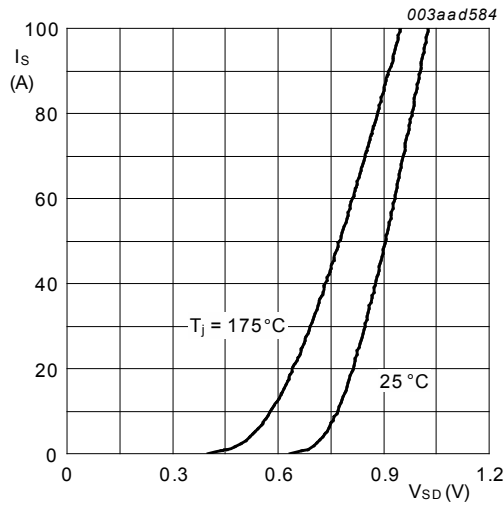
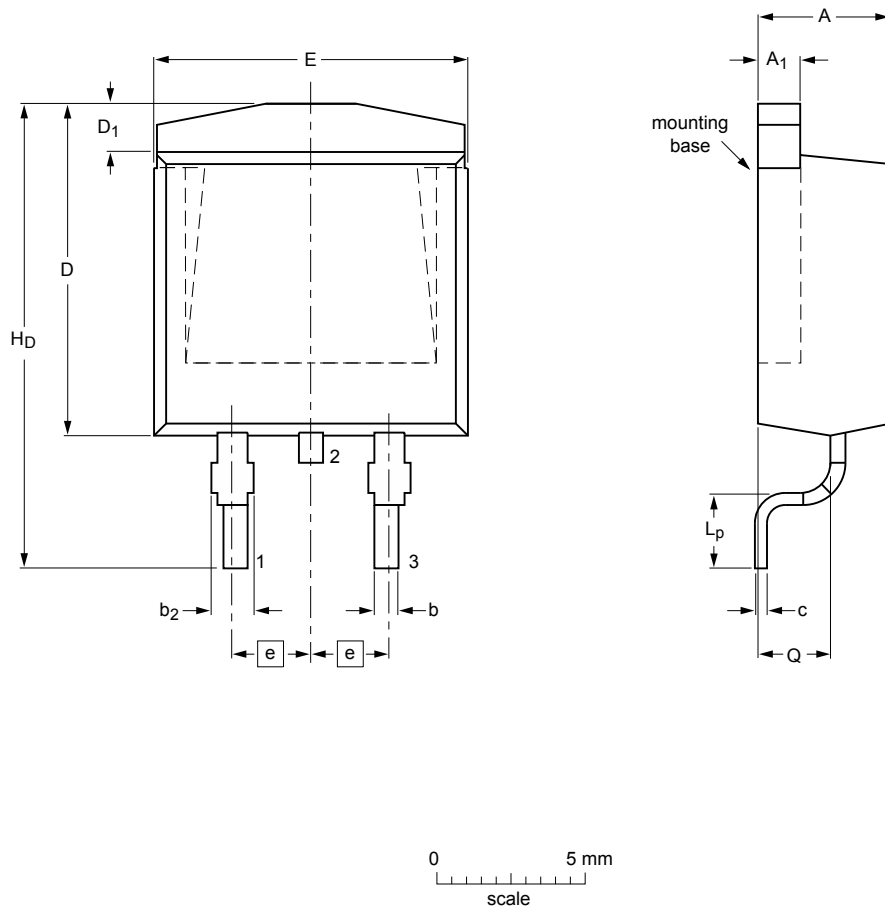


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

### 11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	H <sub>D</sub>	L <sub>p</sub>	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 18. Package outline D2PAK (SOT404)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 21 February 2014