

# UCC21732-Q1 10-A Source/Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection, Isolated Analog Sensing and High-CMTI

## 1 Features

- 5.7-kV<sub>RMS</sub> single channel isolated gate driver
- AEC-Q100 qualified for automotive applications
- SiC MOSFETs and IGBTs up to 2121V<sub>pk</sub>
- 33-V maximum output drive voltage (VDD-VEE)
- ±10-A drive strength and split output
- 150-V/ns minimum CMTI
- 270ns response time fast overcurrent protection
- External active miller clamp
- Internal 2-level turn-off when fault happens
- Isolated analog sensor with PWM output for
  - Temperature sensing with NTC, PTC or thermal diode
  - High voltage DC-Link or phase voltage
- Alarm  $\overline{\text{FLT}}$  on over current and reset from  $\overline{\text{RST/EN}}$
- Fast enable/disable response on  $\overline{\text{RST/EN}}$
- Reject <40ns noise transient and pulse on input pins
- 12V VDD UVLO with power good on RDY
- Inputs/outputs with over/under-shoot transient voltage Immunity up to 5 V
- 130-ns (maximum) propagation delay and 30-ns (maximum) pulse/part skew
- SOIC-16 DW package with creepage and clearance distance > 8mm
- Operating junction temperature –40°C to 150°C

## 2 Applications

- Traction inverter for EVs
- On-board charger and charging pile
- DC/DC Converter for HEV/EVs

## 3 Description

The UCC21732-Q1 is a galvanic isolated single channel gate driver designed for SiC MOSFETs and IGBTs up to 2121-V DC operating voltage with advanced protection features, best-in-class dynamic performance and robustness. UCC21732-Q1 has up to ±10-A peak source and sink current.

The input side is isolated from the output side with SiO<sub>2</sub> capacitive isolation technology, supporting up to 1.5-kV<sub>RMS</sub> working voltage, 12.8-kV<sub>PK</sub> surge immunity with longer than 40 years Isolation barrier life, as well as providing low part-to-part skew, >150V/ns common mode noise immunity (CMTI).

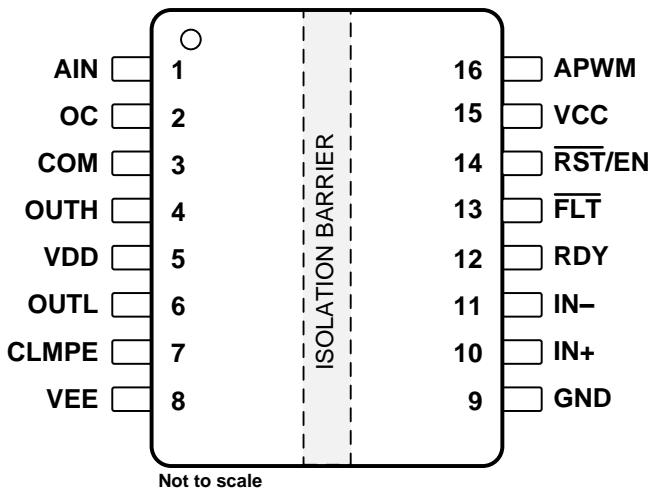
The UCC21732-Q1 includes the state-of-art protection features, such as fast overcurrent and short circuit detection, shunt current sensing support, fault reporting, active miller clamp, input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness. The isolated analog to PWM sensor can be utilized for easier temperature or voltage sensing, further increasing the drivers' versatility and simplifying the system design effort, size and cost.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC21732-Q1	DW SOIC-16	10.3 mm × 7.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Device Pin Configuration



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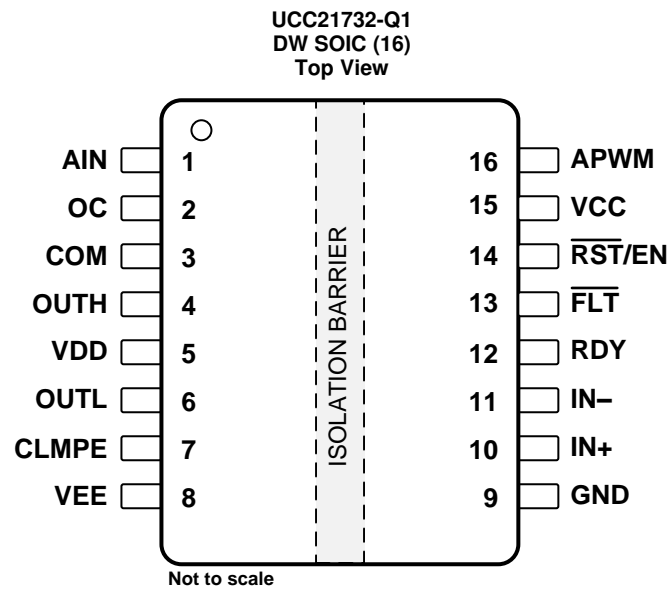
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (April 2019) to Revision B</b>	<b>Page</b>
• Changed marketing status from Advance Information to Production Data .....	<b>1</b>

<b>Changes from Original (February 2019) to Revision A</b>	<b>Page</b>
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## 5 Pin Configuration and Functions



**Table 1. Pin Functions**

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
AIN	1	I	Isolated analog sensing input, parallel a small capacitor to COM for better noise immunity
OC	2	I	Over current detection pin, support lower threshold for SenseFET, DESAT, and Shunt resistor sensing
COM	3	P	Common ground reference, connecting to emitter pin for IGBT and source pin for SiC-MOSFET
OUTH	4	O	Gate driver output pull up
VDD	5	P	Positive supply rail for gate drive voltage, Bypassing a >220nF capacitor to COM to support specified gate driver source peak current capability
OUTL	6	O	Gate driver output pull down
CLMPE	7	O	External Active miller clamp, connecting this pin to the gate of the external miller clamp MOSFET
VEE	8	P	Negative supply rail for gate drive voltage. Bypassing a >220nF capacitor to COM to support specified gate driver sink peak current capability
GND	9	P	Input power supply and logic ground reference
IN+	10	I	Non-inverting gate driver control input
IN-	11	I	Inverting gate driver control input
RDY	12	O	Power good for VCC-GND and VDD-COM. RDY is open drain configuration and can be paralleled with other RDY signals
$\overline{\text{FLT}}$	13	O	Active low fault alarm output upon over current or short circuit. $\overline{\text{FLT}}$ is in open drain configuration and can be paralleled with other faults
$\overline{\text{RST/EN}}$	14	I	The $\overline{\text{RST/EN}}$ serves two purposes: 1) Enable / shutdown of the output side. The FET is turned off by a general turn-off, if terminal EN is set to low; 2) Resets the OC condition signaled on $\overline{\text{FLT}}$ pin. if terminal $\overline{\text{RST/EN}}$ is set to low for more than 1000ns. A reset of signal $\overline{\text{FLT}}$ is asserted at the rising edge of terminal $\overline{\text{RST/EN}}$ . For automatic RESET function, this pin only serves as an EN pin. Enable / shutdown of the output side. The FET is turned off by a general turn-off, if terminal EN is set to low.
VCC	15	P	Input power supply from 3V to 5.5V, bypassing a >100nF capacitor to GND
APWM	16	O	Isolated Analog Sensing PWM output

(1) P = Power, G = Ground, I = Input, O = Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER		MIN	MAX	UNIT	
VCC	VCC – GND	–0.3	6	V	
VDD	VDD – COM	–0.3	36	V	
VEE	VEE – COM	–17.5	0.3	V	
V <sub>MAX</sub>	VDD – VEE	–0.3	36	V	
IN+, IN–, $\overline{\text{RST}}/\text{EN}$		DC	GND–0.3	VCC	V
		Transient, less than 100 ns <sup>(2)</sup>	GND–5.0	VCC+5.0	V
AIN	Reference to COM	–0.3	5	V	
OC	Reference to COM	–0.3	6	V	
OUTH, OUTL		DC	VEE–0.3	VDD	V
		Transient, less than 100 ns <sup>(2)</sup>	VEE–5.0	VDD+5.0	V
CLMPE	Reference to VEE	–0.3	5	V	
RDY, $\overline{\text{FLT}}$ , APWM		GND–0.3	VCC	V	
I <sub><math>\overline{\text{FLT}}</math></sub> , I <sub>RDY</sub>	$\overline{\text{FLT}}$ , and RDY pin input current		20	mA	
I <sub>APWM</sub>	APWM pin output current		20	mA	
T <sub>J</sub>	Junction temperature range	–40	150	°C	
T <sub>stg</sub>	Storage temperature range	–65	150	°C	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Values are verified by characterization on bench.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per AEC Q100-011	±1500

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT	
VCC	VCC–GND	3.0	5.5	V	
VDD	VDD–COM	13	33	V	
V <sub>MAX</sub>	VDD–VEE	–	33	V	
IN+, IN–, $\overline{\text{RST}}/\text{EN}$	Reference to GND	High level input voltage	0.7×VCC	VCC	V
		Low level input voltage	0	0.3×VCC	
AIN	Reference to COM	0.6	4.5	V	
t <sub>RST/EN</sub>	Minimum pulse width that reset the fault	1000		ns	
T <sub>A</sub>	Ambient Temperature	–40	125	°C	
T <sub>J</sub>	Junction temperature	–40	150	°C	

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC21732-Q1	UNIT
		DW (SOIC)	
		16	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	68.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

**Thermal Information (continued)**

THERMAL METRIC <sup>(1)</sup>		UCC21732-Q1	UNIT
		DW (SOIC)	
		16	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	14.1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	32.3	°C/W

**6.5 Power Ratings**

PARAMETER		TEST CONDITIONS	Value	UNIT
$P_D$	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 150kHz, 50% Duty Cycle for 10nF load, T <sub>a</sub> =25°C	985	mW
$P_{D1}$	Maximum power dissipation by transmitter side		20	mW
$P_{D2}$	Maximum power dissipation by receiver side		965	mW

## 6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
<b>GENERAL</b>				
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (Internal clearance) of the double insulation (2 × 0.0085 mm)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage Category per IEC 60664-1	Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 1000 V <sub>RMS</sub>	I-III	
<b>DIN V VDE V 0884-11 (VDE V 0884-11):2017-01<sup>(2)</sup></b>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDb) test	1500	V <sub>RMS</sub>
		DC voltage	2121	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> =V <sub>IOTM</sub> , t = 60 s (qualification test)	8000	V <sub>PK</sub>
		V <sub>TEST</sub> =1.2 × V <sub>IOTM</sub> , t = 1 s (100% production test)	9600	
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 62368-1, 1.2/50 µs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 12800 V <sub>PK</sub> (qualification)	8000	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> = 2545 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> = 3394 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> = 3977 V <sub>PK</sub> , t <sub>m</sub> = 1 s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.5 sin (2πft), f = 1 MHz	~ 1	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	≥ 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	≥ 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	≥ 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL 1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 5700 V <sub>RMS</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 6840 V <sub>RMS</sub> , t = 1 s (100% production)	5700	V <sub>RMS</sub>

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
- (2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device

### 6.7 Safety-Related Certifications

VDE	UL	CSA	CQC	TUV
Plan to certify according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01; DIN EN 61010-1 (VDE 0411-1):2011-07	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 60601-1	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013
Reinforced insulation Maximum transient isolation voltage, 8000 V <sub>PK</sub> ; Maximum repetitive peak isolation voltage, 2121 V <sub>PK</sub> ; Maximum surge isolation voltage, 8000 V <sub>PK</sub>	Single protection, 5700 V <sub>RMS</sub>	Isolation Rating of 5700 V <sub>RMS</sub> ; Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 (2nd Ed.), 1450 V <sub>RMS</sub> max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V <sub>RMS</sub> (354 V <sub>PK</sub> ) max working voltage	Reinforced Insulation, Altitude ≤ 5000m, Tropical climate, 400 V <sub>RMS</sub> maximum working voltage	5700 V <sub>RMS</sub> Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 1000 V <sub>RMS</sub> 5700 V <sub>RMS</sub> Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 1450 V <sub>RMS</sub>
Certification Planned	Certification Planned	Certification Planned	Certification Planned	Certification Planned

### 6.8 Safety Limiting Values

The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance. These limits vary with the ambient temperature, the junction-to-air thermal resistance, and the power supply voltages in different applications.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub> Safety input, output, or supply current	R <sub>θJA</sub> = 68.3°C/W, V <sub>DD</sub> = 15V, V <sub>EE</sub> = -5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			91	mA
	R <sub>θJA</sub> = 68.3°C/W, V <sub>DD</sub> = 20V, V <sub>EE</sub> = -5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			73	
P <sub>S</sub> Safety input, output, or total power	R <sub>θJA</sub> = 68.3°C/W, V <sub>DD</sub> = 20V, V <sub>EE</sub> = -5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1830	mW
T <sub>S</sub> Safety temperature				150	°C



## 6.9 Electrical Characteristics

VCC=3.3V or 5.0V, 1uF capacitor from VCC to GND, VDD-COM=20V, 18V or 15V, COM-VEE =0V, 5V, 8V or 15V, CL=100pF, -40°C<TJ<150°C (unless otherwise noted)<sup>(1)(2)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VCC UVLO THRESHOLD AND DELAY</b>						
V <sub>VCC_ON</sub>	VCC-GND		2.55	2.7	2.85	V
V <sub>VCC_OFF</sub>			2.35	2.5	2.65	
V <sub>VCC_HYS</sub>				0.2		
t <sub>VCCFIL</sub>	VCC UVLO Deglitch time			10		μs
t <sub>VCC+ to OUT</sub>	VCC UVLO on delay to output high	IN+ = VCC, IN- = GND	28	37.8	50	
t <sub>VCC- to OUT</sub>	VCC UVLO off delay to output low		5	10	15	
t <sub>VCC+ to RDY</sub>	VCC UVLO on delay to RDY high	RST/EN = VCC	30	37.8	50	
t <sub>VCC- to RDY</sub>	VCC UVLO off delay to RDY low		5	10	15	
<b>VDD UVLO THRESHOLD AND DELAY</b>						
V <sub>VDD_ON</sub>	VDD-COM		10.5	12.0	12.8	V
V <sub>VDD_OFF</sub>			9.9	10.7	11.8	
V <sub>VDD_HYS</sub>				0.8		
t <sub>VDDFIL</sub>	VDD UVLO Deglitch time			5		μs
t <sub>VDD+ to OUT</sub>	VDD UVLO on delay to output high	IN+ = VCC, IN- = GND	2	5	8	
t <sub>VDD- to OUT</sub>	VDD UVLO off delay to output low		5	10	15	
t <sub>VDD+ to RDY</sub>	VDD UVLO on delay to RDY high	RST/EN = FLT=High		10	15	
t <sub>VDD- to RDY</sub>	VDD UVLO off delay to RDY low		10	15	15	
<b>VCC, VDD QUIESCENT CURRENT</b>						
I <sub>VCCQ</sub>	VCC quiescent current	OUT(H) = High, f <sub>S</sub> = 0Hz, AIN=2V	2.5	3	4	mA
		OUT(L) = Low, f <sub>S</sub> = 0Hz, AIN=2V	1.45	2	2.75	
I <sub>VDDQ</sub>	VDD quiescent current	OUT(H) = High, f <sub>S</sub> = 0Hz, AIN=2V	3.6	4	5.9	mA
		OUT(L) = Low, f <sub>S</sub> = 0Hz, AIN=2V	3.1	3.7	5.3	
<b>LOGIC INPUTS — IN+, IN- and RST/EN</b>						
V <sub>INH</sub>	Input high threshold	V <sub>CC</sub> =3.3V		1.85	2.31	V
V <sub>INL</sub>	Input low threshold	V <sub>CC</sub> =3.3V	0.99	1.52		V
V <sub>INHYS</sub>	Input threshold hysteresis	V <sub>CC</sub> =3.3V		0.33		V
I <sub>IH</sub>	Input high level input leakage current	V <sub>IN</sub> = VCC		90		μA
I <sub>IL</sub>	Input low level input leakage	V <sub>IN</sub> = GND		-90		μA
R <sub>IND</sub>	Input pins pull down resistance	see <a href="#">Detailed Description</a> for more information	28.5	55	113	kΩ
R <sub>INU</sub>	Input pins pull up resistance	see <a href="#">Detailed Description</a> for more information	28.5	55	113	
T <sub>INFIL</sub>	IN+, IN- and RST/EN deglitch (ON and OFF) filter time	f <sub>S</sub> = 50kHz	28	40	50	ns
T <sub>RSTFIL</sub>	Deglitch filter time to reset /FLT		400	650	800	ns
<b>GATE DRIVER STAGE</b>						
I <sub>OUT</sub> , I <sub>OUTH</sub>	Peak source current	C <sub>L</sub> =0.18μF, f <sub>S</sub> =1kHz		10		A
I <sub>OUT</sub> , I <sub>OUTL</sub>	Peak sink current				10	
R <sub>OUTH(3)</sub>	Output pull-up resistance	I <sub>OUT</sub> = -0.1A	1.5	2.5	4.9	Ω
R <sub>OUTL</sub>	Output pull-down resistance	I <sub>OUT</sub> = 0.1A	0.1	0.3	0.7	Ω
V <sub>OUTH</sub>	High level output voltage	I <sub>OUT</sub> = -0.2A, V <sub>DD</sub> =18V		17.5		V
V <sub>OUTL</sub>	Low level output voltage	I <sub>OUT</sub> = 0.2A		60		mV
<b>ACTIVE PULLDOWN</b>						
V <sub>OUTPD</sub>	Output active pull down on OUTL	I <sub>OUTL</sub> or I <sub>OUT</sub> = 0.1 × I <sub>OUT(L)(tpy)</sub> , VDD=OPEN, VEE=COM	1.5	2.0	2.5	V
<b>EXTERNAL MILLER CLAMP</b>						
V <sub>CLMPH</sub>	Miller clamp threshold voltage	Reference to VEE	1.5	2.0	2.5	V

(1) Current are positive into and negative out of the specified terminal.

(2) All voltages are referenced to COM unless otherwise notified.

(3) For internal PMOS only. Refer to [Feature Description](#) for effective pull-up resistance.

**Electrical Characteristics (continued)**

VCC=3.3V or 5.0V, 1uF capacitor from VCC to GND, VDD-COM=20V, 18V or 15V, COM-VEE =0V, 5V, 8V or 15V, C<sub>L</sub>=100pF, -40°C<T<sub>J</sub><150°C (unless otherwise noted)<sup>(1)(2)</sup>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CLMPE</sub>	Output high voltage	Reference to VEE	4.8	5	5.3	V
I <sub>CLMPEH</sub>	Peak source current	C <sub>CLMPE</sub> = 10nF ; guaranteed by design		0.25		A
I <sub>CLMPEL</sub>	Peak sink current	C <sub>CLMPE</sub> = 10nF	0.12	0.25	0.37	A
t <sub>CLMPER</sub>	Rising time	C <sub>CLMPE</sub> = 330pF		20	40	ns
t <sub>DCLMPE</sub>	Miller clamp ON delay time			40	70	ns
<b>SHORT CIRCUIT CLAMPING</b>						
V <sub>CLP-OUT(H)</sub>	V <sub>OUT</sub> -VDD, V <sub>OUTH</sub> -VDD	OUT = Low, I <sub>OUT(H)</sub> = 500mA, t <sub>CLP</sub> =10us		0.9	0.99	V
V <sub>CLP-OUT(L)</sub>	V <sub>OUT</sub> -VDD, V <sub>OUTL</sub> -VDD	OUT = High, I <sub>OUT(L)</sub> = 500mA, t <sub>CLP</sub> =10us		1.8	1.98	V
<b>OC PROTECTION</b>						
I <sub>DCHG</sub>	OC pull down current when	V <sub>OC</sub> = 1V		40		mA
V <sub>OCTH</sub>	Detection Threshold		0.63	0.7	0.77	V
V <sub>OCL</sub>	Voltage when OUT(L) = LOW, Reference to COM	I <sub>OC</sub> = 5mA		0.13		V
t <sub>OCFIL</sub>	OC fault deglitch filter		95	120	180	ns
t <sub>OCOFF</sub>	OC propagation delay to OUT(L) 90%		150	270	400	ns
t <sub>OCFLT</sub>	OC to $\overline{\text{FLT}}$ low delay		300	530	750	ns
<b>2-LEVEL TURNOFF (Triggered by OC)</b>						
V <sub>2LOFF</sub>	2LOFF voltage threshold		8.3	9.0	10.0	V
t <sub>2LOFF</sub>	2LOFF voltage duration		500	700	1000	ns
I <sub>TL1</sub>	High to 2-Level transition sink current			900		mA
I <sub>TL3</sub>	Soft turn-off current on fault conditions		500	900	1200	mA
<b>ISOLATED TEMPERATURE SENSE AND MONITOR (AIN-APWM)</b>						
V <sub>AIN</sub>	Analog sensing voltage range		0.5		4.5	V
I <sub>AIN</sub>	Internal current source	V <sub>AIN</sub> =2.5V, -40°C< T <sub>J</sub> < 150°C	196	203	209	μA
f <sub>APWM</sub>	APWM output frequency	V <sub>AIN</sub> =2.5V	360	400	440	kHz
BW <sub>AIN</sub>	AIN-APWM bandwidth			10		kHz
D <sub>APWM</sub>	APWM Dutycycle	V <sub>AIN</sub> = 0.6V	85	88	91	%
		V <sub>AIN</sub> = 2.5V	47	50	53	
		V <sub>AIN</sub> = 4.5V	7	10	13	
<b>FLT AND RDY REPORTING</b>						
t <sub>RDYHLD</sub>	VDD UVLO RDY low minimum holding time		0.55		1	ms
t <sub>FLTMUTE</sub>	Output mute time on fault	Reset fault through $\overline{\text{RST}}/\text{EN}$	0.55		1	ms
R <sub>ODON</sub>	Open drain output on resistance	I <sub>ODON</sub> = 5mA		30		Ω
V <sub>ODL</sub>	Open drain low output voltage	I <sub>ODON</sub> = 5mA			0.3	V
<b>COMMON MODE TRANSIENT IMMUNITY</b>						
CMTI	Common-mode transient immunity	V <sub>CM</sub> = 1500 V	150			V/ns

## 6.10 Switching Characteristics

VCC=5.0V, 1uF capacitor from VCC to GND, VDD–COM=20V, 18V or 15V, COM–VEE = 3V, 5V or 8V, C<sub>L</sub>=100pF, –40°C<T<sub>J</sub><150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PDHL</sub>	Propagation delay time – High to Low		60	90	130	ns
t <sub>PDLH</sub>	Propagation delay time – Low to High		60	90	130	
PWD	Pulse width distortion  t <sub>PDHL</sub> – t <sub>PDLH</sub>				30	
t <sub>sk-pp</sub>	Part to Part skew	Rising or Falling Propagation Delay			30	
t <sub>r</sub>	Driver output rise time	C <sub>L</sub> =10nF			28	
t <sub>f</sub>	Driver output fall time	C <sub>L</sub> =10nF			24	
f <sub>MAX</sub>	Maximum switching frequency				1	MHz

### 6.11 Insulation Characteristics Curves

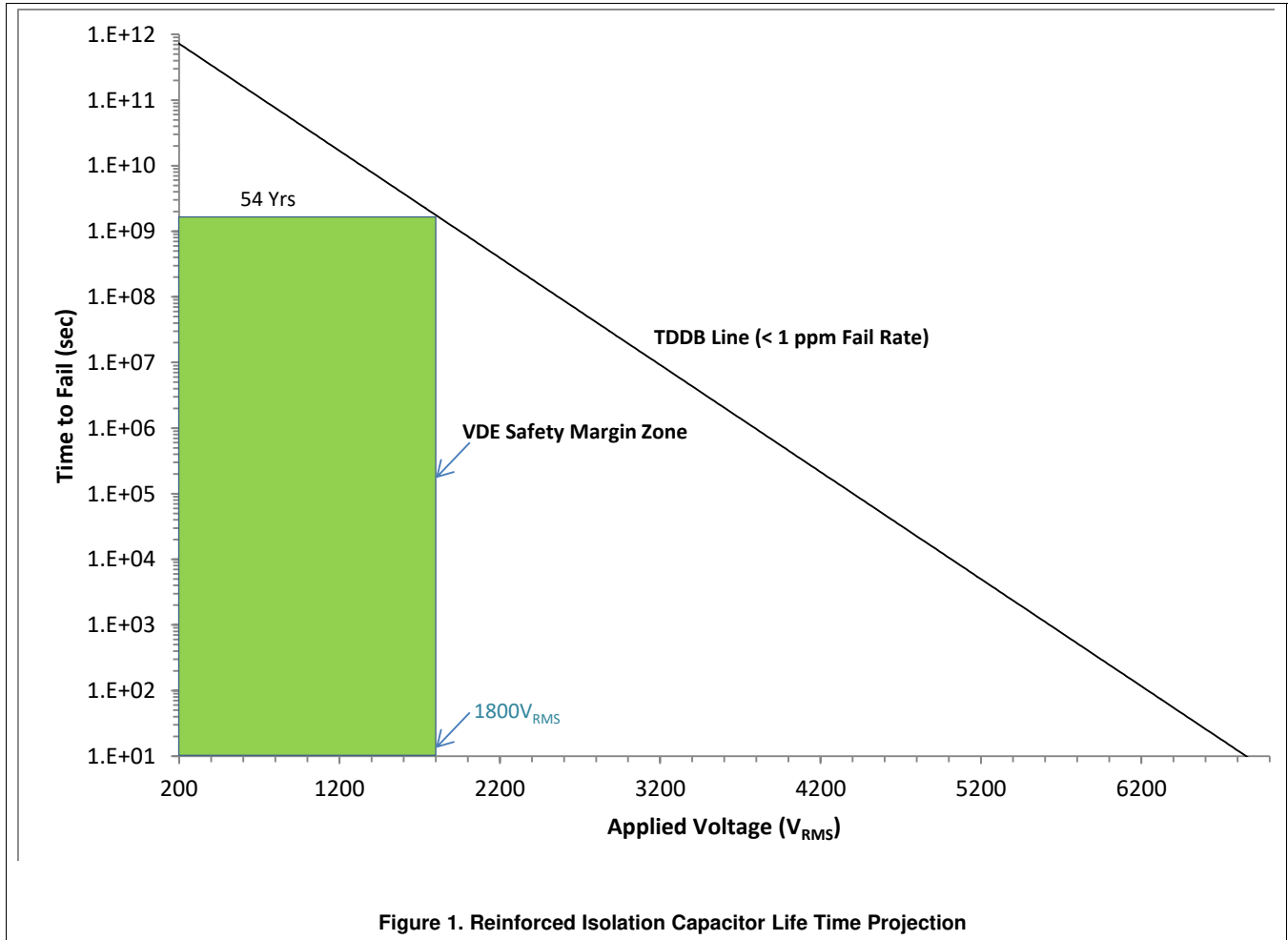


Figure 1. Reinforced Isolation Capacitor Life Time Projection

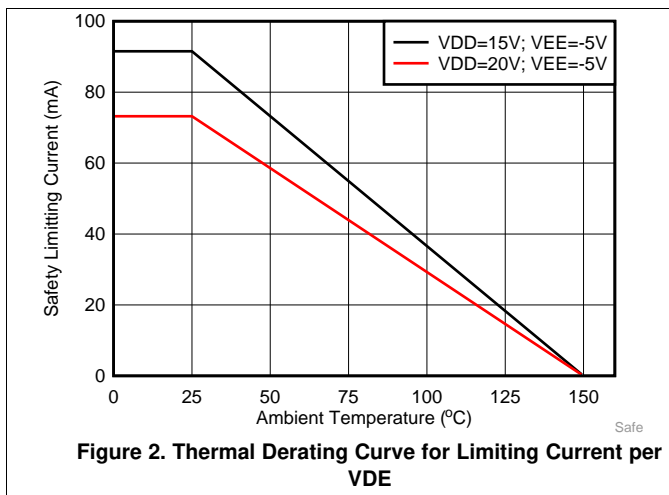


Figure 2. Thermal Derating Curve for Limiting Current per VDE

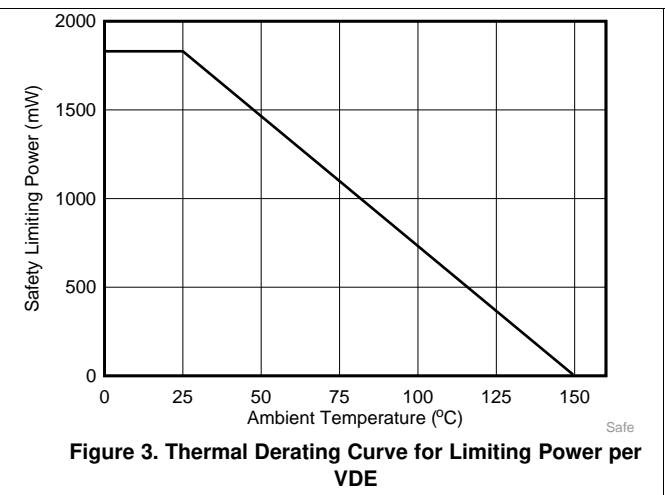
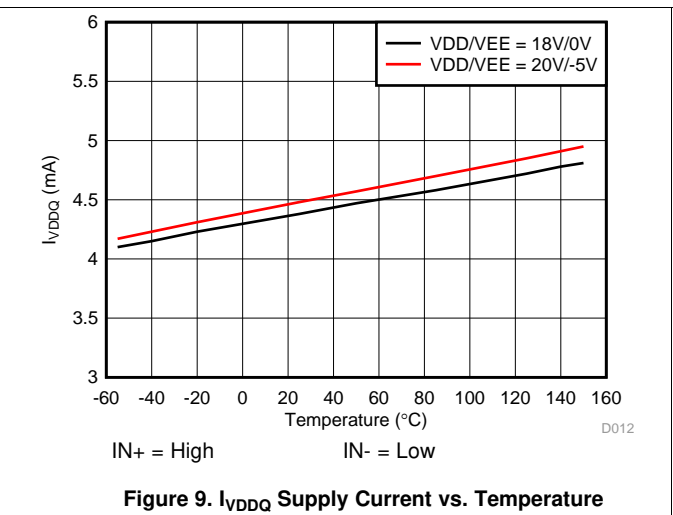
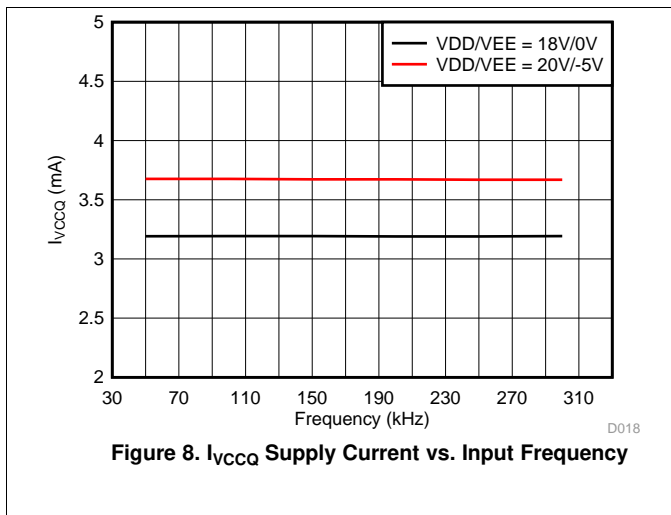
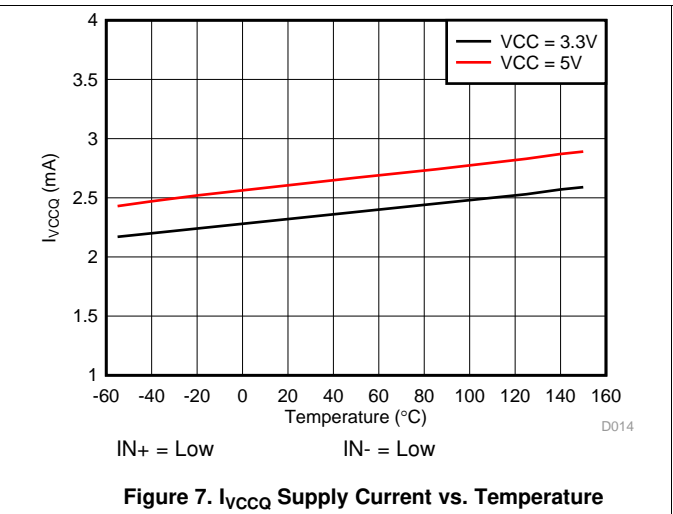
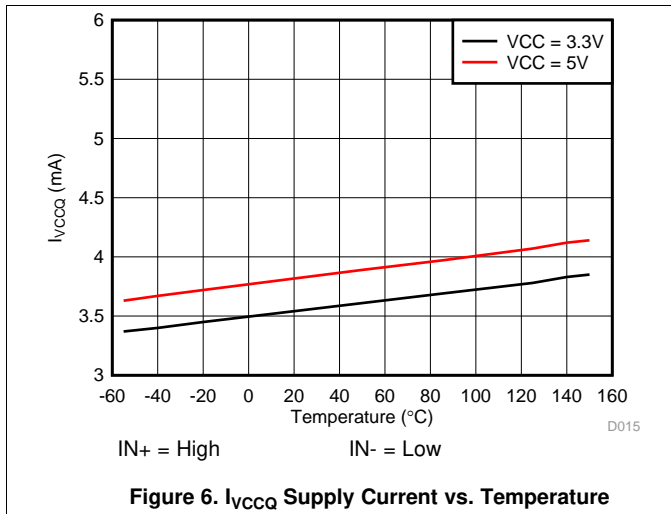
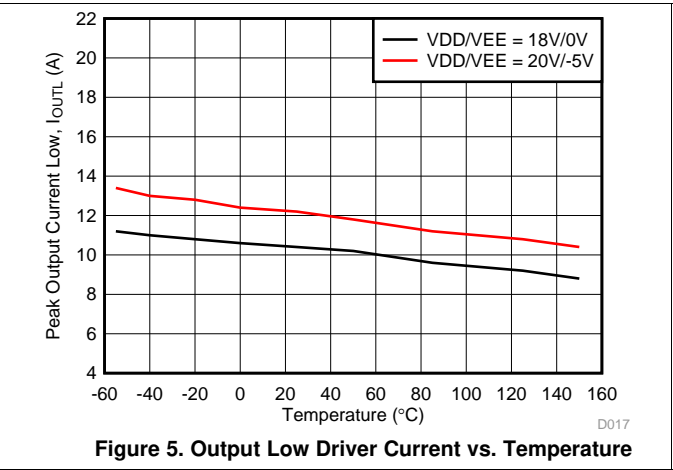
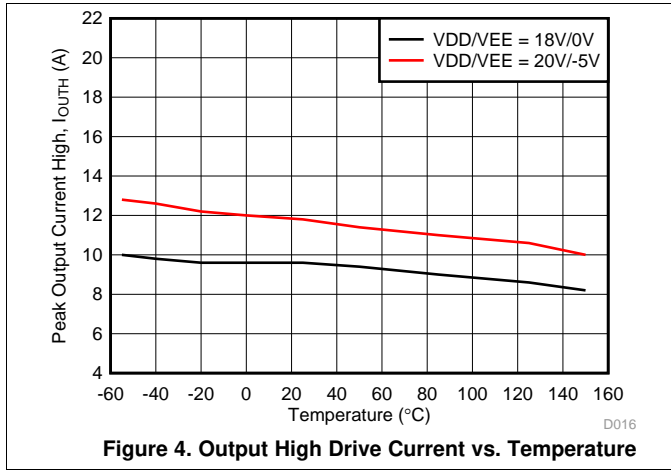
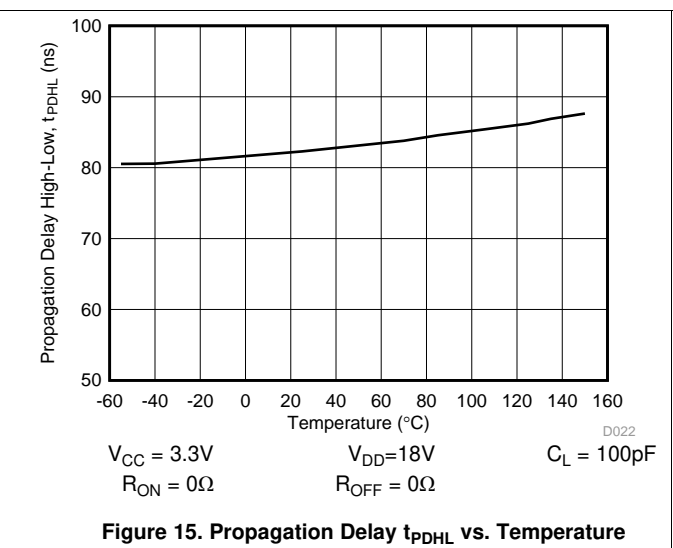
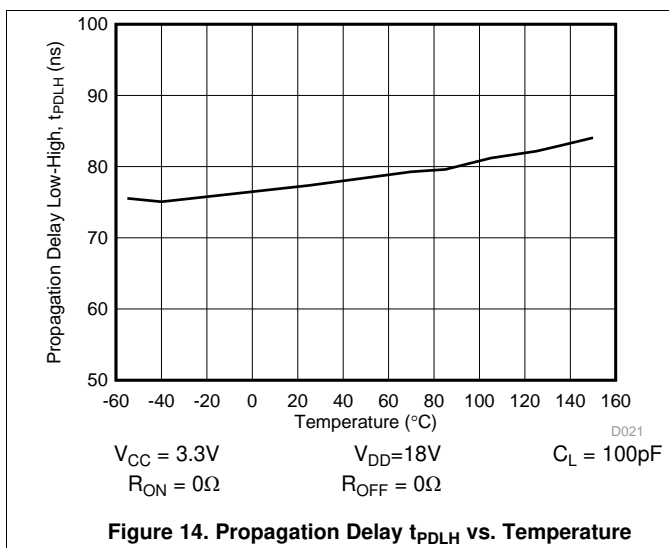
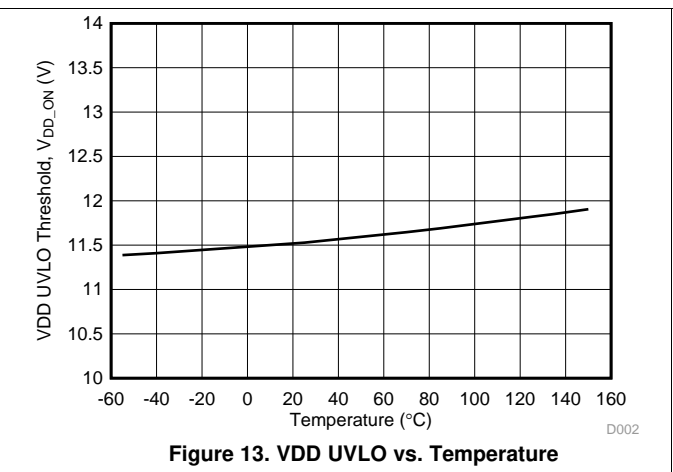
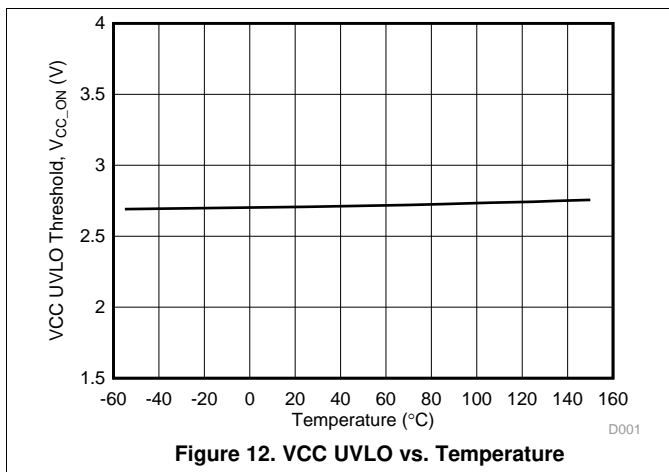
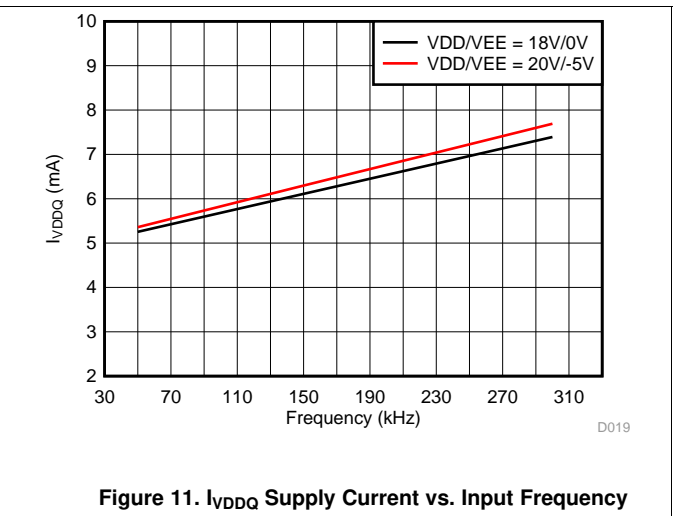
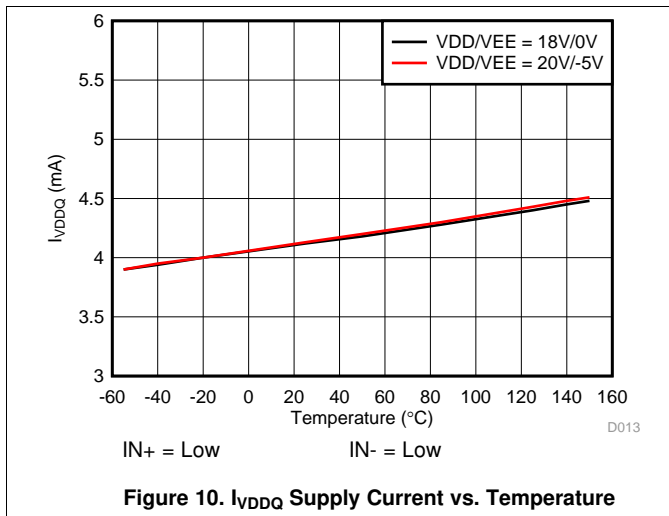


Figure 3. Thermal Derating Curve for Limiting Power per VDE

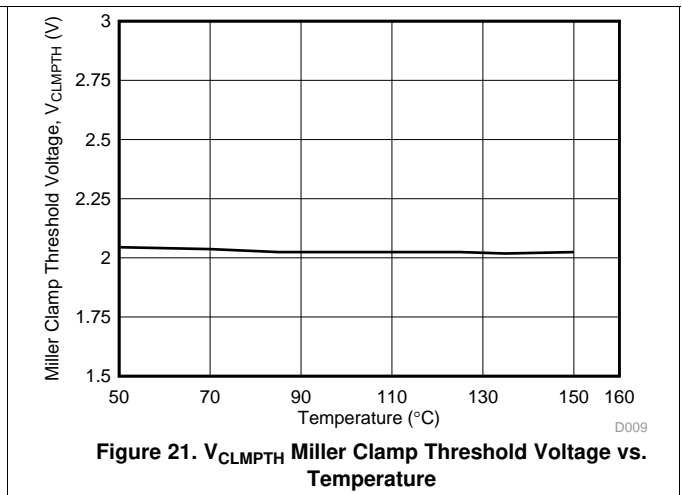
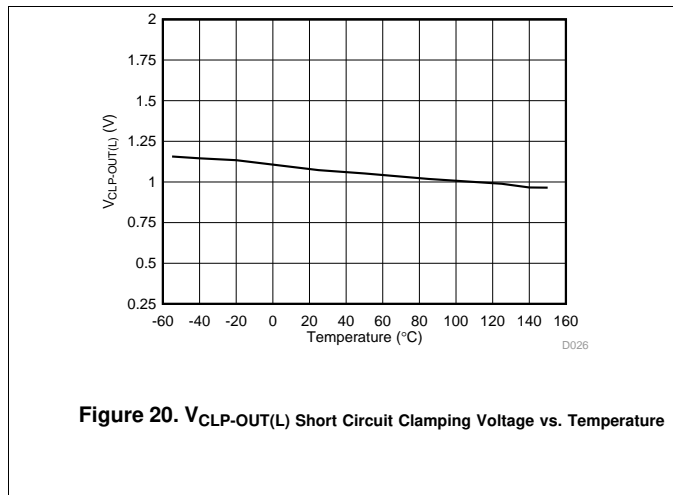
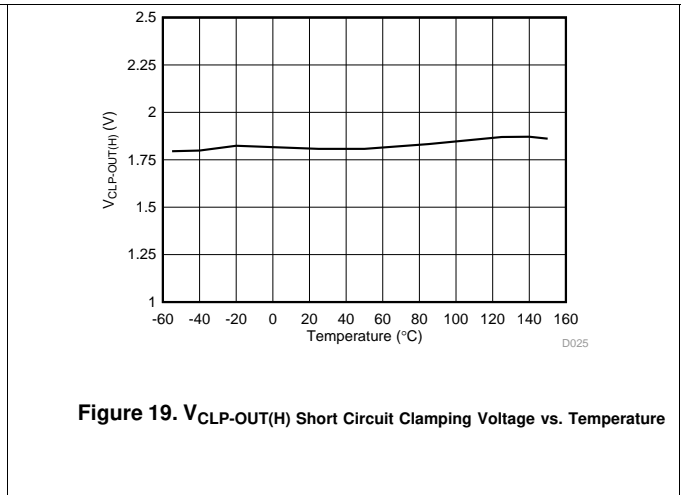
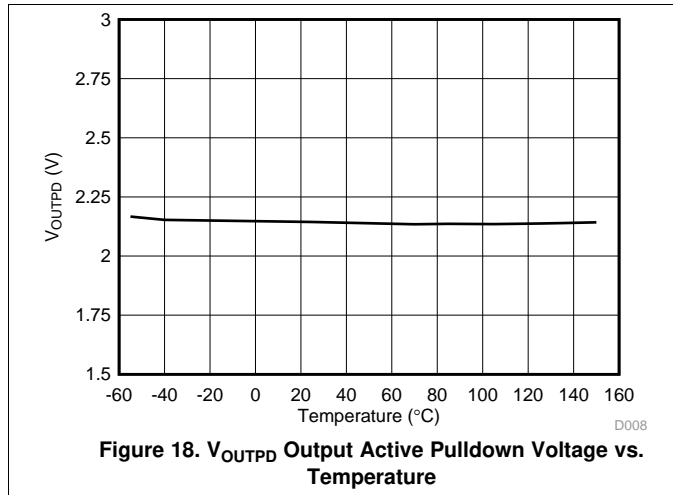
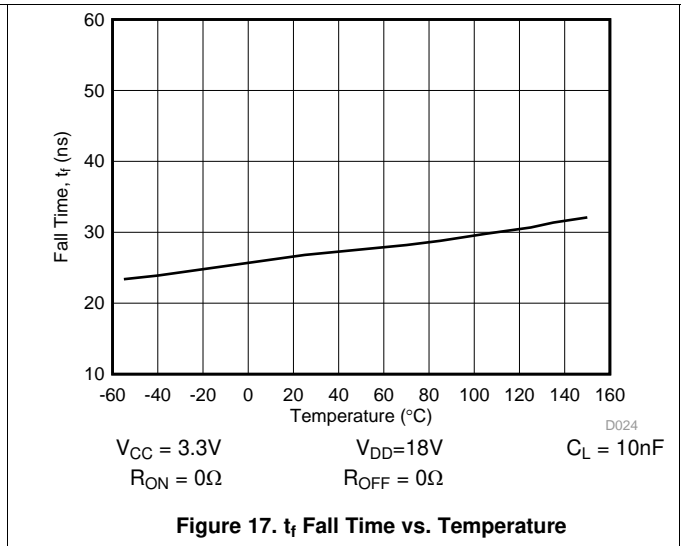
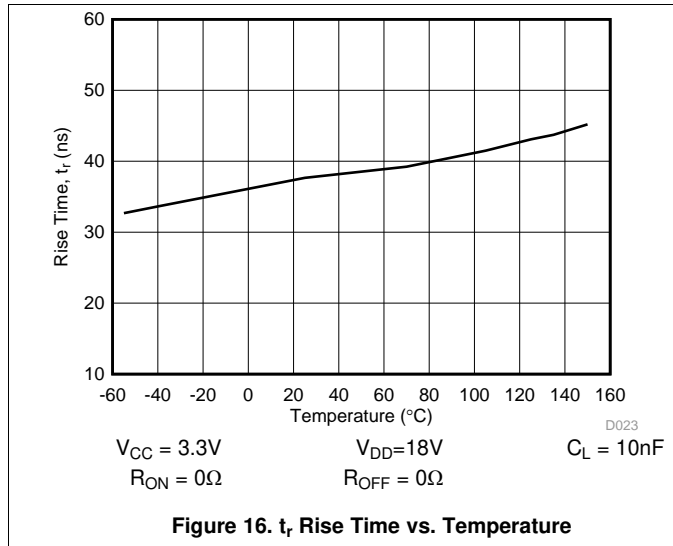
### 6.12 Typical Characteristics



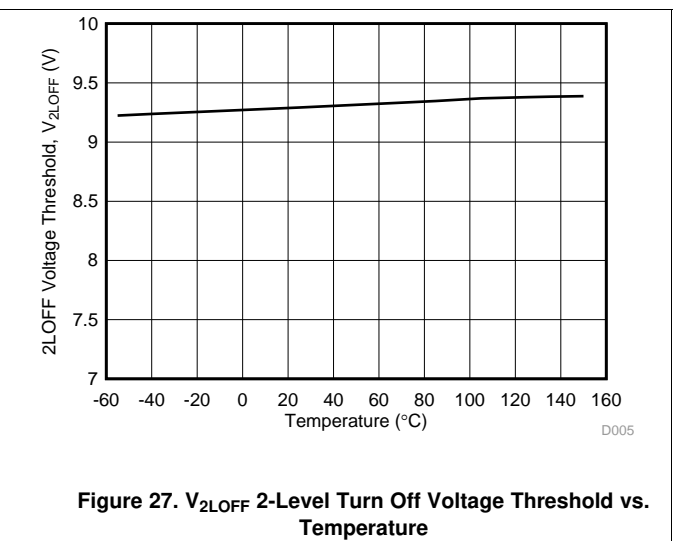
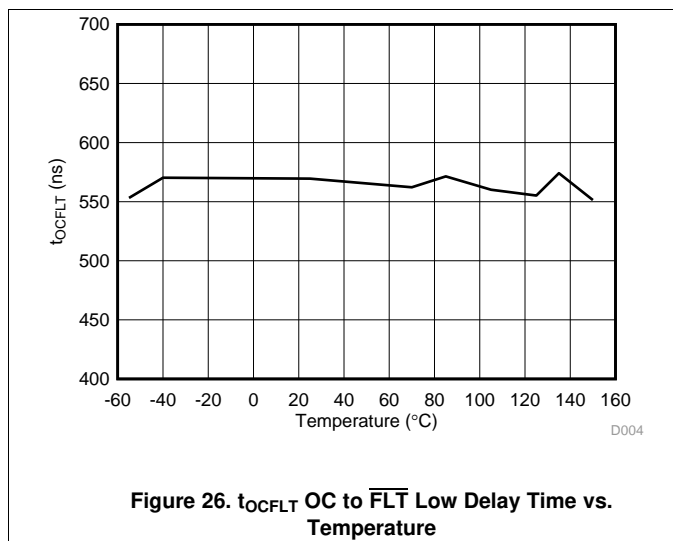
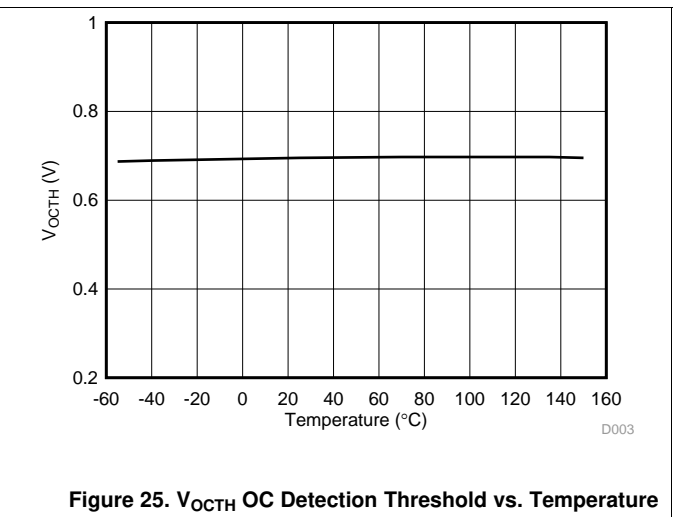
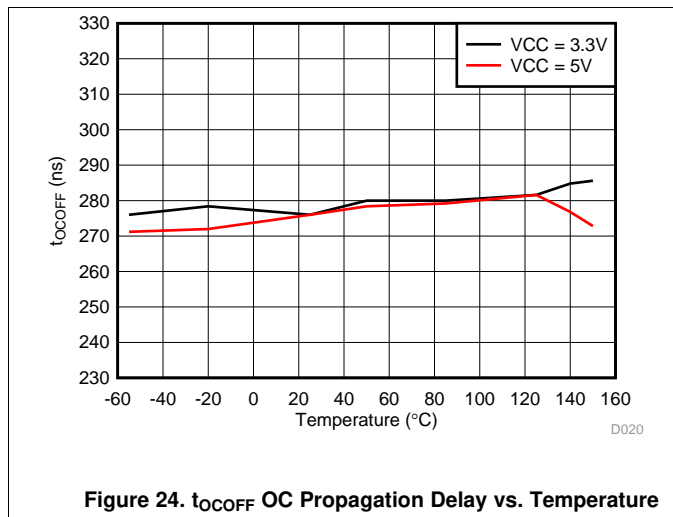
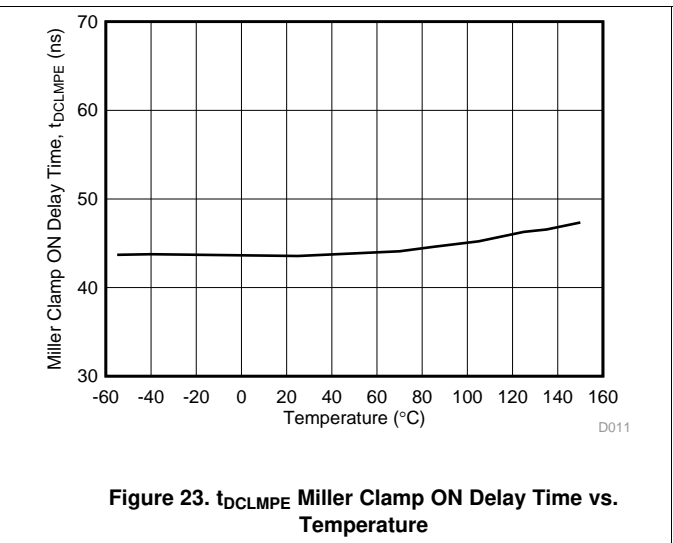
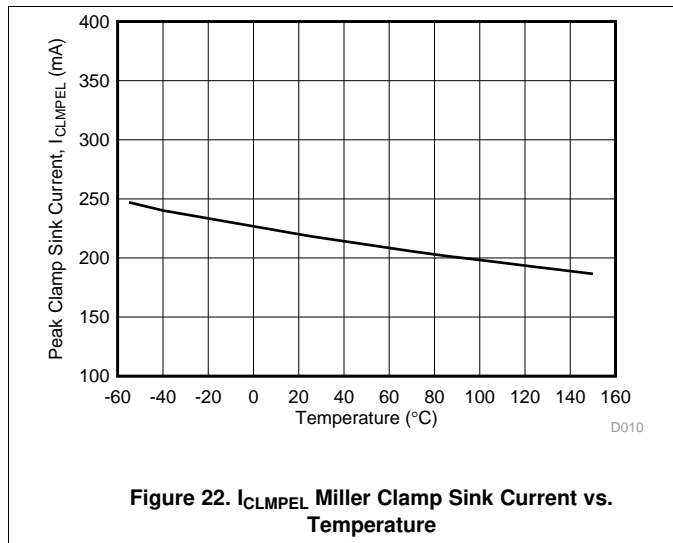
Typical Characteristics (continued)



Typical Characteristics (continued)



Typical Characteristics (continued)





Typical Characteristics (continued)

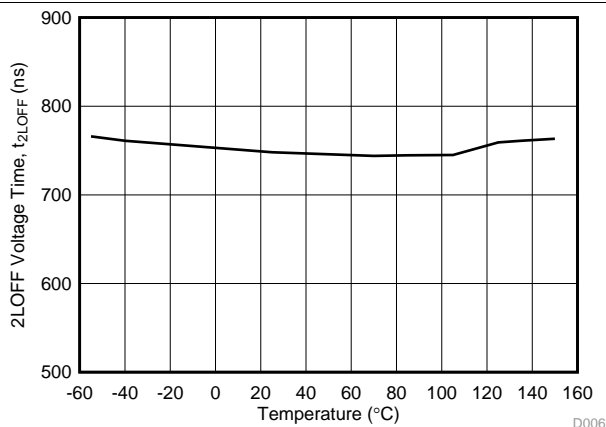


Figure 28. t<sub>2LOFF</sub> 2-Level Turn Off Time vs. Temperature

7 Parameter Measurement Information

7.1 Propagation Delay

7.1.1 Regular Turn-OFF

Figure 29 shows the propagation delay measurement for non-inverting configurations. Figure 30 shows the propagation delay measurement with the inverting configurations.

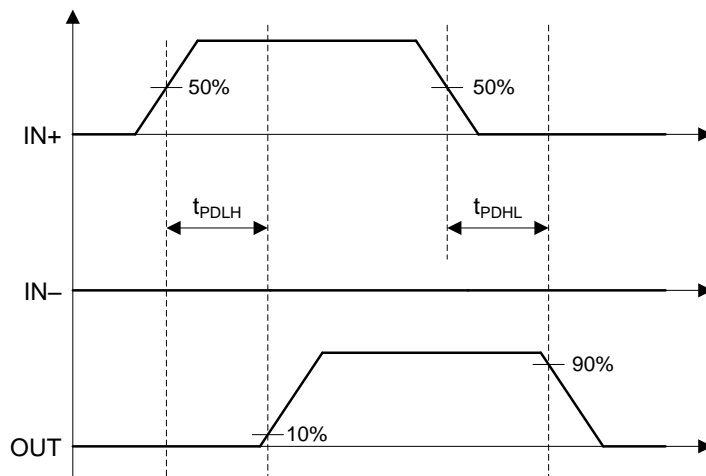
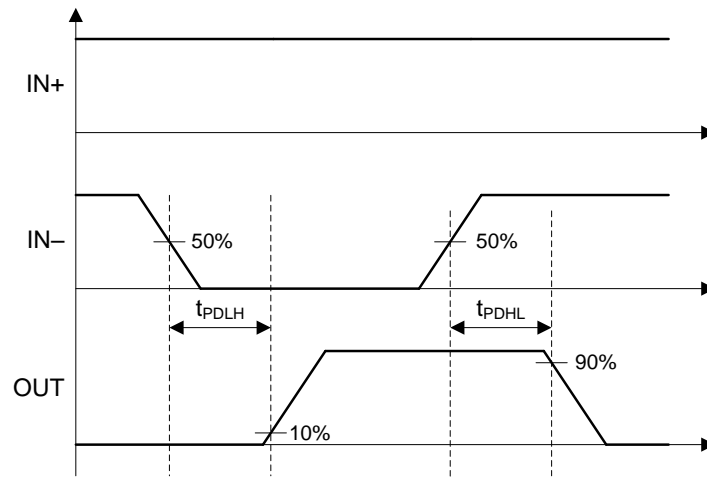


Figure 29. Non-inverting Logic Propagation Delay Measurement

**Propagation Delay (continued)**



**Figure 30. Inverting Logic Propagation Delay Measurement**

## 7.2 Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, i.e. IN+, IN-, RST/EN, a 40ns deglitch filter is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN- PWM pulse is smaller than the input deglitch filter width,  $T_{INFIL}$ , there will be no responses on OUT drive signal. Figure 31 and Figure 32 shows the IN+ pin ON and OFF pulse deglitch filter effect. Figure 33 and Figure 34 shows the IN- pin ON and OFF pulse deglitch filter effect.

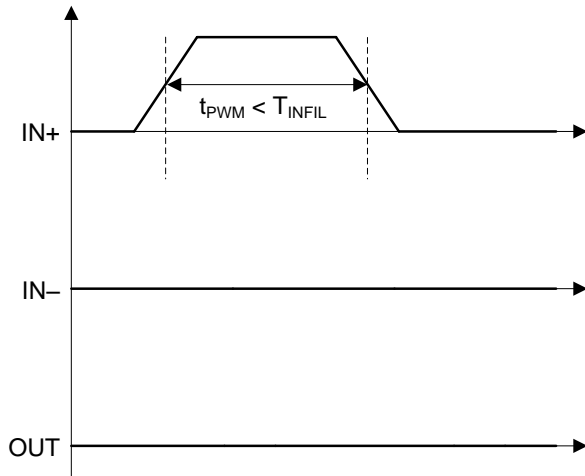


Figure 31. IN+ ON Deglitch Filter

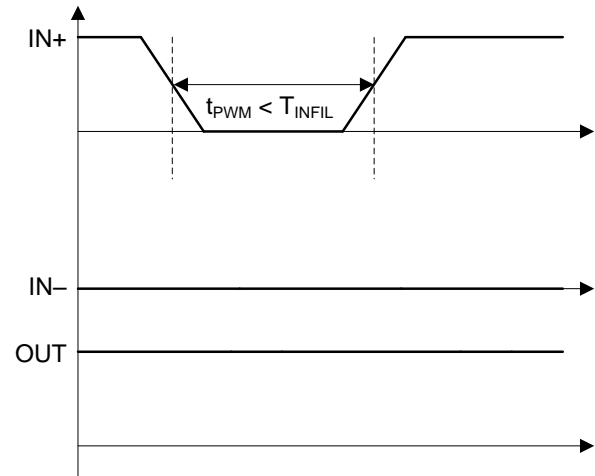


Figure 32. IN+ OFF Deglitch Filter

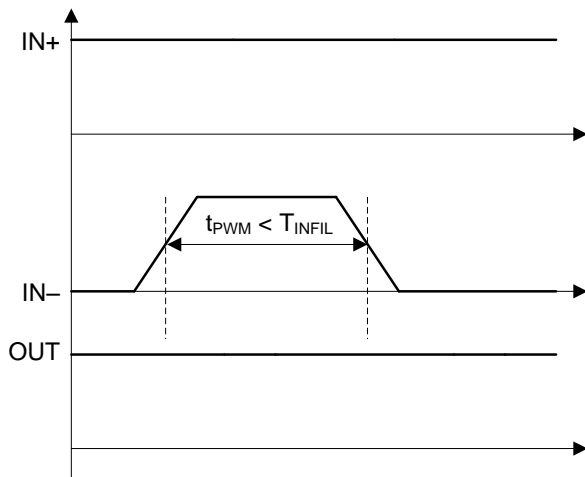


Figure 33. IN- ON Deglitch Filter

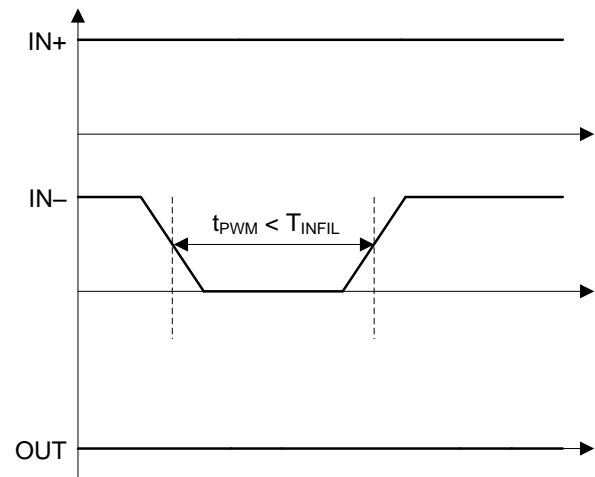
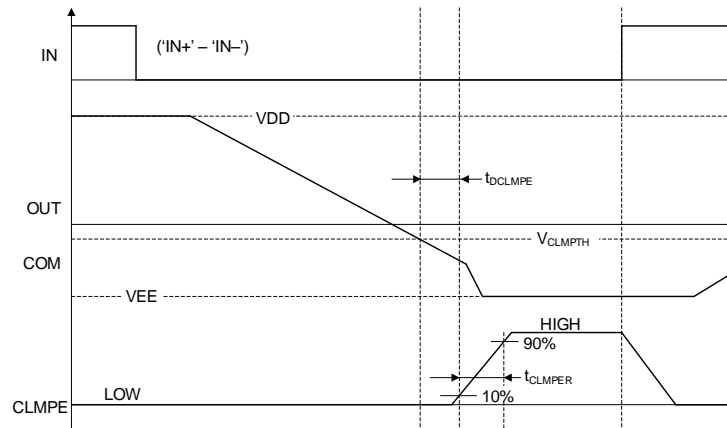


Figure 34. IN- OFF Deglitch Filter

## 7.3 Active Miller Clamp

### 7.3.1 External Active Miller Clamp

For gate driver application with unipolar bias supply or bipolar supply with small negative turn-off voltage, active miller clamp can help add an additional low impedance path to bypass the miller current and prevent the high  $dV/dt$  introduced unintentional turn-on through the miller capacitance. Different from the internal active miller clamp, external active miller clamp function is used for applications where the gate driver may not be close to the power device or power module due to system layout considerations. External active miller clamp function provide a 5V gate drive signal to turn-on the external miller clamp FET when the gate driver voltage is less than miller clamp threshold,  $V_{CLMP\ TH}$ . [Figure 35](#) shows the timing diagram for external active miller clamp function.



**Figure 35. Timing Diagram for External Active Miller Clamp Function**

## 7.4 Under Voltage Lockout (UVLO)

UVLO is one of the key protection features designed to protect the system in case of bias supply failures on VCC — primary side power supply, and VDD — secondary side power supply.

### 7.4.1 VCC UVLO

The VCC UVLO protection details are discussed in this section. Figure 36 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN-APWM.

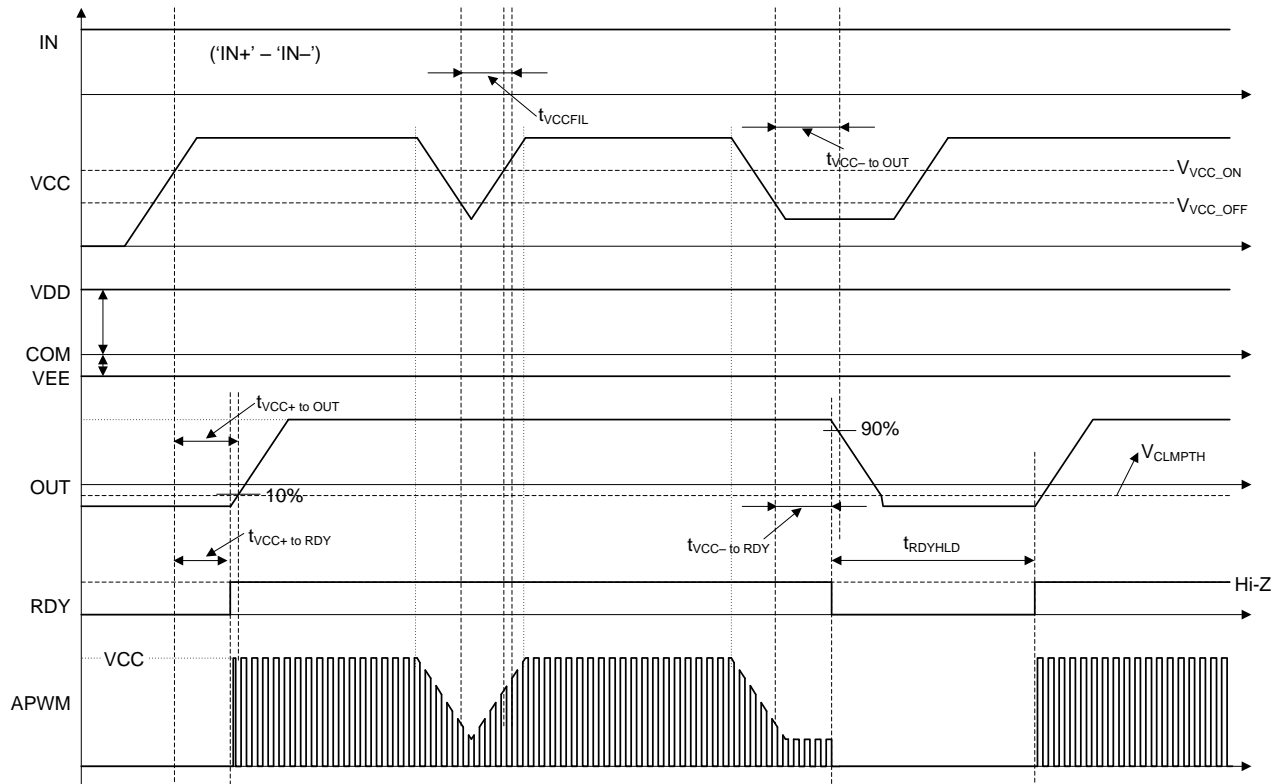


Figure 36. VCC UVLO Protection Timing Diagram

## Under Voltage Lockout (UVLO) (continued)

### 7.4.2 VDD UVLO

The VDD UVLO protection details are discussed in this section. Figure 37 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

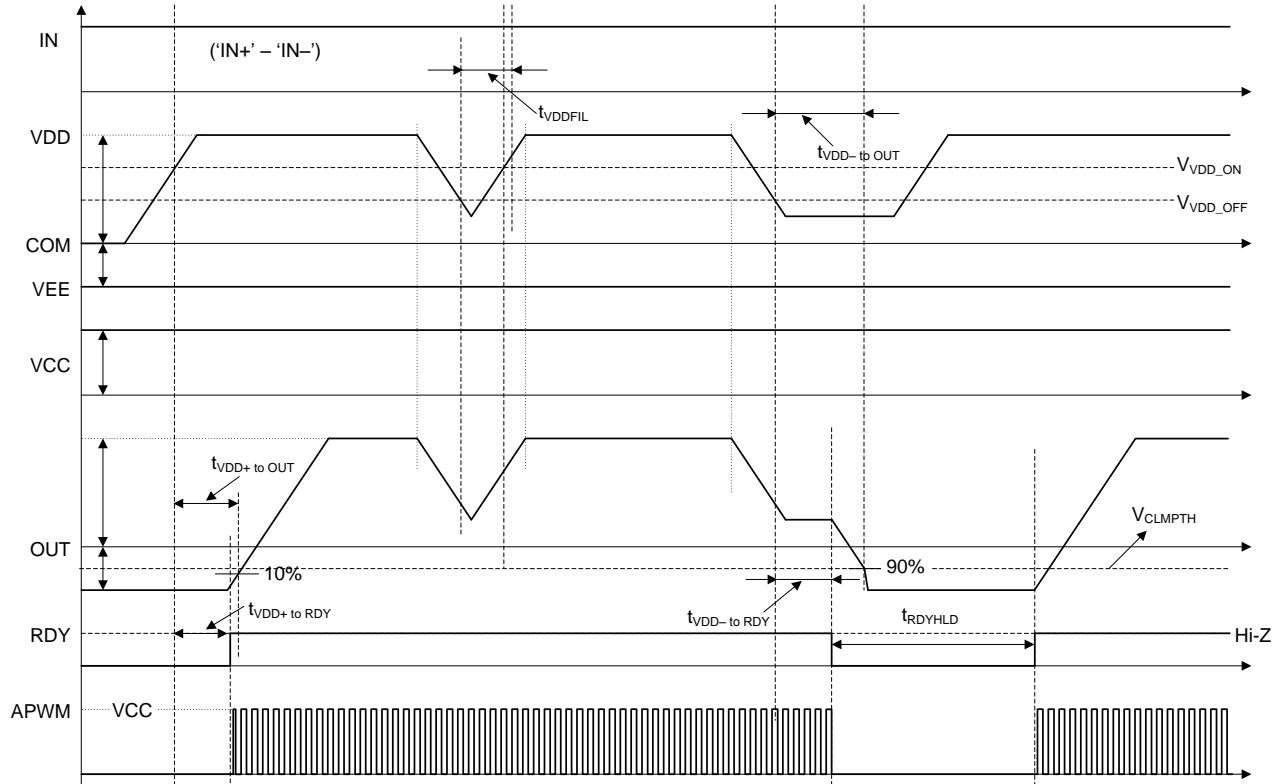


Figure 37. VDD UVLO Protection Timing Diagram

## 7.5 OC (Over Current) Protection

### 7.5.1 OC Protection with 2-Level Turn-OFF

OC Protection is used to sense the current of SiC-MOSFETs and IGBTs under over current or shoot-through condition. Figure 38 shows the timing diagram of OC operation with 2-level turn-off.

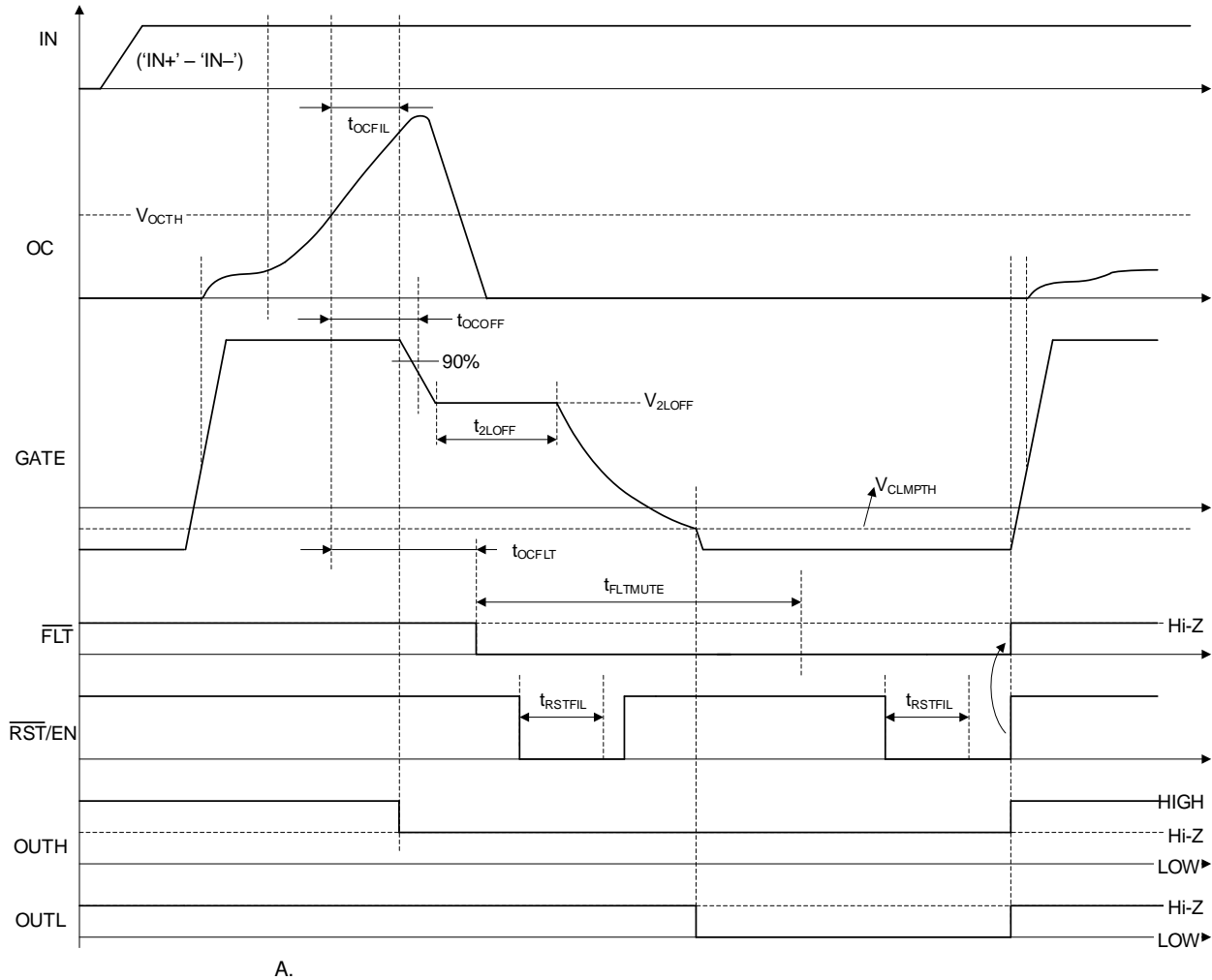


Figure 38. OC Protection with 2-Level Turn-OFF

## 8 Detailed Description

### 8.1 Overview

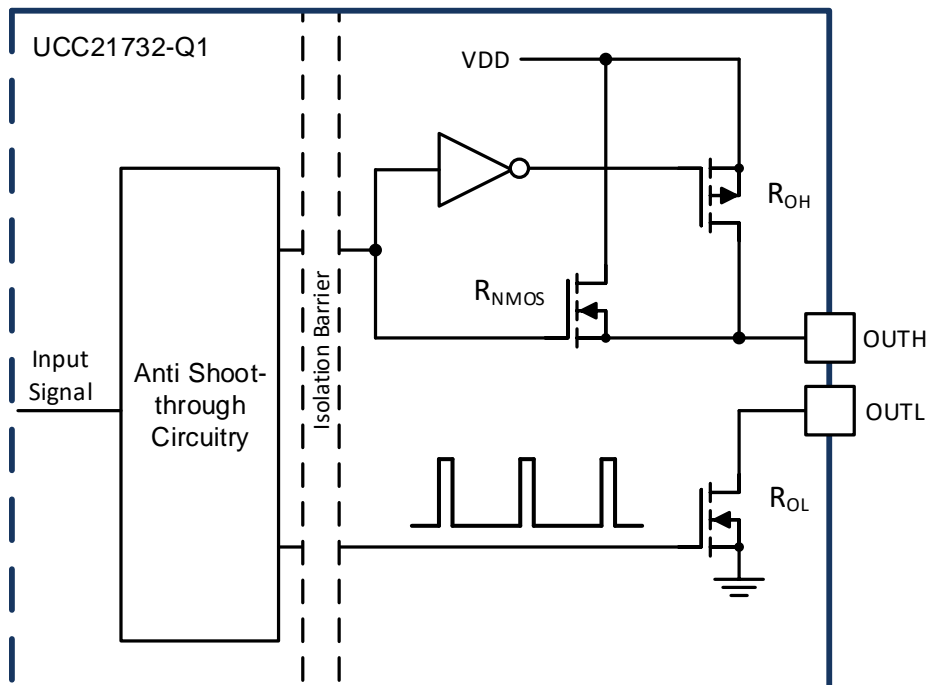
The UCC21732-Q1 device is an advanced isolated gate driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device can support up to 2121V DC operating voltage based on SiC MOSFETs and IGBTs, and can be used to above 10kW applications such as HEV/EV traction inverter, motor drive, on-board and off-board battery charger, solar inverter, etc. The galvanic isolation is implemented by the capacitive isolation technology, which can realize a reliable reinforced isolation between the low voltage DSP/MCU and high voltage side.

The  $\pm 10A$  peak sink and source current of UCC21732-Q1 can drive the SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with external buffer stage. The input side is isolated with the output side with a reinforced isolation barrier based on capacitive isolation technology. The device can support up to 1.5-kV<sub>RMS</sub> working voltage, 12.8-kV<sub>PK</sub> surge immunity with longer than 40 years isolation barrier life. The strong drive strength helps to switch the device fast and reduce the switching loss. While the 150V/ns minimum CMTI guarantees the reliability of the system with fast switching speed. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitor features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. The 12V output side power supply UVLO is suitable for switches with gate voltage  $\geq 15V$ . The active miller clamp feature prevents the false turn on causing by miller capacitance during fast switching. External miller clamp FET can be used, providing more versatility to the system design. The device has the state-of-art overcurrent and short circuit detection time, and fault reporting function to the low voltage side DSP/MCU. The 2-level turn-off with soft turn off is triggered when the overcurrent or short circuit fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches.

The isolated analog to PWM sensor can be used as switch temperature sensing, DC bus voltage sensing, auxiliary power supply sensing, etc. The PWM signal can be fed directly to DSP/MCU or through a low-pass-filter as an analog signal.

### 8.2 Functional Block Diagram





## 8.3 Feature Description

### 8.3.1 Power Supply

The input side power supply VCC can support a wide voltage range from 3V to 5.5V. The device supports both unipolar and bipolar power supply on the output side, with a wide range from 13V to 33V from VDD to VEE. The negative power supply with respect to switch source or emitter is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. The negative voltage is especially important for SiC MOSFET due to its fast switching speed.

### 8.3.2 Driver Stage

UCC21732-Q1 has  $\pm 10A$  peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. UCC21732-Q1 can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 10A. The driver features an important safety function wherein, when the input pins are in floating condition, the OUTH/OUTL is held in LOW state. The split output of the driver stage is depicted in . The driver has rail-to-rail output by implementing a hybrid pull-up structure with a P-Channel MOSFET in parallel with an N-Channel MOSFET, and an N-Channel MOSFET to pulldown. The pull-up NMOS is the same as the pull down NMOS, so the on resistance  $R_{NMOS}$  is the same as  $R_{OL}$ . The hybrid pull-up structure delivers the highest peak-source current when it is most needed, during the miller plateau region of the power semiconductor turn-on transient. The  $R_{OH}$  in represents the on-resistance of the pull-up P-Channel MOSFET. However, the effective pull-up resistance is much smaller than  $R_{OH}$ . Since the pull-up N-Channel MOSFET has much smaller on-resistance than the P-Channel MOSFET, the pull-up N-Channel MOSFET dominates most of the turn-on transient, until the voltage on OUTH pin is about 3V below VDD voltage. The effective resistance of the hybrid pull-up structure during this period is about  $2 \times R_{OL}$ . Then the P-Channel MOSFET pulls up the OUTH voltage to VDD rail. The low pull-up impedance results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

The pull-down structure of the driver stage is implemented solely by a pull-down N-Channel MOSFET. The on-resistance of the N-Channel MOSFET  $R_{OL}$  can be found in the . This MOSFET can ensure the OUTL voltage be pulled down to VEE rail. The low pull-down impedance not only results in high sink current to reduce the turn-off time, but also helps to increase the noise immunity considering the miller effect.

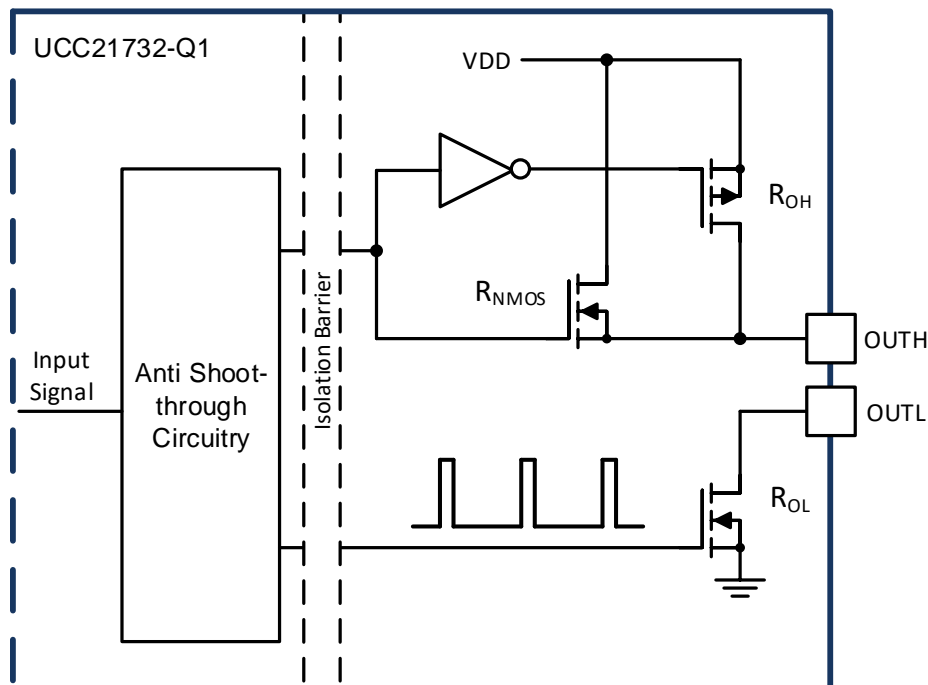


Figure 39. Gate Driver Output Stage

## Feature Description (continued)

### 8.3.3 VCC and VDD Undervoltage Lockout (UVLO)

UCC21732-Q1 implements the internal UVLO protection feature for both input and output power supplies VCC and VDD. When the supply voltage is lower than the threshold voltage, the driver output is held as LOW. The output only goes HIGH when both VCC and VDD are out of the UVLO status. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. For SiC MOSFET and IGBT, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage. UCC21732-Q1 implements 12V threshold voltage of VDD UVLO, with 800mV hysteresis. This threshold voltage is suitable for both SiC MOSFET and IGBT.

The UVLO protection block features with hysteresis and deglitch filter, which help to improve the noise immunity of the power supply. During the turn on and turn off switching transient, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filter, the internal UVLO protection block will ignore small noises during the normal switching transients.

The timing diagrams of the UVLO feature of VCC and VDD are shown in [Figure 36](#), and [Figure 37](#). The RDY pin on the input side is used to indicate the power good condition. The RDY pin is open drain. During UVLO condition, the RDY pin is held in low status and connected to GND. Normally the pin is pulled up externally to VCC to indicate the power good. The AIN-APWM function stops working during the UVLO status. The APWM pin on the input side will be held LOW.

### 8.3.4 Active Pulldown

UCC21732-Q1 implements an active pulldown feature to ensure the OUTH/OUTL pin clamping to VEE when the VDD is open. The OUTH/OUTL pin is in high-impedance status when VDD is open, the active pulldown feature can prevent the output be false turned on before the device is back to control.

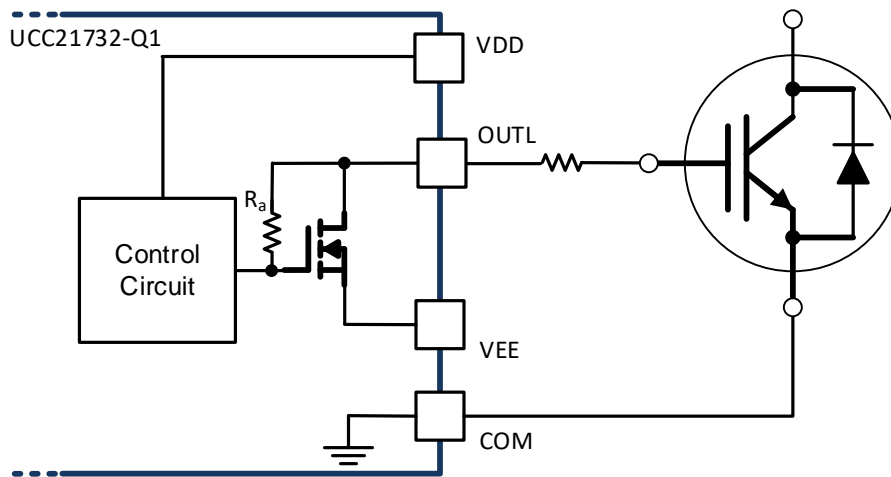


Figure 40. Active Pulldown

### 8.3.5 Short Circuit Clamping

During short circuit condition, the miller capacitance can cause a current sinking to the OUTH/OUTL pin due to the high  $dV/dt$  and boost the OUTH/OUTL voltage. The short circuit clamping feature of UCC21732-Q1 can clamp the OUTH/OUTL pin voltage to be slightly higher than VDD, which can protect the power semiconductors from a gate-source and gate-emitter overvoltage breakdown. This feature is realized by an internal diode from the OUTH/OUTL to VDD.

## Feature Description (continued)

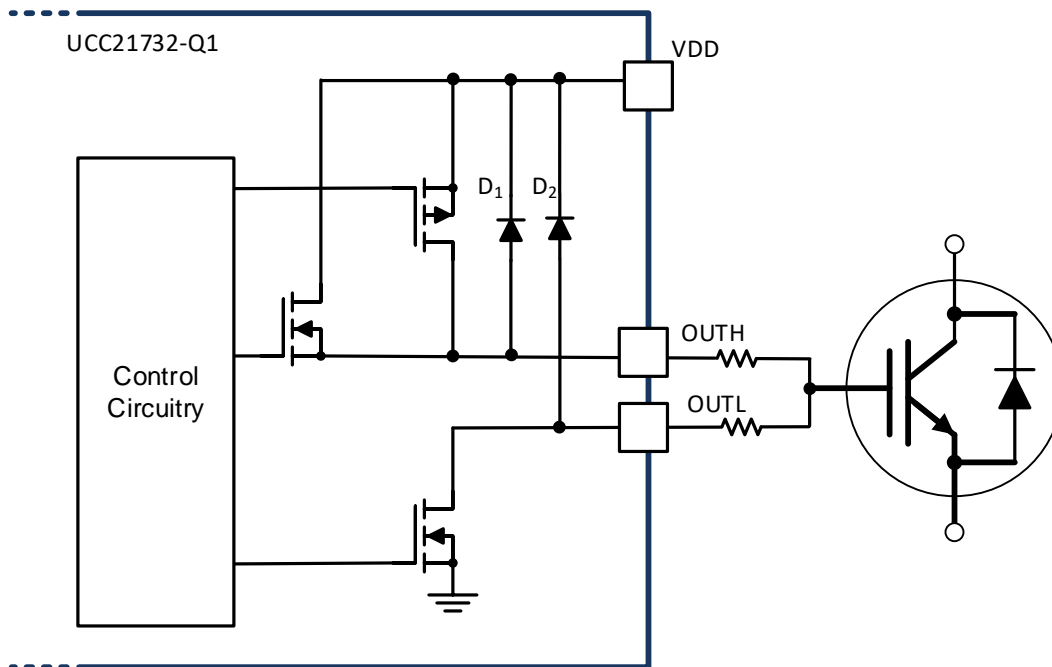
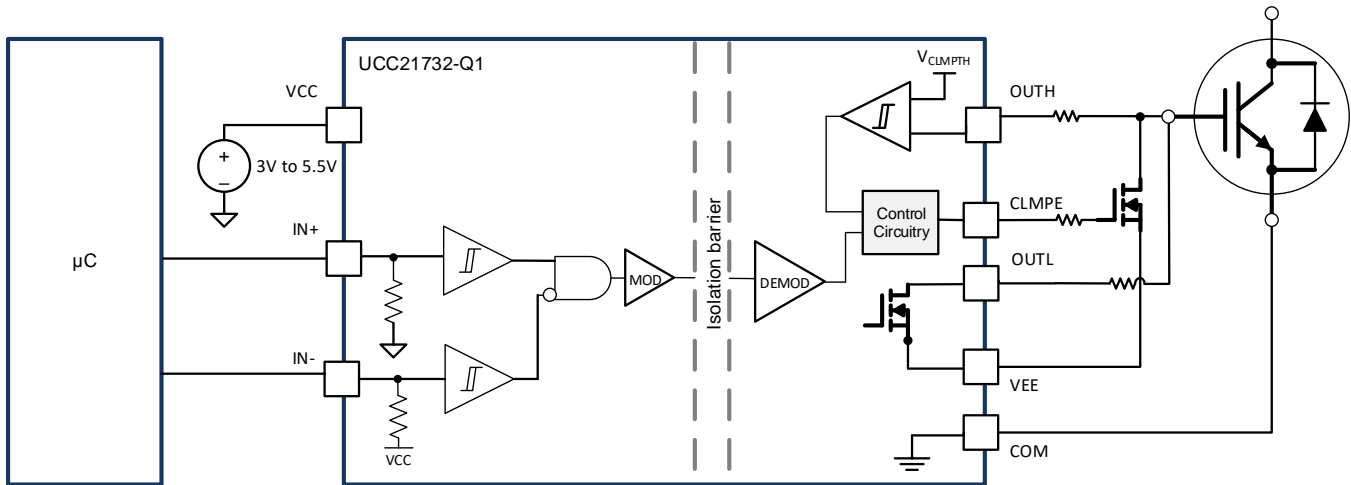


Figure 41. Short Circuit Clamping

### 8.3.6 External Active Miller Clamp

Active miller clamp feature is important to prevent the false turn-on while the driver is in OFF state. In applications which the device can be in synchronous rectifier mode, the body diode conducts the current during the deadtime while the device is in OFF state, the drain-source or collector-emitter voltage remains the same and the  $dV/dt$  happens when the other power semiconductor of the phase leg turns on. The low internal pull-down impedance of UCC21732-Q1 can provide a strong pulldown to hold the OUTL to VEE. However, external gate resistance is usually adopted to limit the  $dV/dt$ . The miller effect during the turn on transient of the other power semiconductor can cause a voltage drop on the external gate resistor, which boost the gate-source or gate-emitter voltage. If the voltage on  $V_{GS}$  or  $V_{GE}$  is higher than the threshold voltage of the power semiconductor, a shoot through can happen and cause catastrophic damage. The active miller clamp feature of UCC21732-Q1 drives an external MOSFET, which connects to the device gate. The external MOSFET is triggered when the gate voltage is lower than  $V_{CLMP_{TH}}$ , which is 2V above VEE, and creates a low impedance path to avoid the false turn on issue.

**Feature Description (continued)**



**Figure 42. Active Miller Clamp**

**8.3.7 Overcurrent and Short Circuit Protection**

The UCC21732-Q1 implements a fast overcurrent and short circuit protection feature to protect the SiC MOSFET or IGBT from catastrophic breakdown during fault. The OC pin of the device has a typical 0.7V threshold with respect to COM, source or emitter of the power semiconductor. When the input is in floating condition, or the output is held in low state, the OC pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The OC pin is in high-impedance state when the output is in high state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in on state. The internal pulldown MOSFET helps to discharge the voltage of OC pin when the power semiconductor is turned off.

The overcurrent and short circuit protection feature can be used to SiC MOSFET module or IGBT module with SenseFET, traditional desaturation circuit and shunt resistor in series with the power loop for lower power applications. For SiC MOSFET module or IGBT module with SenseFET, the SenseFET integrated in the module can scale down the drain current or collector current. With an external high precision sense resistor, the drain current or collector current can be accurately measured. If the voltage of the sensed resistor higher than the overcurrent threshold  $V_{OCTH}$  is detected, the 2-Level turn-off is initiated. A fault will be reported to the input side FLT pin to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the RST/EN pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

The overcurrent and short circuit protection feature can also be paired with desaturation circuit and shunt resistors. The DESAT threshold can be programmable in this case, which increases the versatility of the device. Detailed application diagrams of desaturation circuit and shunt resistor will be given in .

- High current and high di/dt during the overcurrent and short circuit fault can cause a voltage bounce on shunt resistor's parasitic inductance and board layout parasitic, which results in false trigger of OC pin. High precision, low ESL and small value resistor must be used in this approach.
- Shunt resistor approach is not recommended for high power applications and short circuit protection of the low power applications.

The detailed applications of the overcurrent and short circuit feature will be discussed in the Application and Implementation section.

Feature Description (continued)

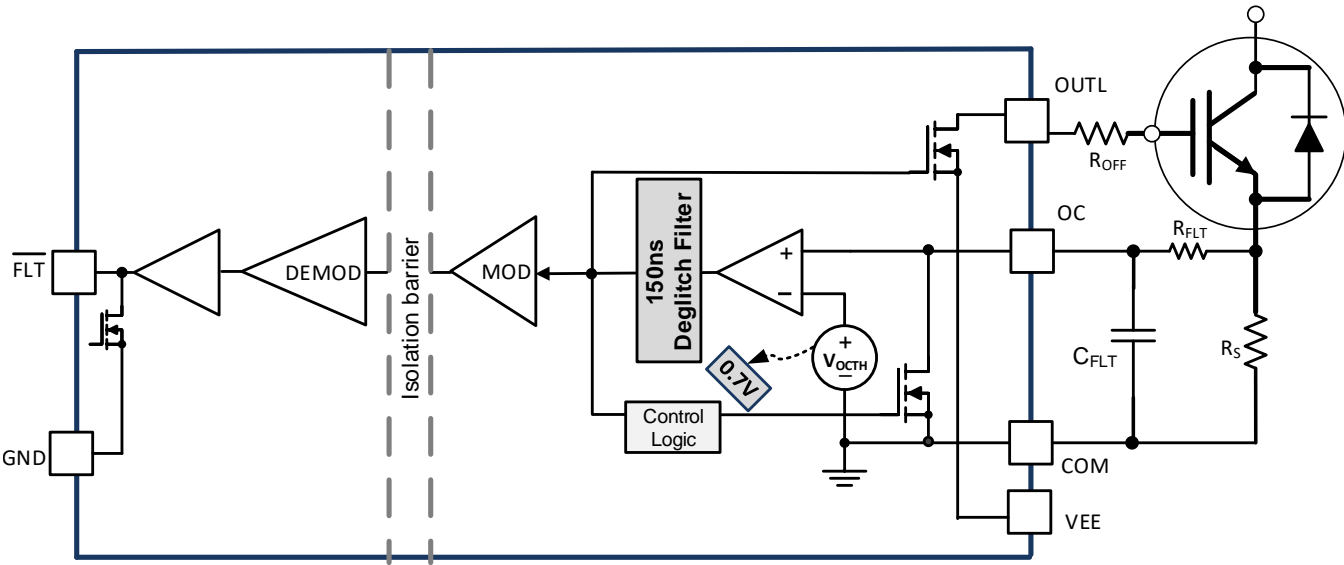


Figure 43. Overcurrent and Short Circuit Protection

8.3.8 2-Level Turn-off

UCC21732-Q1 initiates a fast 2-level turn-off when the overcurrent and short circuit protection is triggered. When the overcurrent and short circuit fault happens, the power power semiconductor transits from the linear region to the saturation region very fast. The channel current is controlled by the gate voltage. By pulling down the gate voltage to a mid-voltage level  $V_{2LOFF}$  and stay for a fixed time  $t_{2LOFF}$ , the channel current can be limited to a much lower level, which significantly reduces the energy dissipation during the fault event. After  $t_{2LOFF}$ , the driver continues to pull down the gate voltage by the soft turn off current  $I_{TL3}$  until it reaches VEE. With  $dI/dt$  of the channel current is controlled by the gate voltage and decreasing in a soft manner, thus the overshoot of the power semiconductor is limited and prevents the overvoltage breakdown. The timing diagram of 2-level turn-off shows in Figure 38.

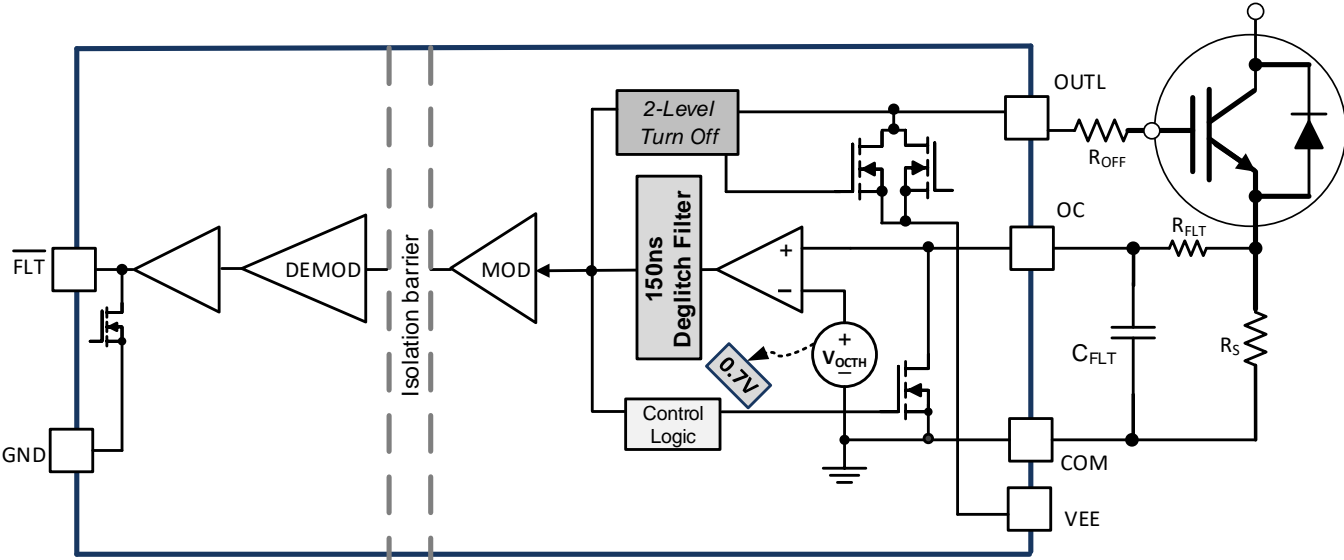


Figure 44. 2-Level Turn-off

## Feature Description (continued)

### 8.3.9 Fault ( $\overline{\text{FLT}}$ , Reset and Enable ( $\overline{\text{RST/EN}}$ ))

The  $\overline{\text{FLT}}$  pin of UCC21732-Q1 is open drain and can report a fault signal to the DSP/MCU when the overcurrent and short circuit fault is detected through OC pin. The  $\overline{\text{FLT}}$  pin is pulled down to GND, and is held in low state unless a reset signal is received from  $\overline{\text{RST/EN}}$ . The device has a fault mute time  $t_{\text{FLTMUTE}}$ , within which the device ignores any reset signal.

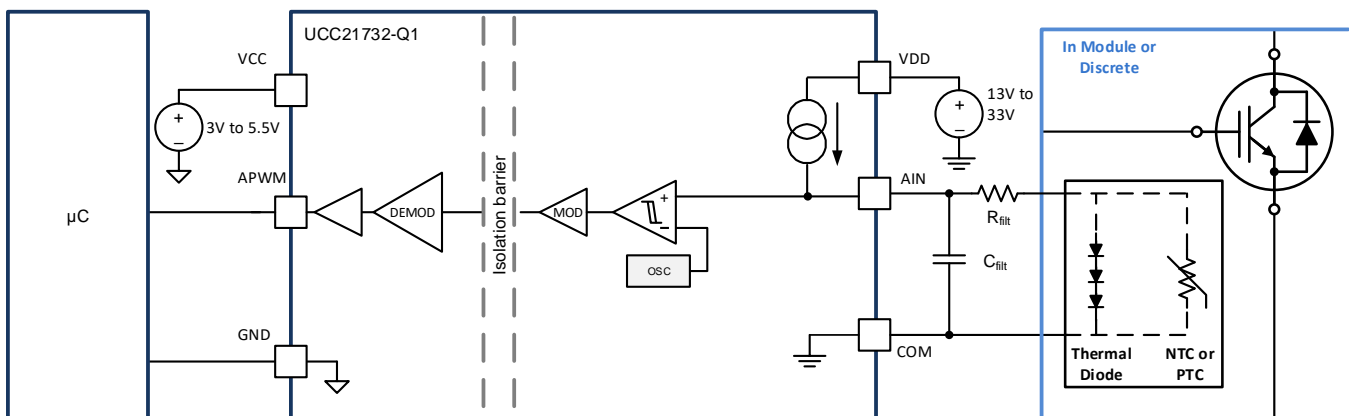
The  $\overline{\text{RST/EN}}$  is pulled down internally. The device is disabled by default if the  $\overline{\text{RST/EN}}$  pin is floating. The pin has two purposes:

- Resets the overcurrent and short circuit fault signaled on  $\overline{\text{FLT}}$  pin. The  $\overline{\text{RST/EN}}$  pin is active low, if the pin is set and held in low state for more than  $t_{\text{RSTFIL}}$ , the fault signal is reset and  $\overline{\text{FLT}}$  is reset back to the high impedance status at the rising edge of  $\overline{\text{RST/EN}}$  pin.
- Enable and shutdown the device. If the  $\overline{\text{RST/EN}}$  pin is pulled low, the driver is disabled and shut down by the regular turn off. The pin must be pulled up externally to enable the part, otherwise the device is disabled by default.

### 8.3.10 Isolated Analog to PWM Signal Function

The UCC21732-Q1 features an isolated analog to PWM signal function from AIN to APWM pin, which allows the isolated temperature sensing, high voltage dc bus voltage sensing, etc. An internal current source  $I_{\text{AIN}}$  in AIN pin is implemented in the device to bias an external thermal diode or temperature sensing resistor. The UCC21732-Q1 encodes the voltage signal  $V_{\text{AIN}}$  to a PWM signal, passing through the reinforced isolation barrier, and output to APWM pin on the input side. The PWM signal can either be transferred directly to DSP/MCU to calculate the duty cycle, or filtered by a simple RC filter as an analog signal. The AIN voltage input range is from 0.6V to 4.5V, and the corresponding duty cycle of the APWM output ranges from 88% to 10%. The duty cycle increases linearly from 10% to 88% while the AIN voltage decreases from 4.5V to 0.6V. This corresponds to the temperature coefficient of the negative temperature coefficient (NTC) resistor and thermal diode. When AIN is floating, the AIN voltage is 5V and the APWM operates at 400kHz with approximately 10% duty cycle. The accuracy of the duty cycle is  $\pm 5\%$  across temperature without one time calibration. The accuracy can be improved to  $\pm 2\%$  with calibration. The accuracy of the internal current source  $I_{\text{AIN}}$  is 3% across temperature.

The isolated analog to PWM signal feature can also support other analog signal sensing, such as the high voltage dc bus voltage, etc. The internal current source  $I_{\text{AIN}}$  should be taken into account when designing the potential divider if sensing a high voltage.



**Figure 45. Isolated Analog to PWM Signal**

## 8.4 Device Functional Modes

lists the device function.

**Table 2. Function Table**

Input							Output				
VCC	VDD	VEE	IN+	IN-	$\overline{\text{RST}}/\text{EN}$	AIN	RDY	$\overline{\text{FLT}}$	OUTH/ OUTL	CLMPE	APWM
PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low	Low
PD	PU	PU	X	X	X	X	HiZ	HiZ	Low	High	Low
PU	PU	PU	X	X	Low	X	HiZ	HiZ	Low	High	Low
PU	Open	PU	X	X	X	X	Low	HiZ	HiZ	HiZ	HiZ
PU	PU	Open	X	X	X	X	Low	HiZ	Low	High	Low
PU	PU	PU	Low	X	High	X	HiZ	HiZ	Low	High	P*
PU	PU	PU	X	High	High	X	HiZ	HiZ	Low	High	P*
PU	PU	PU	High	High	High	X	HiZ	HiZ	Low	High	P*

PU: Power Up ( $V_{CC} \geq 2.85V$ ,  $V_{DD} \geq 13.1V$ ,  $V_{EE} \leq 0V$ ); PD: Power Down ( $V_{CC} \leq 2.35V$ ,  $V_{DD} \leq 9.9V$ ); X: Irrelevant; P\*: PWM Pulse; HiZ: High Impedance

## 9 Applications and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The UCC21732-Q1 device is very versatile because of the strong drive strength, wide range of output power supply, high isolation ratings, high CMTI and superior protection and sensing features. The 1.5-kVRMS working voltage and 12.8-kVPE surge immunity can support up both SiC MOSFET and IGBT modules with DC bus voltage up to 2121V. The device can be used in both low power and high power applications such as the traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies and etc. The device can drive the high power SiC MOSFET module, IGBT module or paralleled discrete device directly without external buffer drive circuit based on NPN/PNP bipolar transistor in totem-pole structure, which allows the driver to have more control to the power semiconductor and saves the cost and space of the board design. UCC21732-Q1 can also be used to drive very high power modules or paralleled modules with external buffer stage. The input side can support power supply and microcontroller signal from 3.3V to 5V, and the device level shifts the signal to output side through reinforced isolation barrier. The device has wide output power supply range from 13V to 33V and support wide range of negative power supply. This allows the driver to be used in SiC MOSFET applications, IGBT application and many others. The 12V UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

UCC21732-Q1 device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short circuit fault. The feature is preferable in a split source SiC MOSFET module or a split emitter IGBT module. For the modules with no integrated current mirror or paralleled discrete semiconductors, the traditional desaturation circuit can be modified to implement short circuit protection. The semiconductor is shutdown when the fault is detected and FLTb pin is pulled down to indicate the fault detection. The device is latched unless reset signal is received from the RST/EN pin.
- 2-level turn-off feature to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power good status can be monitored from the RDY pin.
- Analog signal sensing with isolated analog to PWM signal feature. This feature allows the device to sense the temperature of the semiconductor from the thermal diode or temperature sensing resistor, or dc bus voltage with resistor divider. A PWM signal is generated on the low voltage side with reinforced isolated from the high voltage side. The signal can be fed back to the microcontroller for the temperature monitoring, voltage monitoring and etc.
- The active miller clamp feature protects the power semiconductor from false turn on by driving an external MOSFET. This feature allows the flexibility of the board layout design and the pulldown strength of miller clamp FET.
- Enable and disable function through the RSTb/EN pin.
- Short circuit clamping.
- Active pulldown.



## 9.2 Typical Application

shows the typical application of a half bridge using two UCC21732-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications such as traction inverter in HEV/EV to convert the DC current of the electric vehicle's battery to the AC current to drive the electric motor in the propulsion system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.

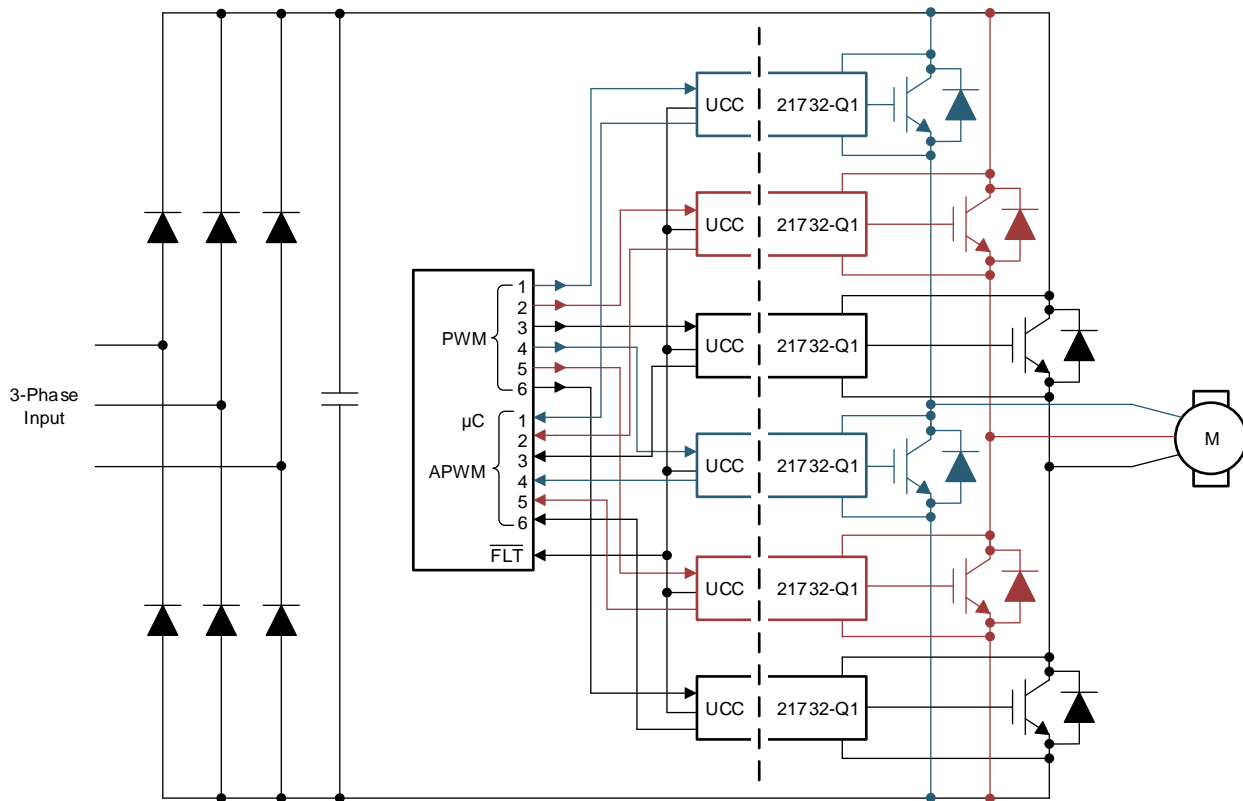


Figure 46. Typical Application Schematic

### 9.2.1 Design Requirements

The design of the power system for end equipment should consider some design requirements to ensure the reliable operation of UCC1732-Q1 through the load range. The design considerations include the peak source and sink current, power dissipation, overcurrent and short circuit protection, AIN-APWM function for analog signal sensing and etc.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are show in .

Table 3. Design Parameters

Parameter	Value
Input Supply Voltage	5V
IN-OUT Configuration	Non-inverting
Positive Output Voltage VDD	15V
Negative Output Voltage VEE	-5V
DC Bus Voltage	800V
Peak Drain Current	300A
Switching Frequency	50kHz
Switch Type	IGBT Module

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Input filters for IN+, IN- and $\overline{RST/EN}$

In the applications of traction inverter or motor drive, the power semiconductors are in hard switching mode. With the strong drive strength of UCC21732-Q1, the  $dV/dt$  can be high, especially for SiC MOSFET. Noise can not only be coupled to the gate voltage due to the parasitic inductance, but also to the input side as the non-ideal PCB layout and coupled capacitance.

UCC21732-Q1 features a 40ns internal deglitch filter to IN+, IN- and  $\overline{RST/EN}$  pin. Any signal less than 40ns can be filtered out from the input pins. For noisy systems, external low pass filter can be added externally to the input pins. Adding low pass filters to IN+, IN- and  $\overline{RST/EN}$  pins can effectively increase the noise immunity and increase the signal integrity. When not in use, the IN+, IN- and  $\overline{RST/EN}$  pins should not be floating. IN- should be tied to GND if only IN+ is used for non-inverting input to output configuration. The purpose of the low pass filter is to filter out the high frequency noise generated by the layout parasitics. While choosing the low pass filter resistors and capacitors, both the noise immunity effect and delay time should be considered according to the system requirements.

### 9.2.2.2 PWM Interlock of IN+ and IN-

UCC21732-Q1 features the PWM interlock for IN+ and IN- pins, which can be used to prevent the phase leg shoot through issue. As shown in , the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in , the PWM\_T is the PWM signal to top side switch, the PWM\_B is the PWM signal to bottom side switch. For the top side gate driver, the PWM\_T signal is given to the IN+ pin, while the PWM\_B signal is given to the IN- pin; for the bottom side gate driver, the PWM\_B signal is given to the IN+ pin, while PWM\_T signal is given to the IN- pin. When both PWM\_T and PWM\_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot through condition.

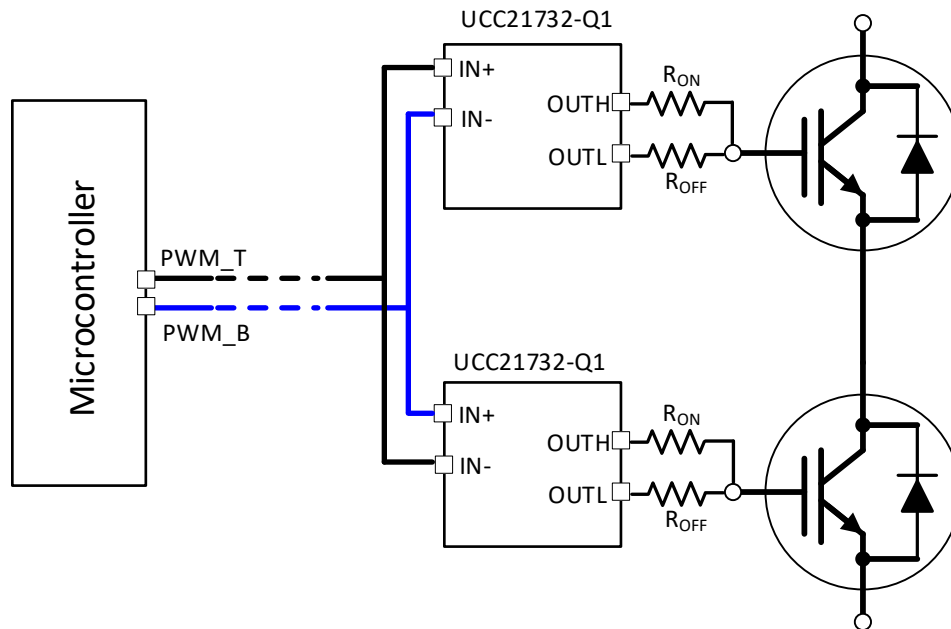


Figure 47. PWM Interlock for a Half Bridge

### 9.2.2.3 $\overline{FLT}$ , RDY and $\overline{RST/EN}$ Pin Circuitry

Both  $\overline{FLT}$  and RDY pin are open-drain output. The  $\overline{RST/EN}$  pin has 50k $\Omega$  internal pulldown resistor, so the driver is in OFF status if the  $\overline{RST/EN}$  pin is not pulled up externally. A 5k $\Omega$  resistor can be used as pullup resistor for the  $\overline{FLT}$ , RDY and  $\overline{RST/EN}$  pins.

To improve the noise immunity due to the parasitic coupling and common mode noise, low pass filters can be added between the  $\overline{FLT}$ , RDY and  $\overline{RST/EN}$  pins and the microcontroller. A filter capacitor between 100pF to 300pF can be added.

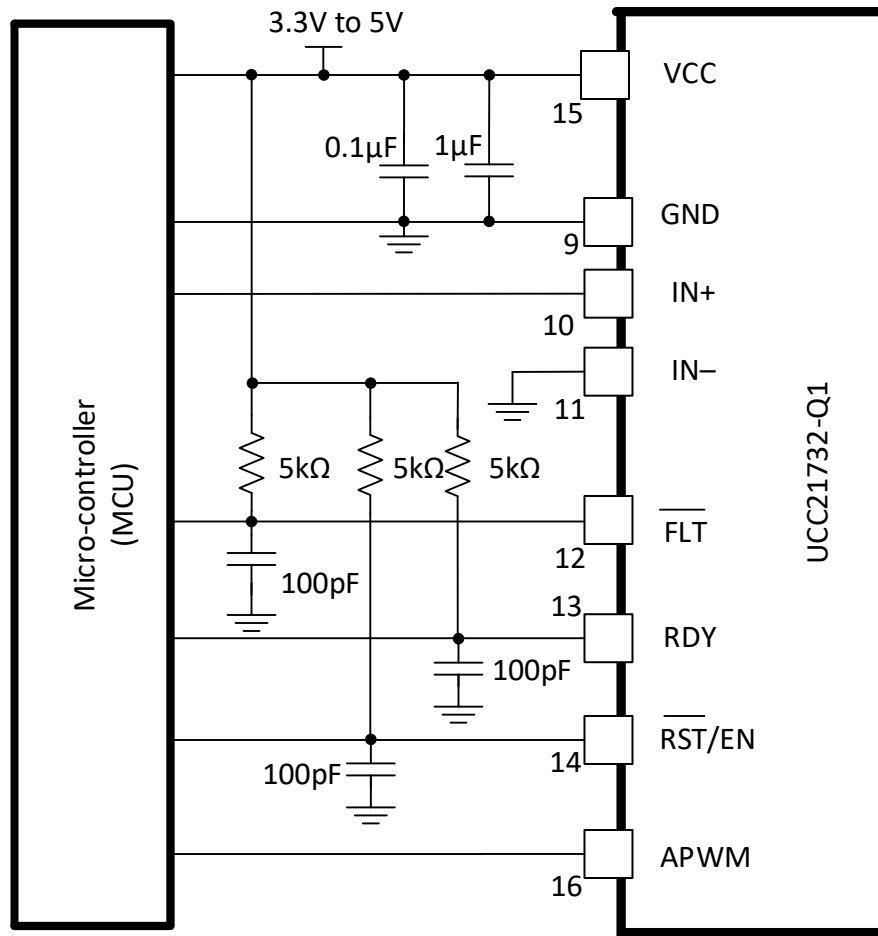
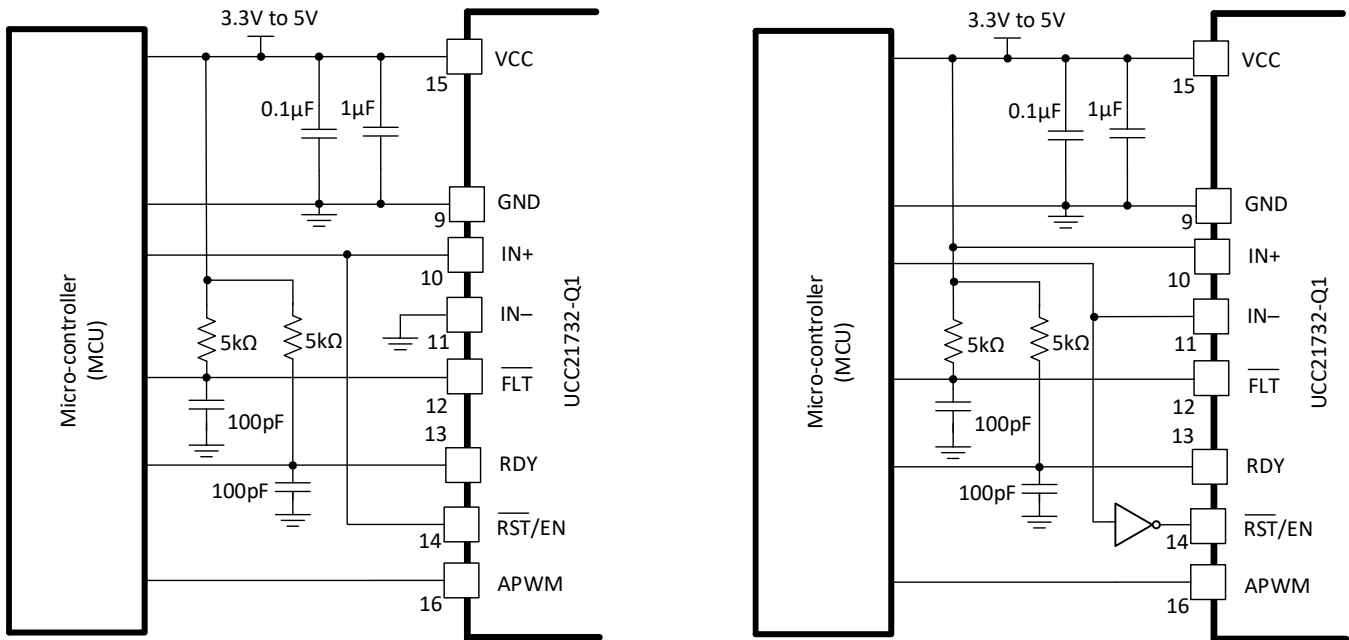


Figure 48.  $\overline{\text{FLT}}$ , RDY and  $\overline{\text{RST/EN}}$  Pins Circuitry

#### 9.2.2.4 $\overline{\text{RST/EN}}$ Pin Control

$\overline{\text{RST/EN}}$  pin has two functions. It can be used to enable and shutdown the outputs of the driver, and reset the fault signaled on the  $\overline{\text{FLT}}$  pin.  $\overline{\text{RST/EN}}$  pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. With a 50k $\Omega$  pulldown resistor existing, the driver is disabled by default.

When the driver is latched after overcurrent or short circuit fault is detected, the  $\overline{\text{FLT}}$  pin and output are latched low and need to be reset by  $\overline{\text{RST/EN}}$  pin.  $\overline{\text{RST/EN}}$  pin is active low. The microcontroller needs to send a signal to  $\overline{\text{RST/EN}}$  pin after the fault mute time  $t_{\text{FLTMUTE}}$  to reset the driver. This pin can also be used to automatically reset the driver. The continuous input signal  $\text{IN}+$  or  $\text{IN}-$  can be applied to  $\overline{\text{RST/EN}}$  pin, so the microcontroller does not need to generate another control signal to reset the driver. If non-inverting input  $\text{IN}+$  is used, then  $\text{IN}+$  can be tied to  $\overline{\text{RST/EN}}$  pin. If inverting input  $\text{IN}-$  is used, then a NOT logic is needed between the inverting PWM signal from the microcontroller and the  $\overline{\text{RST/EN}}$  pin. In this case, the driver can be reset in every switching cycle without an extra control signal from microcontroller to  $\overline{\text{RST/EN}}$  pin.


**Figure 49. Automatic Reset Control**

### 9.2.2.5 Turn on and turn off gate resistors

UCC21732-Q1 features split outputs OUTH and OUTL, which enables the independent control of the turn on and turn off switching speed. The turn on and turn off resistance determine the peak source and sink current, which controls the switching speed in turn. Meanwhile, the power dissipation in the gate driver should be considered to ensure the device is in the thermal limit. At first, the peak source and sink current are calculated as:

$$I_{\text{source\_pk}} = \min\left(10\text{A}, \frac{V_{\text{DD}} - V_{\text{EE}}}{R_{\text{OH\_EFF}} + R_{\text{ON}} + R_{\text{G\_Int}}}\right)$$

$$I_{\text{sink\_pk}} = \min\left(10\text{A}, \frac{V_{\text{DD}} - V_{\text{EE}}}{R_{\text{OL}} + R_{\text{OFF}} + R_{\text{G\_Int}}}\right)$$

(1)

Where

- $R_{\text{OH\_EFF}}$  is the effective internal pull up resistance of the hybrid pull-up structure, which is approximately 2 x  $R_{\text{OL}}$ , about 0.7  $\Omega$
- $R_{\text{OL}}$  is the internal pulldown resistance, about 0.3  $\Omega$
- $R_{\text{ON}}$  is the external turn on gate resistance
- $R_{\text{OFF}}$  is the external turn off gate resistance
- $R_{\text{G\_Int}}$  is the internal resistance of the SiC MOSFET or IGBT module

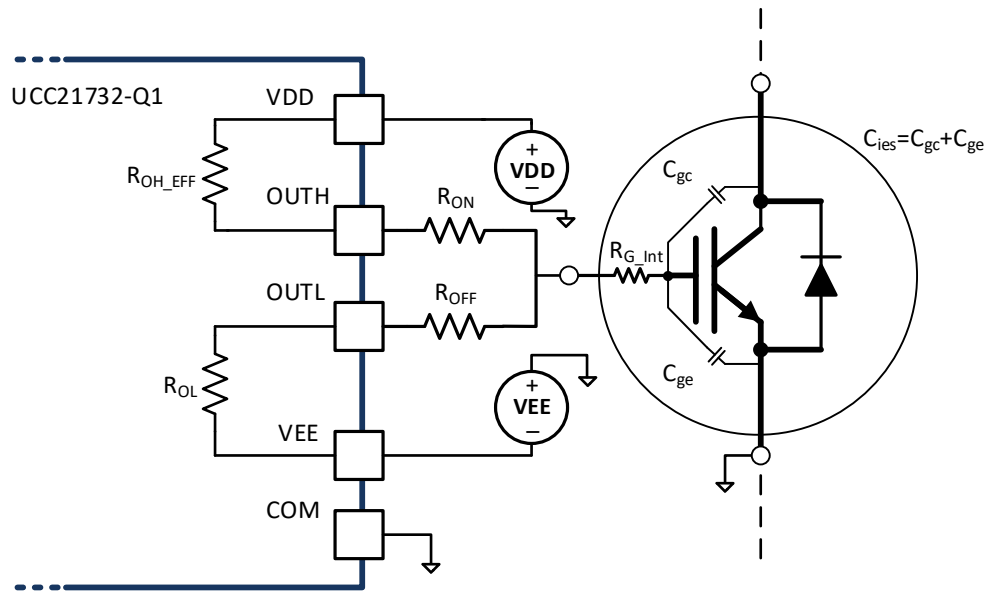


Figure 50. Output Model for Calculating Peak Gate Current

For example, for an IGBT module based system with the following parameters:

- $Q_g = 3300 \text{ nC}$
- $R_{G\_Int} = 1.7 \Omega$
- $R_{ON}=R_{OFF}= 1 \Omega$

The peak source and sink current in this case are:

$$I_{\text{source\_pk}} = \min\left(10\text{A}, \frac{V_{DD} - V_{EE}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}}\right) \approx 5.9\text{A}$$

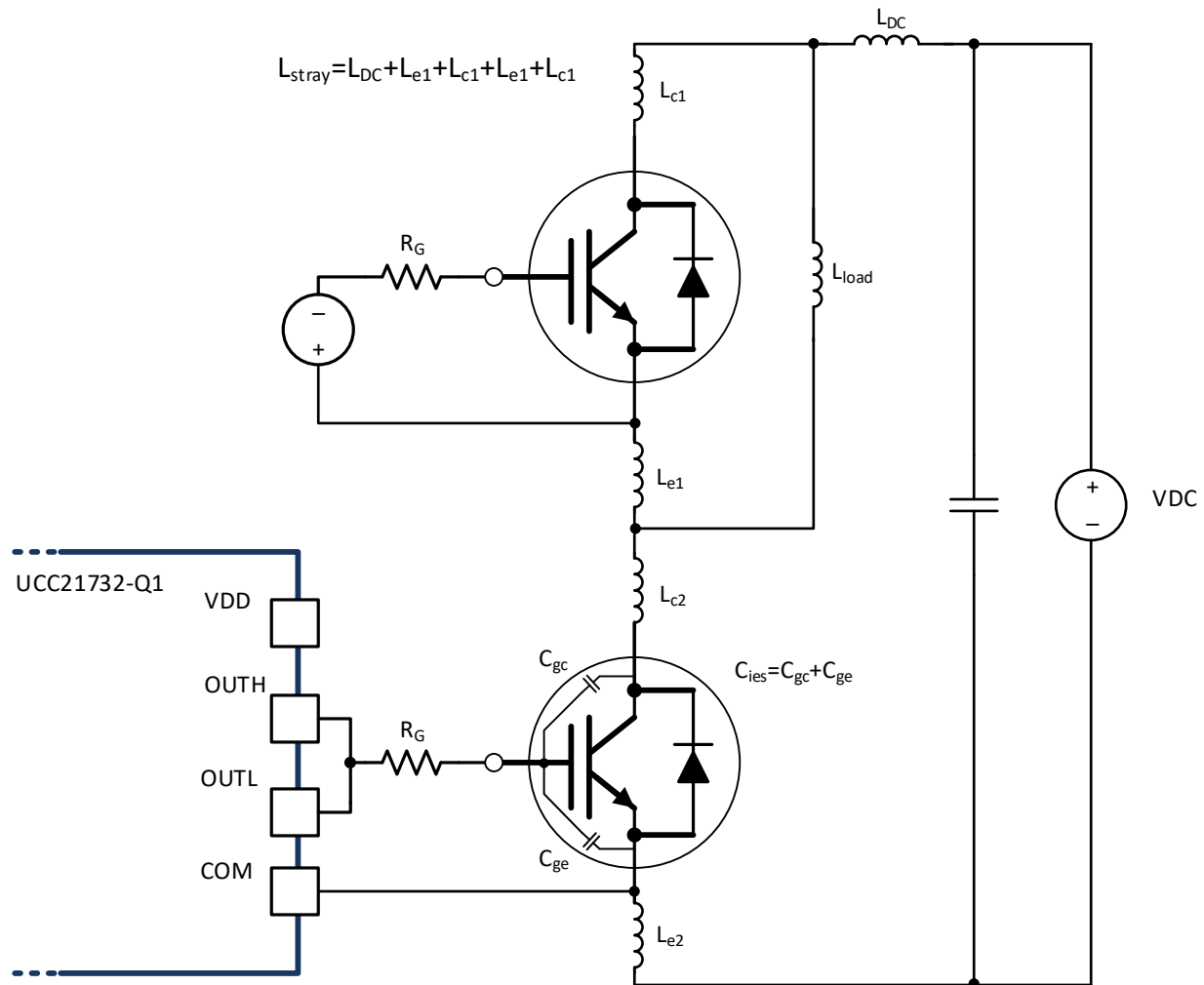
$$I_{\text{sink\_pk}} = \min\left(10\text{A}, \frac{V_{DD} - V_{EE}}{R_{OL} + R_{OFF} + R_{G\_Int}}\right) \approx 6.7\text{A}$$
(2)

Thus by using  $1\Omega$  external gate resistance, the peak source current is 5.9A, the peak sink current is 6.7A. The collector-to-emitter  $dV/dt$  during the turn on switching transient is dominated by the gate current at the miller plateau voltage. The hybrid pullup structure ensures the peak source current at the miller plateau voltage, unless the turn on gate resistor is too high. The faster the collector-to-emitter,  $V_{ce}$ , voltage rises to  $V_{DC}$ , the smaller the turn on switching loss is. The  $dV/dt$  can be estimated as  $Q_{gc}/I_{\text{source\_pk}}$ . For the turn off switching transient, the drain-to-source  $dV/dt$  is dominated by the load current, unless the turn off gate resistor is too high. After  $V_{ce}$  reaches the dc bus voltage, the power semiconductor is in saturation mode and the channel current is controlled by  $V_{ge}$ . The peak sink current determines the  $dI/dt$ , which dominates the  $V_{ce}$  voltage overshoot accordingly. If using relatively large turn off gate resistance, the  $V_{ce}$  overshoot can be limited. The overshoot can be estimated by:

$$\Delta V_{ce} = L_{\text{stray}} \cdot I_{\text{load}} / ((R_{OFF} + R_{OL} + R_{G\_Int}) \cdot C_{ies} \cdot \ln(V_{\text{plat}} / V_{th}))$$
(3)

Where

- $L_{\text{stray}}$  is the stray inductance in power switching loop, as shown in Figure 51
- $I_{\text{load}}$  is the load current, which is the turn off current of the power semiconductor
- $C_{ies}$  is the input capacitance of the power semiconductor
- $V_{\text{plat}}$  is the plateau voltage of the power semiconductor
- $V_{th}$  is the threshold voltage of the power semiconductor



**Figure 51. Stray Parasitic Inductance of IGBTs in a Half-Bridge Configuration**

The power dissipation should be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as:

$$P_{DR} = P_Q + P_{SW} \quad (4)$$

$P_Q$  is the quiescent power loss for the driver, which is  $I_q \times (VDD - VEE) = 5\text{mA} \times 20\text{V} = 0.100\text{W}$ . The quiescent power loss is the power consumed by the internal circuits such as the input stage, reference voltage, logic circuits, protection circuits when the driver is switching when the driver is biased with VDD and VEE, and also the charging and discharging current of the internal circuit when the driver is switching. The power dissipation when the driver is switching can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left( \frac{R_{OH\_EFF}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G\_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g \quad (5)$$

Where

- $Q_g$  is the gate charge required at the operation point to fully charge the gate voltage from VEE to VDD
- $f_{sw}$  is the switching frequency

In this example, the  $P_{SW}$  can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left( \frac{R_{OH\_EFF}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G\_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g = 0.505\text{W} \quad (6)$$

Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.10W + 0.505W = 0.605W \quad (7)$$

When the board temperature is 125°C, the junction temperature can be estimated as:

$$T_j = T_b + \psi_{jb} \cdot P_{DR} \approx 150^\circ\text{C} \quad (8)$$

Therefore, for the application in this example, with 125°C board temperature, the maximum switching frequency is ~50kHz to keep the gate driver in the thermal limit. By using a lower switching frequency, or increasing external gate resistance, the gate driver can be operated at a higher switching frequency.

### 9.2.2.6 External Active Miller Clamp

External active miller clamp feature allows the gate driver to stay at the low status when the gate voltage is detected below  $V_{CLMP_{TH}}$ . When the other switch of the phase leg turns on, the  $dV/dt$  can cause a current through the parasitic miller capacitance of the switch and sink in the gate driver. The sinking current causes a negative voltage drop on the turn off gate resistance, and bumps up the gate voltage to cause a false turn on. The external active miller clamp features allows flexibility of board layout and active miller clamp pulldown strength. Limited by the board layout, if the driver cannot be placed close enough to the switch, external active miller clamp MOSFET can be placed close to the switch and the MOSFET can be chosen according to the peak current needed. Caution must be exercised when the driver is place far from the power semiconductor. Since the device has high peak sink and source current, the high  $dI/dt$  in the gate loop can cause a ground bounce on the board parasitics. The ground bounce can cause a positive voltage bump on CLMPE pin during the turn off transient, and results in the external active miller clamp MOSFET to turn on shortly and add extra drive strength to the sink current. To reduce the ground bounce, a  $2\Omega$  resistance is recommended to the gate of the external active clamp MOSFET.

When the  $V_{OUTH}$  is detected to be lower than  $V_{CLMP_{TH}}$  above VEE, the CLMPE pin outputs a 5V voltage with respect to VEE, the external clamp FET is in linear region and the pulldown current is determined by the peak drain current, unless the on-resistance of the external clamp FET is large.

$$I_{CLMPE\_PK} = \min(I_{D\_PK}, \frac{V_{DS}}{R_{DS\_ON}}) \quad (9)$$

Where

- $I_{D\_PK}$  is the peak drain current of the external clamp FET
- $V_{DS}$  is the drain-to-source voltage of the clamp FET when the CLMPE is activated
- $R_{DS\_ON}$  is the on-resistance of the external clamp FET

The total delay time of the active miller clamp circuit from the gate voltage detection threshold  $V_{CLMP_{TH}}$  can be calculated as  $t_{DCLMPE} + t_{CLMPER}$ .  $t_{CLMPER}$  depends on the parameter of the external active miller clamp MOSFET. As long as the total delay time is longer than the deadtime of high side and low side switches, the driver can effectively protect the switch from false turn on issue caused by miller effect.





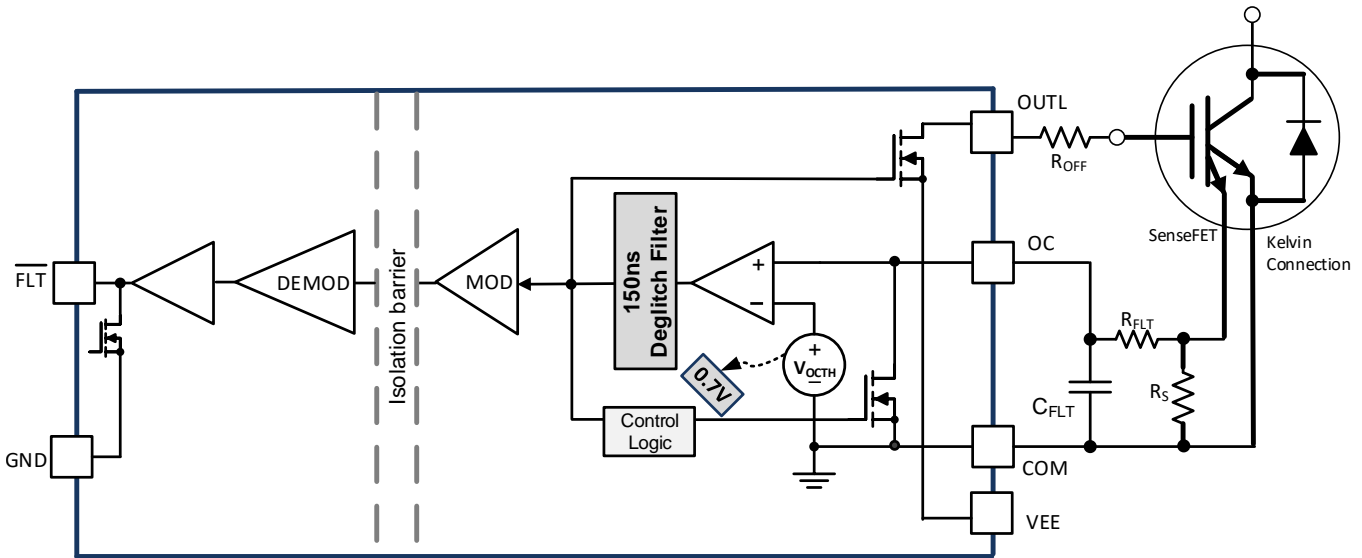


Figure 53. Overcurrent and Short Circuit Protection Based on IGBT Module with SenseFET

#### 9.2.2.7.2 Protection Based on Desaturation Circuit

For SiC MOSFET and IGBT modules without SenseFET, desaturation (DESAT) circuit is the most popular circuit which is adopted for overcurrent and short circuit protection. The circuit consists of a current source, a resistor, a blanking capacitor and a diode. Normally the current source is provided from the gate driver, when the device turns on, a current source charges the blanking capacitor and the diode forward biased. During normal operation, the capacitor voltage is clamped by the switch  $V_{CE}$  voltage. When short circuit happens, the capacitor voltage is quickly charged to the threshold voltage which triggers the device shutdown. For the UCC21732-Q1, the OC pin does not feature an internal current source. The current source should be generated externally from the output power supply. When UCC21732-Q1 is in OFF state, the OC pin is pulled down by an internal MOSFET, which creates an offset voltage on OC pin. By choosing  $R_1$  and  $R_2$  significantly higher than the pulldown resistance of the internal MOSFET, the offset can be ignored. When UCC21732-Q1 is in ON state, the OC pin is high impedance. The current source is generated by the output power supply  $V_{DD}$  and the external resistor divider  $R_1$ ,  $R_2$  and  $R_3$ . The overcurrent detection threshold voltage of the IGBT is:

$$V_{DET} = V_{OCTH} \cdot \frac{R_2 + R_3}{R_3} - V_F \quad (11)$$

The blanking time of the detection circuit is:

$$t_{BLK} = -\frac{R_1 + R_2}{R_1 + R_2 + R_3} \cdot R_3 \cdot C_{BLK} \cdot \ln\left(1 - \frac{R_1 + R_2 + R_3}{R_3} \cdot \frac{V_{OCTH}}{V_{DD}}\right) \quad (12)$$

Where:

- $V_{OCTH}$  is the detection threshold voltage of the gate driver
- $R_1$ ,  $R_2$  and  $R_3$  are the resistance of the voltage divider
- $C_{BLK}$  is the blanking capacitor
- $V_F$  is the forward voltage of the high voltage diode  $D_{HV}$

The modified desaturation circuit has all the benefits of the conventional desaturation circuit. The circuit has negligible power loss, and is easy to implement. The detection threshold voltage of IGBT and blanking time can be programmed by external components. Different with the conventional desaturation circuit, the overcurrent detection threshold voltage of the IGBT can be modified to any voltage level, either higher or lower than the detection threshold voltage of the driver. A parallel schottky diode can be connected between OC and COM pins to prevent the negative voltage on the OC pin in noisy system. Since the desaturation circuit measures the  $V_{CE}$  of the IGBT or  $V_{DS}$  of the SiC MOSFET, not directly the current, the accuracy of the protection is not as high as the SenseFET based protection method. The current threshold cannot be accurately controlled in the protection.

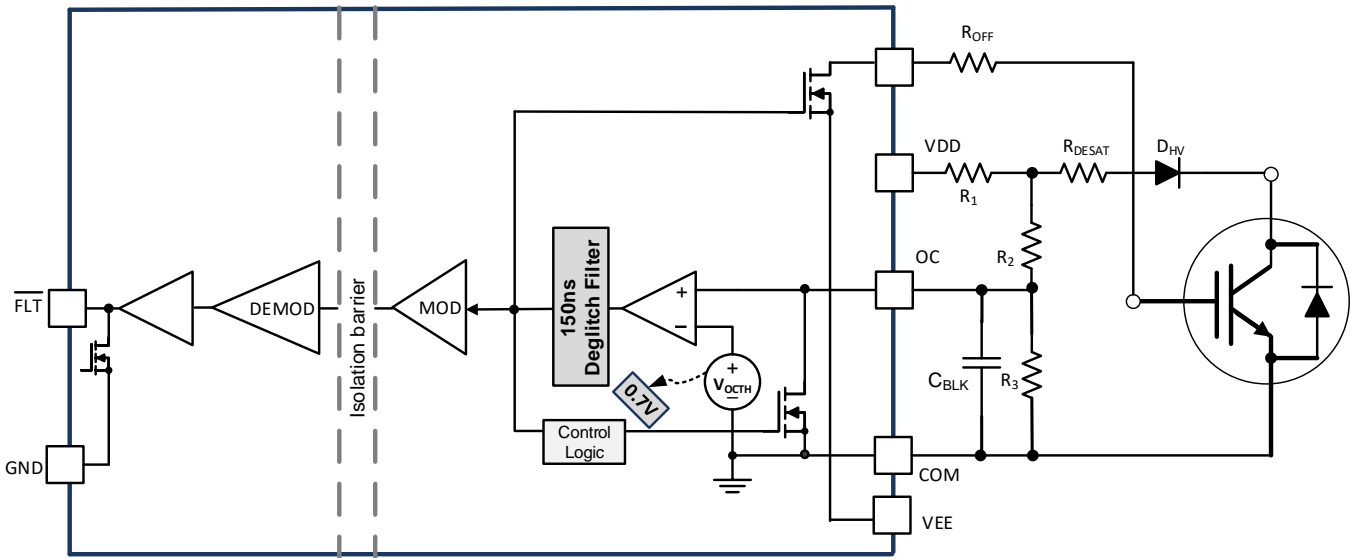


Figure 54. Overcurrent and Short Circuit Protection Based on Desaturation Circuit

9.2.2.7.3 Protection Based on Shunt Resistor in Power Loop

In lower power applications, to simplify the circuit and reduce the cost, a shunt resistor can be used in series in the power loop and measure the current directly. Since the resistor is in series in the power loop, it directly measures the current and can have high accuracy by using a high precision resistor. The resistance needs to be small to reduce the power loss, and should have large enough voltage resolution for the protection. Since the sensing resistor is also in series in the gate driver loop, the voltage drop on the sensing resistor can cause the voltage drop on the gate voltage of the IGBT or SiC MOSFET modules. The parasitic inductance of the sensing resistor and the PCB trace of the sensing loop will also cause a noise voltage source during switching transient, which makes the gate voltage oscillate. Thus, this method is not recommended for high power application, or when  $di/dt$  is high. To use it in low power application, the shunt resistor loop should be designed to have the optimal voltage drop and minimum noise injection to the gate loop.

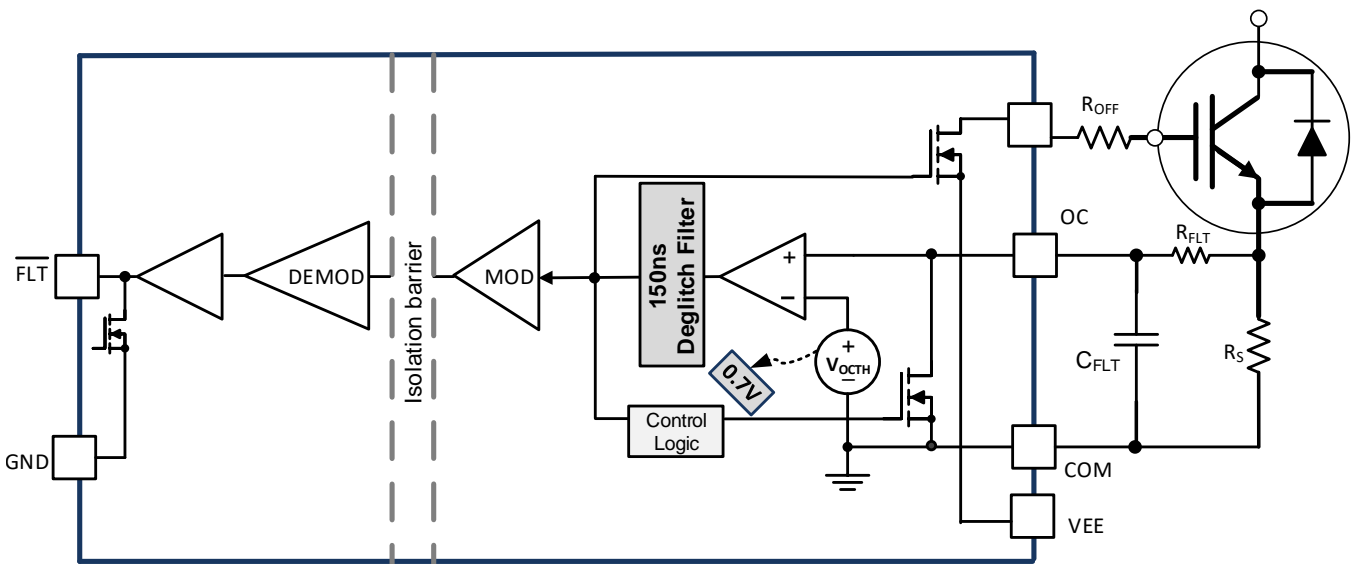


Figure 55. Overcurrent and Short Circuit Protection Based on Shunt Resistor

### 9.2.2.8 Isolated Analog Signal Sensing

The isolated analog signal sensing feature provides a simple isolated channel for the isolated temperature detection, voltage sensing and etc. One typical application of this function is the temperature monitor of the power semiconductor. Thermal diodes or temperature sensing resistors are integrated in the SiC MOSFET or IGBT module close to the dies to monitor the junction temperature. UCC21732-Q1 has an internal 200uA current source with 3% accuracy across temperature, which can forward bias the thermal diodes or create a voltage drop on the temperature sensing resistors. The sensed voltage from the AIN pin is passed through the isolation barrier to the input side and transformed to a PWM signal. The duty cycle of the PWM changes linearly from 10% to 88% when the AIN voltage changes from 4.5V to 0.6V and can be represented using Equation 13.

$$D_{APWM}(\%) = -20 * V_{AIN} + 100 \quad (13)$$

#### 9.2.2.8.1 Isolated Temperature Sensing

A typical application circuit is shown in Figure 56. To sense temperature, the AIN pin is connected to the thermal diode or thermistor which can be discrete or integrated within the power module. A low pass filter is recommended for the AIN input. Since the temperature signal does not have a high bandwidth, the low pass filter is mainly used for filtering the noise introduced by the switching of the power device, which does not require stringent control for propagation delay. The filter capacitance for  $C_{filt}$  can be chosen between 1nF to 100nF and the filter resistance  $R_{filt}$  between 1Ω to 10Ω according to the noise level.

The output of APWM is directly connected to the microcontroller to measure the duty cycle dependent on the voltage input at AIN, using Equation 13.

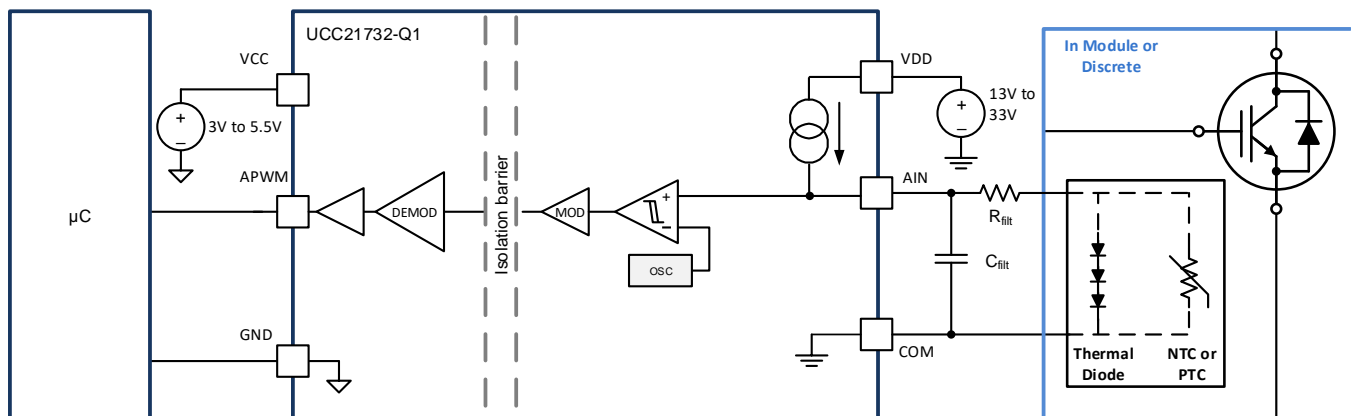


Figure 56. Thermal Diode or Thermistor Temperature Sensing Configuration

When a high-precision voltage supply for VCC is used on the primary side of UCC21732-Q1 the duty cycle output of APWM may also be filtered and the voltage measured using the microcontroller's ADC input pin, as shown in Figure 57. The frequency of APWM is 400kHz, so the value for  $R_{filt\_2}$  and  $C_{filt\_2}$  should be such that the cutoff frequency is below 400kHz. Temperature does not change rapidly, thus the rise time due to the RC constant of the filter is not under a strict requirement.

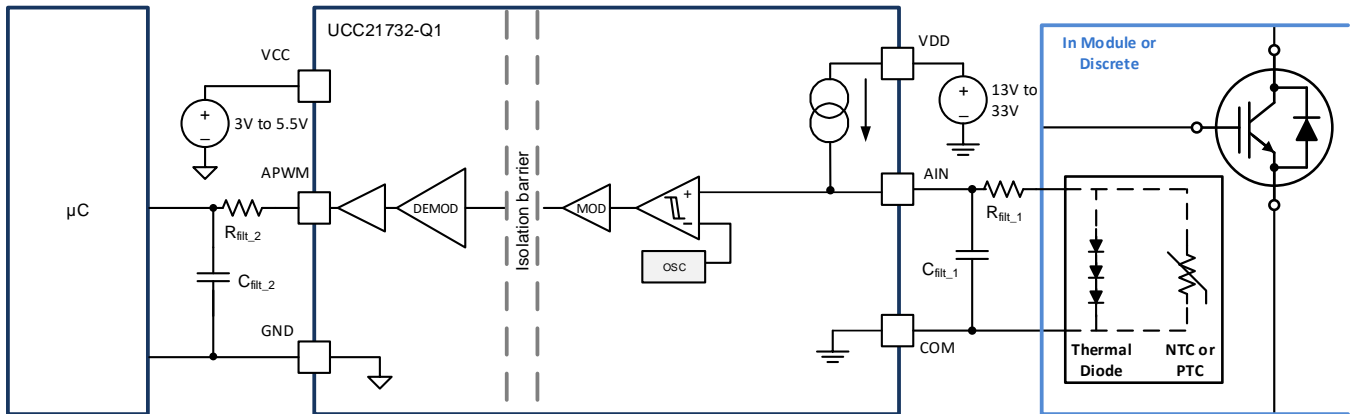


Figure 57. APWM Channel with Filtered Output

The example below shows the results using a 4.7kΩ NTC, NTCS0805E3472FMT, in series with a 3kΩ resistor and also the thermal diode using four diode-connected MMBT3904 NPN transistors. The sensed voltage of the 4 MMBT3904 thermal diodes connected in series ranges from about 2.5V to 1.6V from 25°C to 135°C, corresponding to 50% to 68% duty cycle. The sensed voltage of the NTC thermistor connected in series with the 3kΩ resistor ranges from about 1.5V to 0.6V from 25°C to 135°C, corresponding to 70% to 88% duty cycle. The voltage at VAIN of both sensors and the corresponding measured duty cycle at APWM is shown in Figure 58.

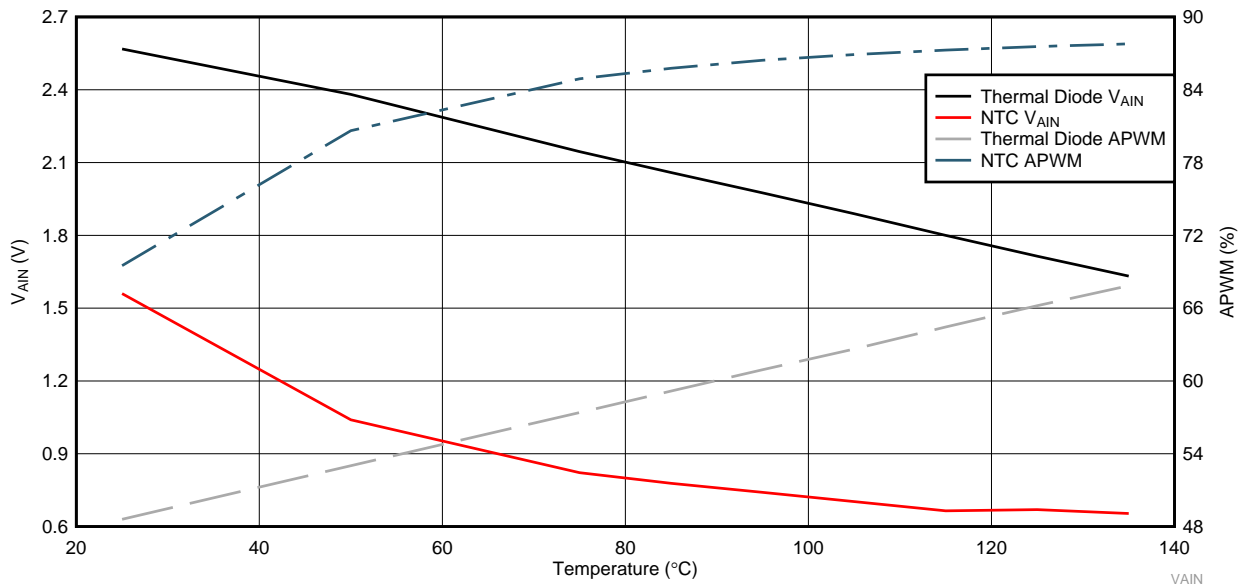


Figure 58. Thermal diode and NTC  $V_{AIN}$  and Corresponding Duty Cycle at APWM

The duty cycle output has an accuracy of  $\pm 3\%$  throughout temperature without any calibration, as shown in Figure 59 but with single-point calibration at 25°C, the duty accuracy can be improved to  $\pm 1\%$ , as shown in Figure 60.

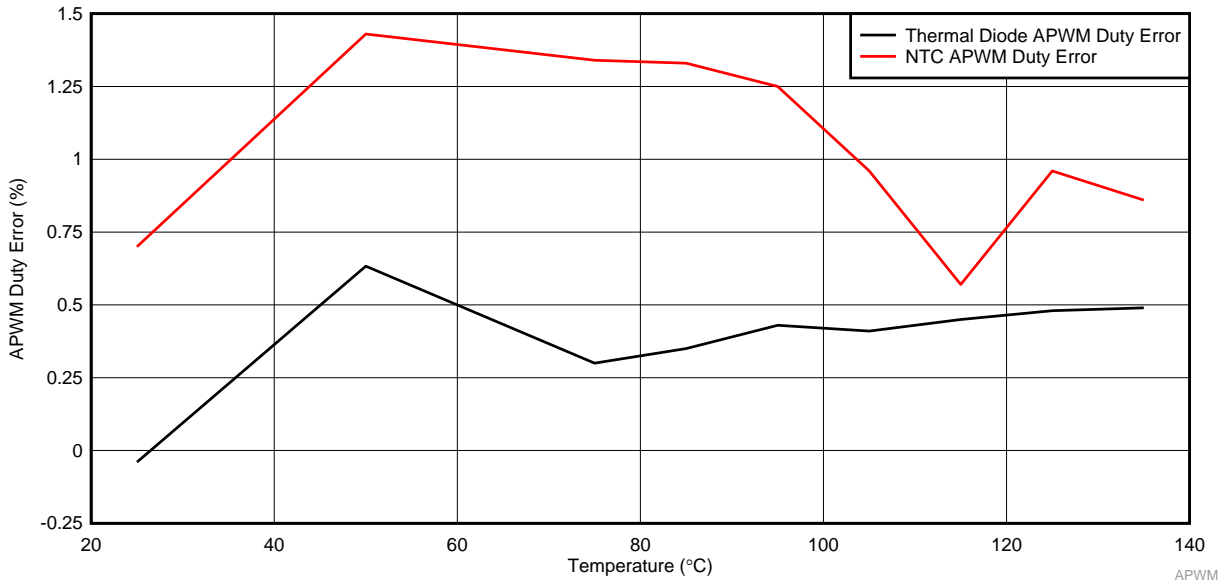


Figure 59. APWM Duty Error Without Calibration

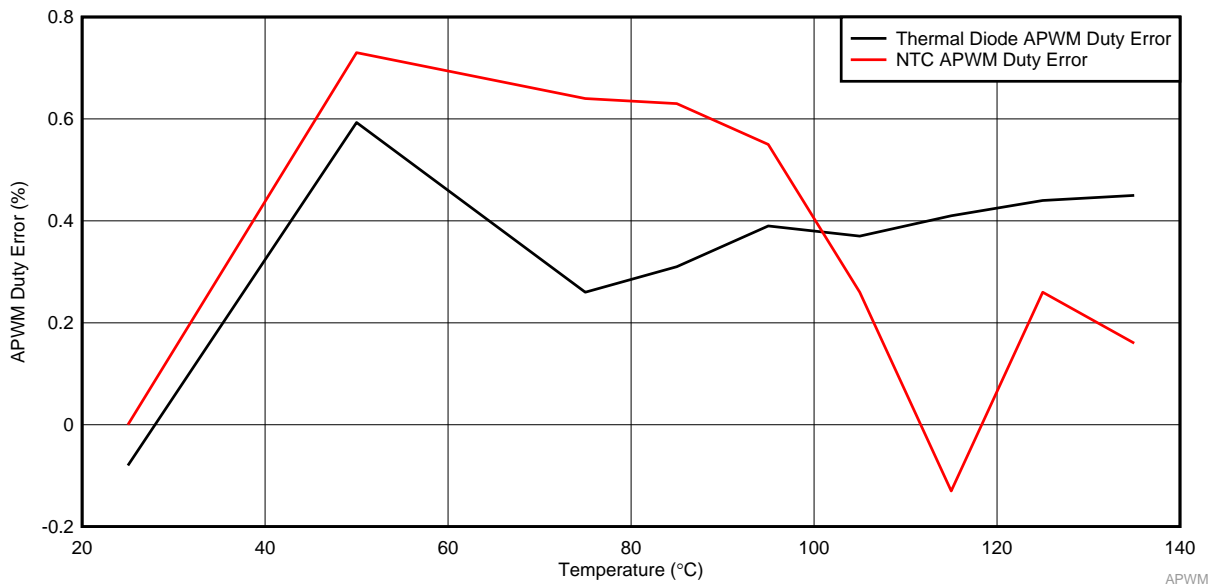


Figure 60. APWM Duty Error with Single-Point Calibration

9.2.2.8.2 Isolated DC Bus Voltage Sensing

The AIN to APWM channel may be used for other applications such as the DC-link voltage sensing, as shown in Figure 61. The same filtering requirements as given above may be used in this case, as well. The number of attenuation resistors,  $R_{atten\_1}$  through  $R_{atten\_n}$ , is dependent on the voltage level and power rating of the resistor. The voltage is finally measured across  $R_{LV\_DC}$  to monitor the stepped-down voltage of the HV DC-link which must fall within the voltage range of AIN from 0.6V to 4.5V. The driver should be referenced to the same point as the measurement reference, thus in the case shown below the UCC21732-Q1 is driving the lower IGBT in the half-bridge and the DC-link voltage measurement is referenced to COM. The internal current source  $I_{AIN}$  should be taken into account when designing the resistor divider. The AIN pin voltage is:

$$V_{AIN} = \frac{R_{LV\_DC}}{R_{LV\_DC} + \sum_{i=1}^n R_{atten\_i}} \cdot V_{DC} + R_{LV\_DC} \cdot I_{AIN} \tag{14}$$

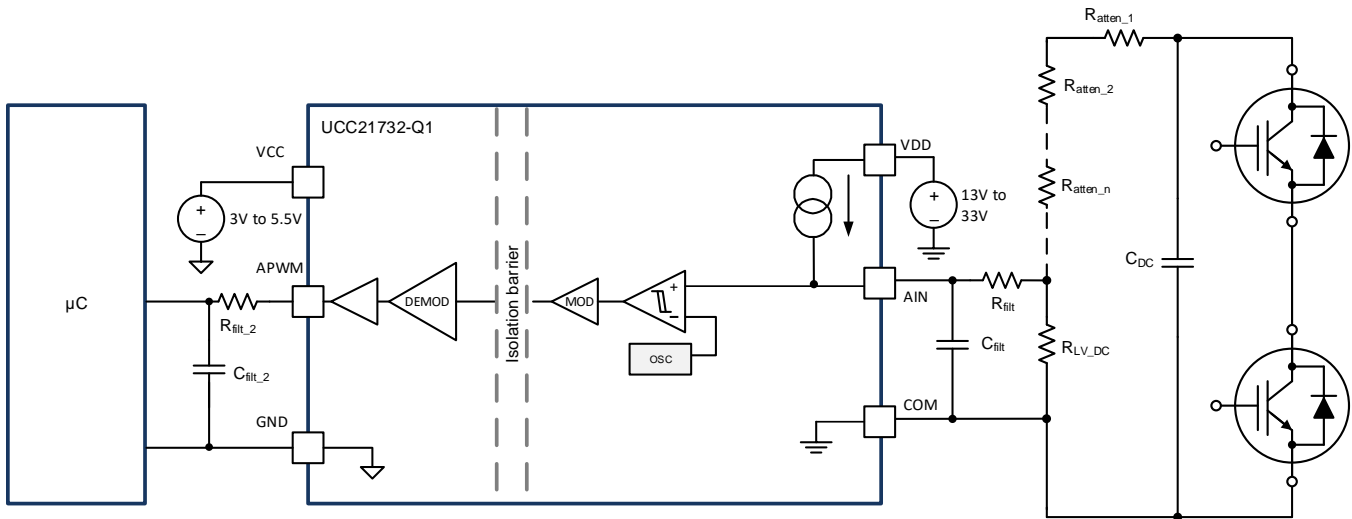


Figure 61. DC-link Voltage Sensing Configuration

**9.2.2.9 Higher Output Current Using an External Current Buffer**

To increase the IGBT gate drive current, a non-inverting current buffer (such as the NPN/PNP buffer shown in Figure 62) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for peak currents up to 15 A, the D44VH10/D45VH10 pair is up to 20 A peak.

In the case of a over-current detection, the soft turn off (STO) is activated. External components must be added to implement STO instead of normal turn off speed when an external buffer is used. C<sub>STO</sub> sets the timing for soft turn off and R<sub>STO</sub> limits the inrush current to below the current rating of the internal FET (10A). R<sub>STO</sub> should be at least (VDD-VEE)/10. The soft turn off timing is determined by the internal current source of 400mA and the capacitor C<sub>STO</sub>. C<sub>STO</sub> is calculated using .

$$C_{STO} = \frac{I_{STO} \cdot t_{STO}}{VDD - VEE} \tag{15}$$

- I<sub>STO</sub> is the the internal STO current source, 400mA
- t<sub>STO</sub> is the desired STO timing

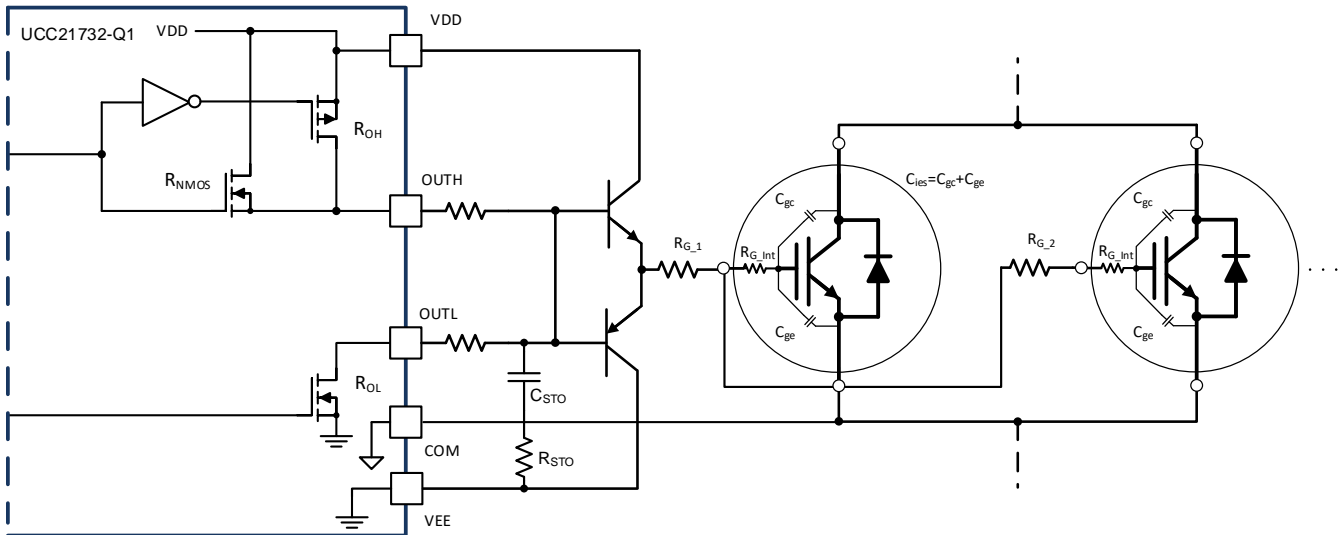


Figure 62. Current Buffer for Increased Drive Strength

## 10 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink current is provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering UCC21732-Q1 has  $\pm 10\text{A}$  peak drive strength and can generate high  $dV/dt$ , a  $10\mu\text{F}$  bypass cap is recommended between VDD and COM, VEE and COM. A  $1\mu\text{F}$  bypass cap is recommended between VCC and GND due to less current comparing with output side power supplies. A  $0.1\mu\text{F}$  decoupling cap is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

## 11 Layout

### 11.1 Layout Guidelines

Due to the strong drive strength of UCC21732-Q1, careful considerations must be taken in PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high  $di/dt$  and voltage spike on the parasitic inductance of PCB traces
- The driver COM pin should be connected to the Kelvin connection of SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow
- If the gate driver is used for the low side switch which the COM pin connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high side switch, which the COM pin is connected to the switch node, ground plane is not recommended
- If ground plane is not used on the output side, separate the return path of the OC and AIN ground loop from the gate loop ground which has large peak source and sink current
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier



## 11.2 Layout Example

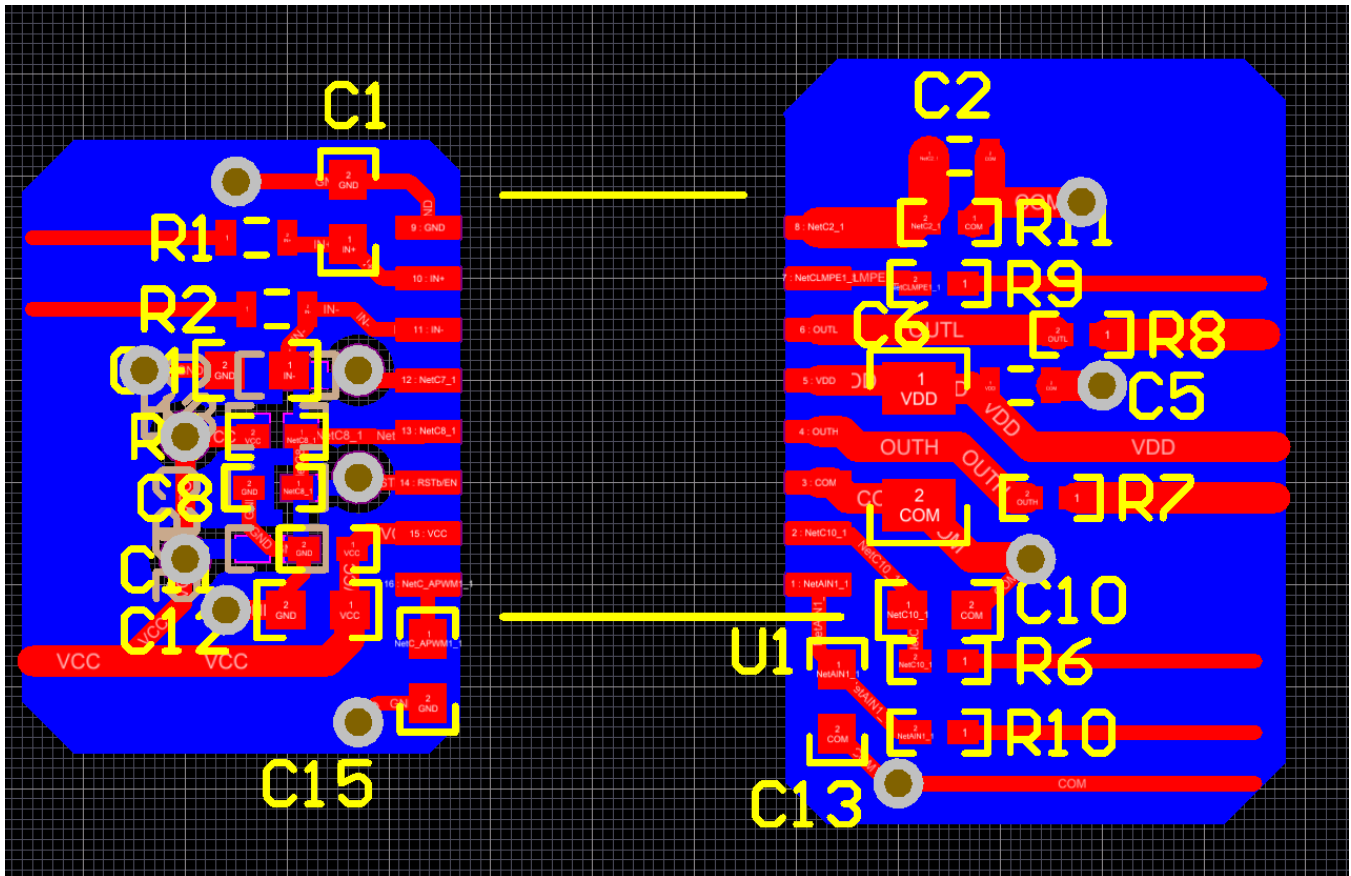


Figure 63. Layout Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- [Isolation Glossary](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resource

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

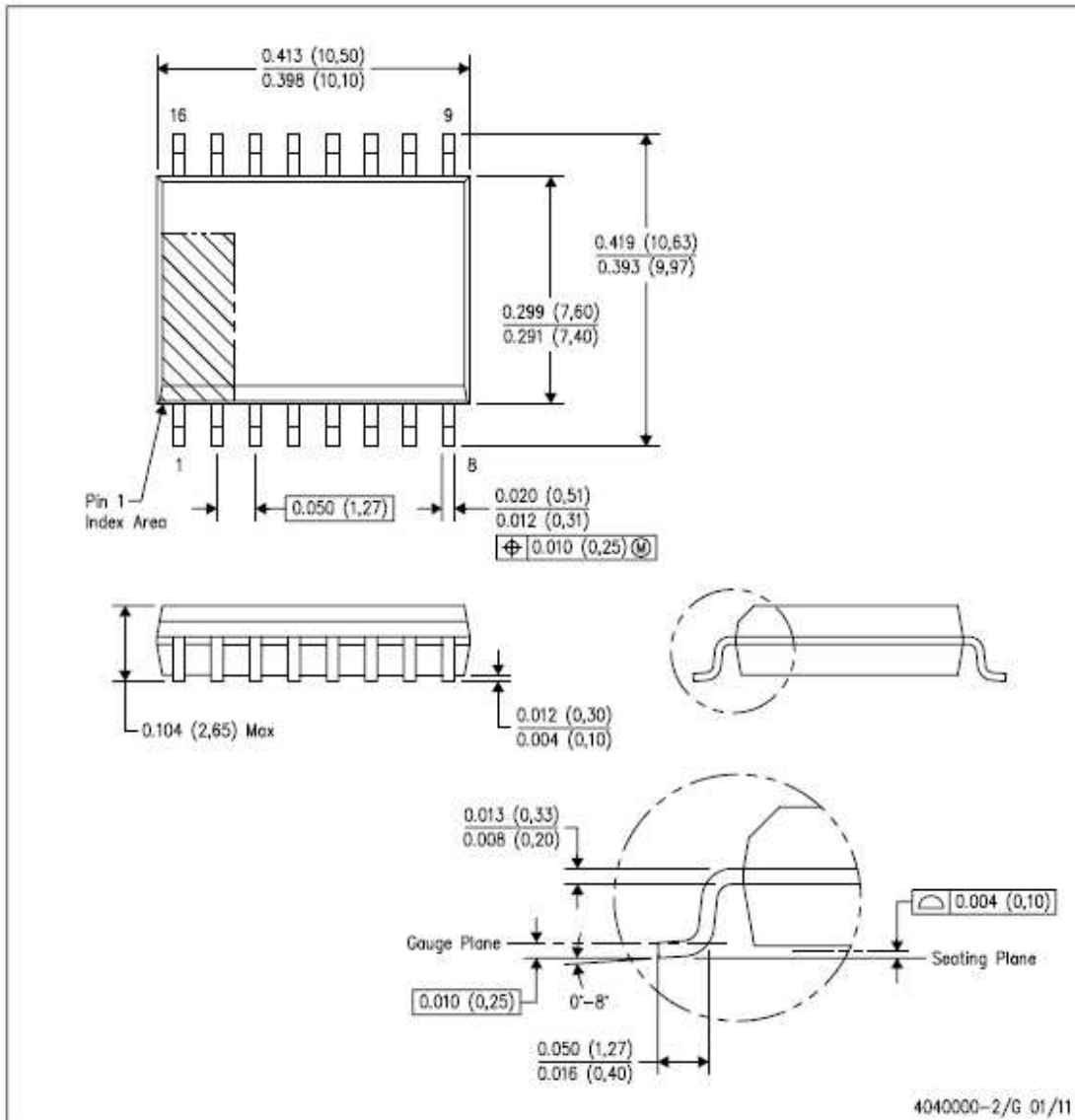
## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**MECHANICAL DATA**

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21732QDWQ1	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21732Q	<a href="#">Samples</a>
UCC21732QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21732Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF UCC21732-Q1 :**

- Catalog: [UCC21732](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## GENERIC PACKAGE VIEW

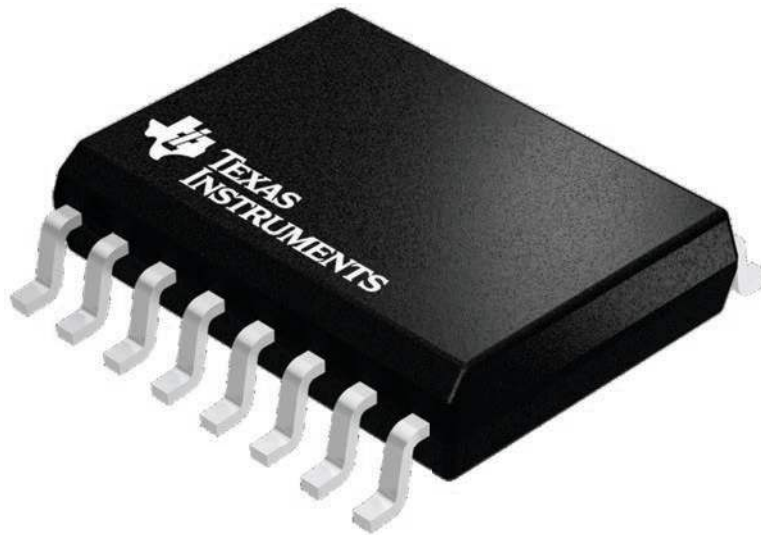
**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A

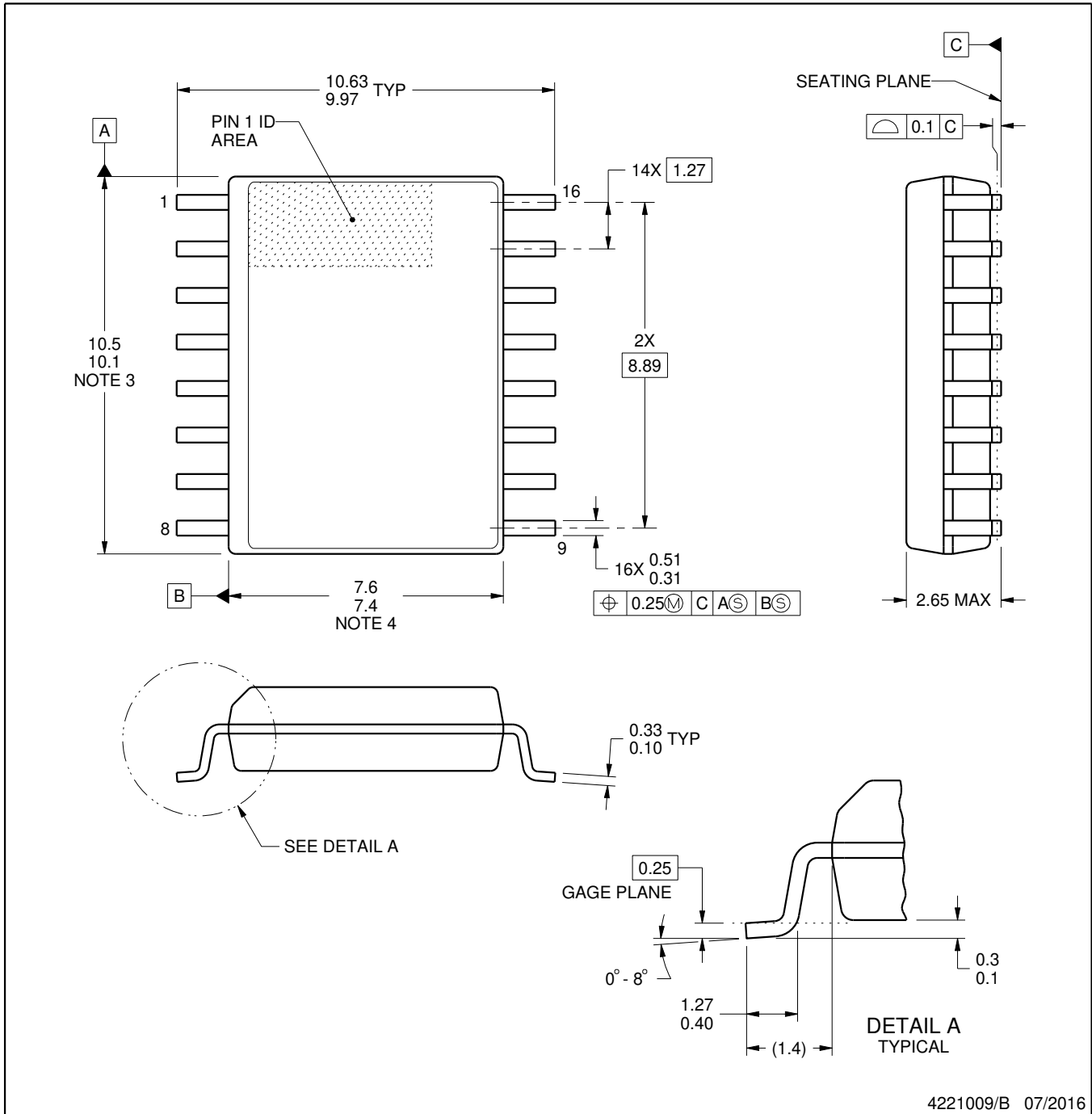


# DW0016B

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

### NOTES:

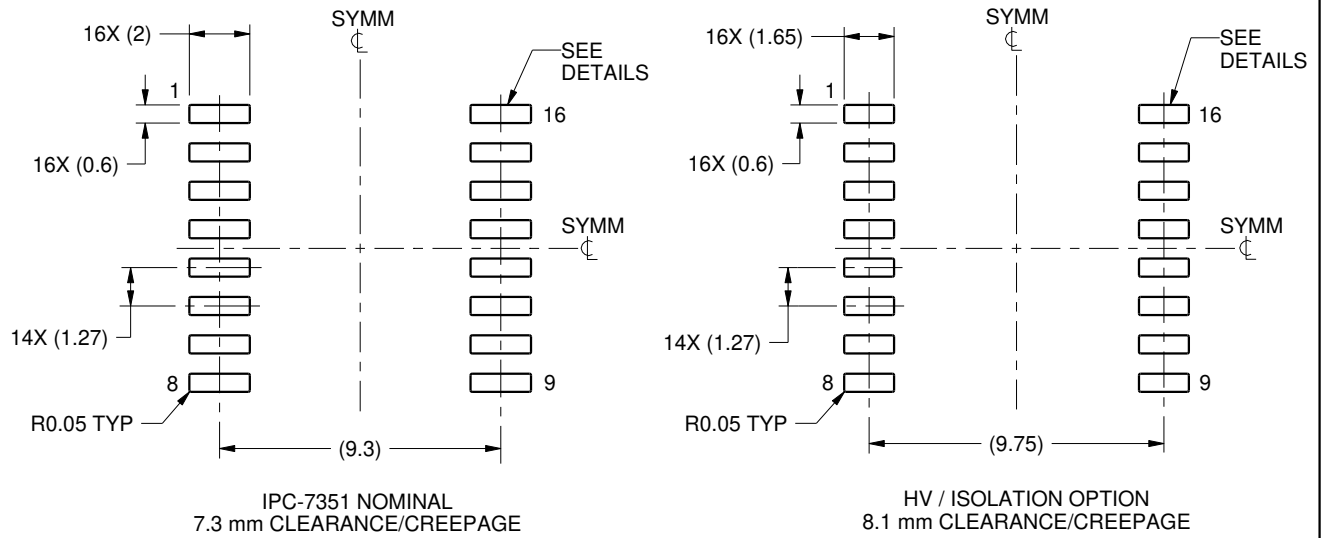
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

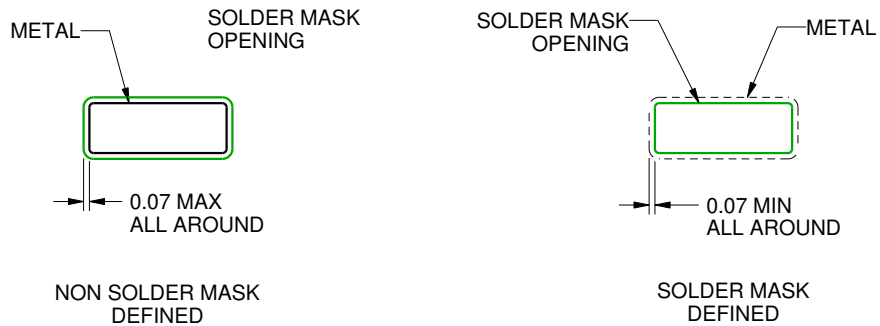
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

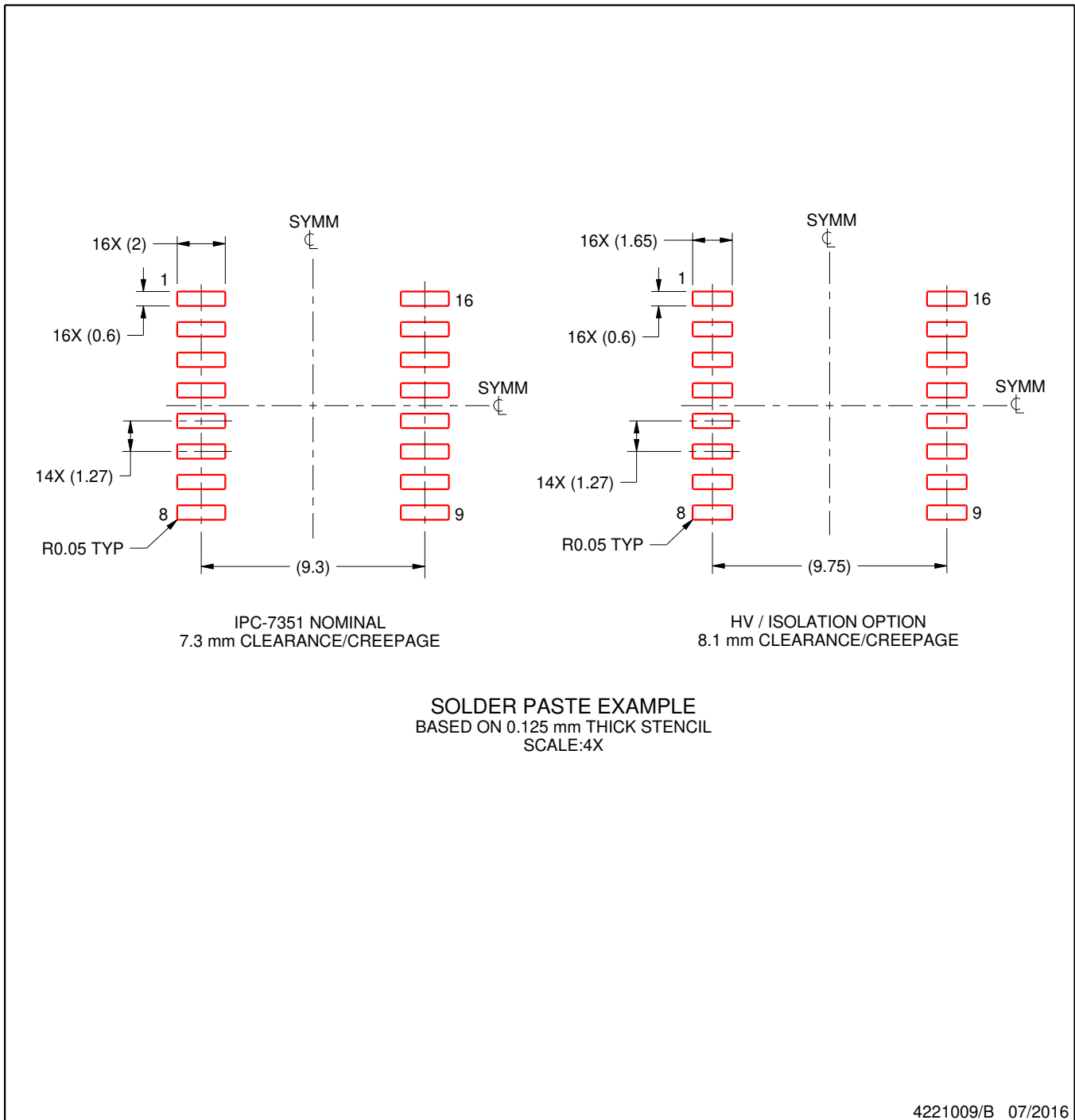


# EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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