

# Inverting Regulator – Buck, Boost, Switching

### **DESCRIPTION**

TS34063 is a monolithic switching regulator and subsystem intended for use as DC-to-DC converter. It consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active peak current limit circuit, driver and high current output switch. The TS34063 is specifically designed to be incorporated in Step-Up, Step-Down and Voltage-Inverting applications with minimum number of external components.

#### **FEATURES**

- Power forward control circuit
- Operating voltage from 3V to 40V
- Low standby current
- Current limit adjustable
- Output switch current up to 1.5A
- Variable oscillator frequency up to 100kHz (max.)
- Output voltage adjustable
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

#### **APPLICATION**

- Charger
- xD-ROM, xDSL products
- DC to DC converter



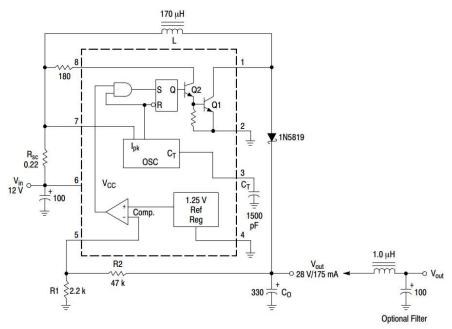


#### Pin Definition:

- 1. Switch Collector
- 2. Switch Emitter
- 3. Timing Capacitor
- 4. GND
- 5. Comparator Inverting Input
- 6. V<sub>CC</sub>
- 7. lpk
- 8. Driver Collector

Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

### **TYPICAL APPLICATION CIRCUIT**



**Step-Up Converter** 

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ABSOLUTE MAXIMUM RATINGS (Note 1)	)		
PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V <sub>CC</sub>	40	V
Comparator Input Voltage Range	V <sub>FB</sub>	-0.3 ~ 40	V
Switch Collector Output Voltage	V <sub>C(SW)</sub>	40	V
Switch Emitter Voltage	V <sub>E(SW)</sub>	40	mA
Switch Collector to Emitter Voltage	V <sub>CE(SW)</sub>	40	mW
Driver Collector Voltage	V <sub>C(DRIVER)</sub>	40	°C
Driver Collector Current (note 1)	I <sub>C(DRIVER)</sub>	100	V
Output Switching Current	I <sub>sw</sub>	1.5	Α
Power Dissipation	P <sub>D</sub>	0.5	W
Operating Ambient Temperature Range	T <sub>OPR</sub>	-40 ~ +85	°C
Junction Temperature Range	TJ	0 ~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~ +150	°C

<b>ELECTRICAL SPECIFICATIONS</b> (V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C unless otherwise noted)						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator						
Frequency	Fosc	$C_T = 1nF$ , $Vpin5 = 0V$	24	33	42	kHz
Charge Current	ICHARGE	$V_{CC} = 5V \sim 40V$	24	30	42	μΑ
Discharge Current	I <sub>DISCHARGE</sub>	$V_{CC} = 5V \sim 40V$	140	200	260	μΑ
Discharge to Charge current ratio	Idischarge / Icharge	Pin7 to Vcc	5.2	6.5	7.5	1
Current Limit Sense Voltage	V <sub>IPK(SENSE)</sub>	Idischarge = Icharge	250		350	mV
Output switch (note1)						
Saturation Voltage	V <sub>CE(SAT)</sub>	Isw= 1A, Pin1, 8 connected		1.0	1.3	٧
Saturation Voltage	V <sub>CE(SAT)</sub>	Isw= 1A, I <sub>D</sub> =50mA		0.45	0.7	V
DC current gain	H <sub>FE</sub>	I <sub>SW</sub> = 1A, V <sub>CE</sub> = 0.5V	50	75		1
Collector off-state current	I <sub>C(OFF)</sub>	V <sub>CE</sub> = 40V		0.01	100	μΑ
Comparator						
Threshold Voltage	$V_{REF}$		1.225	1.25	1.275	V
Line regulation	REGLINE	$V_{CC} = 3V \sim 40V$			6	mV
Total device						
Supply Current	Icc	$V_{CC} = 5V \sim 40V, C_T = 1nF, pin7 = V_{CC},$ pin5 > $V_{TH}$ , pin2 = Gnd, remaining pins open		3	5	mA

### Note:

- 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
- 2. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300mA) and high driver currents (≥30mA), it may take up to 2μs for it to come out of saturation. This condition will shorten the off time at frequencies ≥30kHz and is magnified at high temperature. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a Non-Darlington configuration is used, the following output drive condition is recommended: Forced Bata of output switch: Ic output / (Ic driver − 7mA\*) ≥ 10

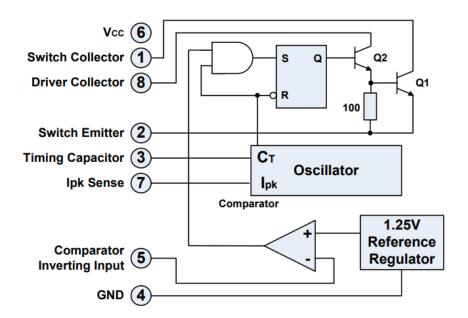
<sup>\*</sup> The 100ohm resistor in the emitter of the driver divide requires about 7mA before the output switch conducts.



## **ORDERING INFORMATION**

ORDERING CODE	PACKAGE	PACKING
TS34063CS RLG	SOP-8	2,500pcs / 13" Reel

## **BLOCK DIAGRAM**



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## **ELECTRICAL CHARACTERISTICS CURVE**

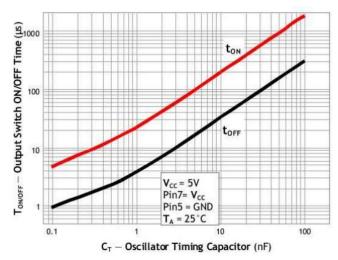


Fig 1. Output Switch On-Off Time vs. Oscillator
Timing Capacitor

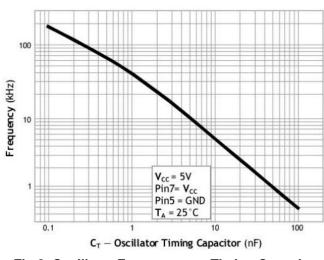


Fig 3. Oscillator Frequency vs. Timing Capacitor

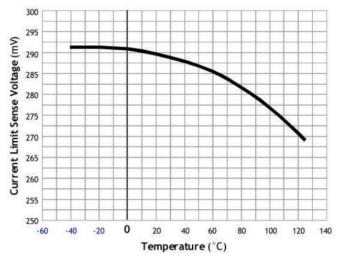


Fig 5. Current Limit Sense Voltage vs. Temperature

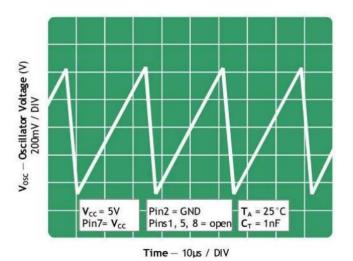


Fig 2. Timing Capacitor Wave Form

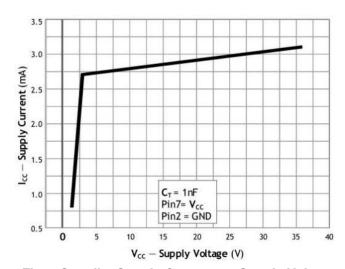
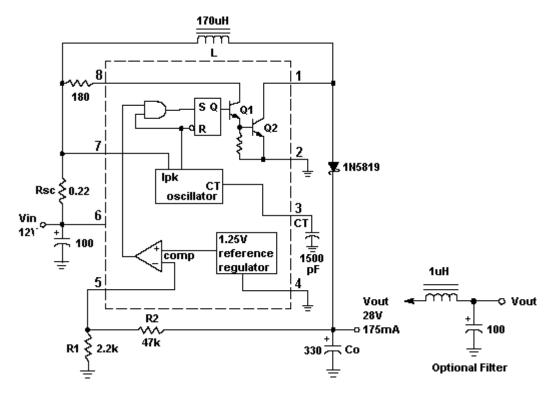


Fig 4. Standby Supply Current vs. Supply Voltage



## **TYPICAL APPLICATION CIRCUIT**



Test	Conditions	Results
Line Regulation	V <sub>IN</sub> = 8V~16V, Io= 175mA	$30mV = \pm 0.05\%$
Load Regulation	V <sub>IN</sub> = 12V, Io= 75mA to 175mA	$10mV = \pm 0.017\%$
Output Ripple	V <sub>IN</sub> =12V, Io= 175mA	400mVpp
Efficiency	V <sub>IN</sub> =12V, Io= 175mA	87.7%
Output Ripple with Optional Filter	V <sub>IN</sub> =12V, Io= 175mA	40mVpp

Fig 6. Step-Up Converter

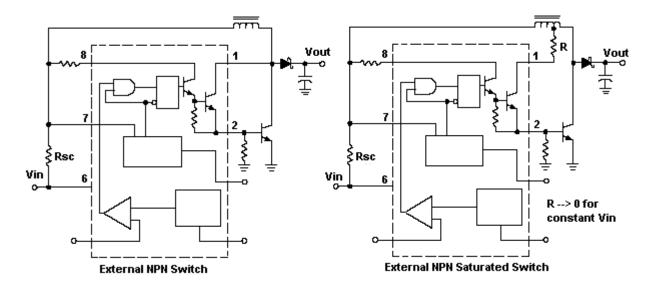
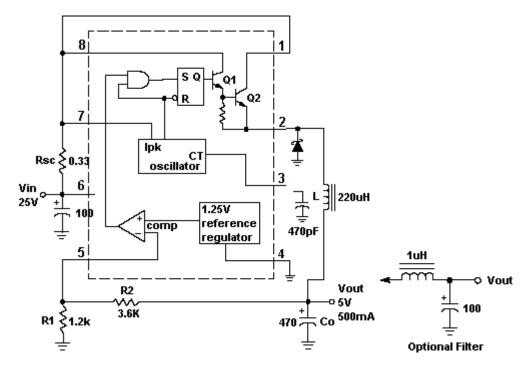


Fig. 7. External current Boost connections for IC peak greater than 1.5A



# **TYPICAL APPLICATION CIRCUIT (CONTINUE)**



Test	Conditions	Results
Line Regulation	V <sub>IN</sub> = 15V~25V, Io= 500mA	12mV = ±12%
Load Regulation	$V_{IN} = 25V$ , $Io = 50mA$ to $500mA$	$3mV = \pm 0.03\%$
Output Ripple	V <sub>IN</sub> =25V, Io= 500mA	120mVpp
Short Circuit Current	$V_{IN}$ =25V, $R_{L}$ = 0.1m $\Omega$	1.1A
Efficiency	V <sub>IN</sub> =25V, Io= 500mA	83.7%
Output Ripple with Optional Filter	V <sub>IN</sub> =25V, Io= 500mA	40mVpp

Fig 8. Step-Down Converter

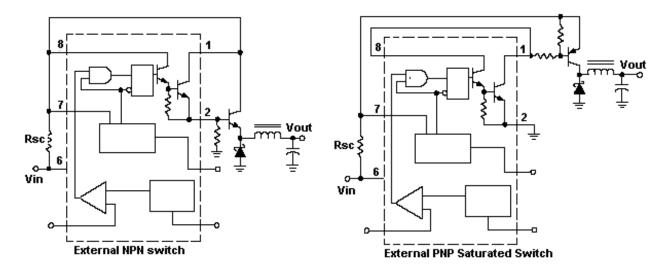
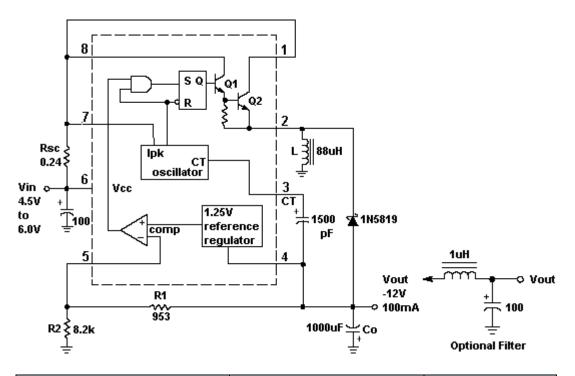


Fig. 9. External current Boost connections for IC peak greater than 1.5A



# **TYPICAL APPLICATION CIRCUIT (CONTINUE)**



Test	Conditions	Results
Line Regulation	V <sub>IN</sub> = 4.5V~6V, lo= 100mA	$3mV = \pm 120.012\%$
Load Regulation	V <sub>IN</sub> = 5V, Io= 10mA to 100mA	$0.022V = \pm 0.09\%$
Output Ripple	V <sub>IN</sub> =5V, Io= 100mA	500mVpp
Short Circuit Current	$V_{IN}$ =5 $V$ , $R_{L}$ = 0.1 $\Omega$	910mA
Efficiency	V <sub>IN</sub> =5V, Io= 100mA	62.2%
Output Ripple with Optional Filter	V <sub>IN</sub> =5V, Io= 100mA	70mVpp

Fig 10. Voltage Inverting Converter

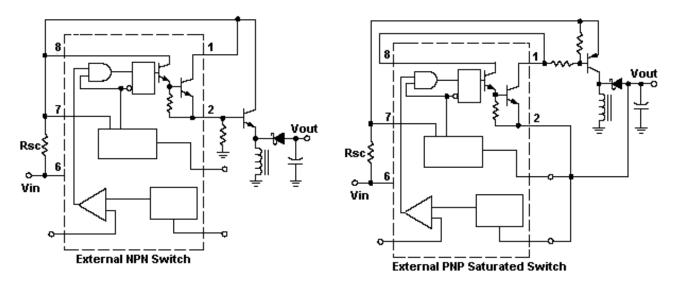


Fig. 11. External current Boost connections for IC peak greater than 1.5A



## **DESIGN FORMULA TABLE**

Test	Step-Up	Step-Down	Voltage Inverting
1 /1	Vout + Vf - Vin(min)	Vout + Vf	<i>Vout</i>   + <i>Vf</i>
t <sub>on</sub> /t <sub>off</sub>	Vcc(min) - Vsat	Vcc – Vsat – Vout	Vcc – Vsat
(1 1 )	1	1	1
(ton + toff)	f min	f min	f min
Ст	4.0 x 10 <sup>-5</sup> ton	4.0 x 10 <sup>-5</sup> ton	4.0 x 10 <sup>−5</sup> ton
I <sub>pk(switch)</sub>	$2lout(max)\left(\frac{ton}{toff}+1\right)$	2lout(max)	$2lout(max)\left(\frac{ton}{toff}+1\right)$
R <sub>sc</sub>	$\left(\frac{0.3}{Ipk(switch)}\right)$	$\left(\frac{0.3}{Ipk(switch)}\right)$	$\left(\frac{0.3}{Ipk(switch)}\right)$
L <sub>(min)</sub>	$\left(\frac{Vin(\min )-Vsat}{Ipk(switch)}\right)^*ton(\max )$	$\left(\frac{Vin(\min) - Vsat - Vout}{Ipk(switch)}\right)^* ton(\max)$	$\left(\frac{Vin(\min) - Vsat}{Ipk(switch)}\right) * ton(\max)$
Co	$\left(9\frac{Iout*ton}{Vripple(pp)}\right)$	$\left(\frac{Ipk(switch)(ton + toff)}{8Vripple(pp)}\right)$	$\left(9\frac{\textit{Iout*ton}}{\textit{Vripple}(pp)}\right)$

- V<sub>sat</sub> = Saturation Voltage of the output switch.
- V<sub>F</sub> = Forward Voltage drop of the rectifier.

### The following power supply characteristics must be chosen:

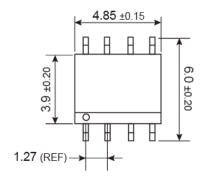
- V<sub>in</sub>= Normal input voltage
- V<sub>out</sub>: Desired Output voltage, |V<sub>OUT</sub>| =1.25 (1+R2 / R1)
- I<sub>out</sub>: Desired output current.
- f<sub>min</sub>: Minimum desired output switching frequency at the selected values for Vin and Io.
- V<sub>ripple(p-p)</sub>: Desired peak-to-peak output ripple voltage. in practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

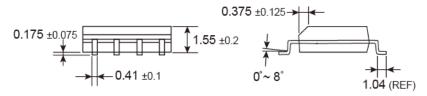
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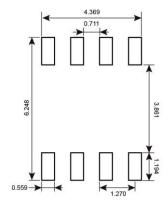
## PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

## SOP-8





# SUGGESTED PAD LAYOUT (Unit: Millimeters)



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# **MARKING DIAGRAM**



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan P =Feb Q =Mar R =Apr

S =May T =Jun U =Jul V =Aug W =Sep X =Oct Y =Nov Z =Dec

**L** = Lot Code  $(1\sim9, A\sim Z)$ 



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