

SN54ABT541, SN74ABT541B OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS093K – JANUARY 1991 – REVISED OCTOBER 1998

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (N) and Ceramic (J) DIPs

description

The SN54ABT541 and SN74ABT541B octal buffers and line drivers are ideal for driving bus lines or buffering memory address registers. The devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

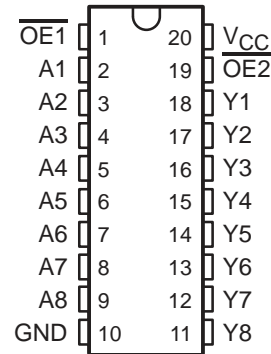
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT541 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT541B is characterized for operation from -40°C to 85°C .

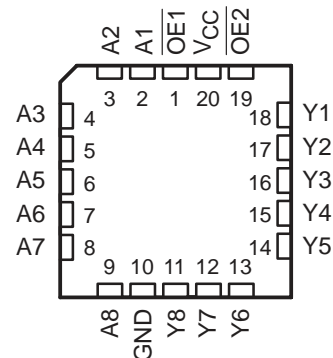
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

SN54ABT541 . . . J OR W PACKAGE
SN74ABT541B . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ABT541 . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



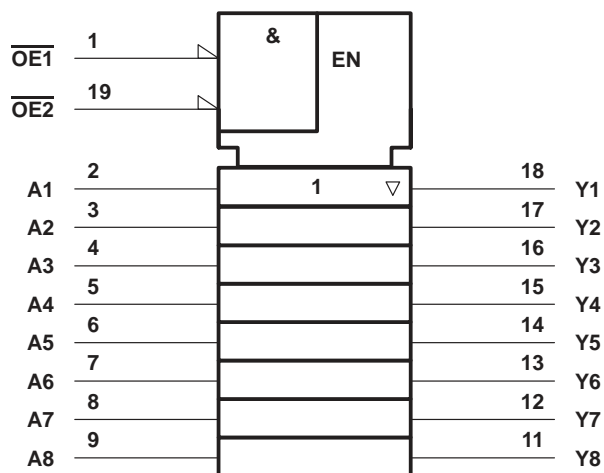
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

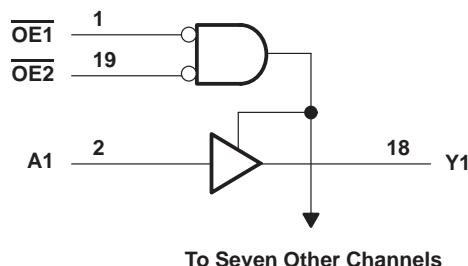
SN54ABT541, SN74ABT541B OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT541	96 mA
SN74ABT541B	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	115°C/W
DW package	97°C/W
N package	67°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

	SN54ABT541		SN74ABT541B		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SN54ABT541, SN74ABT541B OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT541		SN74ABT541B		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA			2.5		2.5		2.5	V
	V _{CC} = 5 V, I _{OH} = -3 mA			3		3		3	
	V _{CC} = 4.5 V	I _{OH} = -24 mA			2		2		
I _{OH} = -32 mA				2*				2	
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA				0.55			V
		I _{OL} = 64 mA				0.55*		0.55	
V _{hys}				100					mV
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, \overline{OE} = X			±50**		±50**		±50	μA
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, \overline{OE} = X			±50**		±50**		±50	μA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			10		10		10	μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-10		-10		-10	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high		50		50		50	μA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.5 V			-50 -140 -180		-50 -180		-50 -180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		5 250		250		250	μA
		Outputs low		22 30		30		30	mA
		Outputs disabled		1 250		250		250	μA
ΔI _{CC} §	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled		1.5		1.5		1.5	mA
		Outputs disabled		50		50		50	μA
		Control inputs		1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V			3					pF
C _o	V _O = 2.5 V or 0.5 V			6					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT541				UNIT	
			V _{CC} = 5 V, T _A = 25°C			MIN		MAX
			MIN	TYP	MAX			
t _{PLH}	A	Y	1	2.6	4.1	1	4.6	ns
t _{PHL}			1	2.9	4.2	1	4.7	
t _{PZH}	\overline{OE}	Y	1.1	3.1	4.8	1.1	5.4	ns
t _{PZL}			2.1	4.4	5.9	2.1	7	
t _{PHZ}	\overline{OE}	Y	2.1	5.1	6.6	2.1	7.5	ns
t _{PLZ}			1.7	4.7	6.2	1.7	6.7	



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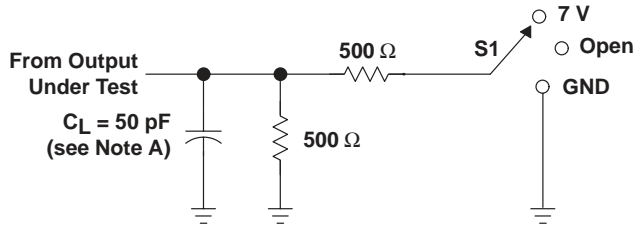
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT541B					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2	3.2	1	3.6	ns
t_{PHL}			1	2.6	3.5	1	3.9	
t_{PZH}	\overline{OE}	Y	2	3.5	4.5	2	4	ns
t_{PZL}			1.9	4	5.1	1.9	5.9	
t_{PHZ}	\overline{OE}	Y	2.2	4.4	5.4	2.2	5.8	ns
t_{PLZ}			1.5	3	4	1.5	4.4	
$t_{sk(o)}^\dagger$					0.5	0.5		ns

† Skew between any two outputs of the same package switching in the same direction

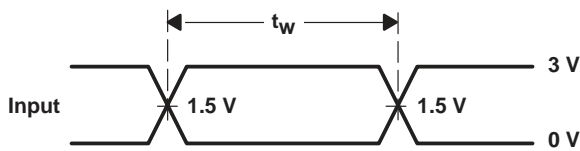


PARAMETER MEASUREMENT INFORMATION

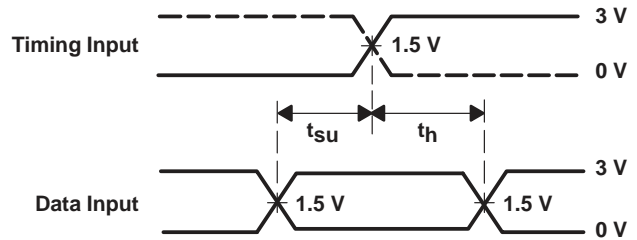


LOAD CIRCUIT

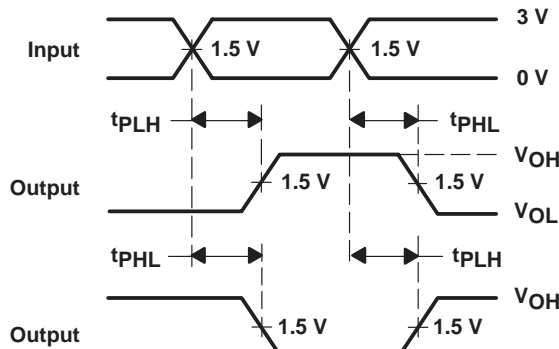
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



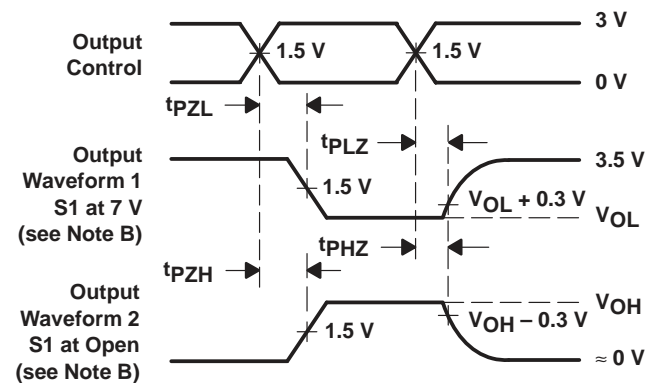
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN54ABT541, Octal Buffers/ Drivers With 3-State Outputs

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN54ABT541
Voltage Nodes (V)	5

FEATURES

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DESCRIPTION

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TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: [sn54abt541.pdf](#) (94 KB, Rev. K) (Updated: 10/06/1998)

APPLICATION NOTES

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- [Advanced BiCMOS Technology \(ABT\) Logic Characterization Information \(Rev. B\)](#) (SCBA008B - Updated: 06/01/1997)
- [Advanced BiCMOS Technology \(ABT\) Logic Enables Optimal System Design \(Rev. A\)](#) (SCBA001A - Updated: 03/01/1997)

Product Folder: SN54ABT541, Octal Buffers/Drivers With 3-State Outputs

- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(Rev. A\)](#) (SCBA012A - Updated: 08/01/1997)
- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices \(Rev. A\)](#) (SCBA006A - Updated: 12/01/1996)
- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Power-Up 3-State \(PU3S\) Circuits in TI Standard Logic Devices](#) (SZZA033 - Updated: 05/10/2002)
- [Quad Flatpack No-Lead Logic Packages \(Rev. C\)](#) (SCBA017C - Updated: 11/22/2002)
- [TI IBIS File Creation, Validation, and Distribution Processes](#) (SZZA034 - Updated: 08/29/2002)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

MORE LITERATURE

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
- [QML Class V Space Products Military Brief \(Rev. A\)](#) (SGZN001A, 257 KB - Updated: 10/07/2002)

USER GUIDES

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- [LOGIC Pocket Data Book](#) (SCYD013, 4837 KB - Updated: 12/05/2002)

PRICING/ AVAILABILITY/ PKG

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ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	DSCC NUMBER	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
5962-9471801Q2A	ACTIVE	LCCC (FK) 20	-55 TO 125		View Contents	1KU 8.58	1	44*	3942 20 May	8 WKS	None Reported View Distributors		
									> 10k 27 May				
5962-9471801QRA	ACTIVE	CDIP (J) 20	-55 TO 125		View Contents	1KU 4.86	1	88*	> 10k 20 May	8 WKS	None Reported View Distributors		
5962-9471801QSA	ACTIVE	CFP (W) 20	-55 TO 125		View Contents	1KU 8.58	1	5*	> 10k 20 May	8 WKS	None Reported View Distributors		
SNJ54ABT541FK	ACTIVE	LCCC (FK) 20	-55 TO 125	5962-9471801Q2A	View Contents	1KU 8.58	1	0*	3889 20 May	8 WKS	None Reported View Distributors		
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SNJ54ABT541J	ACTIVE	CDIP (J) 20	-55 TO 125	5962-9471801QRA	View Contents	1KU 4.86	1	267*	> 10k 20 May	8 WKS	None Reported View Distributors		
SNJ54ABT541W	ACTIVE	CFP (W) 20	-55 TO 125	5962-9471801QSA	View Contents	1KU 8.58	1	0*	> 10k 20 May	8 WKS	None Reported View Distributors		

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SN74ABT541B, Octal Buffers/ Drivers With 3-State Outputs
 DEVICE STATUS: ACTIVE

PARAMETER NAME	SN74ABT541B
Voltage Nodes (V)	5
V _{CC} range (V)	4.5 to 5.5
Input Level	TTL
Output Level	TTL
Output Drive (mA)	-32/64
tpd max (ns)	3.9
Static Current	15.12

FEATURES

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- [Timing Differences of 10-pF Versus 50pF Loading](#) (SCEA004 - Updated: 11/01/1996)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)
- [Understanding and Interpreting Texas Instruments Standard-Logic Products Data Sh \(Rev. A\)](#) (SZZA036A - Updated: 02/27/2003)

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- [Enhanced Plastic Portfolio Brochure](#) (SGZB004, 387 KB - Updated: 08/19/2002)
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- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [Military Brief](#) (SGYN138, 803 KB - Updated: 10/10/2000)
- [Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet \(Rev. A\)](#) (SDYZ001A, 138 KB - Updated: 07/01/1996)
- [Palladium Lead Finish User's Manual](#) (SDYV001, 2041 KB - Updated: 11/01/1996)
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REPORTED DISTRIBUTOR INVENTORY
As Of 09:00 AM GMT, 17 Apr 2003

ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (*C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74ABT541BDBLE	OBSOLETE	SSOP (DB) 20	-40 TO 85	View Contents	1KU		0*		Call**	None Reported View Distributors		
SN74ABT541BDBR	ACTIVE	SSOP (DB) 20	-40 TO 85	View Contents	1KU 0.31	2000	0*	520 21 Apr	2 WKS	EBV Elektronik Europe	> 1k	BUY NOW
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SN74ABT541BPWLE	OBSOLETE	TSSOP (PW) 20	-40 TO 85	View Contents	1KU		0*		Call**			
SN74ABT541BPWR	ACTIVE	TSSOP (PW) 20	-40 TO 85	View Contents	1KU 0.31	2000	0*	> 10k 08 May	3 WKS	None Reported View Distributors		
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