Compact TFT LCD Bias IC for Monitor with VCOM Buffer, Voltage Regulator for Gamma Buffer and Reset Function

Check for Samples: TPS65148

FEATURES

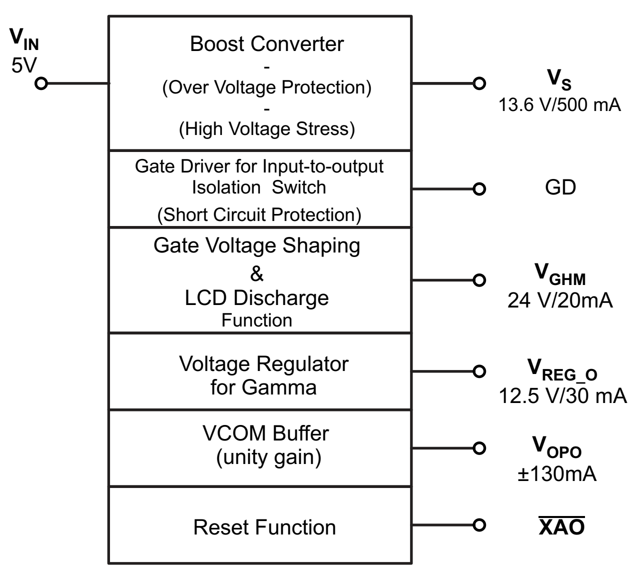
- **2.5V to 6V Input Voltage Range**
- **Up to 18V Boost Converter With 4A Switch Current**
- **630kHz/1.2MHz Selectable Switching Frequency**
- **Adjustable Soft-Start for the Boost Converter**
- **Gate Driver for External Input-to-Output Isolation Switch**
- **0.5% Accuracy Voltage Regulator for Gamma Buffer**
- **Gate Voltage Shaping**
- **VCOM Buffer**
- **Reset Function ($\overline{XAO}$ Signal)**
- **LCD Discharge Function**
- **Overvoltage Protection**
- **Overcurrent Protection**
- **Thermal Shutdown**
- **32-Pin 5*5mm QFN Package**

APPLICATIONS

- **Monitor**
- **TV (5V Input Voltage)**

DESCRIPTION

The TPS65148 offers a compact power supply solution designed to supply the LCD bias voltages required by TFT (Thin Film Transistor) LCD panels running from a typical 5 V supply rail. The device integrates a high power step-up converter for V_S (Source Driver voltage), an accurate voltage rail using an integrated LDO to supply the Gamma Buffer (V_{REG_O}) and a Vcom buffer driving the LCD backplane. In addition to that, a gate voltage shaping block is integrated. The V_{GH} signal (Gate Driver High voltage) supplied by an external positive charge pump, is modulated into V_{GHM} with high flexibility by using a logic input VFLK and an external discharge resistor connected to the RE pin. Also, an external negative charge pump can be set using the boost converter of the TPS65148 to generate V_{GL} (Gate Driver Low voltage). The integrated reset function together with the LCD discharge function available in the TPS65148 provide the signals enabling the discharge of the LCD TFT pixels when powering-off. The device includes safety features like overcurrent protection (OCP) and short-circuit protection (SCP) achieved by an external input-to-output isolation switch, as well as overvoltage protection (OVP) and thermal shutdown.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65148RHB	32-pin QFN	TPS65148

(1) The RHB package is available taped an reeled. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE	UNIT
Input voltage range VIN(2)	–0.3 to 6.5	V
Voltage range on pins COMP, EN, FB, FREQ, GD, HVS, REG_FB, RHVS, SS, VDET, VDPM, VFLK, $\overline{XAO}$ (2)	–0.3 to 6.5	V
Voltage on pins OPI, OPO, REG_I, REG_O, SUP, SW(2)	–0.3 to 20	V
Voltage on pins RE, VGH, VGHM(2)	–0.3 to 36	V
ESD rating HBM	2	kV
ESD rating MM	200	V
ESD rating CDM	500	V
Continuous power dissipation	See Thermal Information Table	
Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65148	UNITS
		RHB	
		32 PINS	
θ_{JA} (2)	Junction-to-ambient thermal resistance	37.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	38.7	
θ_{JB}	Junction-to-board thermal resistance	9.4	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	10.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) $\theta_{JA.}$ given for High-K PCB board.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.5		6	V
V_S, V_{SUP}, V_{REG_I}	Boost converter output voltage range. SUP pin and REG_I pin input supply voltage range	7		18	V
V_{GH}	Gate voltage shaping input voltage range	15		35	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 5 V, V_{REG_I} = V_S = V_{SUP} = 13.6 V, V_{REG_O} = 12.5 V, V_{OPI} = 5 V, V_{GH} = 23 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		6	V
I_{QVIN}	Operating quiescent current into VIN	Device not switching, V_{FB} = 1.240 V + 5%		0.23	0.5	mA
I_{QSUP}	Operating quiescent current into SUP	Device not switching, V_{FB} = 1.240 V + 5%		3	6	mA
I_{QVGH}	Operating quiescent current into VGH	V_{GH} = 24 V, VFLK = 'high'		30	60	µA
I_{QREG_I}	Operating quiescent current into REG_I	REG_O = 'open', V_{REG_FB} = 1.240 V + 5%		0.05	3	µA
I_{SDVIN}	Shutdown current into VIN	V_{IN} = 6 V, EN = GND		35	70	µA
I_{SDSUP}	Shutdown current into SUP	V_{IN} = 6 V, EN = GND, V_{SUP} = 6 V		1	2.5	µA
I_{SDVGH}	Shutdown current into VGH	V_{IN} = 6 V, EN = GND, V_{GH} = 6 V		20	40	µA
I_{SDREG_I}	Shutdown current into REG_I	V_{IN} = 6 V, EN = GND, V_{REG_I} = 6 V, V_{REG_O} = 4.9 V		4	10	µA
V_{UVLO}	Under-voltage lockout threshold	V_{IN} rising	2.1		2.3	V
		Hysteresis		0.1		
T_{SD}	Thermal shutdown	Temperature rising		150		°C
T_{SDHYS}	Thermal shutdown hysteresis			14		°C
LOGIC SIGNALS EN, FREQ, VFLK, HVS						
I_{LEAK}	Input leakage current	EN = FREQ = VFLK = HVS = 6 V			0.1	µA
V_{IH}	Logic high input voltage	V_{IN} = 2.5 V to 6 V	2			V
V_{IL}	Logic low input voltage	V_{IN} = 2.5 V to 6 V			0.4	V
BOOST CONVERTER (V_S)						
V_S	Output voltage boost converter				18	V
V_{OVP}	Overvoltage protection	V_S rising	18.2	19	19.8	V
V_{FB}	Feedback regulation voltage		1.228	1.240	1.252	V
I_{FB}	Feedback input bias current	V_{FB} = 1.240V			0.1	µA
gm	Transconductiance error amplifier gain			107		µA/V
$r_{DS(on)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 5 V, I_{SW} = 'current limit'		0.12	0.18	Ω
		V_{IN} = V_{GS} = 3.3 V, I_{SW} = 'current limit'		0.14	0.22	
I_{LEAK_SW}	SW leakage current	EN = GND, V_{SW} = 18.5 V			30	µA
I_{LIM}	N-Channel MOSFET current limit		4.0	4.8	5.6	A
I_{SS}	Softstart current	V_{SS} = 1.240 V		10		µA
f	Switching frequency	FREQ = 'high'	0.9	1.2	1.5	MHz
		FREQ = 'low'	470	630	790	kHZ
	Line regulation	V_{IN} = 2.5 V to 6 V, I_{OUT} = 1 mA		0.015		%/V
	Load regulation	I_{OUT} = 0 A to 1.3 A		0.22		%/A
LDO - VOLTAGE REGULATOR FOR GAMMA BUFFER (V_{REG_O})						
V_{REG_O}	LDO output voltage range		7		17.6	V
V_{REG_FB}	Feedback regulation voltage	V_{REG_I} = 10 V to 18V, REG_O = REG_FB, I_{REG_O} = 1 mA, T_A = -40°C to 85°C	1.228	1.240	1.252	V
		V_{REG_I} = 10 V to 18V, REG_O = REG_FB, I_{REG_O} = 1 mA, T_A = 25°C	1.234	1.240	1.246	
I_{REG_FB}	Feedback input bias current	V_{REG_FB} = 1.240 V			0.1	µA
I_{SC_REG}	Short circuit current limit	V_{REG_I} = 18 V, REG_O = REG_FB = GND			90	mA
V_{DO}	Dropout voltage	V_{REG_I} = 18 V, I_{REG_O} = 30 mA			400	mV
	Line regulation	V_{REG_I} = 13.6 V to 18 V, I_{REG_O} = 1 mA		0.003		%/V
	Load regulation	I_{REG_O} = 1 mA to 50 mA		0.28		%/A
GATE VOLTAGE SHAPING (V_{GHM})						
I_{DPM}	Capacitor charge current VDPM pin			20		µA
$r_{DS(on)M1}$	VGH to VGHM $r_{DS(on)}$ (M1 PMOS)	VFLK = 'high', I_{VGHM} = 20 mA, V_{GH} = 20 V		13	25	Ω
$r_{DS(on)M2}$	VGHM to RE $r_{DS(on)}$ (M2 PMOS)	VFLK = 'low', I_{VGHM} = 20 mA, V_{GHM} = 7.5 V		13	25	Ω

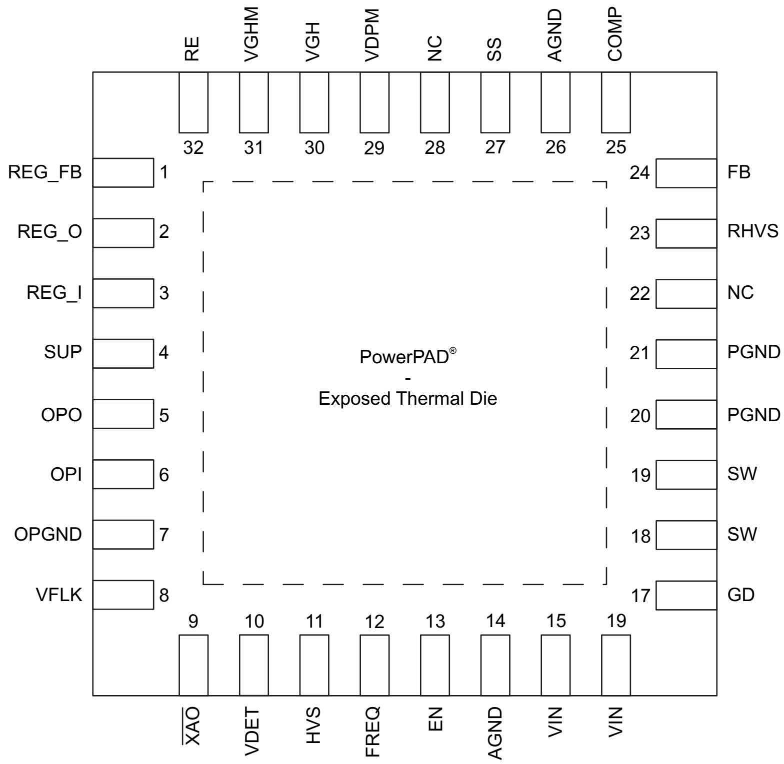
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 5 V, V_{REG_I} = V_S = V_{SUP} = 13.6 V, V_{REG_O} = 12.5 V, V_{OPI} = 5 V, V_{GH} = 23 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESET FUNCTION ($\overline{XAO}$)						
V_{IN_DET}	Operating voltage for V_{IN}		1.6		6.0	V
V_{DET}	Threshold voltage	Falling, V_{IN} = 2.3 V	1.216	1.240	1.264	V
V_{DET_HYS}	Threshold hysterisis			65		mV
$I_{\overline{XAO}\ (ON)}$	Sink current capability(1)	$V_{\overline{XAO}(ON)}$ = 0.5 V	1			mA
$V_{\overline{XAO}(ON)}$	Low voltage level	$I_{\overline{XAO}\ (ON)}$= 1 mA			0.5	V
$I_{LEAK\_\overline{XAO}}$	Leakage current	$V_{\overline{XAO}}$ = V_{IN} = 3.3V			2	µA
VCOM BUFFER (V_{COM})						
V_{SUP}	V_{SUP} supply range(2)	V_{SUP} = V_S	7		18	V
V_{OFFSET}	Input offset voltage	V_{CM} = V_{OPI} = V_{SUP}/2 = 6.8 V	–15		15	mV
I_B	Input bias current	V_{CM} = V_{OPI} = V_{SUP}/2 = 6.8 V	-1		1	µA
V_{CM}	Common mode input voltage range	V_{OFFSET} = 10 mV, I_{OPO} = 10 mA	1		V_S-1.5	V
CMRR	Common mode rejection ratio	V_{CM} = V_{OPI} = V_{SUP}/2 = 6.8 V, 1 MHz		66		dB
V_{OL}	Output voltage swing low	I_{OPO} = 10 mA		0.10	0.25	V
V_{OH}	Output voltage swing high	I_{OPO} = 10 mA	V_S - 1	V_S - 0.65		V
I_{sc}	Short circuit current	Source (V_{OPI} = V_{SUP}/2 = 6.8 V, OPO = GND)	90	130		mA
		Sink (V_{OPI} = V_{SUP}/2 = 6.8 V, V_{OPO} = V_{SUP} = 13.6 V)	110	160		
I_o	Output current	Source (V_{OPI} = V_{SUP}/2 = 6.8, V_{OFFSET} = 15 mV)		130		mA
		Sink (V_{OPI} = V_{SUP}/2 = 6.8, V_{OFFSET} = 15 mV)		130		
PSRR	Power supply rejection ratio			40		dB
SR	Slew rate	A_V = 1, V_{OPI} = 2 V_{PP}		60		V/µs
BW	–3db bandwidth	A_V = 1, V_{OPI} = 60 mV_{PP}		60		MHz
GATE DRIVER (GD)						
I_{GD}	Gate driver sink current	EN = 'high'		10		µA
R_{GD}	Gate driver internal pull up resistance			5		kΩ
HIGH VOLTAGE STRESS TEST (HVS)						
R_{HVS}	RHVS pull down resistance	HVS = 'high', V_{IN} = 2.5V to 6 V, I_{HVS} = 100 µA	400	500	600	Ω
I_{LEAK_RHVS}	RHVS leakage current	HVS = 'low', V_{RHVS} = 5 V			0.1	µA

(1) External pull-up resistor to be chosen so that the current flowing into $\overline{XAO}$ Pin ($V_{\overline{XAO}}$ = 0 V) when active is below $I_{\overline{XAO}\_MIN}$ = 1mA.
(2) Maximum output voltage limited by the Overvoltage Protection and not the maximum power switch rating of the boost converter.

PIN ASSIGNMENT



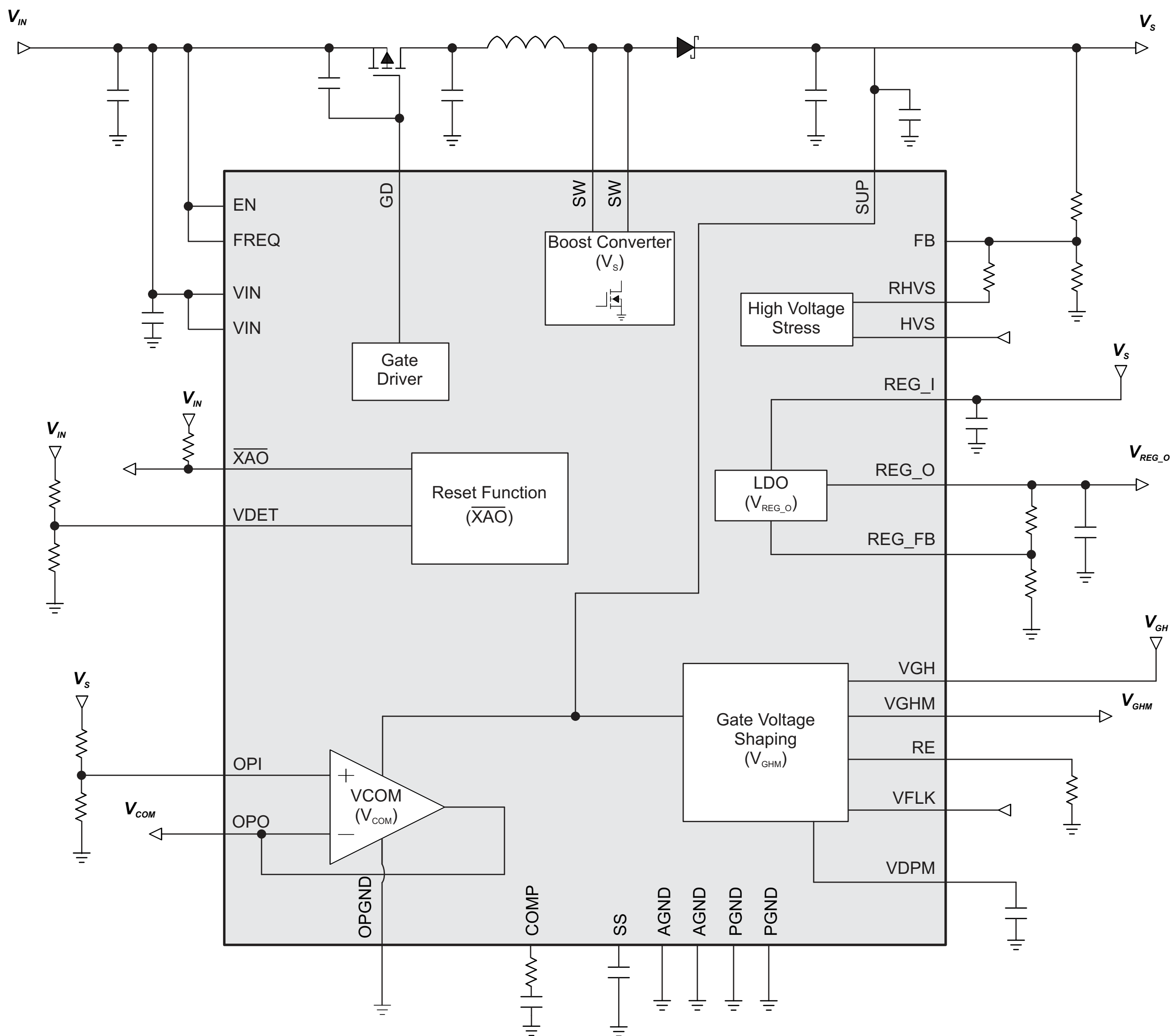
TERMINAL FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
REG_FB	1	I	Voltage regulator feedback pin.
REG_O	2	O	Voltage regulator output pin.
REG_I	3	I	Voltage regulator input pin.
SUP	4	I	Input supply pin for the gate voltage shaping and operational amplifier blocks. Also overvoltage protection sense pin. SUP pin must be supplied by V_S voltage.
OPO	5	O	VCOM Buffer output pin.
OPI	6	I	VCOM Buffer input pin.
OPGND	7		VCOM Buffer analog ground.
VFLK	8	I	Input pin for charge/discharge signal of V_{GHM}. VFLK = 'low' discharges V_{GHM} through RE pin.
$\overline{XAO}$	9	O	Reset function output pin (open-drain). $\overline{XAO}$ signal is active low.
VDET	10	I	Reset function threshold pin. Connect a voltage divider to this pin to set the threshold voltage.
HVS	11	I	High Voltage Stress function logic input pin. Apply a high logic voltage to enable this function
FREQ	12	I	Boost converter frequency select pin. Oscillator is 630 kHz when FREQ is connected to GND and 1.2 MHz when FREQ is connected to VIN.
EN	13	I	Shutdown control input. Apply a logic high voltage to enable the device.
AGND	14, 26, exposed pad		Analog ground.
VIN	15, 16	I	Input supply pin.
GD	17	O	Gate driver pin. Connect the gate of the boost converter's external input-to-output isolation switch to this pin.
SW	18, 19		Switch pin of the boost converter.
PGND	20, 21		Power ground.
NC	22, 28		Not connected.

TERMINAL FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RHVS	23		Voltage level set pin. Connect a resistor to this pin to set V_S voltage when HVS = 'high'.
FB	24	I	Boost converter feedback pin.
COMP	25	I/O	Boost converter compensation pin.
SS	27	I/O	Boost soft-start control pin. Connect a capacitor to this pin if a soft-start is needed. Open = no soft-start.
VDPM	29	I/O	Sets the delay to enable VGHM output. Pin for external capacitor. Floating if no delay needed.
VGH	30	I	Input pin for the positive charge pump voltage.
VGHM	31	O	Gate voltage shaping output pin.
RE	32		Slope adjustment pin for gate voltage shaping. Connect a resistor to this pin to set the discharging slope of V_{GHM} when VFLK = 'low'.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

		FIGURE
Efficiency vs. Load Current	V_{IN} = 5 V, V_S = 13.6 V f = 630 kHz/1.2 MHz	Figure 1
Efficiency vs. Load Current	V_{IN} = 5 V, V_S = 18 V f = 630 kHz/1.2 MHz	Figure 2
PWM Switching Discontinuous Conduction Mode	V_{IN} = 5 V, V_S = 13.6 V/ 2 mA f = 630 kHz	Figure 3
PWM Switching Continuous Conduction Mode	V_{IN} = 5 V, V_S = 13.6 V/ 500 mA f = 630 kHz	Figure 4
Boost Frequency vs. Load Current	V_{IN} = 5 V, V_S = 13.6 V f= 630 kHz/1.2 MHz	Figure 5
Boost Frequency vs. Supply Voltage	V_S = 13.6 V/100 mA f = 630 kHz/1.2 MHz	Figure 6
Load Transient Response Boost Converter High Frequency (1.2 MHz)	V_{IN} = 5 V, V_S = 13.6 V I_{OUT} = 50 mA ~ 400 mA, f = 1.2 MHz	Figure 7
Load Transient Response Boost Converter Low Frequency (630 KHz)	V_{IN} = 5 V, V_S = 13.6 V I_{OUT} = 50 mA ~ 400 mA, f = 630 kHz	Figure 8
Boost Converter Output Current Capability	V_{IN} = 5 V, V_S = 9 V, 13.6 V, 15 V, 18 V f = 1.2 MHz, L = 4.7 µH	Figure 9
Soft-start Boost Converter	V_{IN} = 5 V, V_S = 13.6 V, I_{OUT} = 600 mA	Figure 10
Overvoltage Protection Boost Converter (OVP)	V_{IN} = 5 V, V_S = 13.6 V	Figure 11
Load Transient Response LDO	V_{LVIN} = 5 V, V_S = 13.6 V V_{REG_O} = 12.5 V, I_{LVOUT} = 5 mA - 30 mA	Figure 12
Gate Voltage Shaping	V_{GH} = 23 V	Figure 13
$\overline{XAO}$ Signal and LCD Discharge Function		Figure 14
Power On Sequencing		Figure 15
Power Off Sequencing		Figure 16
Short Circuit Protection (< 114 ms)		Figure 17
Short Circuit Protection (> 114 ms)		Figure 18

For all the following graphics, the inductors used for the measurements are CDRH127 (L = 4.7 µF) for f = 1.2 MHz, and CDRH127LD (L = 10 µF) for f = 630 kHz.

EFFICIENCY vs LOAD CURRENT (V_S = 13.6 V)

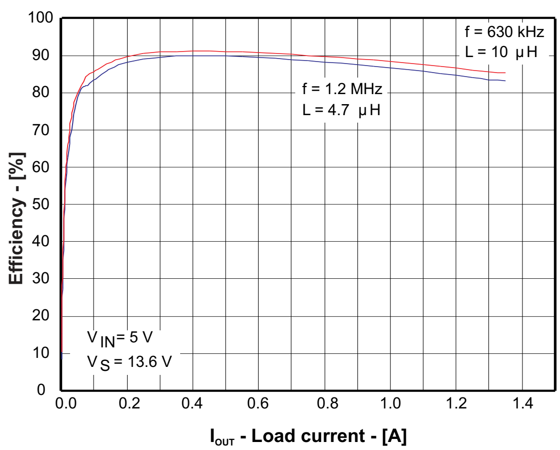


Figure 1.

EFFICIENCY vs Load Current (V_S = 18 V)

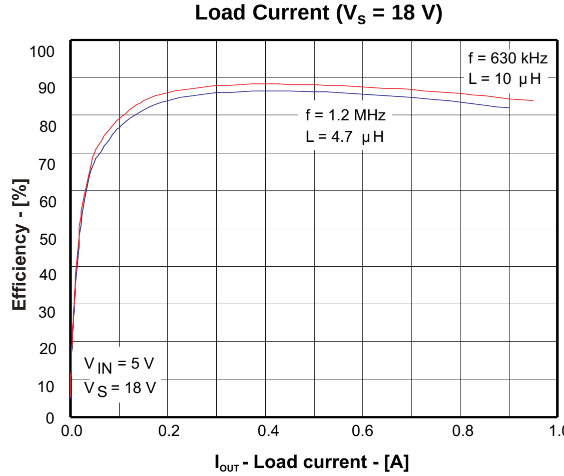


Figure 2.

BOOST CONVERTER PWM SWITCHING DISCONTINUOUS CONDUCTION MODE

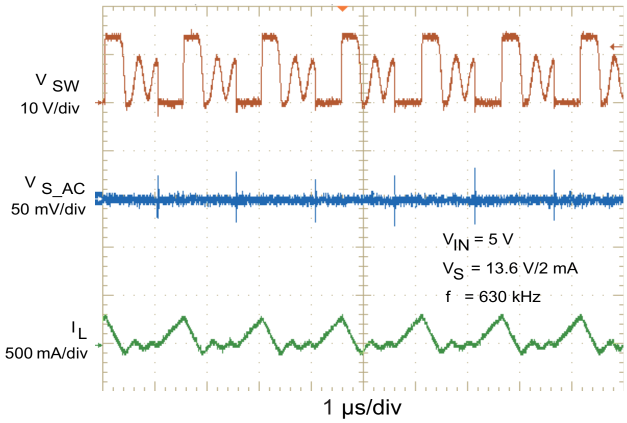


Figure 3.

BOOST CONVERTER PWM SWITCHING CONTINUOUS CONDUCTION MODE

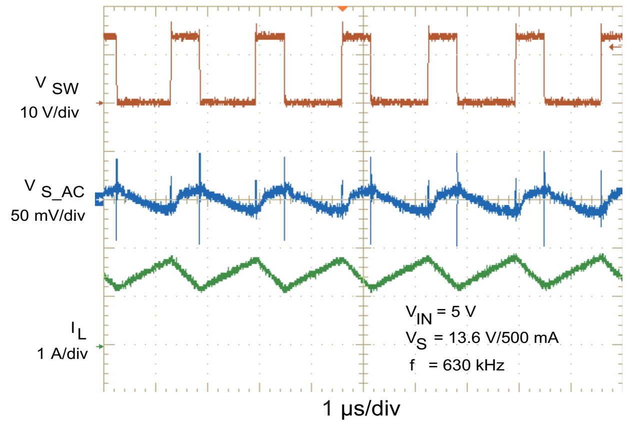


Figure 4.

BOOST CONVERTER FREQUENCY vs LOAD CURRENT

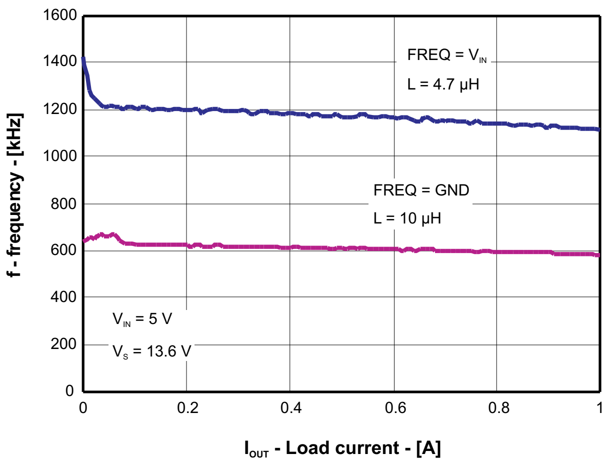


Figure 5.

BOOST CONVERTER FREQUENCY vs SUPPLY VOLTAGE

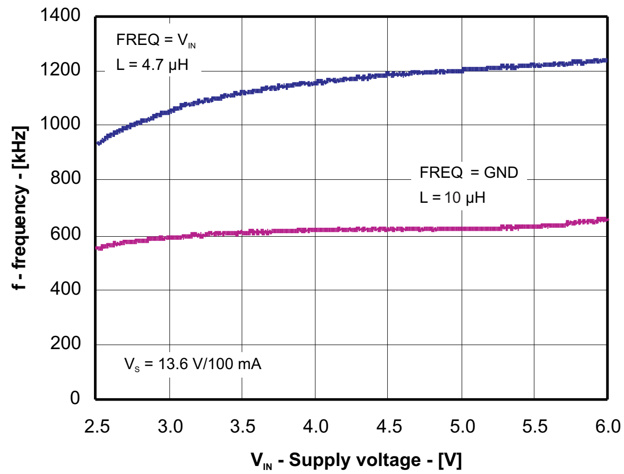


Figure 6.

LOAD TRANSIENT RESPONSE BOOST CONVERTER - HIGH FREQUENCY (1.2 MHz)

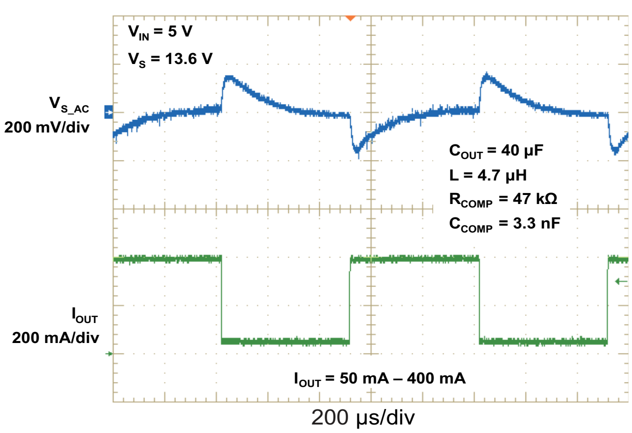


Figure 7.

LOAD TRANSIENT RESPONSE BOOST CONVERTER - LOW FREQUENCY (630 kHz)

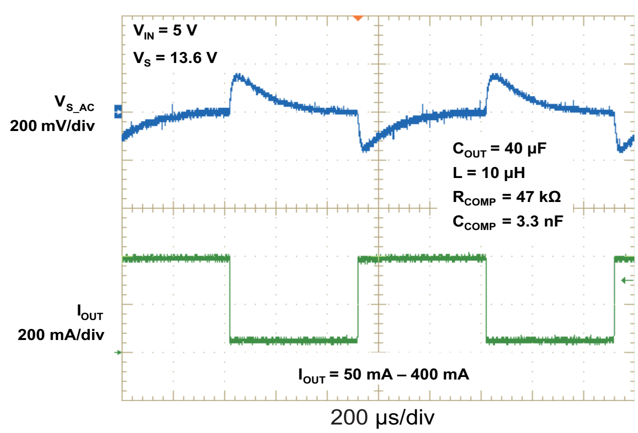


Figure 8.

BOOST CONVERTER OUTPUT CURRENT CAPABILITY

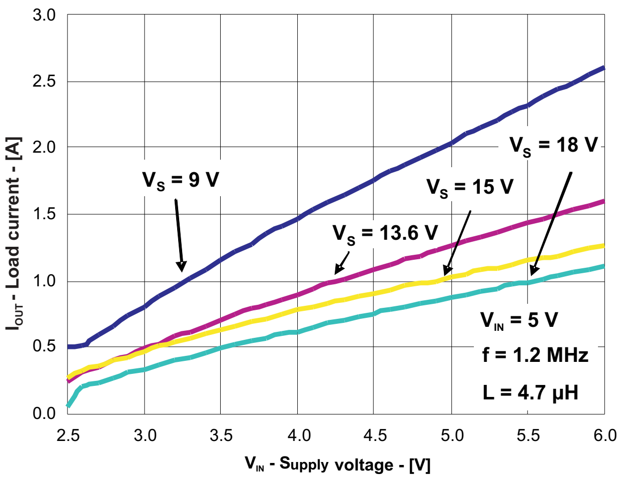


Figure 9.

BOOST CONVERTER SOFT-START

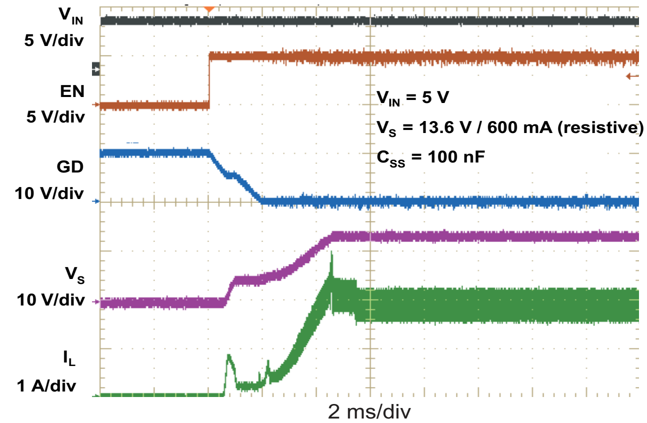


Figure 10.

OVERVOLTAGE PROTECTION BOOST CONVERTER (OVP)

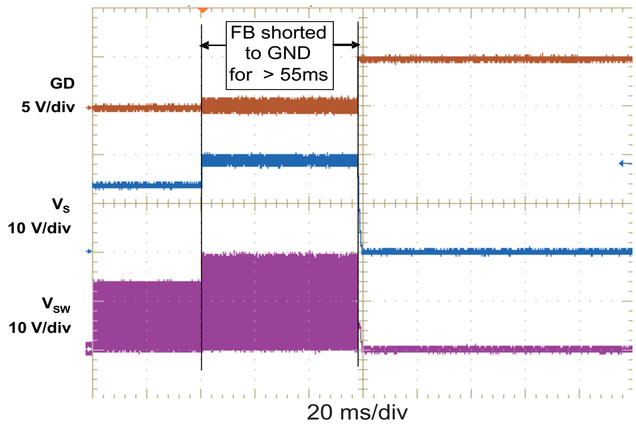


Figure 11.

LOAD TRANSIENT RESPONSE VOLTAGE REGULATOR FOR GAMMA BUFFER

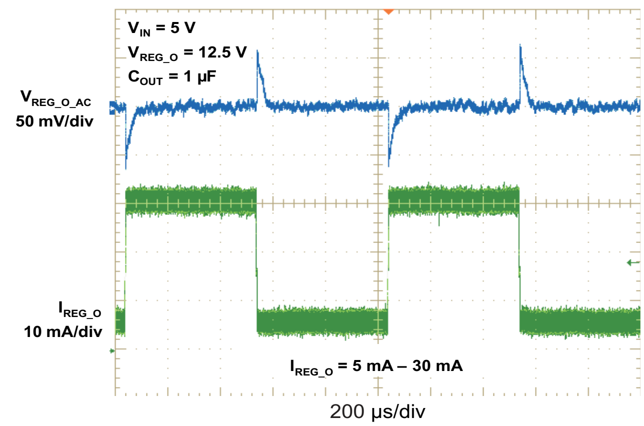


Figure 12.

GATE VOLTAGE SHAPING

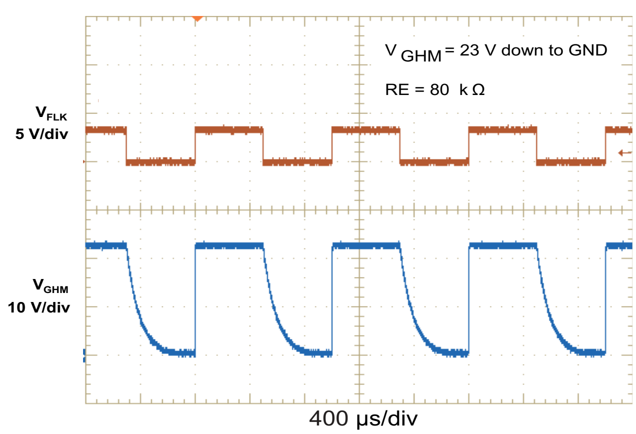


Figure 13.

$\overline{XAO}$ SIGNAL AND LCD DISCHARGE FUNCTION

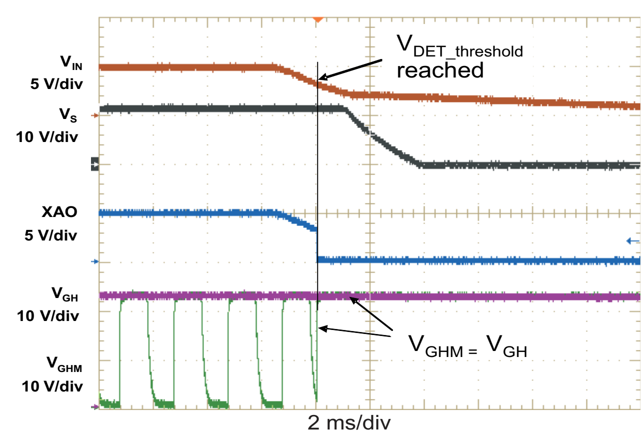


Figure 14.

POWER ON SEQUENCING

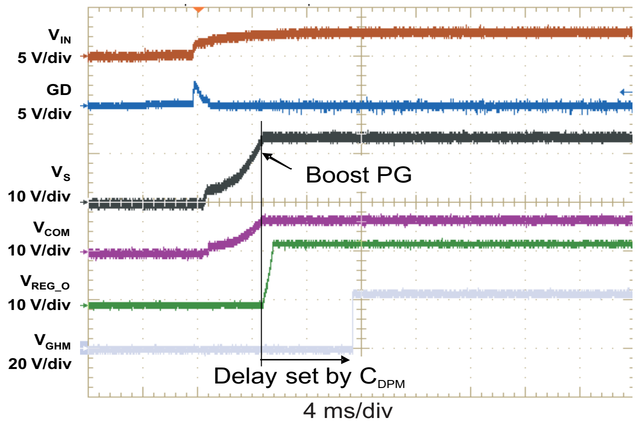


Figure 15.

POWER OFF SEQUENCING

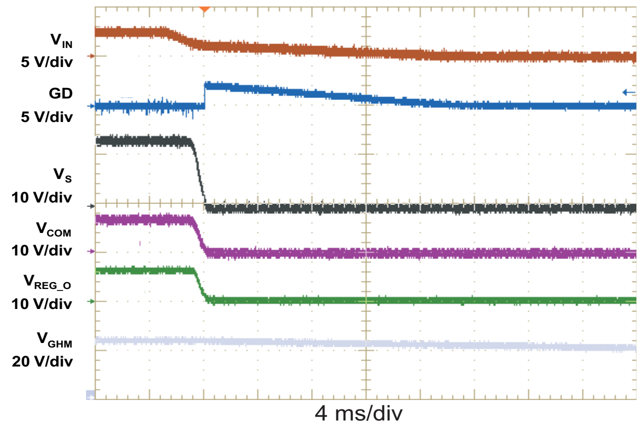


Figure 16.

SHORT CIRCUIT PROTECTION (< 114 ms)

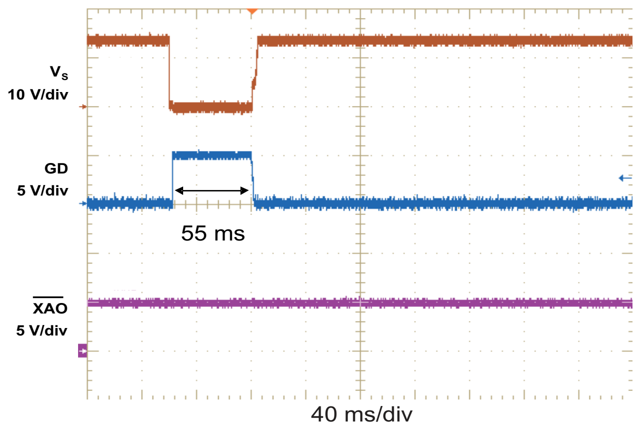


Figure 17.

SHORT CIRCUIT PROTECTION (> 114 ms)

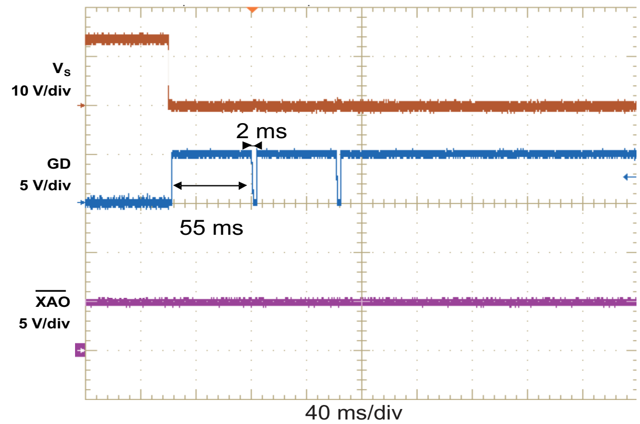


Figure 18.

APPLICATION INFORMATION

BOOST CONVERTER

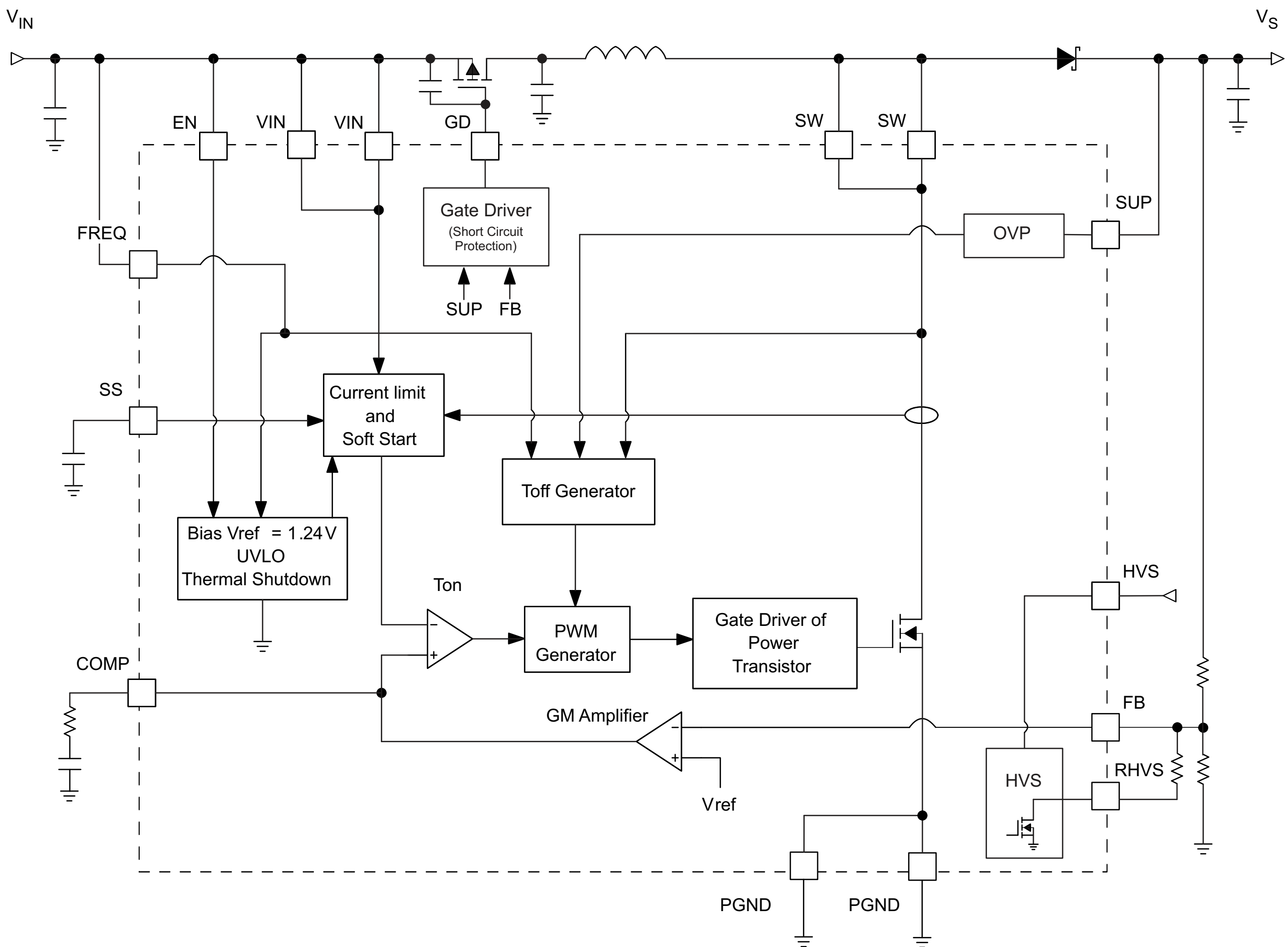


Figure 19. Boost converter block diagram

The boost converter is designed for output voltages up to 18 V with a switch peak current limit of 4 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is selectable between 630 kHz and 1.2 MHz and the minimum input voltage is 2.5 V. To limit the inrush current at start-up a soft-start pin is available.

TPS65148 boost converter's novel topology using adaptive off-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

BOOST CONVERTER DESIGN PROCEDURE

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g. 85%.

1. Duty Cycle: $D = \frac{V_{IN} \times \eta}{V_S}$ (1)
2. Inductor ripple current: $\Delta I_L = \frac{V_{IN\_min} \times D}{f \times L}$ (2)
3. Maximum output current: $I_{OUT\_max} = \left(I_{LIM\_min} - \frac{\Delta I_L}{2}\right) \times (1 - D)$ (3)
4. Peak switch current: $I_{swpeak} = \frac{\Delta I_L}{2} + \frac{I_{OUT}}{1 - D}$ (4)

   I_{swpeak} = Converter switch current (must be < I_{LIM_min} = 4 A)
   f = Converter switching frequency (typically 1.2 MHz or 630 kHz)
   L = Selected inductor value (from the Inductor Selection section)
   η = Estimated converter efficiency (use the number from the efficiency plots or 85% as an estimation)
   ΔI_L = Inductor peak-to-peak ripple current

The peak switch current is the steady state current that the integrated switch, inductor and external Schottky diode have to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

Inductor Selection

The main parameter for the inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated above with additional margin to cover for heavy load transients. An alternative, more conservative, is to choose the inductor with a saturation current at least as high as the maximum switch current limit of 5.6 A. Another important parameter is the inductor DC resistance. Usually the lower the DC resistance the higher the efficiency. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well. At high switching frequencies of 1.2 MHz inductor core losses, proximity effects and skin effects become more important. Usually an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS65148, inductor values between 3.3 μH and 6.8 μH are a good choice with a switching frequency of 1.2 MHz. At 630 kHz, inductors between 7 μH and 13 μH are recommended. Isat > I_{swpeak} imperatively. Possible inductors are shown in Table 1.

Table 1. Inductor Selection

L (μH)	COMPONENT SUPPLIER	COMPONENT CODE	SIZE (LxWxH mm)	DCR TYP (mΩ)	Isat (A)
		1.2 MHz			
6.8	Epcos	B82464G4682M	10.4 x 10.4 x 4.9	20	4.3
4.7	Coiltronics	UP2B-4R7-R	14 x 10.4 x 6	16.5	4.2
4.7	Sumida	CDRH124NP-4R7M	12.3 x 12.3 x 4.5	18	5.7
4.7	Sumida	CDRH127NP-4R7N	12.3 × 12.3 × 8	11.7	6.8
		630 kHz			
10	Coilcraft	DS3316P-103ML	12.95 × 9.4 × 5.08	80	3.5
10	Sumida	CDRH8D43NP-100N	8.3 × 8.3 × 4.5	29	4.0
10	Sumida	CDRH127NP-100N	12.3 × 12.3 × 8	16	5.4
10	Sumida	CDRH127/LDNP-100M	12.3 × 12.3 × 8	15	6.7

Rectifier Diode Selection

To achieve high efficiency a Schottky type should be used for the rectifier diode. The reverse voltage rating should be higher than the maximum output voltage of the converter. The averaged rectified forward current I_F, the Schottky diode needs to be rated for, is equal to the output current I_{OUT}:

$$I_F = I_{OUT} \tag{5}$$

Usually a Schottky diode with 2 A maximum average rectified forward current rating is sufficient for most of the applications. Also, the Schottky rectifier has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage V_F.

$$P_D = I_F \times V_F$$

Typically the diode should be able to dissipate around 500mW depending on the load current and forward voltage.

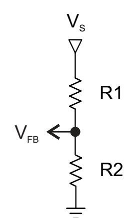
Table 2. Rectifier Diode Selection

CURRENT RATING I_F	V_R	V_F / I_F	COMPONENT SUPPLIER	COMPONENT CODE	PACKAGE TYPE
2 A	20 V	0.44 V/2 A	Vishay	SL22	SMA
2 A	20 V	0.5 V/2 A	Vishay	SS22	SMA

Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50 µA flowing through the feedback divider is enough to cover the noise fluctuation. The resistors are then calculated with 70 µA as:

$$R2 = \frac{V_{FB}}{70\ \mu A} \approx 18\ k\Omega \qquad R1 = R2 \times \left(\frac{V_S}{V_{FB}} - 1\right)$$



with V_{FB} = 1.240 V (6)

Soft-Start (Boost Converter)

To minimize the inrush current during start-up an external capacitor connected to the soft-start pin SS is used to slowly ramp up the internal current limit of the boost converter by charging it with a constant current of typically 10 µA. The inductor peak current limit is directly dependent on the SS voltage and the maximum load current is available after the soft-start is completed (V_{SS} = 0.8 V) or V_S has reached its Power Good value, 90% of its nominal value. The larger the capacitor, the slower the ramp of the current limit and the longer the soft-start time. A 100-nF capacitor is usually sufficient for most of the applications. When the EN pin is pulled low, the soft-start capacitor is discharged to ground.

Frequency Select Pin (FREQ)

The digital frequency select pin FREQ allows to set the switching frequency of the device to 630 kHz (FREQ = 'low') or 1.2 MHz (FREQ = 'high'). A higher switching frequency improves the load transient response but reduces slightly the efficiency. The other benefit of a higher switching frequency is a lower output voltage ripple. Usually, it is recommended to use 1.2 MHz switching frequency unless light load efficiency is of major concern.

Compensation (COMP)

The regulation loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. The compensation capacitor will adjust the low frequency gain and the resistor value will adjust the high frequency gain. Lower output voltages require a higher gain and therefore a lower compensation capacitor value. A good start, that will work for the majority of the applications is R_{COMP} = 47 kΩ and C_{COMP} = 3.3 nF.

Input Capacitor Selection

For good input voltage filtering low ESR ceramic capacitors are recommended. TPS65148 has an analog input VIN. A 1-µF bypass is required as close as possible from VIN to GND.

Two 10-µF (or one 22-µF) ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to Table 3 and typical applications for input capacitor recommendations.

Output Capacitor Selection

For best output voltage filtering a low ESR output capacitor is recommended. Four 10-µF (or two 22-µF) ceramic output capacitors work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to Table 3 for the selection of the output capacitor.

Table 3. Rectifier Input and Output Capacitor Selection

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
10 µF/0805	10 V	Taiyo Yuden	LMK212BJ106KD	C_{IN}
1 µF/0603	10 V	Taiyo Yuden	EMK107BJ105KA	VIN bypass
10 µF/1206	25 V	Taiyo Yuden	TMK316BJ106ML	C_{OUT}

To calculate the output voltage ripple, the following equations can be used:

$$\Delta V_C = \frac{V_S - V_{IN}}{V_S \times f} \times \frac{I_{OUT}}{C} \qquad \Delta V_{C\_ESR} = I_{swpeak} \times R_{C\_ESR} \tag{7}$$

ΔV_{C_ESR} can be neglected in many cases since ceramic capacitors provide very low ESR.

Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages an undervoltage lockout is included that disables the device, if the input voltage falls below 2.0 V.

Gate Drive Pin (GD)

The Gate Drive (GD) allows controlling an external isolation P-channel MOSFET switch. Using a 1-nF capacitor is recommend between the source and the gate of the FET to properly turn it on. GD pin is pulled low when the input voltage is above the undervoltage lockout threshold (UVLO) and when enable (EN) is 'high'. The gate drive has an internal pull up resistor to V_{IN} of typically 5 kΩ. The external P-channel MOSFET must be chosen with $V_T < V_{IN\_min}$ in order to be properly turned on.

Overvoltage Protection (OVP)

The main boost converter has an integrated overvoltage protection to prevent the Power Switch from exceeding the absolute maximum switch voltage rating at pin SW in case the feedback (FB) pin is floating or shorted to GND. In such an event, the output voltage rises and is monitored with the OVP comparator over the SUP pin. As soon as the comparator trips at typically 19 V, the boost converter turns the N-Channel MOSFET off. The output voltage falls below the overvoltage threshold and the converter starts switching again. If the voltage on the FB pin is below 90% of its typical value (1.240 V) for more than 55 ms, the device is latched down. The input voltage V_{IN} needs to be cycled to restart the device. In order to detect the overvoltage, the SUP pin needs to be connected to output voltage of the boost converter V_S. $\overline{XAO}$ output is independent from OVP.

Short Circuit Protection (SCP)

At start-up, as soon as the UVLO is reached and the EN signal is high, the GD pin is pulled 'low'. The feedback voltage of the boost converter V_{FB} as well as the SUP pin voltage (V_S) are sensed. After 2ms, if the voltage on SUP pin has not risen or the FB voltage is below 90% of its typical value (1.240 V), then the GD pin is pulled high for 55ms. After 3 tries, if the device is still in short circuit, it is latched down. The input voltage V_{IN} needs to be cycled to restart the device. The SCP is also valid during normal operation.

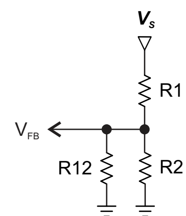
Over Current Protection (OCP)

If the FB voltage is below 90% of its typical value (1.240 V) for more than 55 ms, the GD pin is pulled 'high' and the device latched down. The input voltage V_{IN} needs to be cycled to restart the device.

HIGH VOLTAGE STRESS (HVS) FOR THE BOOST CONVERTER

The TPS65148 incorporates a High Voltage Stress test enabled by pulling the logic pin HVS 'high'. The output voltage of the boost converter V_S is then set to a higher output voltage compared to the nominal programmed output voltage. If unregulated external charge pumps are connected via the boost converter, their outputs will increase as V_S increases. This stress voltage is flexible and set by the resistor connected to RHVS pin. With HVS = 'high' the RHVS pin is pulled to GND. The external resistor connected between FB and RHVS (as shown in Figure 19) is therefore put in parallel to the low-side resistor of the boost converter's feedback divider. The output voltage for the boost converter during HVS test is calculated as:

$$V_{S\_HVS} = V_{FB} \times \frac{R1 + R2 \parallel R12}{R2 \parallel R12} \qquad R12 = \frac{R1 \times R2}{\left(\frac{V_{S\_HVS}}{V_{FB}} - 1\right) \times R2 - R1}$$



with V_{FB} = 1.240 V (8)

If the V_{GH} voltage needs to be set to a higher value by using the HVS test, V_{GH} must be connected to VGH pin without a regulation stage. The V_{GH} voltage will then be equal to V_{S_HVS} times 2 or 3 (depending if a doubler or tripler mode is used for the external positive charge pump). The same circuit changes can be held on the negative charge pump as well if required.

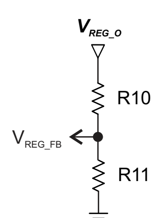
CAUTION

Special caution must be taken in order to limit the voltage on the VGH pin to 35V (maximum recommended voltage).

VOLTAGE REGULATOR FOR GAMMA BUFFER

TPS65148 includes a voltage regulator (Low Dropout Linear Regulator, LDO) to supply the Gamma Buffer with a very stable voltage. The LDO is designed to operate typically with a 4.7 µF ceramic output capacitor (any value between 1 µF and 15 µF works properly) and a ceramic bypass capacitor of minimum 1 µF on its input REG_I connected to ground. The output of the boost converter V_S is usually connected to the input REG_I. The LDO has an internal softstart feature of 2 ms maximum to limit the inrush current. As for the boost converter, a minimum current of 50 µA flowing through the feedback divider is usually enough to cover the noise fluctuation. The resistors are then calculated with 70 µA as:

$$R11 = \frac{V_{REG\_FB}}{70\ \mu A} \approx 18\ k\Omega \qquad R10 = R11 \times \left(\frac{V_{REG\_O}}{V_{REG\_FB}} - 1\right)$$



with V_{REG_FB} = 1.240 V (9)

VCOM BUFFER

The VCOM Buffer power supply pin is the SUP pin connected to the boost converter V_S. To achieve good performance and minimize the output noise, a 1 µF ceramic bypass capacitor is required directly from the SUP pin to ground. The input positive pin OPI is either supplied through a resistive divider from V_S or from an external PMIC. The buffer is not designed to drive high capacitive loads; therefore it is recommended to connect a series resistor at the output to provide stable operation when driving a high capacitive load. With a 3.3 Ω series resistor, a capacitive load of 10 nF can be driven, which is usually sufficient for typical LCD applications.

EXTERNAL CHARGE PUMPS

External Positive Charge Pump

The external positive charge pump provides with the below configuration (figure Figure 20) an output voltage V_{GH} of maximum 3 times the output voltage of the Boost converter V_S. The first stage provides roughly $3*V_S$ in that configuration, and the second stage is used as regulation whose output voltage is selectable. The operation of the charge pump driver can be understood best with Figure 20 which shows an extract of the positive charge pump driver circuit out of the typical application. The voltage on the collector of the bipolar transistor is slightly equal to $3*V_S–4*V_F$. The next stage regulates the output voltage V_{GH}. A Zener diode clamps the voltage at the desired output value and a bipolar transistor is used to provide better load regulation as well as to reduce the quiescent current. Finally the output voltage on V_{GH} will be equal to $V_Z–V_{be}$.

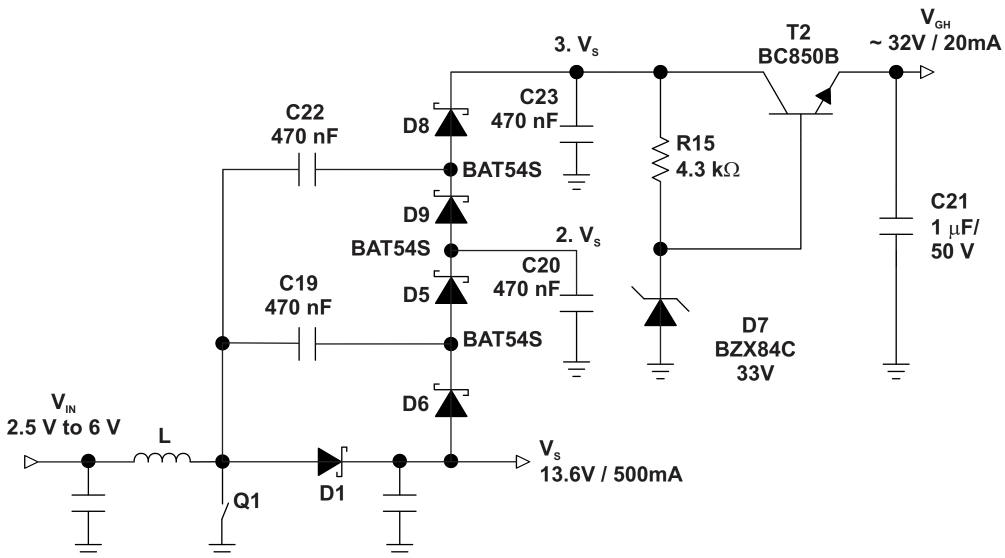


Figure 20. Positive Charge Pump

Doubler Mode: if the V_{GH} voltage can be reached using doubler mode, then the configuration is the same than the one shown in Figure 28.

External Negative Charge Pump

The external negative charge pump works also with two stages (charge pump and regulation). The charge pump provides a negative regulated output voltage. Figure 21 shows the operation details of the negative charge pump. With the first stage, the voltage on the collector of the bipolar transistor is equal to $–V_S+V_F$.

The next stage regulates the output voltage V_{GL}. A resistor and a Zener diode are used to clamp the voltage to the desired output value. The bipolar transistor is used to provide better load regulation as well as to reduce the quiescent current. The output voltage on V_{GL} will be equal to $-V_Z–V_{be}$.

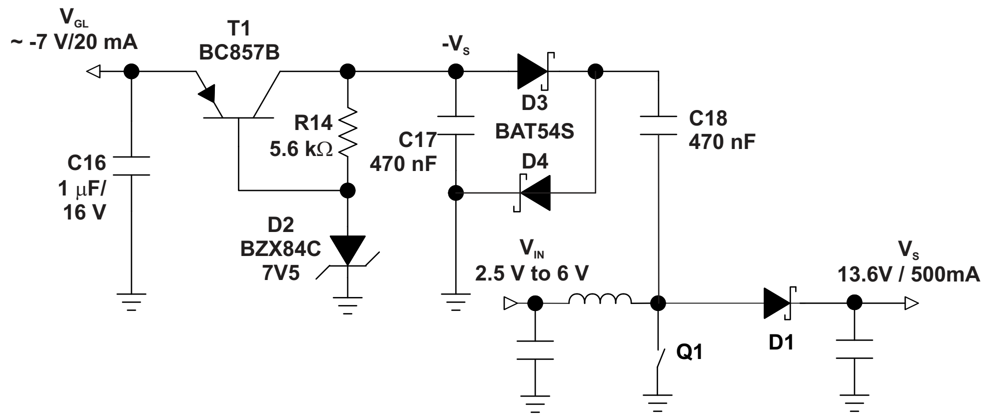


Figure 21. Negative Charge Pump

Components Selection

Capacitors (Charge Pumps)

For best output voltage filtering a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value but depending on the application tantalum capacitors can be used as well.

The rated voltage of the capacitor has to be able to withstand the voltage across it. Capacitors rated at 50 V are enough for most of the applications. Typically a 470-nF capacitance is sufficient for the flying capacitors whereas bigger values like 1 µF or more can be used for the output capacitors to reduce the output voltage ripple.

CAPACITOR	COMPONENT SUPPLIER	COMPONENT CODE	COMMENTS
100 nF/0603	Taiyo Yuden	HMK107BJ104KA	Flying Cap
470 nF/0805	Taiyo Yuden	UMK212BJ474KG	Output Cap 1
1 µF/1210	Taiyo Yuden	HMK325BJ105KN	Output Cap 2

Diodes (Charge Pumps)

For high efficiency, one has to minimize the forward voltage drop of the diodes. Schottky diodes are recommended. The reverse voltage rating must withstand the maximum output voltage V_S of the boost converter. Usually a Schottky diode with 200 mA average forward rectified current is suitable for most of the applications.

CURRENT RATING I_F	V_R	V_F / I_F	COMPONENT SUPPLIER	COMPONENT CODE	PACKAGE TYPE
200 mA	30 V	0.5V / 30mA	International Rectifier	BAT54S	SOT23

GATE VOLTAGE SHAPING FUNCTION

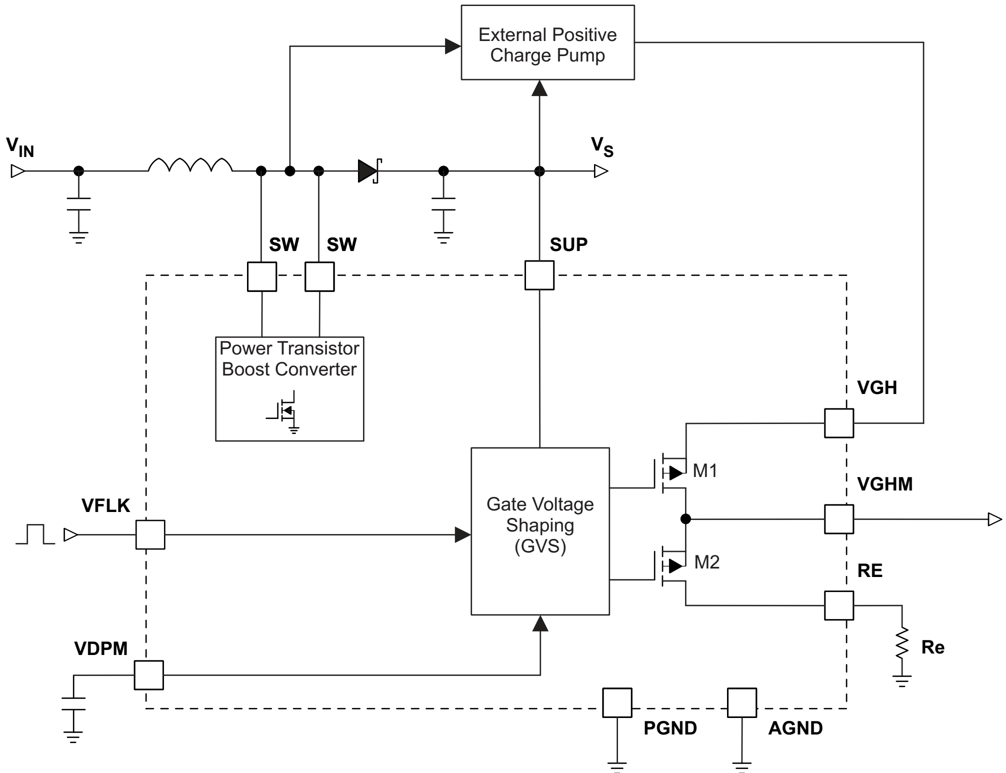


Figure 22. Gate Voltage Shaping Block Diagram

The Gate Voltage Shaping is controlled by the flicker input signal VFLK, except during start-up where it is kept at low state, whatever the VFLK signal is. The VGHM output is enabled once the VDPM voltage is higher than V_{ref} = 1.240 V. The capacitor connected to VDPM (C13 on Figure 27) pin sets the delay from the boost converter Power Good (90% of its nominal value).

$$C_{VDPM} = \frac{I_{DPM} \times t_{DPM}}{V_{ref}} = \frac{20\ \mu A \times t_{DPM}}{1.240\ V} \qquad (10)$$

VFLK = 'high' → $V_{GHM} = V_{GH}$

VFLK = 'low' → V_{GHM} discharges through Re resistor

The slope at which V_{GHM} discharges is set by the external resistor connected to RE, the internal MOSFET $r_{DS(on)}$ (typically 13Ω for M2 – see Figure 22) and by the external gate line capacitance connected to VGHM pin.

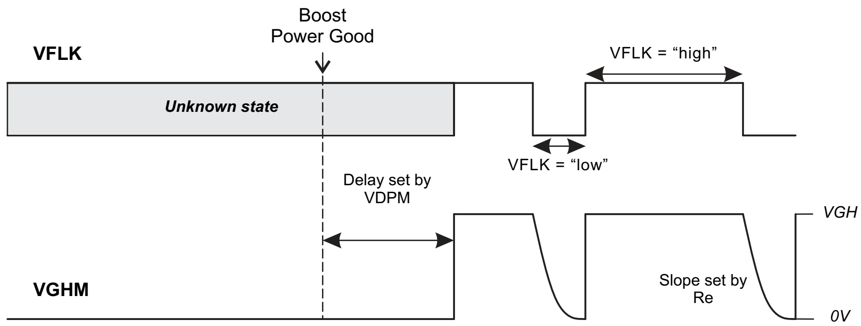


Figure 23. Gate Voltage Shaping Timing

If RE is connected with a resistor to ground (see Figure 23), when VFLK = 'low' V_{GHM} will discharge from V_{GH} down to 0V. Since 5 x τ (τ = R x C) are needed to fully discharge C through R, we can define the time-constant of the gate voltage shaping block as follow:

$\tau = (Re + r_{DS(on)M2}) \times C_{VGHM}$

Therefore, if the discharge of C_{VGHM} should finish during V_{FLK} = 'low':

$$t_{discharge} = 5 \times \tau = t_{V_{FLK}='low'} \quad \Rightarrow \quad RE = \frac{t_{V_{FLK}='low'}}{5 \times C_{VGHM}} - r_{DS(on)M2} \tag{11}$$

NOTE

C_{VGHM} and R_{VGHM} form the parasitic RC network of a pixel gate line of the panel. If they are not known, they can be ignored at the beginning and estimated from the discharge slope of V_{GHM} signal.

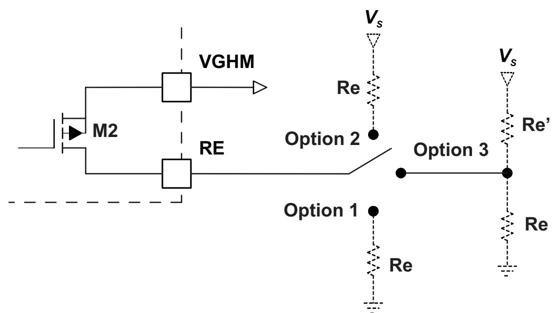


Figure 24. Discharge Path Options for VGHM

Options 2 and 3 from Figure 24 work like option 1 explained above. When M2 is turned on, V_{GHM} discharges with a slope set by Re from V_{GH} level down to V_S in option 2 configuration and down to the voltage set by the resistor divider in option 3 configuration. The discharging slope is set by Re resistor(s).

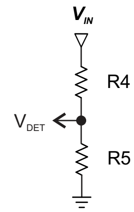
NOTE

When options 2 or 3 are used, V_{GHM} is not held to 0V at startup but to the voltage set on RE pin by the resistors Re and Re’.

RESET FUNCTION

The device has an integrated reset function with an open-drain output capable of sinking 1 mA. The reset function monitors the voltage applied to its sense input VDET. As soon as the voltage on VDET falls below the threshold voltage $V_{DET\_threshold}$ of typically 1.240 V, the reset function asserts its reset signal by pulling $\overline{XAO}$ low. Typically, a minimum current of 50µA flowing through the feedback divider when VDET voltage trips the reference voltage of 1.240 V is required to cover the noise fluctuation. Therefore, to select R4, one has to set the input voltage limit (V_{IN_LIM}) at which the reset function will pull $\overline{XAO}$ to low state. *V_{IN_LIM} must be higher than the UVLO threshold*. The resistors are then calculated with 70 µA as:

$$R5 = \frac{V_{DET}}{70\ \mu A} \approx 18\ k\Omega \qquad R4 = R5 \times \left(\frac{V_{IN\_LIM}}{V_{DET}} - 1\right)$$



with V_{DET} = 1.240 V (12)

The reset function is operational for $V_{IN} \geq 1.6V$:

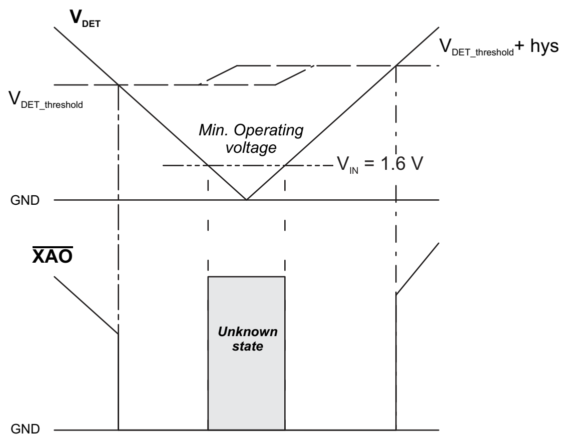


Figure 25. Voltage Detection and $\overline{XAO}$ Pin

The reset function is configured as a standard open-drain output and requires a pull-up resistor. The resistor $R_{\overline{XAO}}$, which must be connected between the $\overline{XAO}$ pin and a positive voltage V_X greater than 2V - 'high' logic level - e.g. V_{IN}, can be chosen as follows:

$$R_{\overline{XAO}\_min} > \frac{V_X}{1\ mA} \qquad \& \qquad R_{\overline{XAO}\_max} < \frac{V_X - 2\ V}{2\ \mu A} \tag{13}$$

THERMAL SHUTDOWN

A thermal shutdown is implemented to prevent damages because of excessive heat and power dissipation. Typically the thermal shutdown threshold for the junction temperature is 150 °C. When the thermal shutdown is triggered the device stops operating until the junction temperature falls below typically 136 °C. Then the device starts switching again. The $\overline{XAO}$ signal is independent of the thermal shutdown.

POWER SEQUENCING

When EN is high and the input voltage V_{IN} reaches the Under Voltage Lockout (UVLO), the device is enabled and the GD pin is pulled low. The boost converter starts switching and the VCOM buffer is enabled. As soon as V_S of the boost converter reaches its Power Good, the voltage regulator for the gamma buffer is enabled and the delay enabling the gate voltage shaping block starts. Once this delay has passed, the VGHM pin output is enabled.

1. GD
2. Boost converter & VCOM Buffer
3. Voltage regulator for Gamma Buffer
4. VGHM (after proper delay)

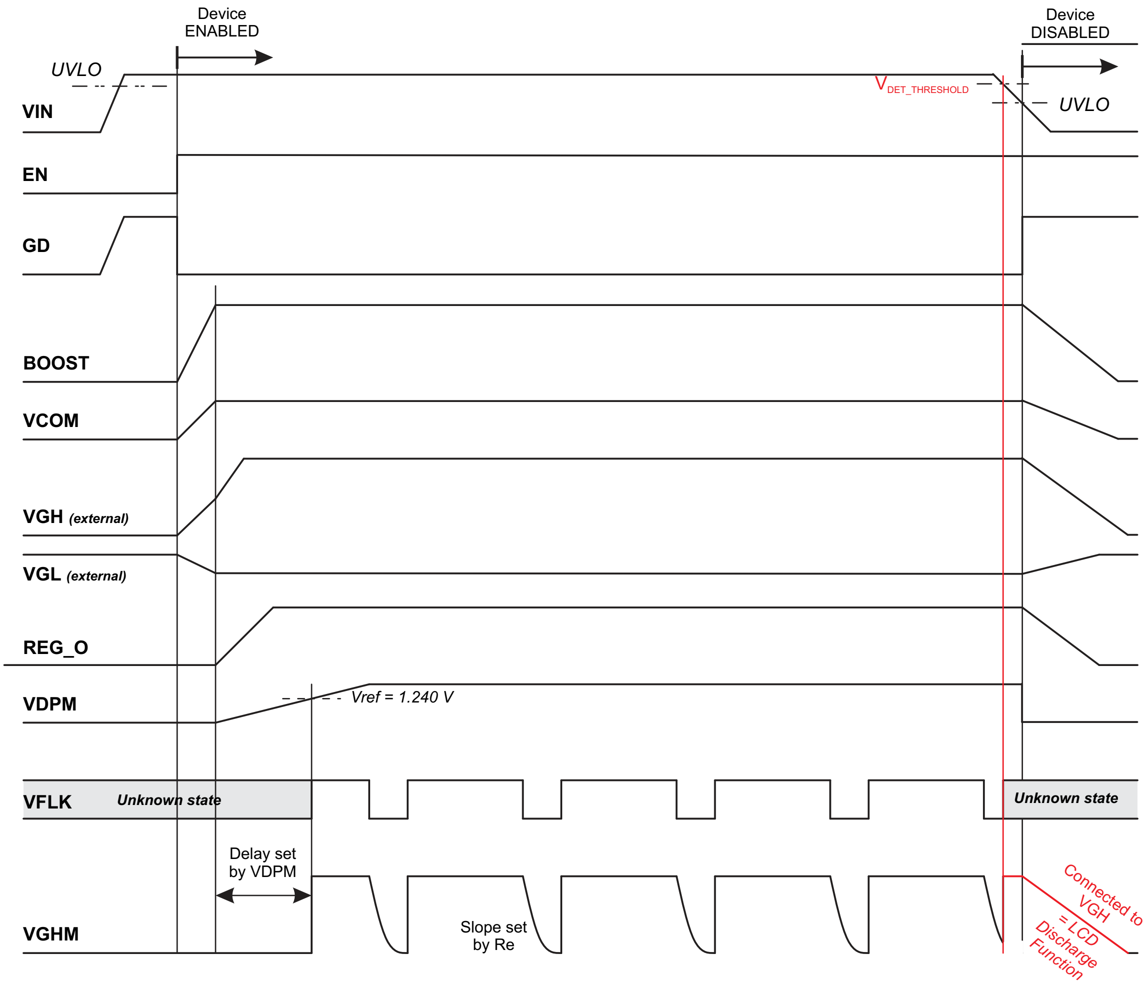


Figure 26. Sequencing TPS65148

Power off sequencing and LCD discharge function

When the input voltage V_{IN} falls below a predefined threshold (set by $V_{DET\_THRESHOLD}$ - see Figure 26), $\overline{XAO}$ is driven low and V_{GHM} is driven to V_{GH}. (Note that when V_{IN} falls below the UVLO threshold, all IC functions are disabled except $\overline{XAO}$ and V_{GHM}). Since VGHM is connected to VGH, it tracks the output of the positive charge pump as it decays. This feature, together with $\overline{XAO}$ can be used to discharge the panel by turning on all the pixel TFTs and discharging them into the gradually decaying V_{GHM} voltage. V_{GHM} is held low during power-up.

APPLICATION INFORMATION

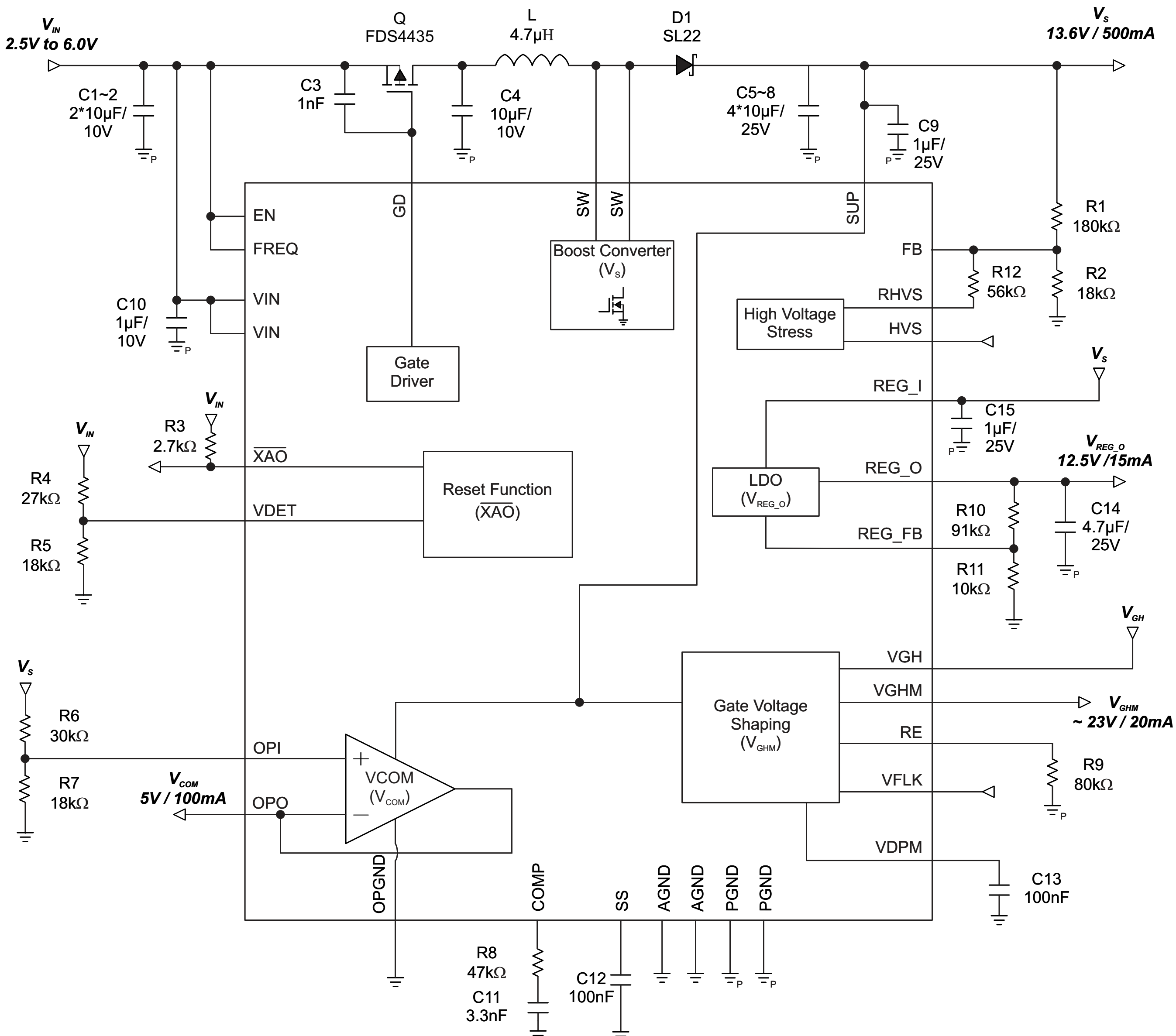


Figure 27. TPS65148 Typical Application

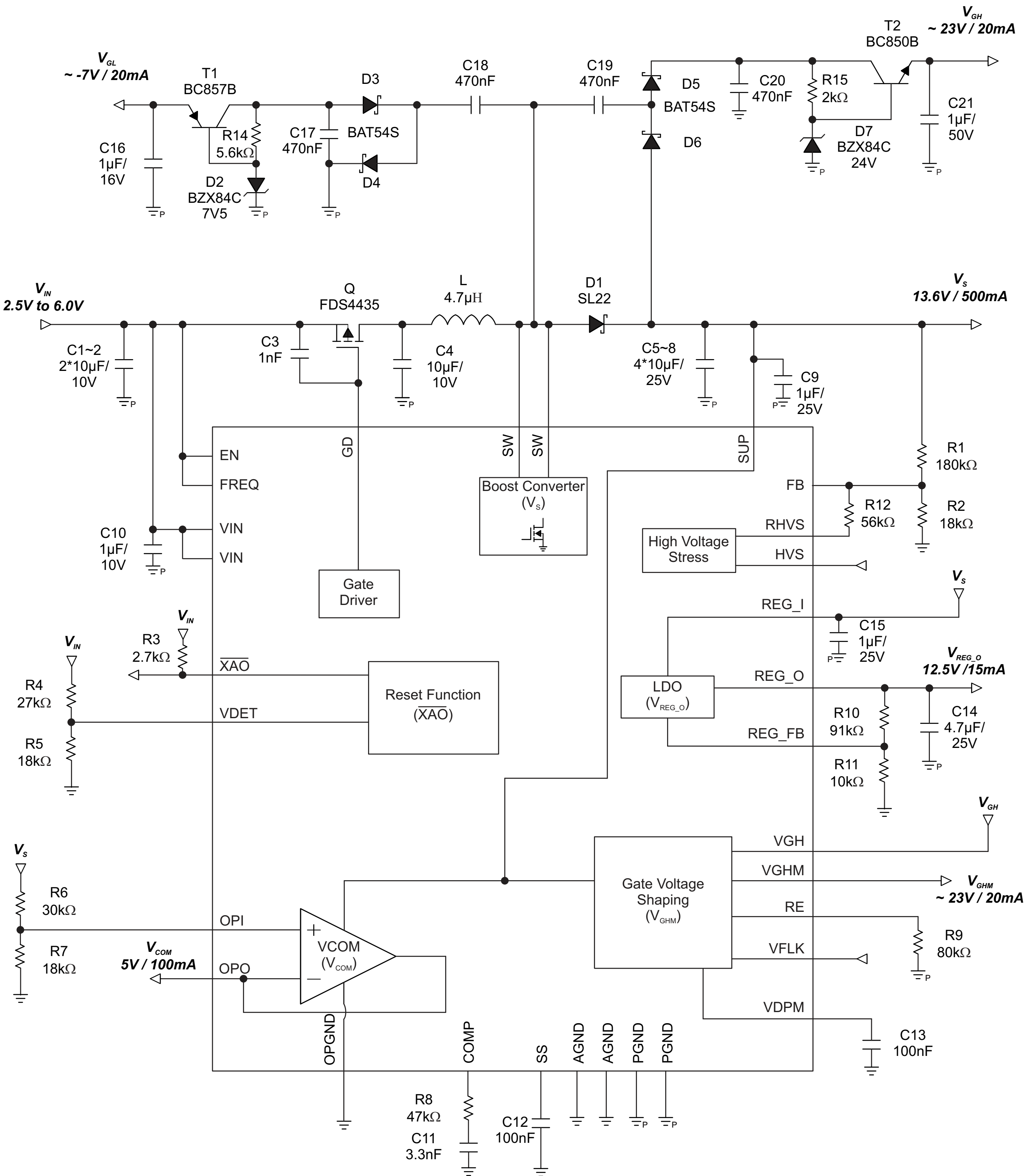


Figure 28. TPS65148 Typical Application with Positive Charge Pump in Doubler Mode Configuration

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65148RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65148	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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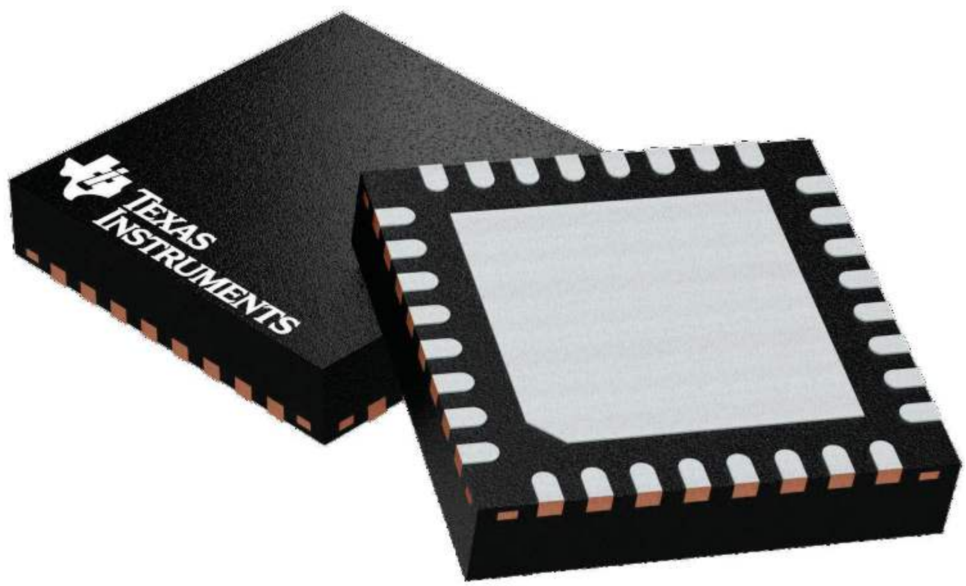
RHB 32

VQFN - 1 mm max height

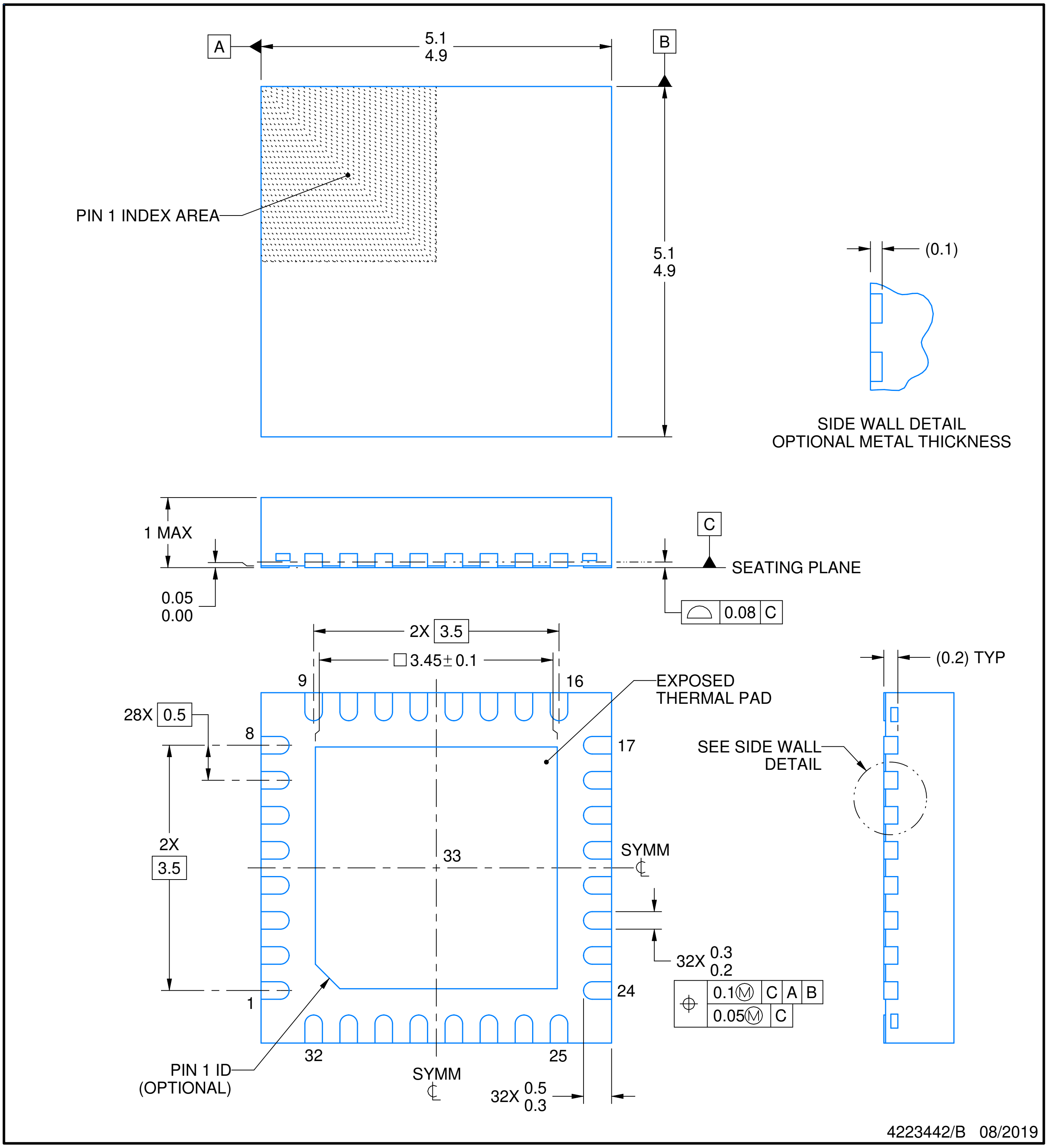
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



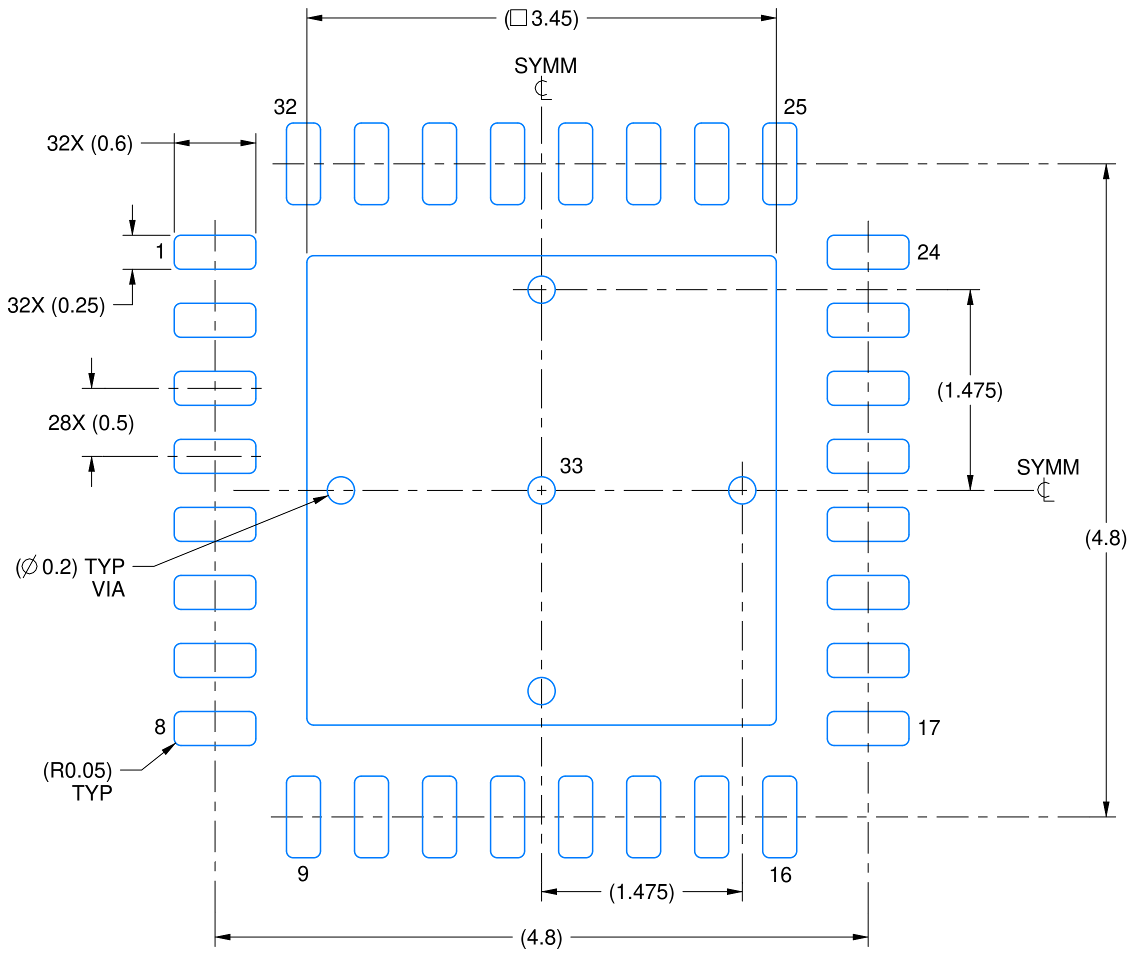
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A

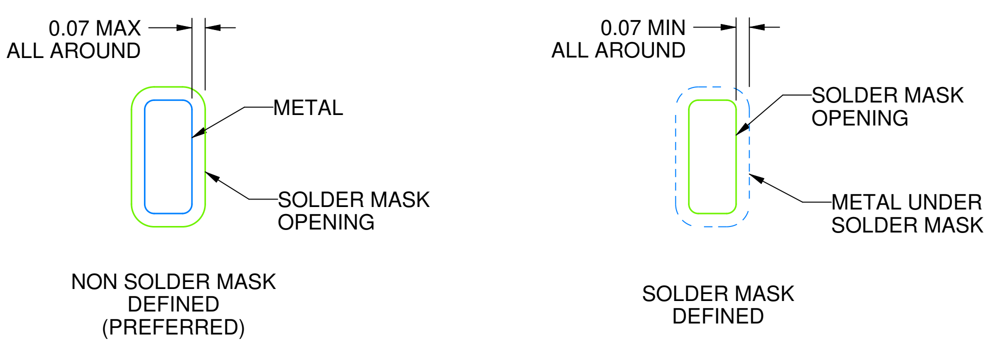


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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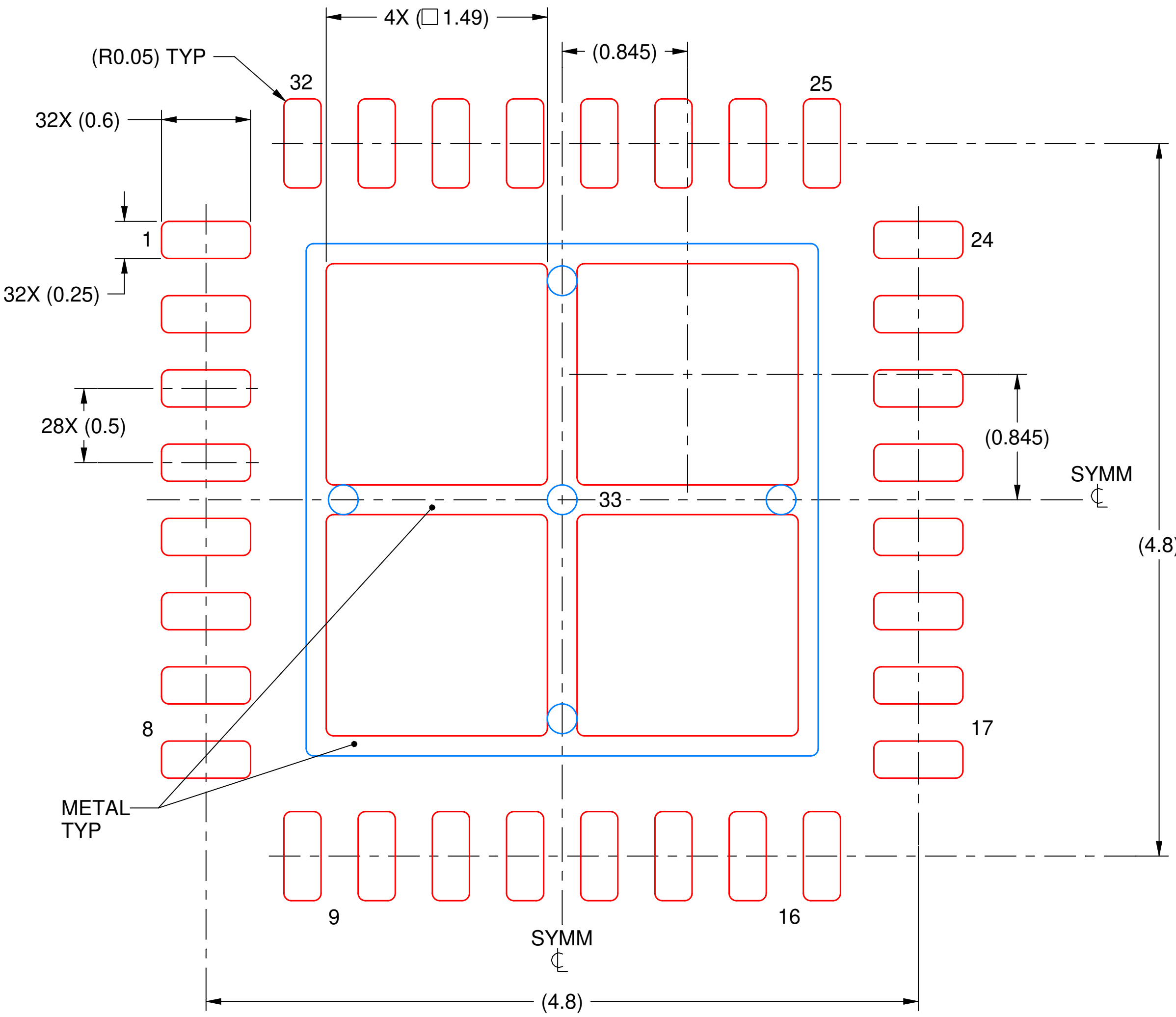
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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