LOW EMI, SPREAD MODULATING, CLOCK GENERATOR

ICS91730

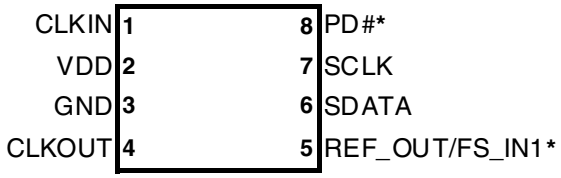
Features/Benefits

- ICS91730 is a Spread Spectrum Clock targeted for Mobile PC and LCD panel applications that generates an EMI-optimized clock signal (EMI peak reduction of 7-14 dB on 3rd-19th harmonics) through use of Spread Spectrum techniques.
- ICS91730 focuses on the lower input frequency range of 14.318 to 80.00 MHz with a spread modulation of 20kHz to 40kHz.

Specifications

- Supply Voltages: VDD = 3.3V ±0.3V
- Frequency range: 14.318 MHz ≤Fin ≥ 80 MHz
- Cyc to Cyc jitter: <150ps
- Output duty cycle 45-55%
- 0°C to +85°C operation
- 8-pin SOIC
- Reference input

Pin Configuration



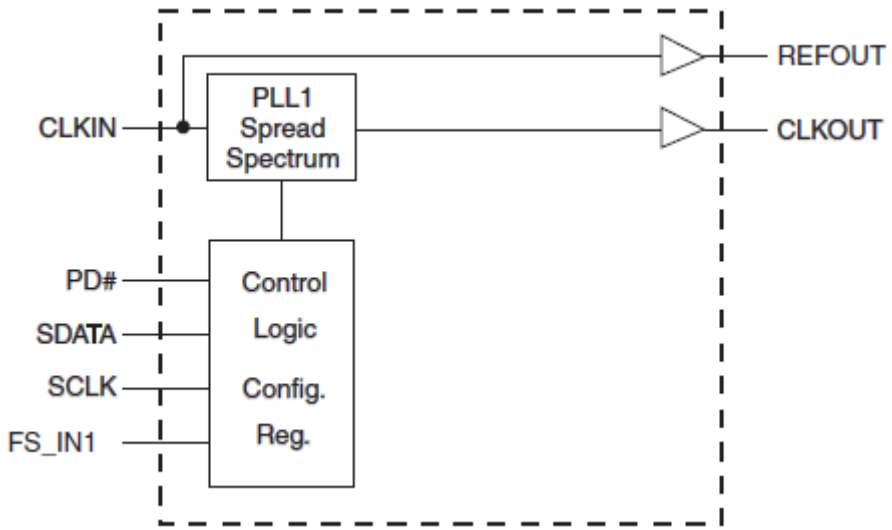
8 Pin SOIC

* Internal Pull-Up Resistor

Functionality

FSIN_1	MHz	Spread % default
0	14.318 MHz in --> 27MHz out	-0.8 down spread
1	27.00MHz in --> 27.00MHz out	-1.25 down spread

Block Diagram



Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	CLKIN	PWR	Input for reference clock.
2	VDD	IN	Power supply, nominal 3.3V
3	GND	OUT	Ground pin.
4	CLKOUT	I/O	Modulated clock output.
5	REF_OUT/FS_IN1*	I/O	Un-modulated 3.3V reference clock output. Frequency select latch input. Refer to the functionality table.
6	SDATA	PWR	Data pin for SMBus circuitry, 5V tolerant.
7	SCLK	PWR	Clock pin of SMBus circuitry, 5V tolerant.
8	PD#*	PWR	Asynchronous active low input pin, with 120Kohm internal pull-up resistor, used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor

Table 1: Frequency Configuration (see I2C Byte0)

	FS4	FS3	FS2	FS1	FS0	Sprd Type	Sprd %
14in/27out	0	0	0	0	0	DOWN SPREAD (-)	0.60
	0	0	0	0	1		0.80
	0	0	0	1	0		1.00
	0	0	0	1	1		1.25
	0	0	1	0	0		1.50
	0	0	1	0	1		2.00
	0	0	1	1	0	CENTER SPD (+/-)	0.50
	0	0	1	1	1		1.00
14in/14out 27in/27out	0	1	0	0	0	DOWN SPREAD (-)	0.60
	0	1	0	0	1		1.00
	0	1	0	1	0		-0.80
	0	1	0	1	1	CTR SPD	+/-0.3
	0	1	1	0	0	DOWN SPREAD (-)	1.50
	0	1	1	0	1		1.75
	0	1	1	1	0		2.00
	0	1	1	1	1		2.50
	1	0	0	0	0		3.00
	1	0	0	0	1		1.25
	1	0	0	1	0	CENTER SPD (+/-)	0.40
	1	0	0	1	1		0.50
	1	0	1	0	0		0.70
	1	0	1	0	1		1.00
	1	0	1	1	0		1.20
	1	0	1	1	1		1.50
48in/48out 66in/66out	1	1	0	0	0	DOWN SPREAD (-)	0.60
	1	1	0	0	1		0.80
	1	1	0	1	0		1.00
	1	1	0	1	1		1.25
	1	1	1	0	0		1.50
	1	1	1	0	1		2.00
	1	1	1	1	0	CENTER SPD (+/-)	0.50
	1	1	1	1	1		1.00

Above is the hard coded 5 bit (32 entry) ROM table.

FS3:0 are ONLY accessible through I2C software programming bits (byte0 bits5:7). FS4 can also be decoded from FS_IN1 latched input hardware pins.

FS_IN1 → FS4. Upon power-up the default is to use hardware selection of FS_IN1 latched value.

FS3 = 0, FS2 = 0, FS1 = 0, FS0 = 1 upon power-up (refer to the functionality table on page 1).

To access non-default spread entries in the ROM, byte0 programming should be used. In order to change the power up default of FS_IN1 = 1 (-1.25% down spread) to any other spread % entry, first change byte0bit 0 to software selection by switching this bit to a '1' and then program the desired percentage by changing byte0 bits 7:3.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$D5_{(H)}$	$D4_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Byte 0	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	-	FS0	Spread/FS0	RW	Srpead Pecentage See Table1 These are I2C bits only		1
Bit 6	-	FS1	Spread/FS1	RW			0
Bit 5		FS2	Spread/FS2	RW			0
Bit 4		FS3	Spread/FS3	RW			0
Bit 3		FS4	FS4	RW			0
Bit 2		PD# Tri_Sate	PD# Tri_Sate	RW	Hi-Z	LOW	1
Bit 1		Spread Enable	Spread Enable	RW	OFF	ON	1
Bit 0		HW/SW Control	Spread Spectrum Control FS 3:4 Hard/Software Select	RW	HW	SW	0

Byte 1	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7		REF_OUT	REF_OUT_Enable	RW	Disable	Enable	1
Bit 6	-	REF_OUT	Slew Rate REF-OUT	RW	Nominal	Fast	1
Bit 5		FS-IN_1	FS-IN_1 Readback	R	-	-	X
Bit 4		(Reserved)	(Reserved)	R	-	-	0
Bit 3		CLK_OUT	Slew Rate CLK-OUT	RW	Nominal	Fast	1
Bit 2		CLK_OUT	CLK_OUT_Enable	RW	Disable	Enable	1
Bit 1		(Reserved)	(Reserved)	R	-	-	1
Bit 0		(Reserved)	(Reserved)	R	-	-	1

Byte 2	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	x	-	(Reserved)	-	-	-	1
Bit 6	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 5	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 4	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 3	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 2	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 1	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 0	x	(Reserved)	(Reserved)	RW	Disable	Enable	1

Byte 3	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 6	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 5	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 4	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 3	x	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 4	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 6	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 5	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 4	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 3	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 5	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	-	-	-	1
Bit 6	X	(Reserved)	(Reserved)	-	-	-	1
Bit 5	X	(Reserved)	(Reserved)	-	-	-	1
Bit 4	X	(Reserved)	(Reserved)	-	-	-	1
Bit 3	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 6	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	Revision ID Bit 3	(Reserved)	R	-	-	1
Bit 6	X	Revision ID Bit 2	(Reserved)	R	-	-	1
Bit 5	X	Revision ID Bit 1	(Reserved)	R	-	-	1
Bit 4	X	Revision ID Bit 0	(Reserved)	R	-	-	1
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	1
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	1
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	1
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS91730. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Supply Voltage..... 3.7 V
Voltage on any pin with respect to GND ... -0.5 to +3.7 V
Storage Temperature..... –55°C to +125°C
Power Dissipation ..... 0.5 W

Electrical Characteristics–Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Powerdown Current	$I_{DD3.3PD}$			1	5	mA
Operating Current	$I_{DD3.3OP}$	fin = 14.318MHz[2]	27		41	mA
		fin = 66.67MHz[2]	32		50	mA
Input Frequency	Fi	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance	Lpin				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	Ts	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

[2]Operating current depends on both the input and output frequencies. The values shown represent the upper and lower extremes. The higher the input/output frequency, the higher the current draw. The relationship is linear.

Electrical Characteristics–CLKOUT

T_A = 0 - 85°C; V_{DD} = 3.3V +/-5%; C_L = 15 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	
Rise Time	tr3	V_{OL} = 0.41V, V_{OH} = 0.86V	0.5	0.6	1	ns
Fall Time	tf3	V_{OH} = 0.86V V_{OL} = 0.41V	0.5	0.6	1	ns
Duty Cycle	d_{t3}	measurement from differential wavefrom - 0.35V to +035V	45	50	55	%
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		50	150	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics–REF

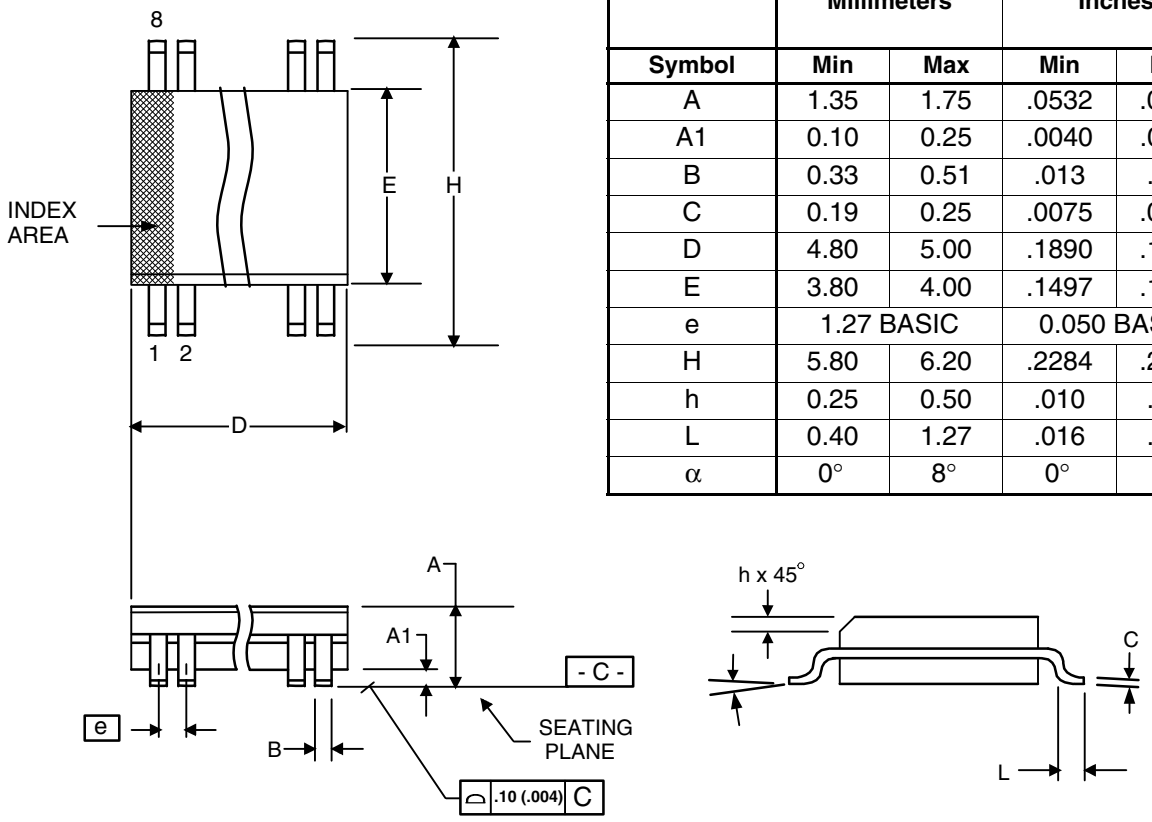
T_A = 0 - 85°C; V_{DD} = 3.3V +/-5%; C_L = 15 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			14.318		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.2	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.2	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		105	300	ps

[1]Guaranteed by design, not 100% tested in production.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
91730AMLF	Tubes	8-pin SOIC	0 to +85°C
91730AMLFT	Tape and Reel	8-pin SOIC	0 to +85°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	Who	Description	Page #
B	06/25/04		Add Lead Free package description to Ordering Information	10
C	06/29/04		Add Revision History table to datasheet.	11
D	05/23/05		1. Revise ABS max ratings. 2. Updated REF Electrical Characteristics table. 3. Updated LF ordering information from "lead free" to "RoHS compliant".	8-10
E	06/04/08		Updated MLF ordering info	9
F	06/16/11	RDW	1. Added operating current specs that were inadvertantly ommitted 2. Updated ordering info to latest format 3. Changed CL from "10-20 pF" to 15 pF	1, 7-9

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.