

BLF8G10L-160; BLF8G10LS-160

Power LDMOS transistor

Rev. 4 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 920 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Test signal	f (MHz)	I_{DQ} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	920 to 960	1100	30	35	19.7	29	-38 [1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier. Carrier spacing 5 MHz.

1.2 Features and benefits

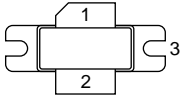
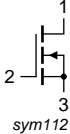
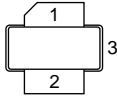
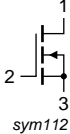
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (920 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 920 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF8G10L-160 (SOT502A)			
1	drain		 sym112
2	gate		
3	source		
BLF8G10LS-160 (SOT502B)			
1	drain		 sym112
2	gate		
3	source		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G10L-160	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF8G10LS-160	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 35\text{ W}$; $V_{DS} = 30\text{ V}$; $I_{Dq} = 1100\text{ mA}$	0.50	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.2\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 220\text{ mA}$	1.5	2.0	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	5	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	37.0	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	0.5	μA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 7.7\text{ A}$	-	14.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 7.7\text{ A}$	-	86	-	$\text{m}\Omega$

7. Test information

Table 7. Functional test information

Test signal: 2-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; $f_1 = 920\text{ MHz}; f_2 = 925\text{ MHz}; f_3 = 955\text{ MHz}; f_4 = 960\text{ MHz};$ RF performance at $V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}; T_{case} = 25\text{ °C};$ unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 35\text{ W}$	19	19.7	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 35\text{ W}$	-	-15	-10	dB
η_D	drain efficiency	$P_{L(AV)} = 35\text{ W}$	27	29	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 35\text{ W}$	-	-38	-34	dBc

7.1 Ruggedness in class-AB operation

The BLF8G10L-160 and BLF8G10LS-160 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}; P_L = 130\text{ W (CW)}; f = 920\text{ MHz to }960\text{ MHz}.$

7.2 Impedance information

Table 8. Typical impedance information

$I_{Dq} = 1100 \text{ mA}$; main transistor $V_{DS} = 30 \text{ V}$.
 Z_S and Z_L defined in Figure 1.

f (MHz)	Z_S (Ω)	Z_L (Ω)
925	4.0 – j3.8	1.7 – j2.5
942	4.4 – j4.2	1.5 – j2.2
960	4.6 – j4.1	1.4 – j2.3

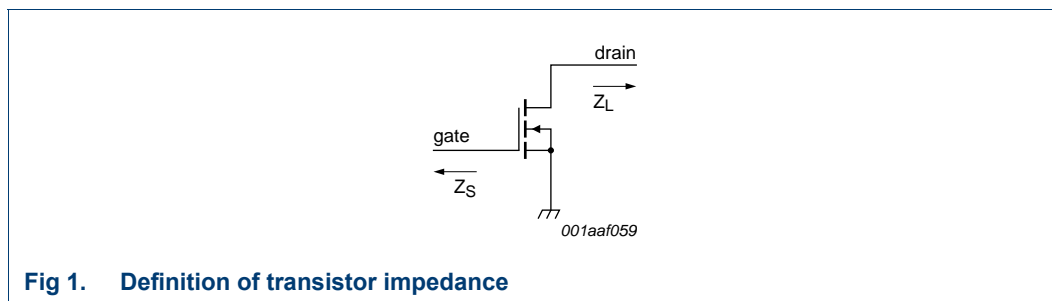
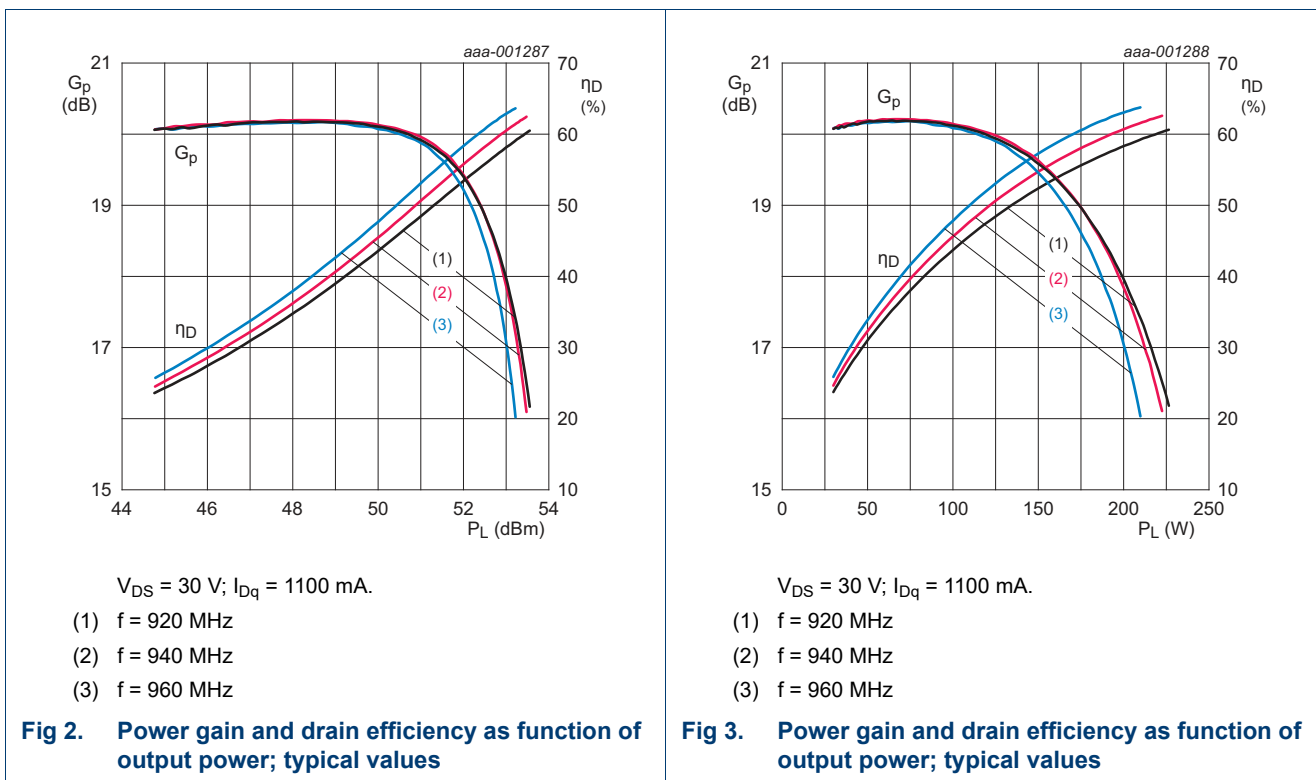
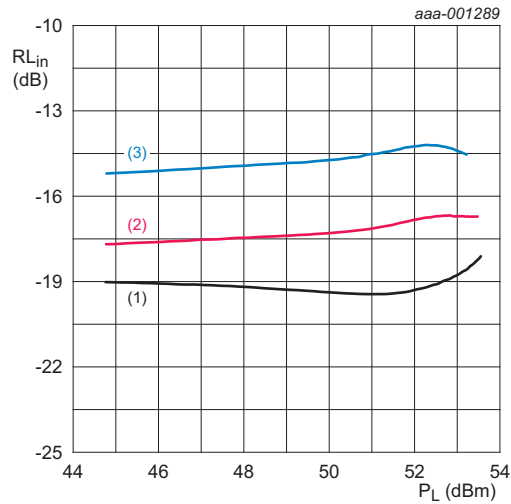


Fig 1. Definition of transistor impedance

7.3 CW pulse

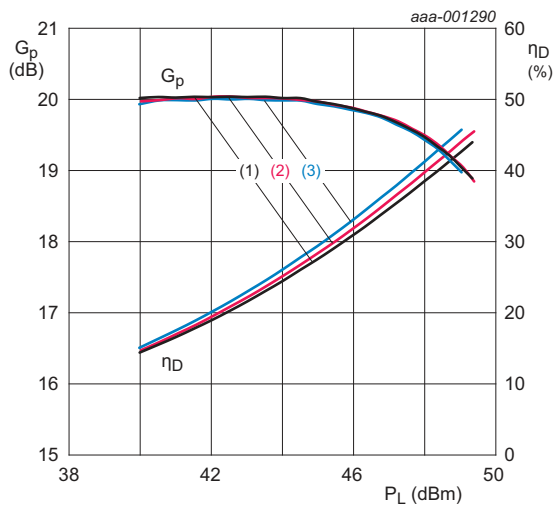




$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}$.
 (1) $f = 920\text{ MHz}$
 (2) $f = 940\text{ MHz}$
 (3) $f = 960\text{ MHz}$

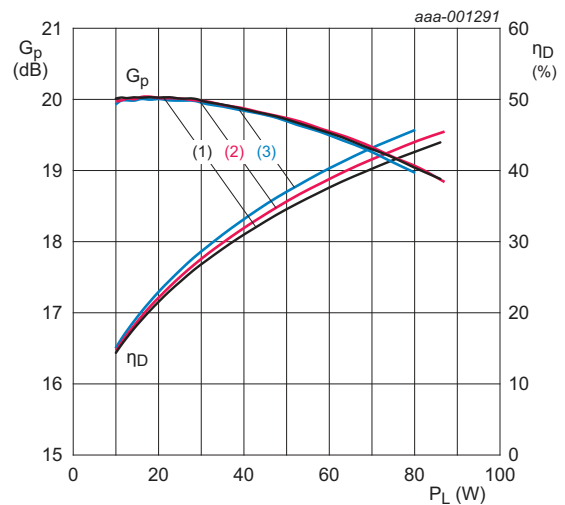
Fig 4. Input return loss as a function of output power; typical values

7.4 2-Carrier W-CDMA



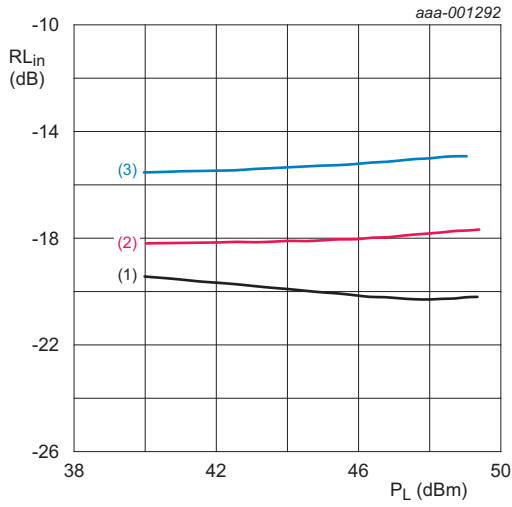
$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}$.
 (1) $f = 920\text{ MHz}$
 (2) $f = 940\text{ MHz}$
 (3) $f = 960\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values



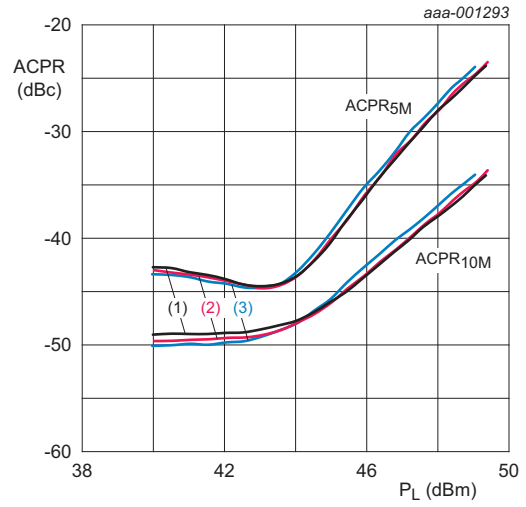
$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}$.
 (1) $f = 920\text{ MHz}$
 (2) $f = 940\text{ MHz}$
 (3) $f = 960\text{ MHz}$

Fig 6. Power gain and drain efficiency as function of output power; typical values



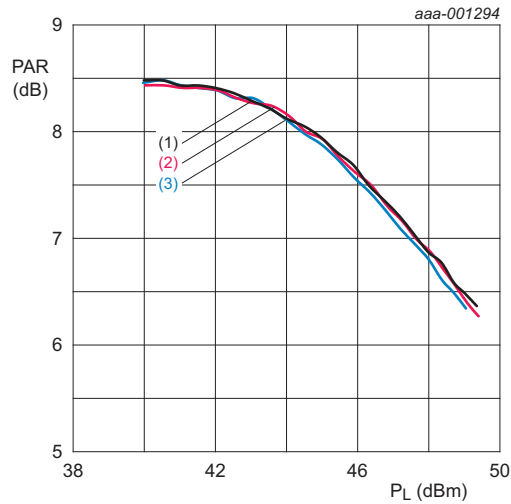
$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}.$
 (1) $f = 920\text{ MHz}$
 (2) $f = 940\text{ MHz}$
 (3) $f = 960\text{ MHz}$

Fig 7. Input return loss as a function of output power; typical values



$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}.$
 (1) $f = 920\text{ MHz}$
 (2) $f = 940\text{ MHz}$
 (3) $f = 960\text{ MHz}$

Fig 8. Adjacent channel power ratio (5 MHz and 10 MHz) as function of output power; typical values



$V_{DS} = 30\text{ V}; I_{Dq} = 1100\text{ mA}.$
 (1) $f = 920\text{ MHz}$
 (2) $f = 940\text{ MHz}$
 (3) $f = 960\text{ MHz}$

Fig 9. Peak-to-average ratio as a function of output power; typical values

7.5 Circuit

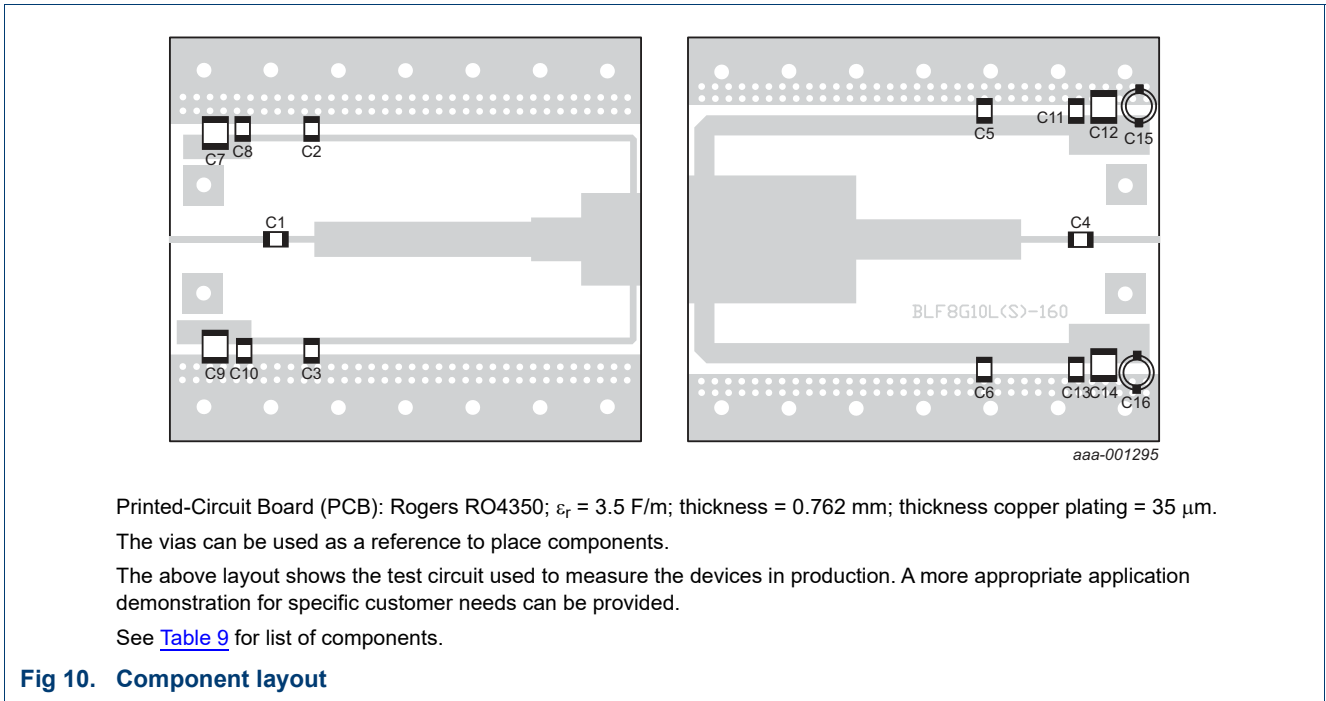


Table 9. List of components

See [Figure 10](#) for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	82 pF	ATC 800B
C7, C9, C12, C14	multilayer ceramic chip capacitor	10 μF	Murata
C8, C10, C11, C13	multilayer ceramic chip capacitor	1 μF	Murata
C15, C16	electrolytic capacitor	470 μF ; 63 V	

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

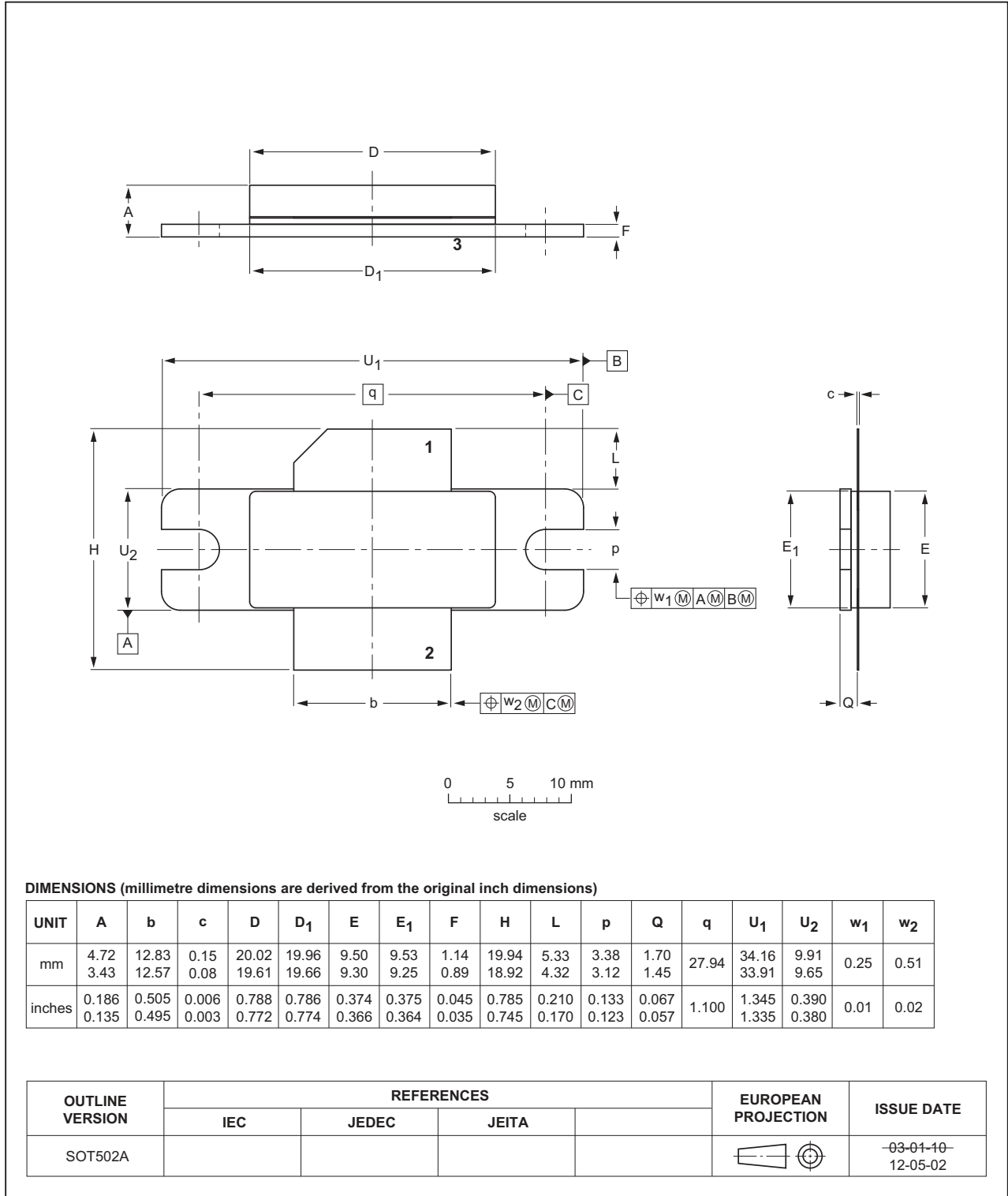


Fig 11. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B

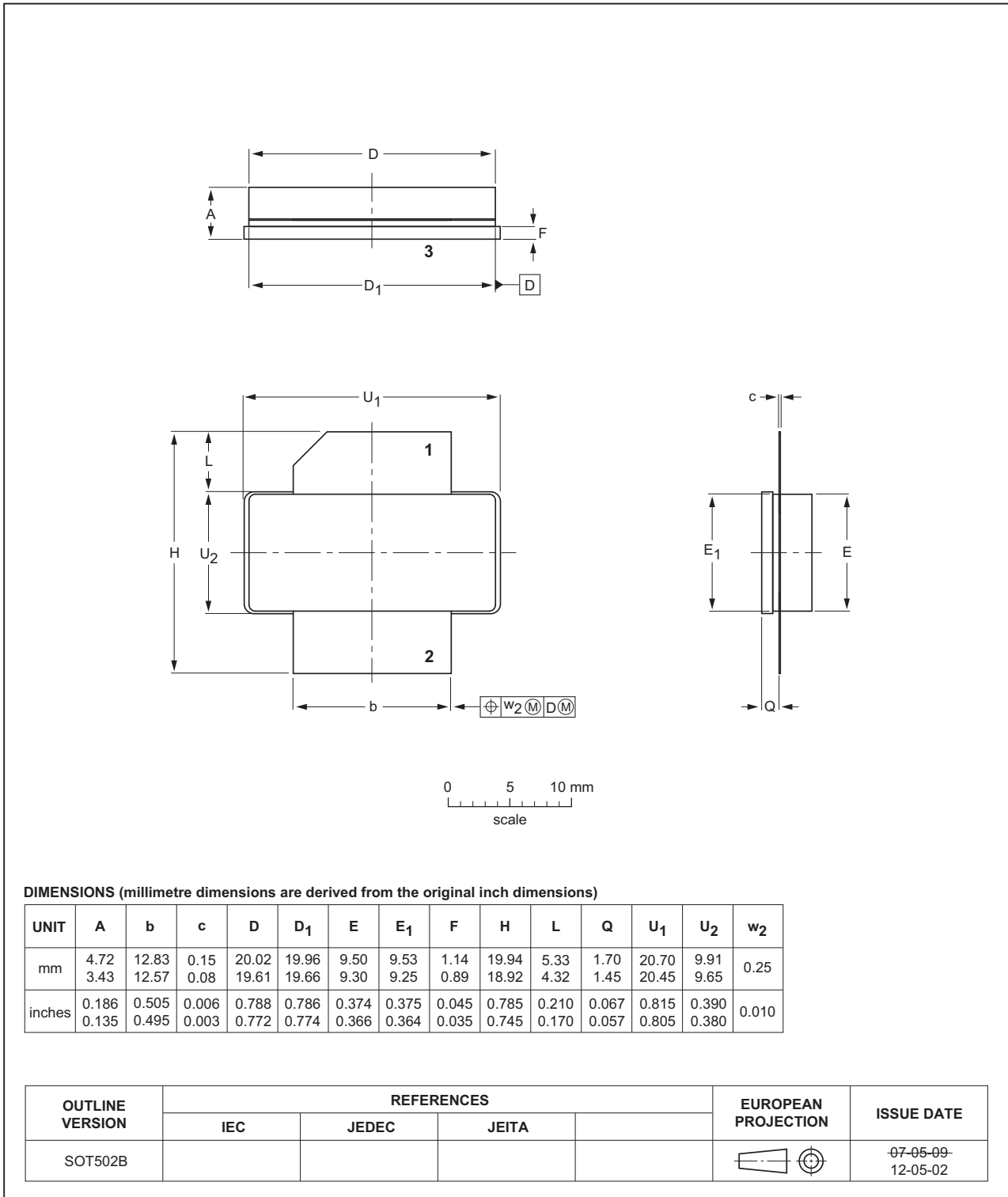


Fig 12. Package outline SOT502B

9. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G10L-160_8G10LS-160#4	20150901	Product data sheet	-	BLF8G10L-160_8G10LS-160 v.3
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
BLF8G10L-160_8G10LS-160 v.3	20120216	Product data sheet		BLF8G10L-160_8G10LS-160 v.2
BLF8G10L-160_8G10LS-160 v.2	20111121	Preliminary data sheet		BLF8G10L-160_8G10LS-160 v.1
BLF8G10L-160_8G10LS-160 v.1	20110519	Objective data sheet	-	-

11. Legal information

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Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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