

56-pin CK505 for Intel Systems

ICS9LPRS525

Recommended Application:

56-pin CK505 compatible clock, w/fully integrated Vreg and series resistors on differential outputs

Output Features:

- 2 - CPU differential low power push-pull pairs
- 7 - SRC differential push-pull pairs
- 1 - CPU/SRC selectable differential low power push-pull pair
- 1 - SRC/DOT selectable differential low power push-pull pair
- 1 - SRC/SE selectable differential push-pull pair/Single-ended outputs
- 5 - PCI, 33MHz
- 1 - USB, 48MHz
- 1 - REF, 14.318MHz

Key Specifications:

- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/- 100ppm frequency accuracy on all outputs
- SRC outputs meet PCIe Gen2 when sourced from PLL3

Features/Benefits:

- Supports spread spectrum modulation, 0 to -0.5% down spread
- Supports CPU clks up to 400MHz
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning

Table 1: CPU Frequency Select Table

| FS _L C ² B0b7 | FS _L B ¹ B0b6 | FS _L A ¹ B0b5 | CPU MHz | SRC MHz | PCI MHz | REF MHz | USB MHz | DOT MHz |
|----------------------------------------|----------------------------------------|----------------------------------------|------------|------------|------------|------------|------------|------------|
| 0 | 0 | 0 | 266.66 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 |
| 0 | 0 | 1 | 133.33 | | | | | |
| 0 | 1 | 0 | 200.00 | | | | | |
| 0 | 1 | 1 | 166.66 | | | | | |
| 1 | 0 | 0 | 333.33 | | | | | |
| 1 | 0 | 1 | 100.00 | | | | | |
| 1 | 1 | 0 | 400.00 | | | | | |
| 1 | 1 | 1 | Reserved | | | | | |

1. FS_LA and FS_LB are low-threshold inputs. Please see V_{IL,FS} and V_{IH,FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS_LC is a three-level input. Please see the V_{IL,FS} and V_{IH,FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Pin Configuration

| | | | |
|-----------------------|----|----|-------------------------|
| PCI0/CR#_A | 1 | 56 | SCLK |
| VDDPCI | 2 | 55 | SDATA |
| PCI1/CR#_B | 3 | 54 | REF0/FSLC/TEST_SEL |
| PCI2/TME | 4 | 53 | VDDREF |
| PCI3/CFG0 | 5 | 52 | X1 |
| PCI4/SRC5_EN | 6 | 51 | X2 |
| PCI_F5/ITP_EN | 7 | 50 | GNDREF |
| GNDPCI | 8 | 49 | FSLB/TEST_MODE |
| VDD48 | 9 | 48 | CK_PWRGD/PD# |
| USB_48MHz/FSLA | 10 | 47 | VDDCPU |
| GND48 | 11 | 46 | CPUT0_LRS |
| VDD96IO | 12 | 45 | CPUC0_LRS |
| DOTT_96_LRS/SRCT0_LRS | 13 | 44 | GNDCPU |
| DOTC_96_LRS/SRCC0_LRS | 14 | 43 | CPUT1_F_LRS |
| GND | 15 | 42 | CPUC1_F_LRS |
| VDD | 16 | 41 | VDDCPUIO |
| SRCT1_LRS/SE1 | 17 | 40 | NC |
| SRCC1_LRS/SE2 | 18 | 39 | CPUT2_ITP_LRS/SRCT8_LRS |
| GND | 19 | 38 | CPUC2_ITP_LRS/SRCC8_LRS |
| VDDPLL3IO | 20 | 37 | VDDSRCIO |
| SRCT2_LRS/SATAT_LRS | 21 | 36 | SRCT7_LRS/CR#_F |
| SRCC2_LRS/SATAC_LRS | 22 | 35 | SRCC7_LRS/CR#_E |
| GNDSRC | 23 | 34 | GNDSRC |
| SRCT3_LRS/CR#_C | 24 | 33 | SRCT6_LRS |
| SRCC3_LRS/CR#_D | 25 | 32 | SRCC6_LRS |
| VDDSRCIO | 26 | 31 | VDDSRC |
| SRCT4_LRS | 27 | 30 | PCI_STOP#/SRCT5_LRS |
| SRCC4_LRS | 28 | 29 | CPU_STOP#/SRCC5_LRS |

56-SSOP & TSSOP

Pin Description

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | PCI0/CR#_A | I/O | 3.3V PCI clock output or Clock Request control A for either SRC0 or SRC2 pair The power-up default is PCI0 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 0 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CRA#_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 7 0 = PCI0 enabled (default) 1= CRA# enabled. Byte 5, bit 6 controls whether CRA# controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CRA# controls SRC0 pair (default), 1= CRA# controls SRC2 pair |
| 2 | VDDPCI | PWR | Power supply for PCI clocks, nominal 3.3V |
| 3 | PCI1/CR#_B | I/O | 3.3V PCI clock output/Clock Request control B for either SRC1 or SRC4 pair The power-up default is PCI1 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the PCI output must first be disabled in byte 2, bit 1 of SMBus address space . After the PCI output is disabled (high-Z), the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CRB#_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 5 0 = PCI1 enabled (default) 1= CRB# enabled. Byte 5, bit 6 controls whether CRB# controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CRB# controls SRC1 pair (default) 1= CRB# controls SRC4 pair |
| 4 | PCI2/TME | I/O | 3.3V PCI clock output / Trusted Mode Enable(TME) Latched Input. This pin is sampled on power-up as follows 0=Overclocking of CPU and SRC allowed 1=Overclocking of CPU and SRC NOT allowed After being sampled on power-up, this pin becomes a 3.3V PCI Output |
| 5 | PCI3/CFG0 | I/O | 3.3V PCI clock output/Configuration Strap. See PCI3 Configuration Table for more information |
| 6 | PCI4/SRC5_EN | I/O | 3.3V PCI clock output / SRC5 pair or PCI_STOP#/CPU_STOP# enable strap. On powerup, the logic value on this pin determines if the SRC5 pair is enabled or if CPU_STOP#/PCI_STOP# is enabled (pins 29 and 30). The latched value controls the pin function on pins 29 and 30 as follows 0 = PCI_STOP#/CPU_STOP# 1 = SRC5/SRC5# |
| 7 | PCI_F5/ITP_EN | I/O | Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 38 and 39 are an ITP or SRC pair. 0 =SRC8/SRC8# 1 = ITP/ITP# |
| 8 | GNDPCI | PWR | Ground pin for the PCI outputs |
| 9 | VDD48 | PWR | Power pin for the 48MHz output and PLL.3.3V |
| 10 | USB_48MHz/FSLA | I/O | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V. |
| 11 | GND48 | PWR | Ground pin for the 48MHz outputs |
| 12 | VDD96IO | PWR | Power supply for DOT96 outputs, 1.05V to 3.3V. |
| 13 | DOTT_96_LRS/SRCT0_LRS | OUT | True clock of low power differential SRC or DOT96 with integrated 33 ohm Rs. The power-up default function is SRC0. After powerup, this pin function may be changed to DOT96 via SMBus Byte 1, bit 7 as follows: 0= SRC0 1=DOT96 |
| 14 | DOTC_96_LRS/SRCC0_LRS | OUT | Complement clock of low power differential SRC or DOT96 with integrated 33 ohm Rs. The power-up default function is SRC0#. After powerup, this pin function may be changed to DOT96# via SMBus Byte 1, bit 7 as follows 0= SRC0# 1=DOT96# |
| 15 | GND | PWR | Ground pin. |
| 16 | VDD | PWR | Power supply, nominal 3.3V |
| 17 | SRCT1_LRS/SE1 | OUT | True clock of low power differential SRC1 clock pair with integrated 33 ohm Rs. / 3.3V single-ended output. The powerup default is 100 MHz SRC, -0.5% downspread. The pin function may be changed via SMBus B1b[4:1] |
| 18 | SRCC1_LRS/SE2 | OUT | Complement clock of low power differential SRC1 clock pair with integrated 33 ohm Rs / 3.3V single-ended output. The powerup default is 100 MHz SRC, -0.5% downspread. The pin function may be changed via SMBus B1b[4:1] |
| 19 | GND | PWR | Ground pin. |
| 20 | VDDPLL3IO | PWR | Power supply for PLL3 outputs. 1.05V to 3.3V. |
| 21 | SRCT2_LRS/SATAT_LRS | OUT | True clock of low power differential SRC/SATA clock pair with integrated Rs. |
| 22 | SRCC2_LRS/SATAC_LRS | OUT | Complement clock of low power differential push-pull SRC/SATA clock pair with integrated 33 ohm Rs. |
| 23 | GNDSRC | PWR | Ground pin for the SRC outputs |
| 24 | SRCT3_LRS/CR#_C | I/O | True clock of low power differential SRC clock pair with integrated 33 ohm Rs./ Clock Request control C for either SRC0 or SRC2 pair. The power-up default is SRCCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 0 or SRC pair 2 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC output must first be disabled in byte 4, bit 7 of SMBus address space . After the SRC output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 2 or pair 0 using the CRC#_EN bit located in byte 5 of SMBUs address space. Byte 5, bit 3 0 = SRCCLK3 enabled (default) 1= CRC# enabled. Byte 5, bit 2 controls whether CRC# controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CRC# controls SRC0 pair (default), 1= CRC# controls SRC2 pair |

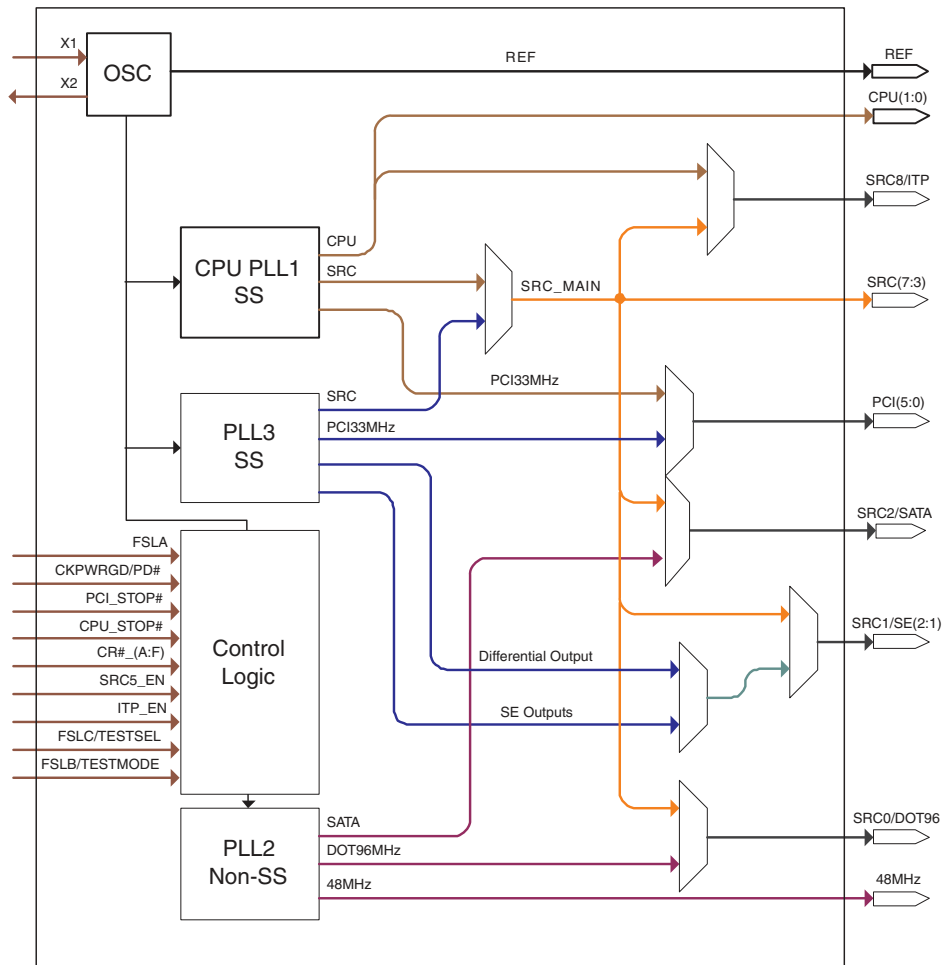
Pin Description (continued)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25 | SRCC3_LRS/CR#_D | I/O | Complementary clock of low power differential SRC clock pair with integrated 33 ohm Rs/ Clock Request control D for either SRC1 or SRC4 pair. The power-up default is SRCLK3 output, but this pin may also be used as a Clock Request control of SRC pair 1 or SRC pair 4 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC output must first be disabled in byte 4, bit 7 of SMBus address space. After the SRC output is disabled, the pin can then be set to serve as a Clock Request pin for either SRC pair 1 or pair 4 using the CRD#_EN bit located in byte 5 of SMBus address space. Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CRD# enabled. Byte 5, bit 0 controls whether CRD# controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CRD# controls SRC1 pair (default), 1 = CRD# controls SRC4 pair |
| 26 | VDDSRCIO | PWR | Power supply for SRC outputs. 1.05V to 3.3V. |
| 27 | SRCT4_LRS | OUT | True clock of low power differential SRC clock pair with integrated 33 ohm Rs. |
| 28 | SRCC4_LRS | OUT | Complement clock of low power differential SRC clock pair with 33 ohm integrated Rs. |
| 29 | CPU_STOP#/SRCC5_LRS | I/O | Stops all CPUCLK, except those set to be free running clocks / Complement clock of low power differential SRC pair with 33 ohm integrated Rs. |
| 30 | PCI_STOP#/SRCT5_LRS | I/O | Stops all PCICLKs at logic 0 level, when low. Free running PCICLKs are not effected by this input. / True clock of low power differential SRC pair with integrated 33 ohm Rs. |
| 31 | VDDSRC | PWR | Supply for SRC PLL, 3.3V nominal |
| 32 | SRCC6_LRS | OUT | Complement clock of low power differential SRC clock pair with 33 ohm integrated Rs. |
| 33 | SRCT6_LRS | OUT | True clock of low power differential SRC clock pair with integrated 33 ohm Rs. |
| 34 | GNDSRC | PWR | Ground pin for the SRC outputs |
| 35 | SRCC7_LRS/CR#_E | I/O | Complement clock of differential push-pull SRC clock pair with 33 ohm integrated Rs. / Clock Request control E for SRC6 pair. The power-up default is SRC7#, but this pin may also be used as a Clock Request control of SRC6 via SMBus. Before configuring this pin as a Clock Request Pin, the SRC7 output pair must first be disabled in byte 3, bit 3 of SMBus configuration space. After the SRC output is disabled (high-Z), the pin can then be set to serve as a Clock Request for SRC6 pair using byte 6, bit 7 of SMBus configuration space Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CRE# enabled |
| 36 | SRCT7_LRS/CR#_F | I/O | True clock of differential push-pull SRC clock pair/ Clock Request control 8 for SRC8 pair The power-up default is SRC7, but this pin may also be used as a Clock Request control of SRC8 via SMBus. Before configuring this pin as a Clock Request Pin, the SR |
| 37 | VDDSRCIO | PWR | Power supply for SRC outputs. 1.05V to 3.3V. |
| 38 | CPUC2_ITP_LRS/SRCC8_LRS | OUT | Complement clock of low power differential CPU2/Complement clock of differential SRC pair. 33 ohm Rs is integrated. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8# 1 = ITP# |
| 39 | CPUT2_ITP_LRS/SRCT8_LRS | OUT | True clock of low power differential CPU2/True clock of differential SRC pair. 33 ohm Rs is integrated. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8 1 = ITP |
| 40 | NC | N/A | No Connect |
| 41 | VDDCPUIO | PWR | Power supply for CPU outputs, 1.05V to 3.3V. |
| 42 | CPUC1_F_LRS | OUT | Complementary clock of low power differential push-pull CPU output with integrated 33 ohm Rs. This CPU clock is free running during iAMT. |
| 43 | CPUT1_F_LRS | OUT | True clock of differential push-pull CPU clock pair with integrated 33 ohm Rs. This clock is free running during iAMT. |
| 44 | GNDCPU | PWR | Ground pin for the CPU outputs |
| 45 | CPUC0_LRS | OUT | Complement clock of low power differential CPU clock pair with integrated 33 ohm Rs. |
| 46 | CPUT0_LRS | OUT | True clock of low power differential CPU clock pair with integrated 33 ohm Rs. |
| 47 | VDDCPU | PWR | Supply for CPU PLL, 3.3V nominal |
| 48 | CK_PWRGD/PD# | IN | Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode |
| 49 | FSLB/TEST_MODE | IN | 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table. |
| 50 | GNDREF | PWR | Ground pin for the REF outputs. |
| 51 | X2 | OUT | Crystal output, Nominally 14.318MHz |
| 52 | X1 | IN | Crystal input, Nominally 14.318MHz. |
| 53 | VDDREF | PWR | Ref. XTAL power supply, nominal 3.3V |
| 54 | REF0/FSLC/TEST_SEL | I/O | 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. /TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table |
| 55 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 56 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |

General Description

ICS9LPRS525 is compliant Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for Intel desktop chipsets. ICS9LPRS525 is driven with a 14.318MHz crystal. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support.

Block Diagram



Power Groups

| Pin Number | | Description |
|------------|--------|----------------------|
| VDD | GND | |
| 41, 47 | 44 | CPUCLK |
| 16 | 15 | Master Clock, Analog |
| 26, 31, 37 | 23, 34 | SRCCLK |
| 20 | 19 | PLL3/SE |
| 12 | 11 | DOT 96Mhz |
| 9 | 11 | USB 48 |
| 53 | 50 | Xtal, REF |
| 2 | 8 | PCICLK |

Absolute Maximum Ratings - DC Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|------------------------|-----------------|-------------------------------------|-----------|-----|-------|-------|
| Maximum Supply Voltage | VDDxxx | Supply Voltage | | 4.6 | V | 7 |
| Maximum Supply Voltage | VDDxxx_IO | Low-Voltage Differential I/O Supply | | 3.8 | V | 7 |
| Maximum Input Voltage | V _{IH} | 3.3V Inputs | | 4.6 | V | 4,5,7 |
| Minimum Input Voltage | V _{IL} | Any Input | GND - 0.5 | | V | 4,7 |
| Storage Temperature | T _s | - | -65 | 150 | °C | 4,7 |
| Case Temperature | T _c | | | 115 | °C | 4,7 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | V | 6,7 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied, nor guaranteed.

³Maximum input voltage is not to exceed VDD

Electrical Characteristics - Input/Supply/Common Output DC Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-----------------------------------------------|-------------------------|---------------------------------------------------------------------------------------------------------|-----------------------|-----------------------|-------|-------|
| Ambient Operating Temp | T _{ambient} | - | 0 | 70 | °C | |
| Supply Voltage | VDDxxx | Supply Voltage | 3.135 | 3.465 | V | |
| Supply Voltage | VDDxxx_IO | Low-Voltage Differential I/O Supply | 0.9975 | 3.465 | V | 10 |
| Input High Voltage | V _{IHSE} | Single-ended 3.3V inputs | 2 | V _{DD} + 0.3 | V | 3 |
| Input Low Voltage | V _{ILSE} | Single-ended 3.3V inputs | V _{SS} - 0.3 | 0.8 | V | 3 |
| Low Threshold Input- High Voltage | V _{IH_FS_TEST} | 3.3 V +/-5% | 2 | VDD + 0.3 | V | 8 |
| Low Threshold Input- FSC = '1' Voltage | V _{IH_FS_FSC} | 3.3 V +/-5% | 0.7 | 1.5 | V | 8 |
| Low Threshold Input- FSA,FSB = '1' Voltage | V _{IH_FS_FSAB} | 3.3 V +/-5% | 0.7 | VDD+0.3 | V | |
| Low Threshold Input-Low Voltage | V _{IL_FS} | 3.3 V +/-5% | V _{SS} - 0.3 | 0.35 | V | |
| PCI3/CFG0 Input | V _{IL_CFGHI} | Optional input, 2.75V typ. | 2.4 | VDD+0.3 | V | 9, 10 |
| PCI3/CFG0 Input | V _{IL_CFGMID} | Optional input, 1.65V typ. | 1.3 | 2 | V | 9, 10 |
| PCI3/CFG0 Input | V _{IL_CFGLO} | Optional input, 0.55V typ. | V _{SS} - 0.3 | 0.9 | V | 9, 10 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | 5 | uA | 2 |
| Input Leakage Current | I _{INRES} | Inputs with pull up or pull down resistors V _{IN} = V _{DD} , V _{IN} = GND | -200 | 200 | uA | |
| Output High Voltage | V _{OHSE} | Single-ended outputs, I _{OH} = -1mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OLSE} | Single-ended outputs, I _{OL} = 1 mA | | 0.4 | V | 1 |
| Operating Supply Current | I _{DDOP3.3} | Full Active, C _L = Full load; I _{DD} 3.3V | | 115 | mA | |
| | I _{DDPIO} | Full Active, C _L = Full load; IDD IO | | 55 | mA | 10 |
| iAMT Mode Current | I _{DDIAMT3.3} | M1 mode, 3.3V Rail | | 36 | mA | |
| | I _{DDIAMTIO} | M1 Mode, IO Rail | | 10 | mA | |
| Powerdown Current | I _{DDPD3.3} | Power down mode, 3.3V Rail | | 5 | mA | |
| | I _{DDPDIO} | Power down mode, IO Rail | | 0.1 | mA | 10 |
| Input Frequency | F _i | V _{DD} = 3.3 V | | 15 | MHz | |
| Pin Inductance | L _{pin} | | | 7 | nH | |
| Input Capacitance | C _{IN} | Logic Inputs | 1.5 | 5 | pF | |
| | C _{OUT} | Output pin capacitance | | 6 | pF | |
| | C _{INX} | X1 & X2 pins | | 6 | pF | |
| Clk Stabilization | T _{STAB} | From VDD Power-Up or de-assertion of PD to 1st clock | | 1.8 | ms | |
| Tdrive_CR_off | T _{DRCROFF} | Output stop after CR deasserted | | 400 | ns | |
| Tdrive_CR_on | T _{DRCRON} | Output run after CR asserted | | 0 | us | |
| Tdrive_CPU | T _{DRSRC} | CPU output enable after PCI_STOP# de-assertion | | 10 | ns | |
| Tfall_SE | T _{FALL} | Fall/rise time of all 3.3V control inputs from 20-80% | | 10 | ns | |
| Trise_SE | T _{RISE} | | | 10 | ns | |
| SMBus Voltage | V _{DD} | | 2.7 | 5.5 | V | |
| Low-level Output Voltage | V _{OLSMB} | @ I _{PULLUP} | | 0.4 | V | |
| Current sinking at V _{OLSMB} = 0.4 V | I _{PULLUP} | SMB Data Pin | 4 | | mA | |
| SCLK/SDATA Clock/Data Rise Time | T _{RI2C} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | 1000 | ns | |
| SCLK/SDATA Clock/Data Fall Time | T _{FI2C} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | 300 | ns | |
| Maximum SMBus Operating Frequency | F _{SMBUS} | | | 100 | kHz | |

NOTES on Input/Supply/Common Output DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

- ¹Signal is required to be monotonic in this region.
- ²input leakage current does not include inputs with pull-up or pull-down resistors
- ³3.3V referenced inputs are: PCI_STOP#, CPU_STOP#, TME, SRC5_EN, ITP_EN, SCLK, SDATA, TESTMODE, TESTSEL, CKPWRGD and CR# inputs if selected.
- ⁴Intentionally blank
- ⁵Maximum VIH is not to exceed VDD
- ⁶Human Body Model
- ⁷Operation under these conditions is neither implied, nor guaranteed.
- ⁸Frequency Select pins which have tri-level input
- ⁹PCI3/CFG0 is optional

AC Electrical Characteristics - Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|----------------------------|-----------|--------------------------|------|------|-------|-------|
| Rising Edge Slew Rate | tSLR | Averaging on | 2.5 | 4 | V/ns | 2, 3 |
| Falling Edge Slew Rate | tFLR | Averaging on | 2.5 | 4 | V/ns | 2, 3 |
| Slew Rate Variation | tSLVAR | Averaging on | | 20 | % | 1, 10 |
| Differential Voltage Swing | VSWING | Averaging off | 300 | | mV | 2 |
| Crossing Point Voltage | VXABS | Averaging off | 300 | 550 | mV | 1,4,5 |
| Crossing Point Variation | VXABSVAR | Averaging off | | 140 | mV | 1,4,9 |
| Maximum Output Voltage | VHIGH | Averaging off | | 1150 | mV | 1,7 |
| Minimum Output Voltage | VLOW | Averaging off | -300 | | mV | 1,8 |
| Duty Cycle | DCYC | Averaging on | 45 | 55 | % | 2 |
| CPU[1:0] Skew | CPUSKEW10 | Differential Measurement | | 100 | ps | 1 |
| CPU[2..ITP:0] Skew | CPUSKEW20 | Differential Measurement | | 150 | ps | 1 |
| SRC[10:0] Skew | SRCSKEW | Differential Measurement | | 3000 | ps | 1,6 |

NOTES on DIF Output AC Specs: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

- ¹Measurement taken for single ended waveform on a component test board (not in system)
- ²Measurement taken from differential waveform on a component test board. (not in system)
- ³Slew rate emasured through V_swing voltage range centered about differential zero
- ⁴Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)
- ⁵Only applies to the differential rising edge (Clock rising, Clock# falling)
- ⁶Total distributed intentional SRC to SRC skew. Maximum allowable interpair skew is 150 ps.
- ⁷The max voltage including overshoot.
- ⁸The min voltage including undershoot.
- ⁹The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross induced modulation by setting C_cross_delta to be smaller than V_Cross absolute
- ¹⁰Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage

Clock Jitter Specs - Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|-----------------------------|---------|--------------------------|-----|-----|-------|-------|
| CPU Jitter - Cycle to Cycle | CPUJC2C | Differential Measurement | | 85 | ps | 1 |
| SRC Jitter - Cycle to Cycle | SRCJC2C | Differential Measurement | | 125 | ps | 1 |
| DOT Jitter - Cycle to Cycle | DOTJC2C | Differential Measurement | | 250 | ps | 1 |

NOTES on DIF Output Jitter: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

- ¹Jitter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the receiver

Differential Clock Tolerances

| | CPU | SRC | DOT96 | | |
|-----------------------|--------|--------|-------|--|-----|
| PPM tolerance | 100 | 100 | 100 | | ppm |
| Cycle to Cycle Jitter | 85 | 125 | 250 | | ps |
| Spread | -0.50% | -0.50% | 0 | | % |

Clock Periods - Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|----------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| CPU | 100.00 | 9.91400 | | 9.99900 | 10.00000 | 10.00100 | | 10.08600 | ns | 1,2 |
| | 133.33 | 7.41425 | | 7.49925 | 7.50000 | 7.50075 | | 7.58575 | ns | 1,2 |
| | 166.67 | 5.91440 | | 5.99940 | 6.00000 | 6.00060 | | 6.08560 | ns | 1,2 |
| | 200.00 | 4.91450 | | 4.99950 | 5.00000 | 5.00050 | | 5.08550 | ns | 1,2 |
| | 266.67 | 3.66462 | | 3.74962 | 3.75000 | 3.75037 | | 3.83537 | ns | 1,2 |
| | 333.33 | 2.91470 | | 2.99970 | 3.00000 | 3.00030 | | 3.08530 | ns | 1,2 |
| | 400.00 | 2.41475 | | 2.49975 | 2.50000 | 2.50025 | | 2.58525 | ns | 1,2 |
| SRC/SATA | 100.00 | 9.87400 | 9.99900 | 10.00000 | 10.00100 | 10.12600 | ns | 1,2 | | |
| DOT96 | 96.00 | 10.16563 | 10.41563 | 10.41667 | 10.41771 | 10.66771 | ns | 1,2 | | |

Clock Periods - Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| CPU | 99.75 | 9.91406 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.13607 | ns | 1,2 |
| | 133.00 | 7.41430 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.62330 | ns | 1,2 |
| | 166.25 | 5.91444 | 5.99944 | 6.01444 | 6.01504 | 6.01564 | 6.03064 | 6.11564 | ns | 1,2 |
| | 199.50 | 4.91453 | 4.99953 | 5.01203 | 5.01253 | 5.01303 | 5.02553 | 5.11053 | ns | 1,2 |
| | 266.00 | 3.66465 | 3.74965 | 3.75902 | 3.75940 | 3.75977 | 3.76915 | 3.85415 | ns | 1,2 |
| | 332.50 | 2.91472 | 2.99972 | 3.00722 | 3.00752 | 3.00782 | 3.01532 | 3.10032 | ns | 1,2 |
| | 399.00 | 2.41477 | 2.49977 | 2.50602 | 2.50627 | 2.50652 | 2.51277 | 2.59777 | ns | 1,2 |
| SRC | 99.75 | 9.87406 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.17607 | ns | 1,2 |

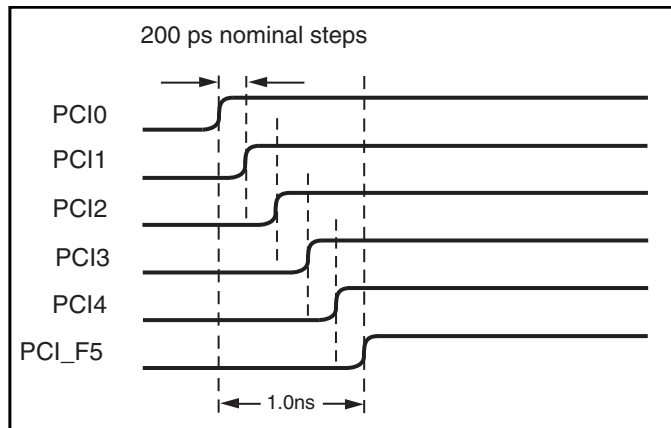
¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy specifications are guaranteed with the assumption that the crystal input is tuned to exactly 14.31818MHz.

Electrical Characteristics - PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|------------------------------|-----------------------|----------------------------------------|----------|----------|-------|-------|
| Long Accuracy | ppm | see T _{period} min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | T _{period} | 33.33MHz output no spread | 29.99700 | 30.00300 | ns | 2 |
| | | 33.33MHz output spread | 30.08421 | 30.23459 | ns | 2 |
| Absolute min/max period | T _{abs} | 33.33MHz output no spread | 29.49700 | 30.50300 | ns | 2 |
| | | 33.33MHz output nominal/spread | 29.56617 | 30.58421 | ns | 2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.55 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -33 | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 30 | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | 38 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Pin to Pin Skew | t _{skew} | V _T = 1.5 V | | 250 | ps | 2 |
| Intentional PCI to PCI delay | t _{skew} | V _T = 1.5 V | 100 | 200 | ps | 2 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 55 | % | 2 |
| Jitter, Cycle to cycle | t _{JCYC-CYC} | V _T = 1.5 V | | 500 | ps | 2 |

Intentional PCI Clock to Clock Delay



Electrical Characteristics - USB48MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|-------------------------|-----------------------|----------------------------------------|----------|----------|-------|-------|
| Long Accuracy | ppm | see T _{period} min-max values | -100 | 100 | ppm | 2,4 |
| Clock period | T _{period} | 48.00MHz output nominal | 20.83125 | 20.83542 | ns | 2,3 |
| Absolute min/max period | T _{abs} | 48.00MHz output nominal | 20.48125 | 21.18542 | ns | 2 |
| CLK High Time | T _{HIGH} | | 8.216563 | 11.15198 | V | |
| CLK Low time | T _{LOW} | | 7.816563 | 10.95198 | V | |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.55 | V | |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -29 | | mA | |
| | | V _{OH} @ MAX = 3.135 V | | -23 | mA | |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 29 | | mA | |
| | | V _{OL} @ MAX = 0.4 V | | 27 | mA | |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 2 | V/ns | 1 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 2 | V/ns | 1 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 55 | % | 2 |
| Jitter, Cycle to cycle | t _{JCYC-CYC} | V _T = 1.5 V | | 350 | ps | 2 |

Electrical Characteristics - REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-------------------------|----------|----------------------------------------|----------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 2, 4 |
| Clock period | Tperiod | 14.318MHz output nominal | 69.82033 | 69.86224 | ns | 2, 3 |
| Absolute min/max period | Tab | 14.318MHz output nominal | 69.83400 | 70.84800 | ns | 2 |
| CLK High Time | THIGH | | 29.97543 | 38.46654 | V | |
| CLK Low time | TLOW | | 29.57543 | 38.26654 | V | |
| Output High Voltage | VOH | IOH = -1 mA | 2.4 | | V | |
| Output Low Voltage | VOL | IOL = 1 mA | | 0.4 | V | |
| Output High Current | IOH | VOH @MIN = 1.0 V, VOH@MAX = 3.135 V | -33 | -33 | mA | |
| Output Low Current | IOL | VOL @MIN = 1.95 V, VOL @MAX = 0.4 V | 30 | 38 | mA | |
| Rising Edge Slew Rate | tSLR | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1 |
| Falling Edge Slew Rate | tFLR | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1 |
| Duty Cycle | dt1 | VT = 1.5 V | 45 | 55 | % | 2 |
| Jitter, Cycle to cycle | tjcy-cyc | VT = 1.5 V | | 1000 | ps | 2 |

NOTES on SE outputs: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹Edge rate in system is measured from 0.8V to 2.0V.

²Duty cycle, Period and Jitter are measured with respect to 1.5V

³The average period over any 1us period of time

⁴Using frequency counter with the measurement interval equal or greater than 0.15s, target frequencies are 14.318180 MHz, 33.333333MHz and 48.000000MHz

Table 1: CPU Frequency Select Table

| FS _L C ² B0b7 | FS _L B ¹ B0b6 | FS _L A ¹ B0b5 | CPU MHz | SRC MHz | PCI MHz | REF MHz | USB MHz | DOT MHz |
|----------------------------------------|----------------------------------------|----------------------------------------|------------|------------|------------|------------|------------|------------|
| 0 | 0 | 0 | 266.66 | 100.00 | 33.33 | 14.318 | 48.00 | 96.00 |
| 0 | 0 | 1 | 133.33 | | | | | |
| 0 | 1 | 0 | 200.00 | | | | | |
| 0 | 1 | 1 | 166.66 | | | | | |
| 1 | 0 | 0 | 333.33 | | | | | |
| 1 | 0 | 1 | 100.00 | | | | | |
| 1 | 1 | 0 | 400.00 | | | | | |
| 1 | 1 | 1 | Reserved | | | | | |

1. FS_LA and FS_LB are low-threshold inputs. Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.
Also refer to the Test Clarification Table.
2. FS_LC is a three-level input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Table 2: PLL3 Quick Configuration (only applies in Mode 0, see Table 6)

| B1b4 | B1b3 | B1b2 | B1b1 | Pin 17 | Pin 18 | Spread | Comment |
|------|------|------|------|----------------|--------|------------------|------------------------------------|
| | | | | MHz | MHz | % | |
| 0 | 0 | 0 | 0 | PLL 3 disabled | | | |
| 0 | 0 | 0 | 1 | 100.00 | 100.00 | 0.5% Down Spread | SRC clocks from SRC_MAIN |
| 0 | 0 | 1 | 0 | 100.00 | 100.00 | 0.5% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 0 | 1 | 1 | 100.00 | 100.00 | 1% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 1 | 0 | 0 | 100.00 | 100.00 | 1.5% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 1 | 0 | 1 | 100.00 | 100.00 | 2% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 1 | 1 | 0 | 100.00 | 100.00 | 2.5% Down Spread | Only SRCCLK1 from PLL3 |
| 0 | 1 | 1 | 1 | N/A | N/A | N/A | N/A |
| 1 | 0 | 0 | 0 | 24.576 | 24.576 | None | 24.576Mhz on SE1 and SE2 |
| 1 | 0 | 0 | 1 | 24.576 | 98.304 | None | 24.576Mhz on SE1, 98.304Mhz on SE2 |
| 1 | 0 | 1 | 0 | 98.304 | 98.304 | None | 98.304Mhz on SE1 and SE2 |
| 1 | 0 | 1 | 1 | 27.000 | 27.000 | None | 27Mhz on SE1 and SE2 |
| 1 | 1 | 0 | 0 | 25.000 | 25.000 | None | 25Mhz on SE1 and SE2 |
| 1 | 1 | 0 | 1 | N/A | N/A | N/A | N/A |
| 1 | 1 | 1 | 0 | N/A | N/A | N/A | N/A |
| 1 | 1 | 1 | 1 | N/A | N/A | N/A | N/A |

Table 3: IO_Vout select table

| B9b2 | B9b1 | B9b0 | IO_Vout |
|------|------|------|---------|
| 0 | 0 | 0 | 0.3V |
| 0 | 0 | 1 | 0.4V |
| 0 | 1 | 0 | 0.5V |
| 0 | 1 | 1 | 0.6V |
| 1 | 0 | 0 | 0.7V |
| 1 | 0 | 1 | 0.8V |
| 1 | 1 | 0 | 0.9V |
| 1 | 1 | 1 | 1.0V |

Table 4: Device ID table

| B8b7 | B8b6 | B8b5 | B8b4 | Comment |
|------|------|------|------|--------------|
| 0 | 0 | 0 | 0 | 56 pin TSSOP |

Table 5: Slew Rate Selection Table

| Bit 1 | Bit 0 | Slew Rate |
|-------|-------|-----------------|
| 0 | 0 | HI-Z |
| 0 | 1 | 0.7X (1.4V/ns) |
| 1 | 0 | 0.8X (1.6 V/ns) |
| 1 | 1 | 1X (2.0 V/ns) |

Table 6. PCI3 Configuration Table

| PCI3/CFG0 HW Strap | PCI2/TME HW Strap | Note: 2 bits are needed since CFG0 is tri-level input | | SRC_Main_SE L (Byte 0, bit 2) | Config Mode |
|-----------------------|----------------------|----------------------------------------------------------|-------------------------------|-------------------------------------|-------------|
| | | PCI3_CFG1 (Byte 11, bit 7) | PCI3_CFG0 (Byte 11, bit 6) | | |
| Low | 0 or 1 | 0 | 0 | 0 | 0 = Default |
| Mid | 0 or 1 | 0 | 1 | 1 | 1 |
| High | TME=0 | 1 | 0 | 1 | 2 |
| High | TME=1 | 1 | 1 | 1 | 3 |

Table 7. PLL Modes for PCI3 Configurations

| Config Mode | PLL1 | | PLL2 | | PLL3 | | SRC1 | PLL Source |
|----------------|-----------------|--------|-----------|-----|---------|------|----------|------------------------------|
| | Outputs | SSC | Outputs | SSC | Outputs | SSC | | |
| 0 = Default | CPU/SRC/ PCI | Down | USB | NA | - | - | 100MHz | PLL1 (Table 2 applies) |
| 1 | CPU | Down | USB | NA | SRC/PCI | Down | 100MHz | PLL3 |
| 2 | CPU | Center | USB | NA | SRC/PCI | Down | 100MHz | PLL3 |
| 3 | CPU | Center | USB/LAN25 | NA | SRC/PCI | Down | 25MHz SE | PLL2* |

*Note: In Mode 3, Byte 8, bit (1:0) must be set to '1' to enable pin 17,18

Table 8. ME Clock Selection Table

| PCIF5/ ITP_EN | iAMT_EN | CPU2_AMT_EN | CPU1_AMT_EN | Description |
|------------------|---------|-------------|-------------|-------------------------------------|
| x | 1 | 0 | 0 | Reserved |
| x | 1 | 0 | 1 | Default, CPU1 = iAMT Clock |
| 1 | 1 | 1 | 0 | CPU2 = iAMT Clock |
| 1 | 1 | 1 | 1 | CPU1 and CPU2 both run in iAMT mode |

PCI_STOP# Power Management

| SMBus OE Bit | PCI_STOP# | Single-ended Clocks | | Differential Clocks (Except CPU) | |
|--------------|-----------|---------------------|--------------|-------------------------------------|--------------|
| | | Stoppable | Free running | Stoppable | Free running |
| Enable | 1 | Running | Running | Running | Running |
| | 0 | Low | Low | CK= High CK# = Low | Running |
| | | | | CK= Pull down CK# = Low | Running |
| Disable | X | Low | | CK= Pull down, CK# = Low | |

CPU_STOP# Power Management

| SMBus OE Bit | PCI_STOP# | Differential Clocks | |
|--------------|-----------|----------------------------|--------------|
| | | Stoppable | Free running |
| Enable | 1 | Running | Running |
| | 0 | CK= High CK# = Low | Running |
| | | CK= Pull down CK# = Low | Running |
| Disable | X | Low | |

CR# Power Management

| SMBus OE Bit | CR# | Differential Clocks | |
|--------------|-----|---------------------------|--------------|
| | | Stoppable | Free running |
| Enable | 1 | Running | Running |
| | 0 | CK= Pull down, CK# = Low | |
| Disable | X | CK = Pull down, CK# = Low | |

PD# Power Management

| Device State | Single-ended Clocks | | Differential Clocks (Except CPU1) | CPU1 |
|----------------------------------------|---------------------|-----------------|--------------------------------------|----------------------------|
| | w/o Latched input | w/Latched input | | |
| Latches Open | Low | Hi-Z | CK= Pull down, CK# = Low | CK= Pull down, CK# = Low |
| Power Down | | | CK= Pull down CK# = Low | CK= Pull down CK# = Low |
| M1 | | | CK= Pull down CK# = Low | Running |
| Virtual Power Cycle to Latches Open | | | CK= Pull down, CK# = Low | CK= Pull down, CK# = Low |

General SMBus serial interface information for the ICS9LPRS525

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|-----------------------------|-----------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address $D2_{(H)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | X Byte |
| ○ | | |
| ○ | | |
| ○ | | |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

| Index Block Read Operation | | |
|----------------------------|-----------------|----------------------|
| Controller (Host) | | ICS (Slave/Receiver) |
| T | starT bit | |
| Slave Address $D2_{(H)}$ | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address $D3_{(H)}$ | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count = X |
| ACK | | X Byte |
| ACK | | |
| ○ | | |
| ○ | | |
| ○ | | |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

Byte 0 FS Readback and PLL Selection Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------------------------------------------|---------------------|---------|
| 7 | - | FSLC | CPU Freq. Sel. Bit (Most Significant) | R | See Table 1 : CPU Frequency Select Table | | Latch |
| 6 | - | FSLB | CPU Freq. Sel. Bit | R | | | Latch |
| 5 | - | FSLA | CPU Freq. Sel. Bit (Least Significant) | R | | | Latch |
| 4 | - | iAMT_EN | Set via SMBus or dynamically by CK505 if detects dynamic M1 | RW | Legacy Mode | iAMT Enabled | 0 |
| 3 | | Reserved | Reserved | RW | | | 0 |
| 2 | - | SRC_Main_SEL | Select source for SRC Main | RW | SRC Main = PLL1 | SRC Main = PLL3 | Latch |
| 1 | - | SATA_SEL | Select source for SATA clock | RW | SATA = SRC_Main | SATA = PLL2 | 0 |
| 0 | - | PD_Restore | 1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at '1' if device is in iAMT mode. | RW | Configuration Not Saved | Configuration Saved | 1 |

Byte 1 DOT96 Select and PLL3 Quick Config Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-------|--------------|--------------------------------|------|------------------------------------------------------------------------------------|-------------------|---------|
| 7 | 13/14 | SRC0_SEL | Select SRC0 or DOT96 | RW | SRC0 | DOT96 | 0 |
| 6 | - | PLL1_SSC_SEL | Select 0.5% down or center SSC | RW | Down spread | Center spread | Latch |
| 5 | | PLL3_SSC_SEL | Select 0.5% down or center SSC | RW | Down spread | Center spread | 0 |
| 4 | | PLL3_CF3 | PLL3 Quick Config Bit 3 | RW | See Table 2: PLL3 Quick Configuration Only applies if Byte 0, bit 2 = 0. | | 0 |
| 3 | | PLL3_CF2 | PLL3 Quick Config Bit 2 | RW | | | 0 |
| 2 | | PLL3_CF1 | PLL3 Quick Config Bit 1 | RW | | | 0 |
| 1 | | PLL3_CF0 | PLL3 Quick Config Bit 0 | RW | | | 1 |
| 0 | | PCI_SEL | PCI_SEL | RW | PCI from PLL1 | PCI from SRC_MAIN | 1 |

Byte 2 Output Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|----------|---------------------------------------------------------|------|-----------------|----------------|---------|
| 7 | | REF_OE | Output enable for REF, if disabled output is tri-stated | RW | Output Disabled | Output Enabled | 1 |
| 6 | | USB_OE | Output enable for USB | RW | Output Disabled | Output Enabled | 1 |
| 5 | | PCIF5_OE | Output enable for PCI5 | RW | Output Disabled | Output Enabled | 1 |
| 4 | | PCI4_OE | Output enable for PCI4 | RW | Output Disabled | Output Enabled | 1 |
| 3 | | PCI3_OE | Output enable for PCI3 | RW | Output Disabled | Output Enabled | 1 |
| 2 | | PCI2_OE | Output enable for PCI2 | RW | Output Disabled | Output Enabled | 1 |
| 1 | | PCI1_OE | Output enable for PCI1 | RW | Output Disabled | Output Enabled | 1 |
| 0 | | PCIO_OE | Output enable for PCIO | RW | Output Disabled | Output Enabled | 1 |

Byte 3 Output Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-------------|-------------------------------|------|-----------------|----------------|---------|
| 7 | | Reserved | Reserved | RW | - | - | 1 |
| 6 | | Reserved | Reserved | RW | - | - | 1 |
| 5 | | Reserved | Reserved | RW | - | - | 1 |
| 4 | | SRC8/ITP_OE | Output enable for SRC8 or ITP | RW | Output Disabled | Output Enabled | 1 |
| 3 | | SRC7_OE | Output enable for SRC7 | RW | Output Disabled | Output Enabled | 1 |
| 2 | | SRC6_OE | Output enable for SRC6 | RW | Output Disabled | Output Enabled | 1 |
| 1 | | SRC5_OE | Output enable for SRC5 | RW | Output Disabled | Output Enabled | 1 |
| 0 | | SRC4_OE | Output enable for SRC4 | RW | Output Disabled | Output Enabled | 1 |

Byte 4 Output Enable and Spread Spectrum Disable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|---------------|---------------------------------|------|-----------------|----------------|---------|
| 7 | | SRC3_OE | Output enable for SRC3 | RW | Output Disabled | Output Enabled | 1 |
| 6 | | SATA/SRC2_OE | Output enable for SATA/SRC2 | RW | Output Disabled | Output Enabled | 1 |
| 5 | | SRC1_OE | Output enable for SRC1 | RW | Output Disabled | Output Enabled | 1 |
| 4 | | SRC0/DOT96_OE | Output enable for SRC0/DOT96 | RW | Output Disabled | Output Enabled | 1 |
| 3 | | CPU1_OE | Output enable for CPU1 | RW | Output Disabled | Output Enabled | 1 |
| 2 | | CPU0_OE | Output enable for CPU0 | RW | Output Disabled | Output Enabled | 1 |
| 1 | | PLL1_SSC_ON | Enable PLL1's spread modulation | RW | Spread Disabled | Spread Enabled | 1 |
| 0 | | PLL3_SSC_ON | Enable PLL3's spread modulation | RW | Spread Disabled | Spread Enabled | 1 |

Byte 5 Clock Request Enable/Configuration Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-----------|----------------------------------------------------------------------------|------|---------------|---------------|---------|
| 7 | | CR#_A_EN | Enable CR#_A (clk req), PCI0_OE must be = 1 for this bit to take effect | RW | Disable CR#_A | Enable CR#_A | 0 |
| 6 | | CR#_A_SEL | Sets CR#_A to control either SRC0 or SRC2 | RW | CR#_A -> SRC0 | CR#_A -> SRC2 | 0 |
| 5 | | CR#_B_EN | Enable CR#_B (clk req) | RW | Disable CR#_B | Enable CR#_B | 0 |
| 4 | | CR#_B_SEL | Sets CR#_B -> SRC1 or SRC4 | RW | CR#_B -> SRC1 | CR#_B -> SRC4 | 0 |
| 3 | | CR#_C_EN | Enable CR#_C (clk req) | RW | Disable CR#_C | Enable CR#_C | 0 |
| 2 | | CR#_C_SEL | Sets CR#_C -> SRC0 or SRC2 | RW | CR#_C -> SRC0 | CR#_C -> SRC2 | 0 |
| 1 | | CR#_D_EN | Enable CR#_D (clk req) | RW | Disable CR#_D | Enable CR#_D | 0 |
| 0 | | CR#_D_SEL | Sets CR#_D -> SRC1 or SRC4 | RW | CR#_D -> SRC1 | CR#_D -> SRC4 | 0 |

Byte 6 Clock Request Enable/Configuration and Stop Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-------------------------|------------------------------------------------|------|---------------|--------------------------------------|---------|
| 7 | | CR#_E_EN | Enable CR#_E (clk req) -> SRC6 | RW | Disable CR#_E | Enable CR#_E | 0 |
| 6 | | CR#_F_EN | Enable CR#_F (clk req) -> SRC8 | RW | Disable CR#_F | Enable CR#_F | 0 |
| 5 | | Reserved | Reserved | RW | - | - | 0 |
| 4 | | Reserved | Reserved | RW | - | - | 0 |
| 3 | | Reserved | Reserved | RW | - | - | 0 |
| 2 | | Reserved | Reserved | RW | - | - | 0 |
| 1 | | SSCD_STP_CRTL (SRC1) | If set, SSCD (SRC1) stops with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |
| 0 | | SRC_STP_CRTL | If set, SRCs (except SRC1) stop with PCI_STOP# | RW | Free Running | Stops with PCI_STOP# assertion | 0 |

Byte 7 Vendor ID/ Revision ID

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-----------------|----------------------------------|------|-----------------|---|---------|
| 7 | | Rev Code Bit 3 | Revision ID | R | Vendor specific | | X |
| 6 | | Rev Code Bit 2 | | R | | | X |
| 5 | | Rev Code Bit 1 | | R | | | X |
| 4 | | Rev Code Bit 0 | | R | | | X |
| 3 | | Vendor ID bit 3 | Vendor ID ICS is 0001, binary | R | | | 0 |
| 2 | | Vendor ID bit 2 | | R | | | 0 |
| 1 | | Vendor ID bit 1 | | R | | | 0 |
| 0 | | Vendor ID bit 0 | | R | | | 1 |

Byte 8 Device ID and Output Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------------|------------------------------------------------------------------------------------------------|------|---------------|---------|---------|
| 7 | | Device_ID3 | Table of Device identifier codes, used for differentiating between CK505 package options, etc. | R | 56-pin device | | 0 |
| 6 | | Device_ID2 | | R | | | 0 |
| 5 | | Device_ID1 | | R | | | 0 |
| 4 | | Device_ID0 | | R | | | 0 |
| 3 | | Reserved | Reserved | RW | - | - | 0 |
| 2 | | Reserved | Reserved | RW | - | - | 0 |
| 1 | | SE1_OE | Output enable for SE1 | RW | Disabled | Enabled | 0 |
| 0 | | SE2_OE | Output enable for SE2 | RW | Disabled | Enabled | 0 |

Byte 9 Output Control Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|------------------|-----------------------------------------------------|------|-----------------------------------------------|--------------------------------|---------|
| 7 | | PCIF5_STOP_EN | Allows control of PCIF5 with assertion of PCI_STOP# | RW | Free running | Stops with PCI_STOP# assertion | 0 |
| 6 | | TME_Readback | Trusted Mode Enable (TME) strap status | R | normal operation | no overclocking | Latch |
| 5 | | REF Strength | Sets the REF output drive strength | RW | 1X (2Loads) | 2X (3 Loads) | 1 |
| 4 | | Test Mode Select | Allows test select, ignores REF/FSC/TestSel | RW | Outputs HI-Z | Outputs = REF/N | 0 |
| 3 | | Test Mode Entry | Allows entry into test mode, ignores FSB/TestMode | RW | Normal operation | Test mode | 0 |
| 2 | | IO_VOUT2 | IO Output Voltage Select (Most Significant Bit) | RW | See Table 3: V_IO Selection (Default is 0.8V) | | 1 |
| 1 | | IO_VOUT1 | IO Output Voltage Select | RW | | | 0 |
| 0 | | IO_VOUT0 | IO Output Voltage Select (Least Significant Bit) | RW | | | 1 |

Byte 10 Stop Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-------------------|-----------------------------------------|----------------------------------------|----------------------|--------------|-----------|
| 7 | | SRC5_EN Readback | Readback of SRC5 enable latch | R | CPU/PCI Stop Enabled | SRC5 Enabled | Latch |
| 6 | | Reserved | Reserved | RW | - | - | 0 |
| 5 | | Reserved | | RW | - | - | 0 |
| 4 | | Reserved | | RW | - | - | 0 |
| 3 | | Reserved | | RW | - | - | 0 |
| 2 | | Reserved | | RW | - | - | 0 |
| 1 | | CPU 1 Stop Enable | | Enables control of CPU1 with CPU_STOP# | RW | Free Running | Stoppable |
| 0 | | CPU 0 Stop Enable | Enables control of CPU 0 with CPU_STOP# | RW | Free Running | Stoppable | 1 |

Byte 11 iAMT Enable Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|-------------------|-----------------------------------------------------------------------|------|------------------------------|----------------------|---------|
| 7 | | PCI3_CFG1 | See PCI3 Configuration Table 28 | R | See PCI3 Configuration Table | | Latch |
| 6 | | PCI3_CFG0 | | R | | | Latch |
| 5 | | Reserved | Reserved | RW | - | - | 0 |
| 4 | | Reserved | Reserved | RW | - | - | 1 |
| 3 | | CPU2_AMT_EN | Determines if CPU2 runs in M1 mode. Only valid if ITP_EN=1. See Note. | RW | Does not Run | Runs | 0 |
| 2 | | CPU1_AMT_EN | Determines if CPU1 runs in M1 mode. See Note. | RW | Does not Run | Runs | 1 |
| 1 | | PCI-E_GEN2 | Determines if PCI-E Gen2 compliant | R | non-Gen2 | PCI-E Gen2 Compliant | 1 |
| 0 | | CPU 2 Stop Enable | Enables control of CPU 0 with CPU_STOP# | RW | Free Running | Stoppable | 1 |

NOTE: A value of '00' for Bit(3:2) in Byte 11 is reserved and not a valid configuration.

Byte 12 Byte Count Register

| Bit | Pin | Name | Description | Type | 0 | 1 | Default |
|-----|-----|----------|--------------------------------------------------|------|---|---|---------|
| 7 | | Reserved | | RW | | | 0 |
| 6 | | Reserved | | RW | | | 0 |
| 5 | | BC5 | Read Back byte count register, max bytes = 32 | RW | | | 0 |
| 4 | | BC4 | | RW | | | 0 |
| 3 | | BC3 | | RW | | | 1 |
| 2 | | BC2 | | RW | | | 1 |
| 1 | | BC1 | | RW | | | 0 |
| 0 | | BC0 | | RW | | | 1 |

Byte 13 to 28 Reserved

Byte 29 Slew Rate Control

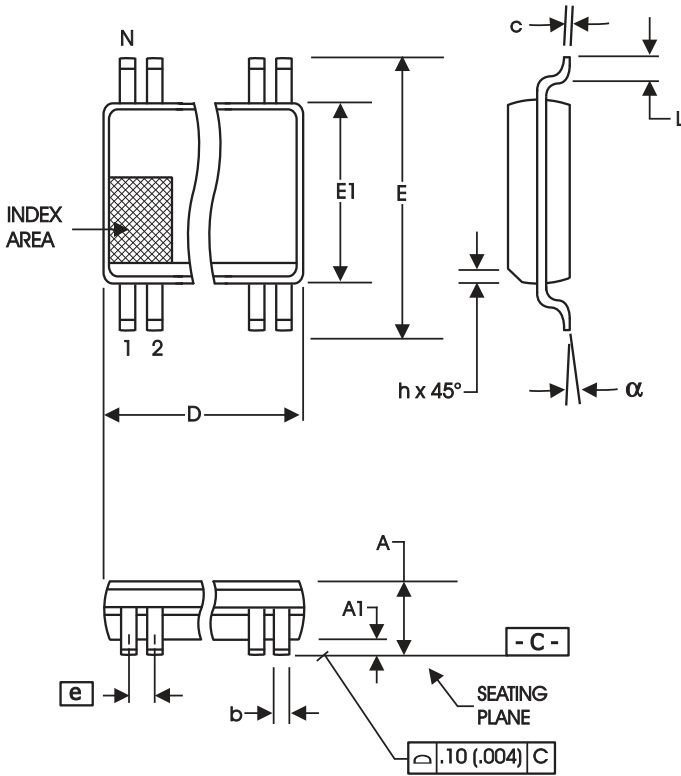
| Bit | Pin | Name | Description | RW | 0 | 1 | Default |
|-----|-----|---------------|-----------------------------|----|-------------------------------|---------|---------|
| 7 | | USB_Slew1 | USB Slew Rate Control (MSB) | RW | See Slew Rate Selection Table | | 1 |
| 6 | | USB_Slew0 | USB Slew Rate Control (LSB) | RW | | | 0 |
| 5 | | PCI_Slew1 | PCI Slew Rate Control (MSB) | RW | See Slew Rate Selection Table | | 1 |
| 4 | | PCI_Slew0 | PCI Slew Rate Control (LSB) | RW | | | 1 |
| 3 | | Reserved | | RW | | | 1 |
| 2 | | REF Slew Rate | Changes Ref Slew Rate | RW | 1.2V/ns | 2.2V/ns | 1 |
| 1 | | Reserved | | RW | | | 0 |
| 0 | | Reserved | | RW | | | 0 |

Test Clarification Table

| Comments | HW | | SW | | OUTPUT |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|------------------------------|---------------------------|--------------------------|--------|
| | FSLC/ TEST_SEL HW PIN | FSLB/ TEST_MODE HW PIN | TEST ENTRY BIT B9b3 | REF/N or HI-Z B9b4 | |
| | <2.0V | X | 0 | 0 | NORMAL |
| Power-up w/ TEST_SEL = 1 to enter test mode | >2.0V | 0 | X | 0 | HI-Z |
| Cycle power to disable test mode | >2.0V | 0 | X | 1 | REF/N |
| FSLC./TEST_SEL -->3-level latched input | >2.0V | 1 | X | 0 | REF/N |
| If power-up w/ V>2.0V then use TEST_SEL | | | | | |
| If power-up w/ V<2.0V then use FSLC | | | | | |
| FSLB/TEST_MODE -->low Vth input | >2.0V | 1 | X | 1 | REF/N |
| TEST_MODE is a real time input | | | | | |
| If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through B9b3. If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N FSLB/TEST_Mode pin is not used. Cycle power to disable test mode, one shot control | <2.0V | X | 1 | 0 | HI-Z |
| | <2.0V | X | 1 | 1 | REF/N |

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B9b4: 1= REF/N, Default = 0 (HI-Z)



56-Lead, 300 mil Body, 25 mil, SSOP

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|-------|--------------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| alpha | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 56 | 18.31 | 18.55 | .720 | .730 |

Reference Doc.: JEDEC Publication 95, MO-118

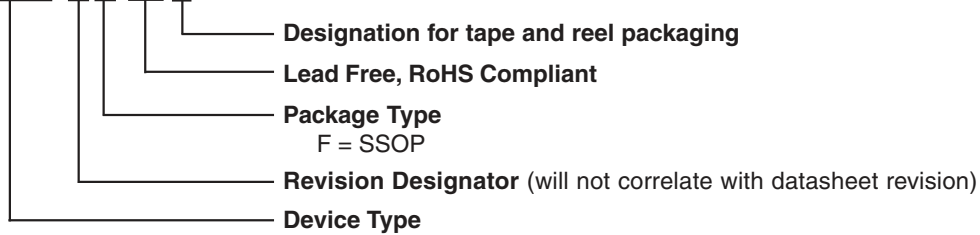
10-0034

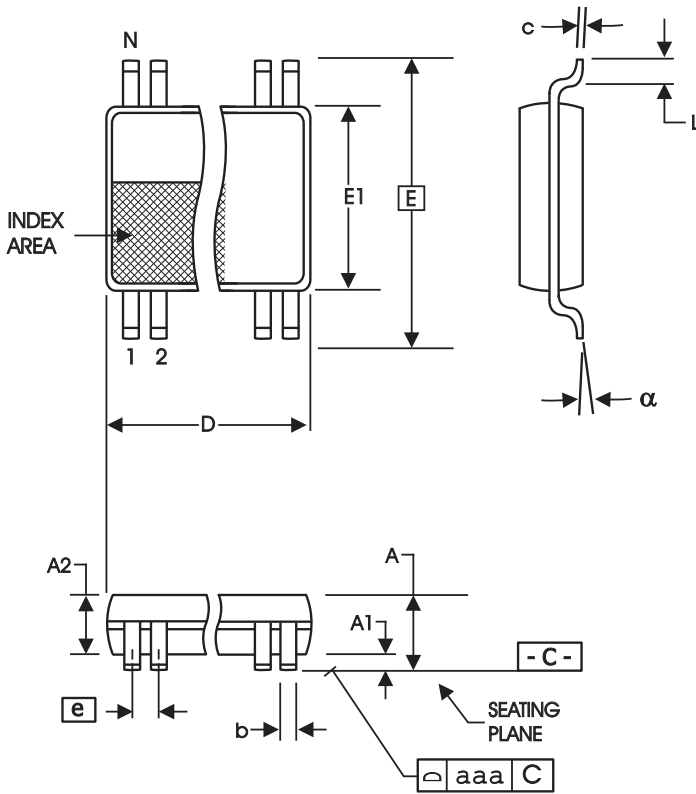
Ordering Information

9LPRS525AFLFT

Example:

XXXX A F LFT





56-Lead 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.17 | 0.27 | .007 | .011 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | .236 | .244 |
| e | 0.50 BASIC | | 0.020 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| alpha | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|-------|----------|------|
| | MIN | MAX | MIN | MAX |
| 56 | 13.90 | 14.10 | .547 | .555 |

Reference Doc.: JEDEC Publication 95, M O-153

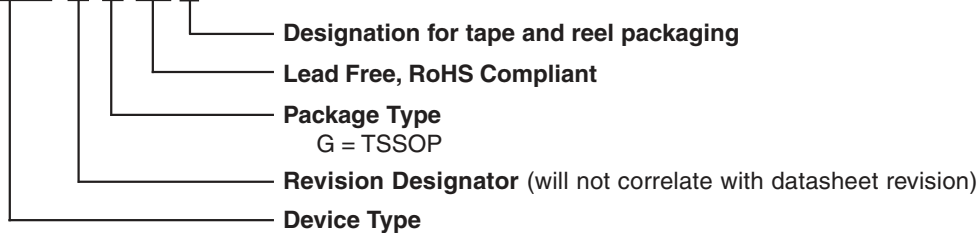
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Ordering Information

9LPRS525AGLFT

Example:

XXXX A G L F T



Revision History

| Rev. | Issue Date | Description | Page # |
|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| 0.1 | 7/21/2008 | Initial Release | - |
| 0.2 | 08/06/08 | 1. Updated pinout to remove Vout reference on pin 40 2. Updated VDD_IO pin descriptions to show 1.05V to 3.3V operation | 1, 3 |
| 0.3 | 8/8/2008 | 1. Fixed Pagination of Pin Descriptions 2. Changed reference to PCI3 Config Table in Pindes to match table name 3. Added Byte 29 for Slew Rate control | 2,3,17 |
| 0.4 | 10/10/2008 | 1) Byte 11, bit 5 is now reserved. 2) Byte 29, bits 7:6 default to 0.8X slew rate ('10') 3) Removed reference to STOP drive mode in Power management table. 4) Corrected REF slew rate control from Byte 29b3 to Byte 29b2. 5) Clarified description of Byte 11, bits 2 and 3 to reflect CK505 ME clock selection table. 6) Marked as Reserved all bits that are not in the 56-pin version of the device | Various |
| 0.5 | 4/28/2009 | 1) updated tables 2, 6 and 7 to clarify interaction of Config Modes with SRC1 2) Updated ordering revision to A | 10, 11, 19, 20 |
| A | 4/28/2009 | Released to final | |
| B | 1/21/2010 | Updated Power Groups table | 4 |
| C | 4/20/2010 | Updated Abs Max table with Case Temp. parameter | 5 |

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