

# BTS41k0S-ME-N

Smart High-Side NMOS-Power Switch

## Datasheet

Rev 1.1, 2012-05-08

## Table of Contents

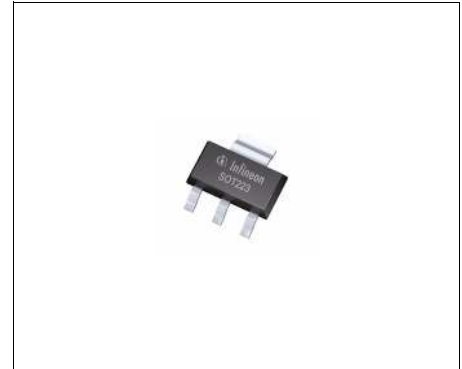
<b>1</b>	<b>Overview</b> .....	<b>3</b>
<b>2</b>	<b>Block Diagram and Terms</b> .....	<b>4</b>
<b>3</b>	<b>Pin Configuration</b> .....	<b>5</b>
3.1	Pin Assignment .....	5
3.2	Pin Definitions and Functions .....	5
<b>4</b>	<b>General Product Characteristics</b> .....	<b>6</b>
4.1	Absolute Maximum Ratings .....	6
4.2	Functional Range .....	7
4.3	Thermal Resistance .....	7
<b>5</b>	<b>Electrical Characteristics</b> .....	<b>8</b>
<b>6</b>	<b>Typical Performance Graphs</b> .....	<b>10</b>
<b>7</b>	<b>Application Information</b> .....	<b>14</b>
7.1	Application Diagram .....	14
7.2	Special features .....	15
7.3	Typical Application Waveforms .....	16
7.4	Protection behavior .....	17
<b>8</b>	<b>Package outlines and footprint</b> .....	<b>18</b>
<b>9</b>	<b>Revision History</b> .....	<b>19</b>



## 1 Overview

### Features

- Current controlled input
- Capable of driving all kind of loads (inductive, capacitive and resistive)
- Negative voltage clamped at output with inductive loads
- Current limitation
- Very low standby current
- Thermal shutdown with restart
- Overload protection
- Short circuit protection
- Overvoltage protection (including load dump)
- Reverse battery protection
- Loss of GND and loss of V<sub>bb</sub> protection
- ESD-Protection
- Improved electromagnetic compatibility (EMC)
- Green Product (RoHS compliant)
- AEC Qualified



PG-SOT223-4

### Description

The **BTS41k0S-ME-N** is a protected 1 Ω single channel Smart High-Side NMOS-Power Switch in a **PG-SOT223-4** package with charge pump and current controlled input, monolithically integrated in a smart power technology.

### Product Summary

Overvoltage protection  $V_{S(AZ)} = \text{min.}62\text{V}$   
 Operating voltage range  $4,9\text{V} < V_S < 45\text{V}$   
 On-state resistance  $R_{ON} \text{ typ } 1\Omega$   
 Operating Temperature range  $T_j = -40^\circ\text{C to } 150^\circ\text{C}$

### Application

- All types of resistive, inductive and capacitive loads in automotive applications
- Current controlled power switch for 12V, 24V and 45V DC automotive and industrial applications
- Driver for electromagnetic relays
- Signal amplifier

Type	Package	Marking
BTS41k0S-ME-N	PG-SOT223-4	41k0SN

## 2 Block Diagram and Terms

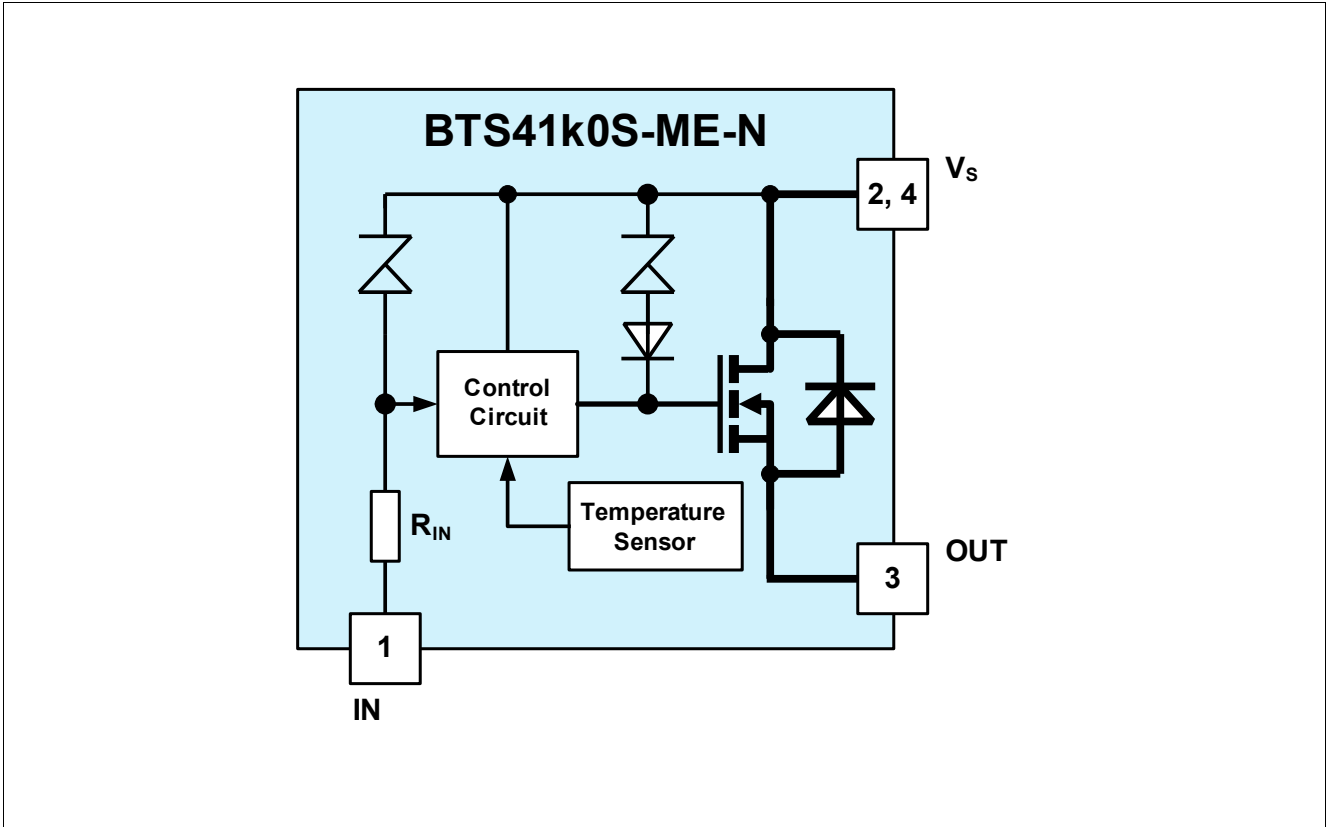


Figure 1 Block diagram

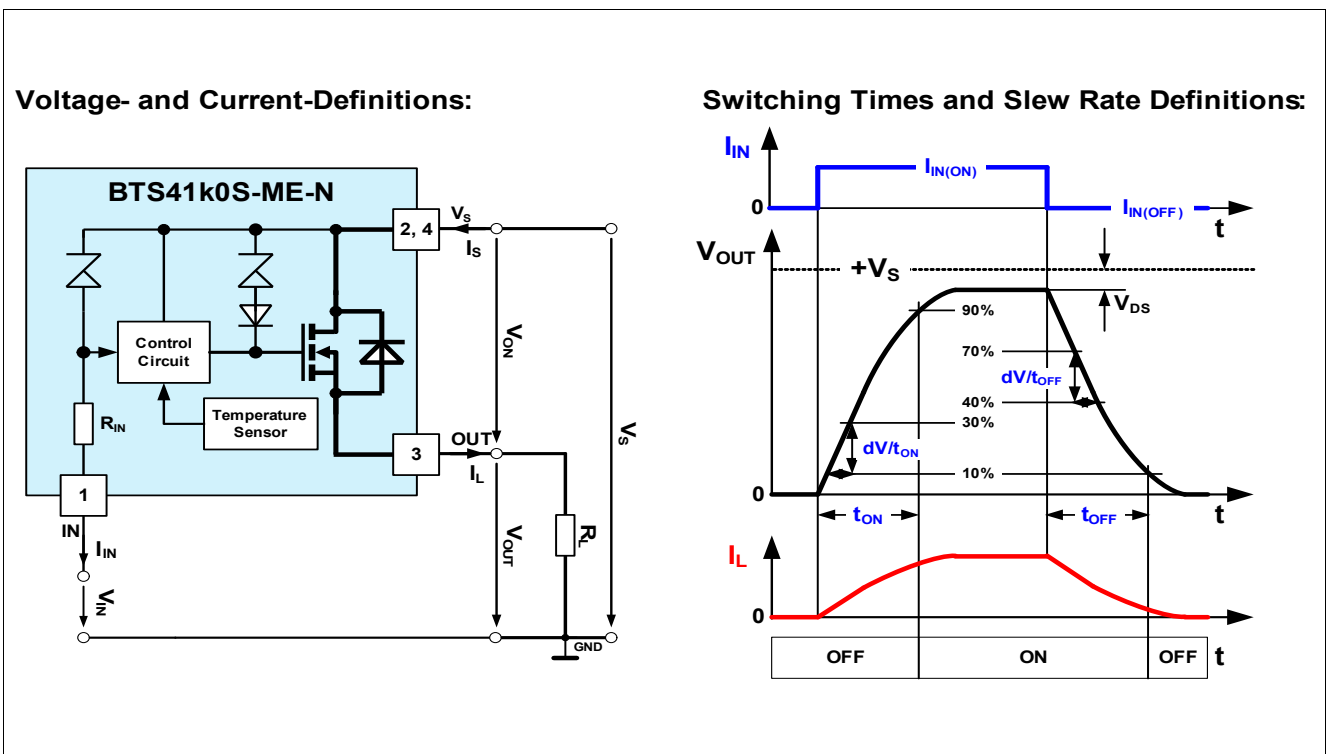


Figure 2 Terms - parameter definition

### 3 Pin Configuration

#### 3.1 Pin Assignment

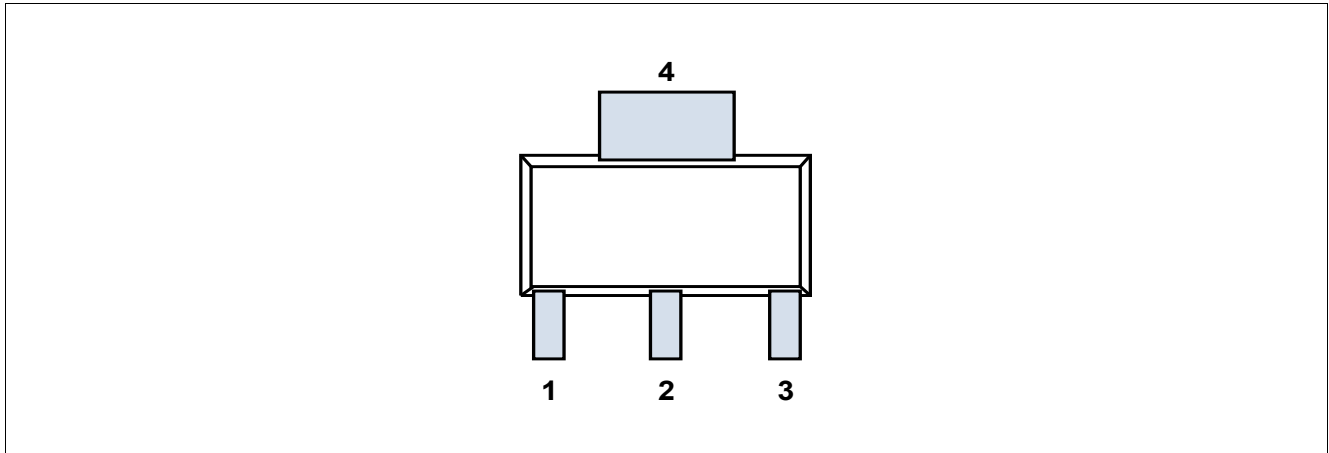


Figure 3 Pin configuration top view, PG-SOT223-4

#### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	<b>IN</b>	Input, activates the power switch in case of connection to GND
2	<b>VS</b>	Supply voltage
3	<b>OUT</b>	Output to the load
4	<b>VS</b>	Supply voltage

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Absolute maximum ratings** <sup>1)</sup> $T_j = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  all voltages with respect to ground, currents flowing into the device unless otherwise specified in "Terms"

Pos.	Parameter	Symbol	Limit values		Unit	Conditions
			Min.	Max.		
<b>Supply voltage <math>V_S</math></b>						
4.1.1	Voltage	$V_S$		60	V	
<b>Output stage OUT</b>						
4.1.2	Output Current; (Short circuit current see electrical characteristics)	$I_{OUT}$			A	self limited
<b>Input IN</b>						
4.1.3	Input Current	$I_{IN}$	-15	15	mA	
<b>Temperatures</b>						
4.1.4	Junction Temperature	$T_j$	-40	150	$^{\circ}\text{C}$	
4.1.5	Storage Temperature	$T_{stg}$	-55	150	$^{\circ}\text{C}$	
<b>Power dissipation</b>						
4.1.6	$T_a = 25^{\circ}\text{C}$ Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm <sup>2</sup> (one layer, 70mm thick) copper area for Vbb connection. PCB is vertical without blown air	$P_{tot}$		1.7	W	
<b>Inductive load switch-off energy dissipation</b>						
4.1.7	$T_j = 150^{\circ}\text{C}$ ; $I_L = 0.15\text{A}$ ; single pulse <sup>1)</sup>	$E_{AS}$		1000	mJ	
<b>Load dump protection</b>						
4.1.8	$V_{LoadDump} = V_A + V_S$ $R_L = 2\Omega$ ; $t_d = 400\text{ms}$ ; $V_{IN} = \text{H or L}$ $I_L = 0.15\text{A}$ ; $V_S = 13.5\text{V}$ $V_S = 27\text{V}$ $V_{LoadDump}$ is set up without the device under test connected to the generator per ISO 7637-1 and DIN 40839	$V_{LoadDump}$ $V_{LoadDump}$		93.5 127	V V	
<b>ESD Susceptibility</b>						
4.1.9	ESD susceptibility (input pin)	$V_{ESD}$	-1	1	kV	HBM <sup>2)</sup>
4.1.10	ESD susceptibility (all other pins)	$V_{ESD}$	-5	5	kV	HBM <sup>2)</sup>

1) Not subject to production test, specified by design

2) ESD susceptibility HBM according to EIA/JESD 22-A 114.

*Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are not designed for continuous or repetitive operation.*

## 4.2 Functional Range

Pos.	Parameter	Symbol	Limit values		Unit	Conditions
			Min.	Max.		
4.2.1	Nominal Operating Voltage	$V_S$	4.9	45	V	$V_S$ increasing
4.2.2	Standby Current	$I_{S(off)}$	2	10	uA	IN open

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 4.3 Thermal Resistance

This thermal data was generated in accordance to JEDEC JESD51 standards.

More information on [www.jedec.org](http://www.jedec.org).

**Table 1 Thermal Resistance<sup>1)</sup>**

Pos.	Parameter	Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
4.3.1	Thermal Resistance - Junction to soldering point, pin4	$R_{thj-pin4}$		15		K/W	
4.3.2	Thermal Resistance - Junction to Ambient - 1s0p, minimal footprint	$R_{thJA\_1s0p}$		86		K/W	<sup>2)</sup>
4.3.3	Thermal Resistance - Junction to Ambient - 1s0p, 600mm <sup>2</sup>	$R_{thJA\_1s0p\_600mm^2}$		60		K/W	<sup>3)</sup>

1) Not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

3) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm<sup>2</sup>; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70µm Cu.

## 5 Electrical Characteristics

$V_S = 9V$  to  $45V$ ;  $T_j = -40^\circ C$  to  $150^\circ C$ ; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms"); typical values at  $V_S = 13.5V$ ,  $T_j = 25^\circ C$

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Powerstage (PMOS and Diode to GND)</b>							
5.0.1	NMOS ON Resistance	$R_{DSON}$		0.8	1.5	$\Omega$	$I_{OUT} = 150mA$ ; $T_j = 25^\circ C$ ; IN connected to GND
5.0.2	NMOS ON Resistance	$R_{DSON}$		1.5	3.0	$\Omega$	$I_{OUT} = 150mA$ ; $T_j = 150^\circ C$ ; IN connected to GND
5.0.3	NMOS ON Resistance	$R_{DSON}$		2	5	$\Omega$	$I_{OUT} = 50mA$ ; $T_j = 25^\circ C$ ; $V_S = 6V$ ; IN connected to GND
5.0.4	Nominal Load Current <sup>1)</sup> ; device on PCB <sup>2)</sup>	$I_{L(nom)}$	0.2			A	$T_a = 85^\circ C$ ; $T_j = 150^\circ C$ ;
<b>Timings of Power Stages</b>							
5.0.5	Turn ON Time <sup>3)</sup> (to 90% of $V_{out}$ ); $V_S$ to GND transition of $V_{IN}$	$t_{ON}$			125 <sup>4)</sup>	$\mu s$	$V_S = 13.5V$ ; $R_L = 270\Omega$
5.0.6	Turn ON Time <sup>3)</sup> (to 90% of $V_{out}$ ); $V_S$ to GND transition of $V_{IN}$	$t_{ON}$		45	100	$\mu s$	$V_S = 13.5V$ ; $R_L = 270\Omega$ ; $T_j = 25^\circ C$
5.0.7	Turn OFF Time <sup>3)</sup> (to 10% of $V_{out}$ ); GND to $V_S$ transition of $V_{IN}$	$t_{OFF}$			175 <sup>4)</sup>	$\mu s$	$V_S = 13.5V$ ; $R_L = 270\Omega$
5.0.8	Turn OFF Time <sup>3)</sup> (to 10% of $V_{out}$ ); GND to $V_S$ transition of $V_{IN}$	$t_{OFF}$		40	140	$\mu s$	$V_S = 13.5V$ ; $R_L = 270\Omega$ ; $T_j = 25^\circ C$
5.0.9	ON-Slew Rate <sup>3)</sup> (10 to 30% of $V_{out}$ ); $V_S$ to GND transition of $V_{IN}$	$dV_{OUT}/dt_{ON}$			6 <sup>4)</sup>	V / $\mu s$	$V_S = 13.5V$ ; $R_L = 270\Omega$
5.0.10	ON-Slew Rate <sup>3)</sup> (10 to 30% of $V_{out}$ ); $V_S$ to GND transition of $V_{IN}$	$dV_{OUT}/dt_{ON}$		1.3	4.0	V / $\mu s$	$V_S = 13.5V$ ; $R_L = 270\Omega$ ; $T_j = 25^\circ C$
5.0.11	OFF-Slew Rate <sup>3)</sup> ; (70 to 40% of $V_{out}$ ); GND to $V_S$ transition of $V_{IN}$	$dV_{OUT}/dt_{OFF}$			8 <sup>4)</sup>	V / $\mu s$	$V_S = 13.5V$ ; $R_L = 270\Omega$
5.0.12	OFF-Slew Rate <sup>3)</sup> ; (70 to 40% of $V_{out}$ ); GND to $V_S$ transition of $V_{IN}$	$dV_{OUT}/dt_{OFF}$		1.7	4.0	V / $\mu s$	$V_S = 13.5V$ ; $R_L = 270\Omega$ ; $T_j = 25^\circ C$
<b>Standby current consumption</b>							
5.0.13	Standby current	$I_{S(off)}$		2	10	$\mu A$	IN open



**Electrical Characteristics**

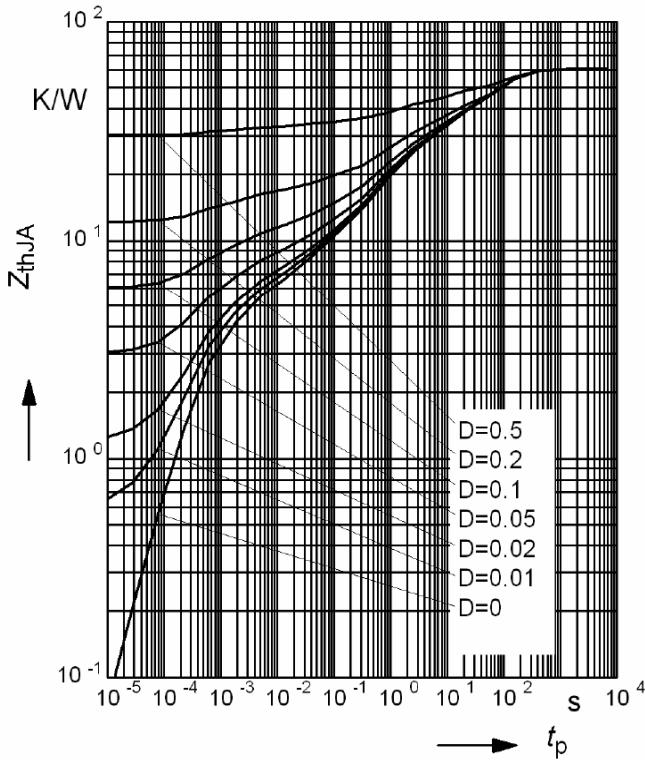
$V_S = 9V$  to  $45V$ ;  $T_j = -40^\circ C$  to  $150^\circ C$ ; all voltages with respect to ground, currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms"); typical values at  $V_S = 13.5V$ ,  $T_j = 25^\circ C$

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Protection functions <sup>5)</sup></b>							
5.0.14	Initial peak short circuit current limit IN conected to GND	$I_{L(SCp)}$			1.2	A	$T_j = -40^\circ C$ ; $V_S = 13.5V$ $t_m = 100\mu s$
5.0.15	Initial peak short circuit current limit IN conected to GND	$I_{L(SCp)}$		0.9		A	$T_j = 25^\circ C$ ; $V_S = 13.5V$ $t_m = 100\mu s$
5.0.16	Initial peak short circuit current limit IN conected to GND	$I_{L(SCp)}$	0.2			A	$T_j = 150^\circ C$ ; $V_S = 13.5V$ $t_m = 100\mu s$
5.0.17	Repetitive short circuit current limit IN conected to GND	$I_{L(SCr)}$		0.7		A	
5.0.18	Output clamp at $V_{OUT} = V_S - V_{ON(CL)}$ (inductive load switch off)	$V_{ON(CL)}$	60			V	$I_S = 4mA$
5.0.19	Overvoltage protection $V_{OUT} = V_S - V_{ON(CL)}$	$V_{S(AZ)}$	62	68		V	$I_S = 1mA$
5.0.20	Thermal overload trip temperature <sup>4)</sup>	$T_{jTrip}$	150			$^\circ C$	
5.0.21	Thermal hysteresis <sup>4)</sup>	$T_{HYS}$		10		$^\circ C$	
<b>Input interface</b>							
5.0.22	Off state input current	$I_{IN(off)}$			0.05	mA	$T_j = -25^\circ C$ ; $R_L = 270\Omega$ $V_{OUT} \leq 0.1V$
5.0.23	Off state input current	$I_{IN(off)}$			0.04	mA	$T_j = 150^\circ C$ ; $R_L = 270\Omega$ $V_{OUT} \leq 0.1V$
5.0.24	On state input current; IN connected to GND <sup>6)</sup>	$I_{IN(on)}$		0.3	1.0	mA	
5.0.25	Input resistance	$R_{IN}$	0.5	1.0	2.5	k $\Omega$	
<b>Reverse Battery</b>							
5.0.26	Continuous reverse drain current	$I_{DRev}$			0.2	A	
5.0.27	Forward voltage of the drain-source reverse diode	$V_{FDS}$		770		mV	$I_{FDS} = 200mA$ $I_{IN} \leq 0.05mA$

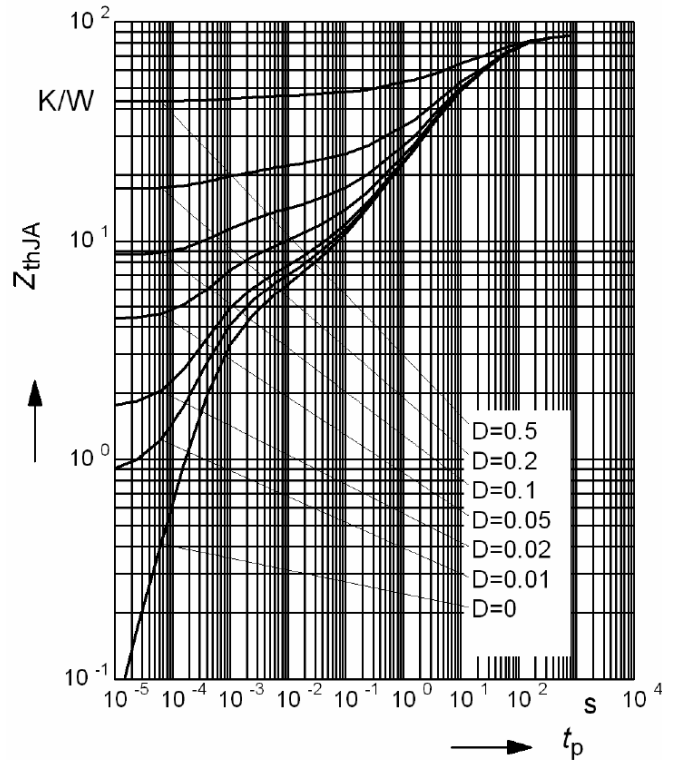
- 1) Nominal Load Current is limited by the current limitation; see protection function data
- 2) Device on 50mm x 50mm x 1,5mm epoxy FR4 PCB with 6cm<sup>2</sup> (one layer copper 70um thick) copper area for supply voltage connection. PCB in vertical position with blown air
- 3) Timing values only with high input slewrates ( $t_{rIN} = t_{fIN} \leq 50ns$ ); otherwise slower
- 4) Not tested in production
- 5) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.
- 6) Driver circuit must be able to sink currents > 1mA

## 6 Typical Performance Graphs

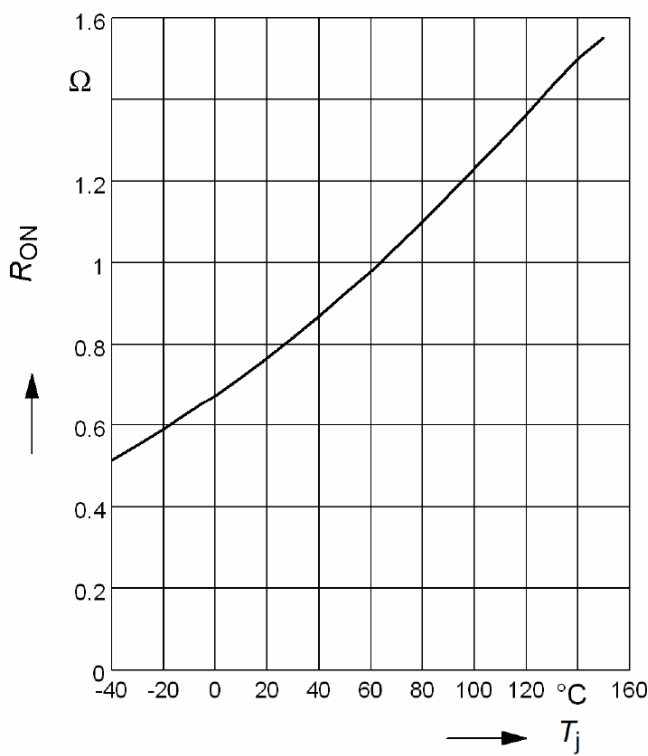
Transient Thermal Impedance  $Z_{thJA}$  versus Pulse Time  $t_p$  @ 6cm<sup>2</sup> heatsink area ( $D = t_p/T$ )



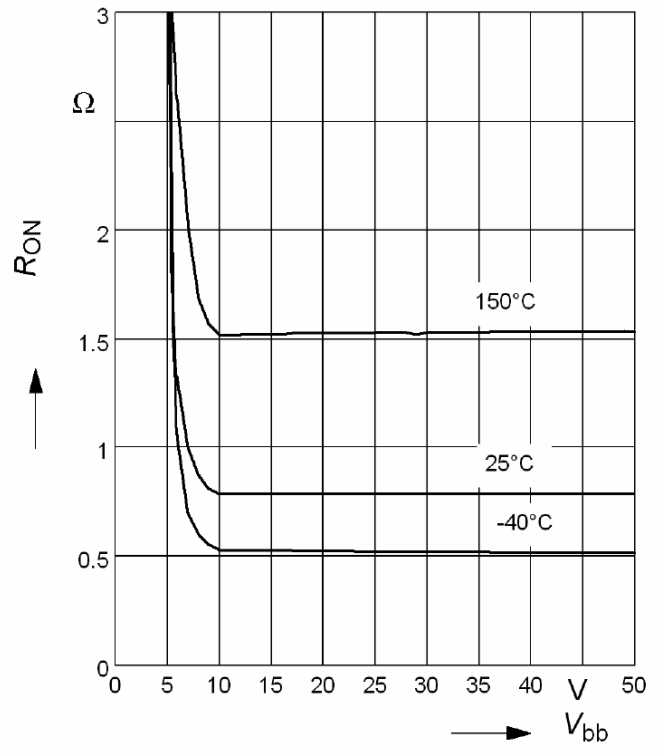
Transient Thermal Impedance  $Z_{thJA}$  versus Pulse Time  $t_p$  @ min footprint ( $D = t_p/T$ )



On-Resistance  $R_{DSON}$  versus Junction Temperature  $T_j$  @  $V_s = 9V$ ;  $I_L = 150mA$

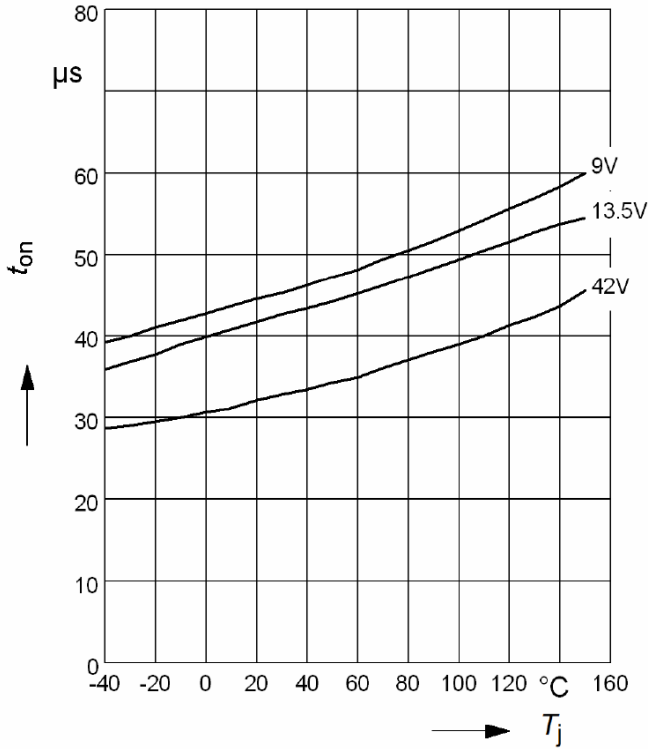


On-Resistance  $R_{DSON}$  versus Supply Voltage  $V_s = V_{bb}$  @  $I_L = 150mA$ ;  $T_j = \text{par.}$

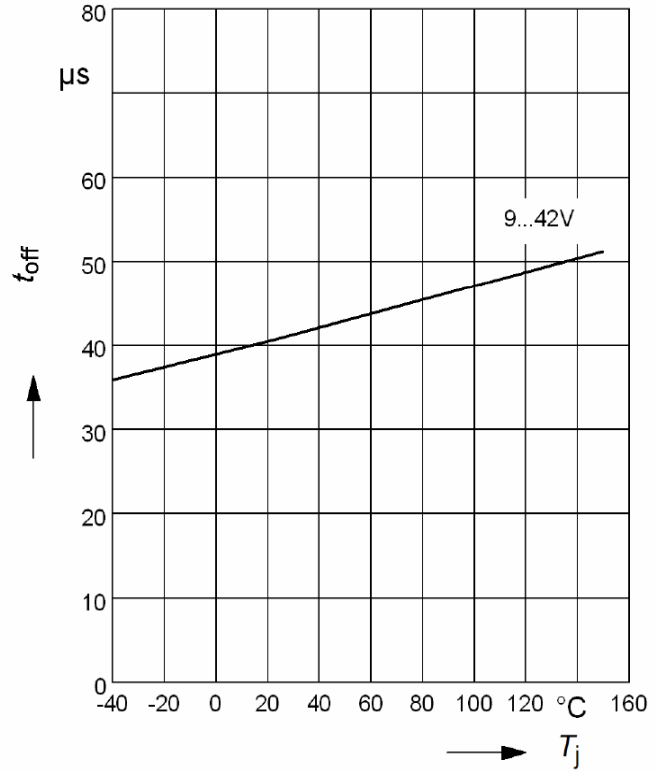


Typical Performance Graphs

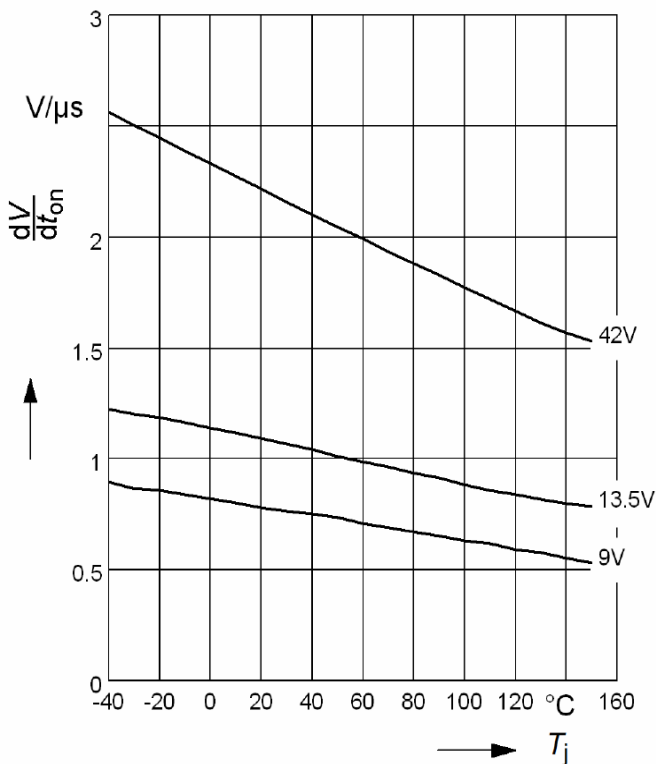
Switch ON Time  $t_{ON}$  versus Junction Temperature  $T_j$  @  $R_L = 270\Omega$ ;  $V_S = \text{par.}$



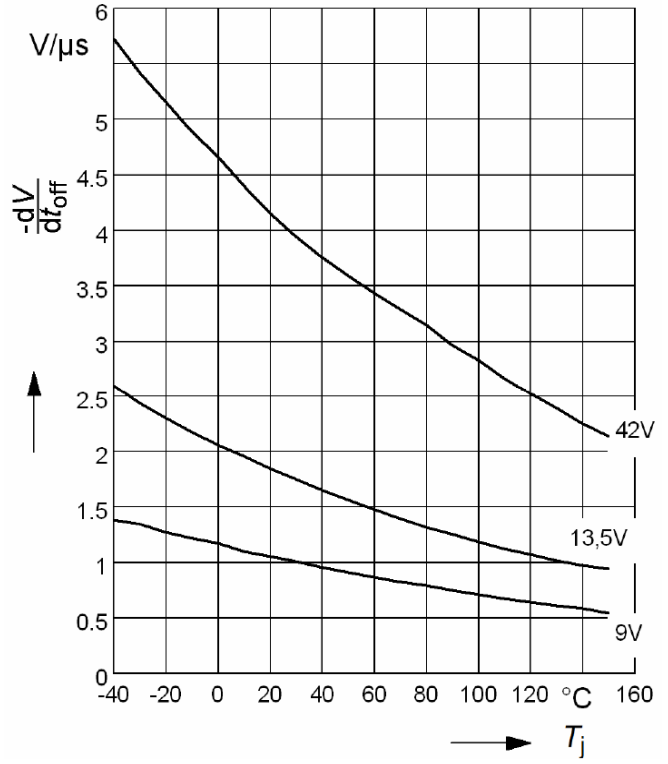
Switch OFF Time  $t_{OFF}$  versus Junction Temperature  $T_j$  @  $R_L = 270\Omega$ ;  $V_S = \text{par.}$



ON Slewrate  $SR_{ON}$  versus Junction Temperature  $T_j$  @  $R_L = 270\Omega$ ;  $V_S = \text{par.}$

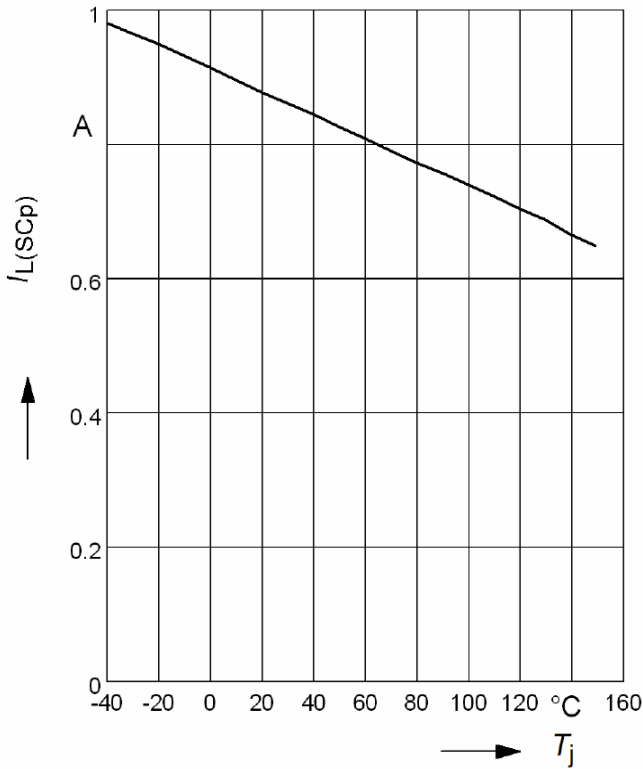


OFF Slewrate  $SR_{OFF}$  versus Junction Temperature  $T_j$  @  $R_L = 270\Omega$ ;  $V_S = \text{par.}$

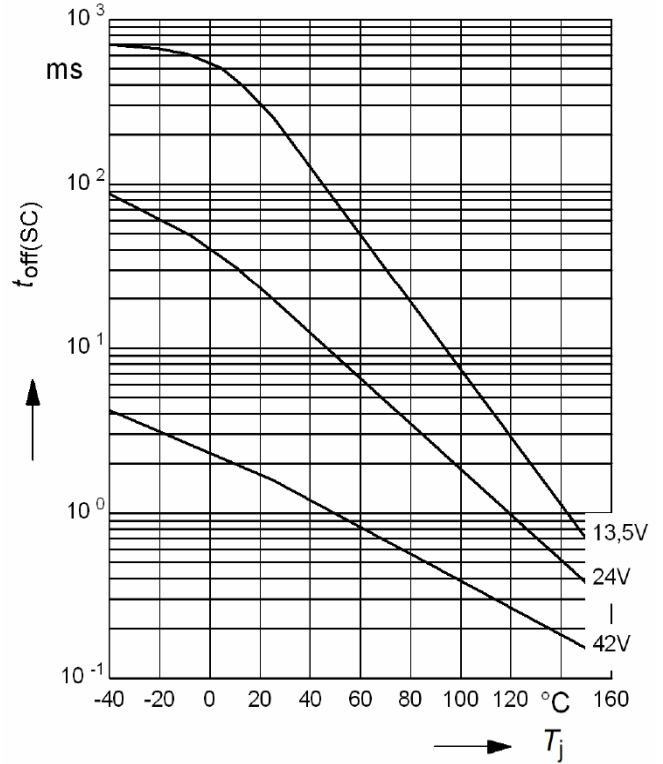


Typical Performance Graphs

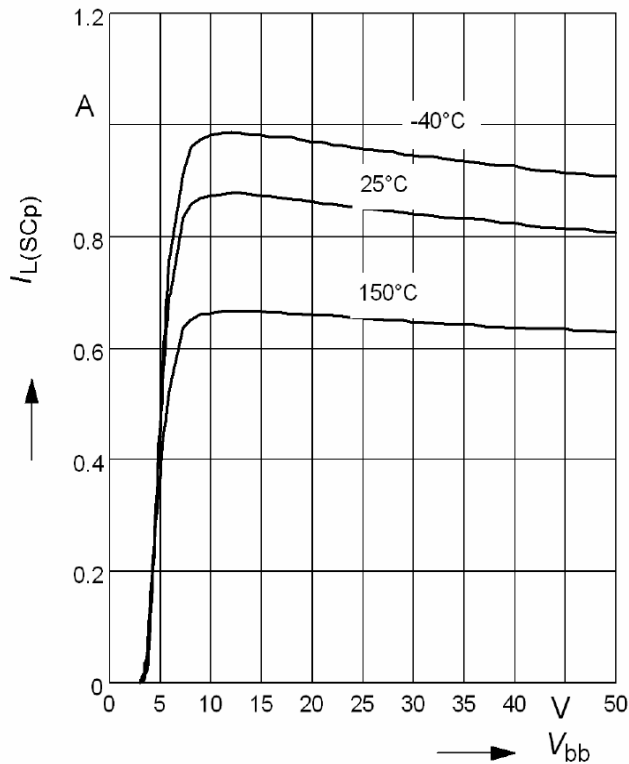
Initial Peak Short Circuit Current Limit  $I_{L(SCp)}$  versus Junction Temperature  $T_j$  @  $V_S=13,5V$ ;  $t_m=100\mu s$



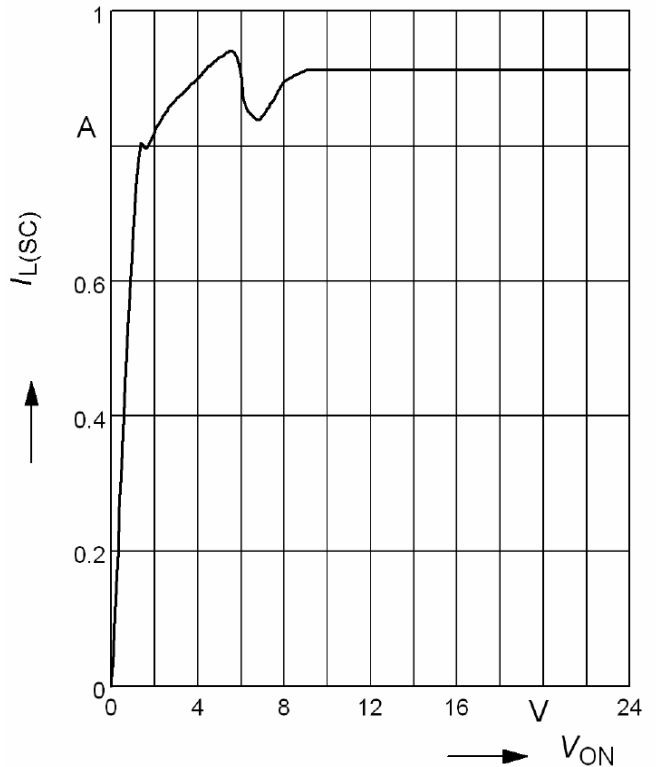
Initial Short Circuit Shutdown Time  $t_{off(SC)}$  versus Junction Start-Temperature  $T_{j\ start}$ ;  $V_S=$  parameter



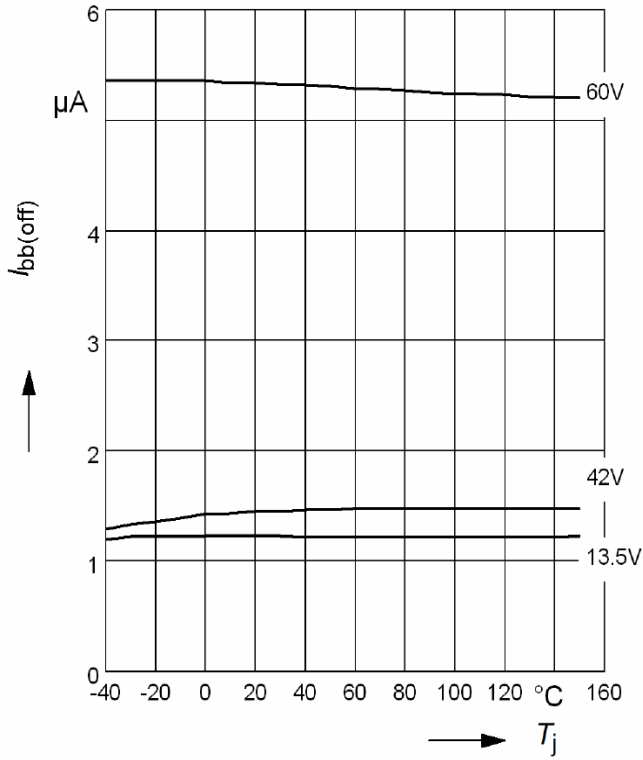
Initial Peak Short Circuit Current Limit  $I_{L(SCp)}$  versus Supply Voltage  $V_S = V_{bb}$  @  $T_j=$  parameter;  $t_m=100\mu s$



Current Limitation Characteristic  $I_{L(SC)}$  versus Drain Source Voltage Drop  $V_{ON}$  @  $V_S=13,5V$



Stand By Current Consumption  $I_{S(off)}$  versus Junction Temperature  $T_j$  @ pin IN open )



## 7 Application Information

### 7.1 Application Diagram

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty for a certain functionality, condition or quality of the device.

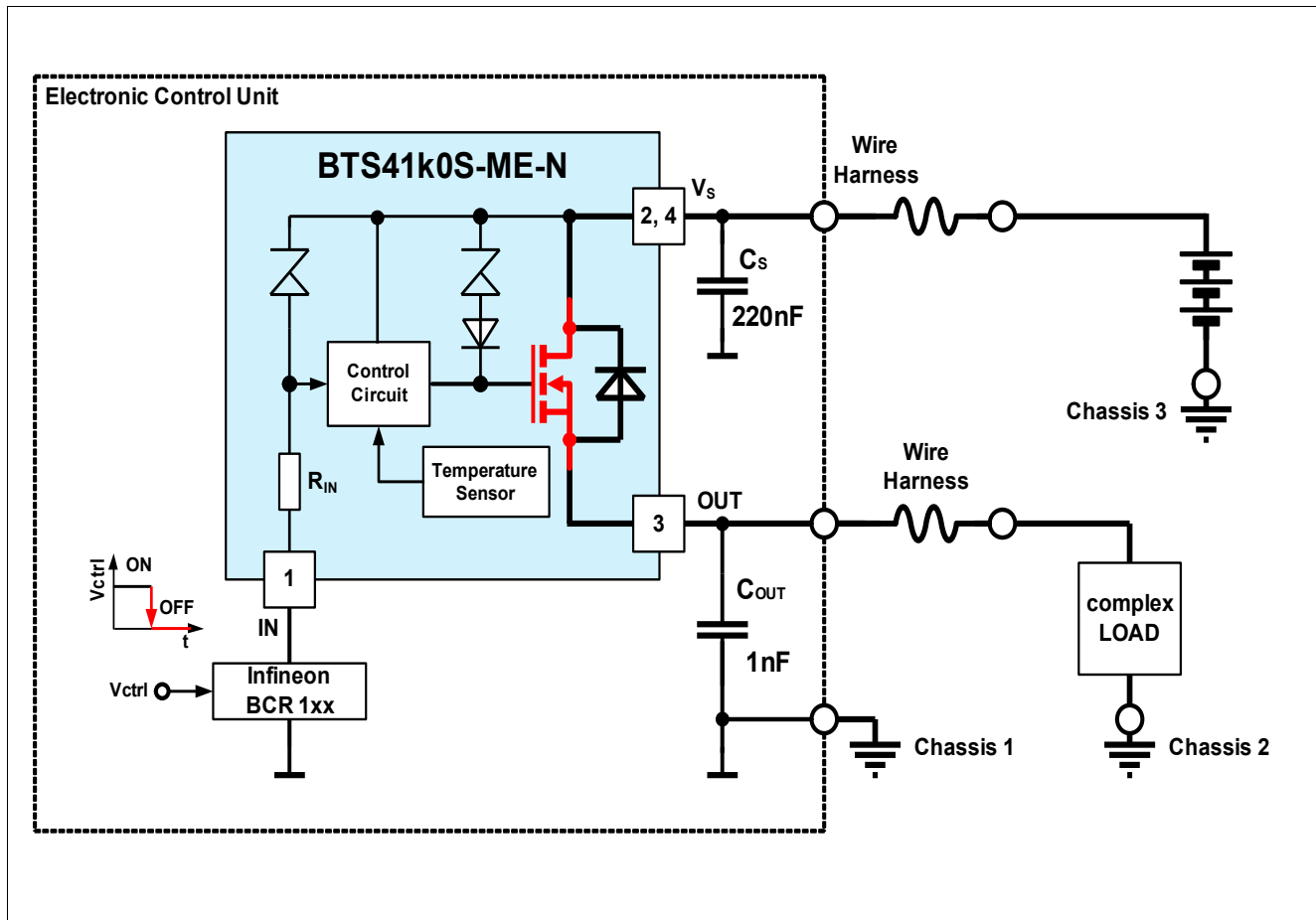


Figure 4 Application Diagram

The **BTS41k0S-ME-N** can be connected directly to the battery of a supply network. It is recommended to place a ceramic capacitor (e.g.  $C_S = 220\text{nF}$ ) between supply and GND of the ECU to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex load (resistive, capacitive or inductive) must be connected to the output pin OUT.

A built-in current limit protects the device against destruction.

The **BTS41k0S-ME-N** can be switched on and off with a low power levelshifter switch e.g. Infineon BCR1xx.

The IN pin must be pulled down to GND potential to switch the **BTS41k0S-ME-N** on. If no current is pulled down, the IN-node will float up to  $V_S$  potential by an internal pull up. In this mode the **BTS41k0S-ME-N** is deactivated with very low current consumption.

The output voltage slope is controlled during on and off transition to minimize emissions. Only a small CerCap  $C_{OUT} = 1\text{nF}$  is recommended to attenuate RF noise.

In the following chapters the main features, some typical waveforms and the protection behaviour of the **BTS41k0S-ME-N** is shown. For further details please refer to application notes on the Infineon homepage.

7.2 Special features

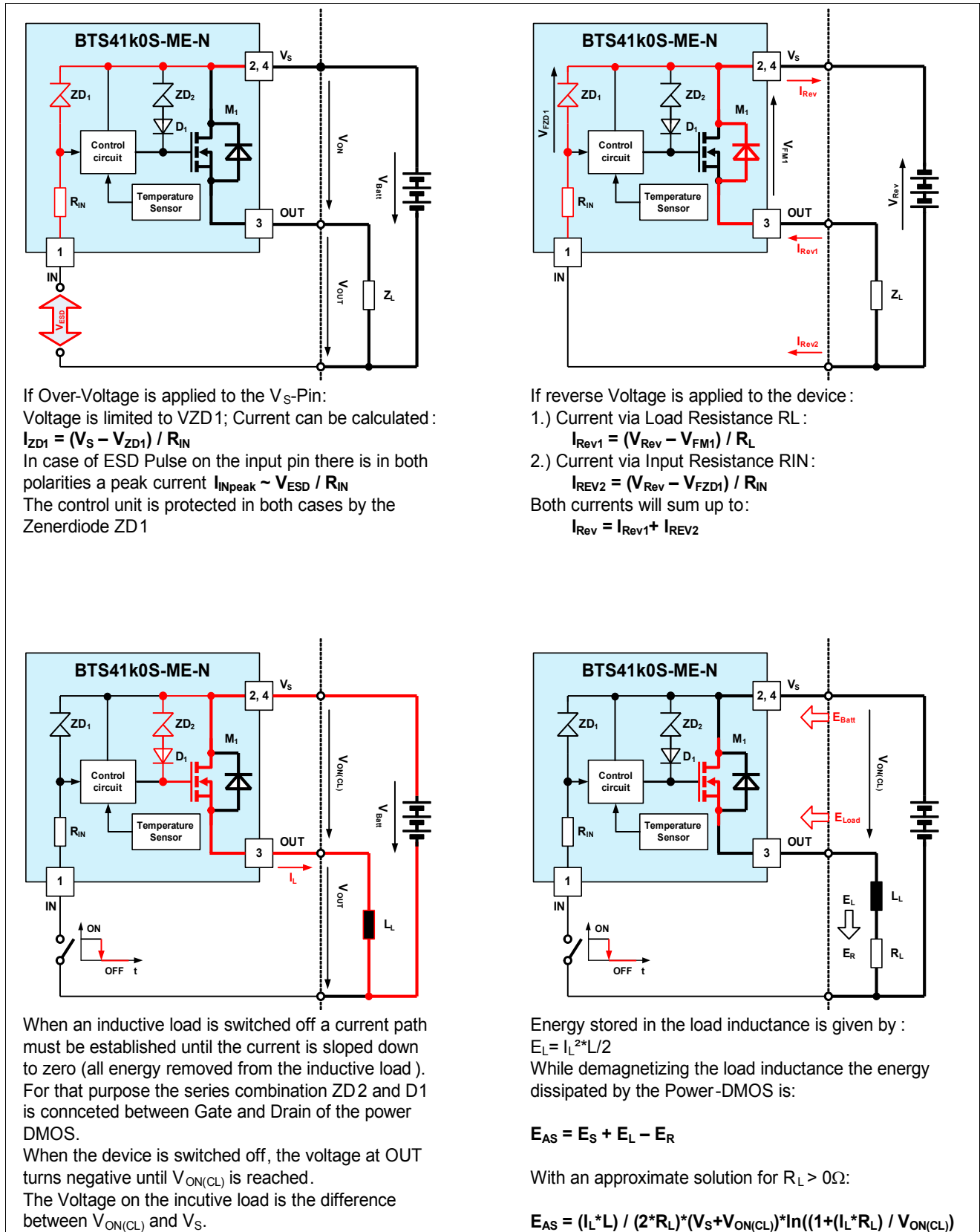


Figure 5 Special Feature descriptions

### 7.3 Typical Application Waveforms

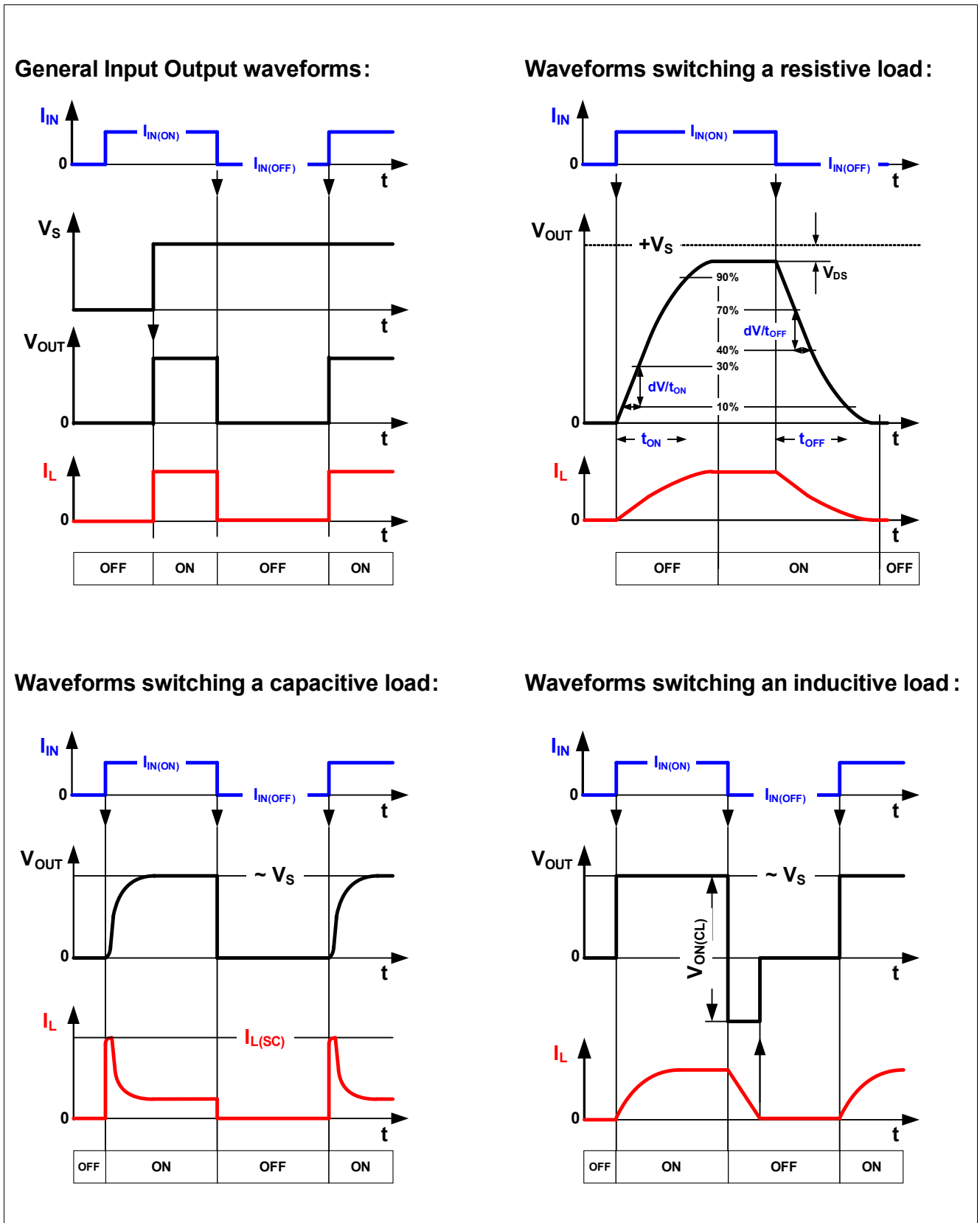


Figure 6 Typical application waveforms



### 7.4 Protection behavior

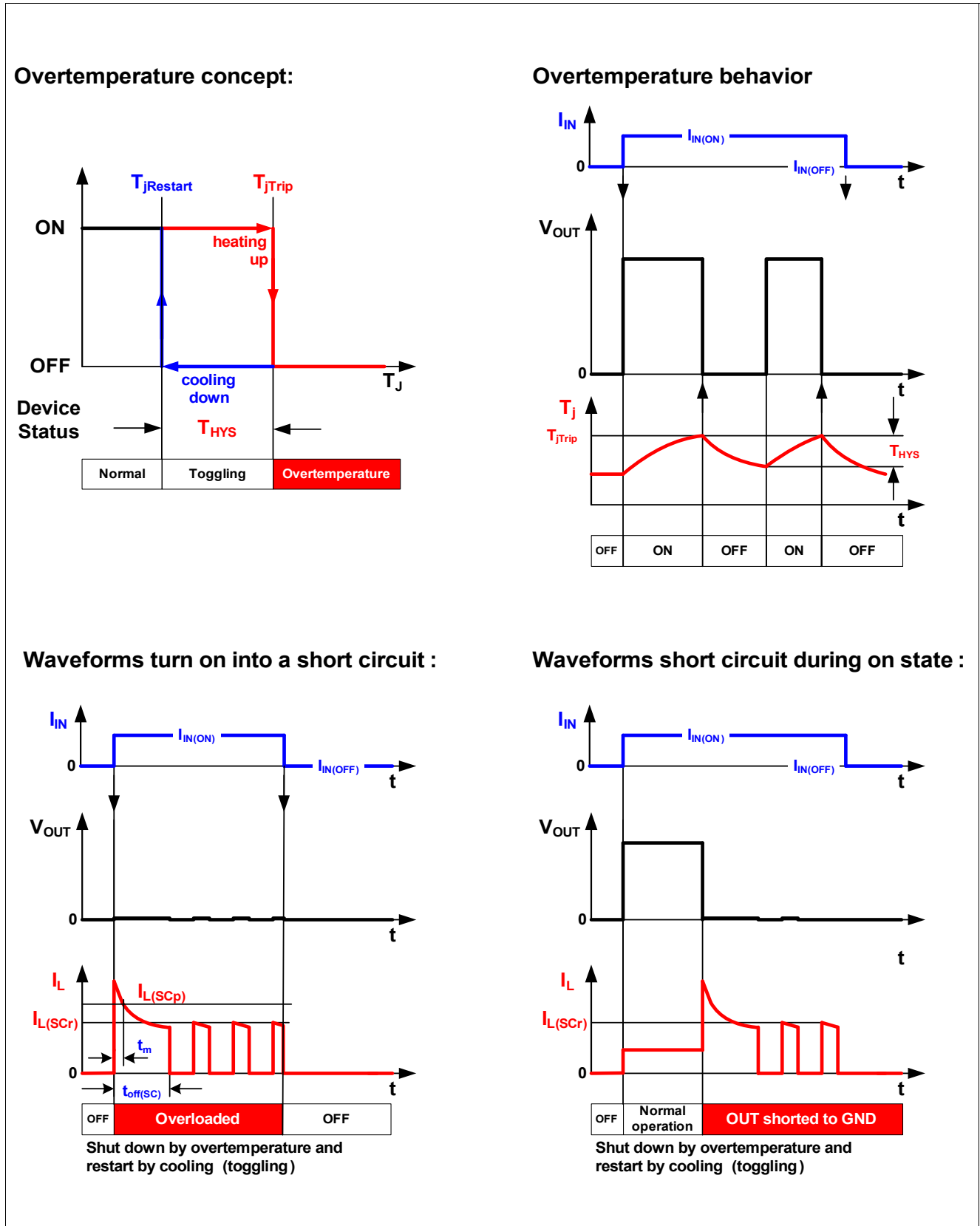
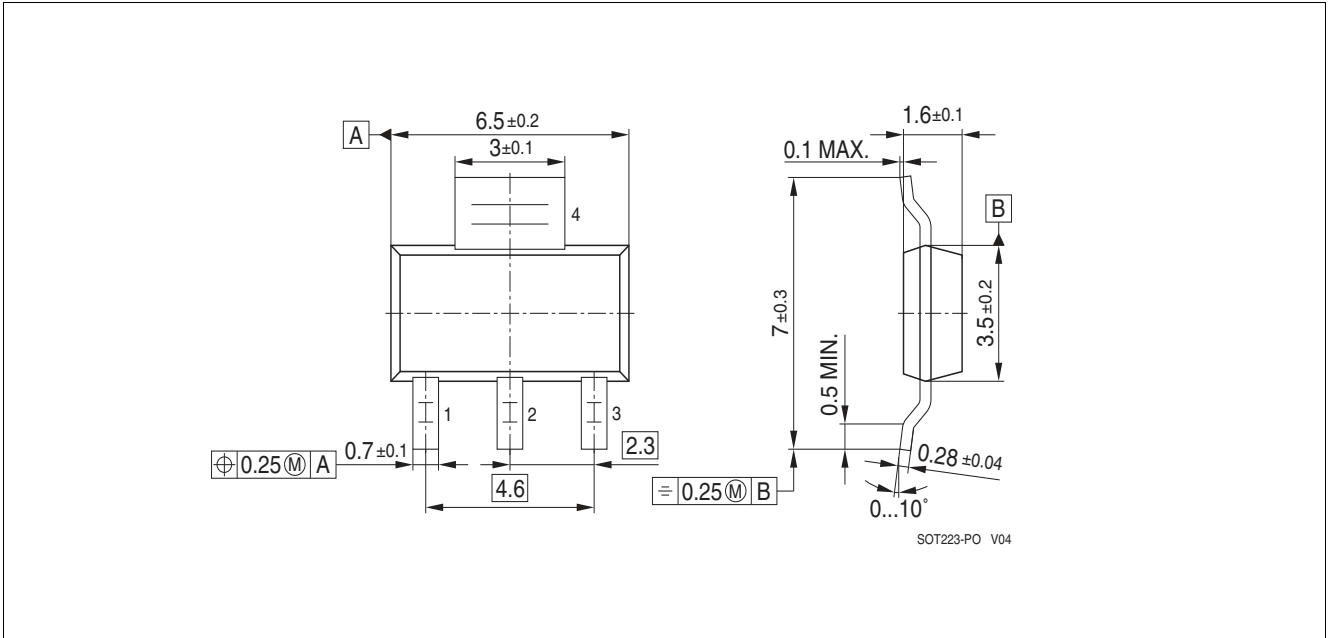


Figure 7 Protective behaviour waveforms of the BTS41k0S-ME-N

## 8 Package outlines and footprint



**Figure 8 PG-SOT223-4** (Plastic Dual Small Outline Package, RoHS-Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020)

## 9 Revision History

Revision	Date	Changes
V 1.1	12-05-08	Page 9: Line 5.0.27 changed from max 600mV to typ. 770mV
		Page 13: Graph EAS vs IOU deleted

**Edition 2012-05-08**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

**© 2011-11-23 Infineon Technologies AG  
All Rights Reserved.**

### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### **Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### **Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.