

**QUAD/DUAL SUPERCAPACITOR AUTO BALANCING (SAB™) MOSFET ARRAY**

**GENERAL DESCRIPTION**

The ALD810029/ALD910029 are additional members of the ALD8100xx (quad) and ALD9100xx (dual) family of Supercapacitor Auto Balancing MOSFETs, or SAB™ MOSFETs. SAB MOSFETs are built with production proven EPAD® technology and are designed to address voltage and leakage-current balancing of supercapacitors connected in series. Supercapacitors, also known as ultracapacitors or supercaps, connected in series can be leakage-current balanced by using a combination of one or more devices connected across each supercapacitor stack to prevent over-voltages.

The ALD810029 offers a set of unique, precise operating voltage and current characteristics for each of four SAB MOSFET devices, as shown in its Operating Electrical Characteristics table. It can be used to balance up to four supercapacitors connected in series. The ALD910029 has its own set of unique precision Operating Electrical Characteristics for each of its two SAB MOSFET devices, suitable for up to two series-connected supercapacitors.

Each SAB MOSFET features a precision gate threshold voltage in the  $V_t$  mode, which is 2.90V when the gate-drain source terminals ( $V_{GS} = V_{DS}$ ) are connected together at a drain-source current of  $I_{DS(ON)} = 1\mu A$ . In this mode, input voltage  $V_{IN} = V_{GS} = V_{DS}$ . Different  $V_{IN}$  produces an Output Current  $I_{OUT} = I_{DS(ON)}$  characteristic and results in an effective variable resistor that varies in value exponentially with  $V_{IN}$ . This  $V_{IN}$ , when connected across each supercapacitor in a series, balances each supercapacitor to within its voltage and current limits.

When  $V_{IN} = 2.90V$  is applied to an ALD810029/ALD910029, its  $I_{OUT}$  is  $1\mu A$ . For a 100mV increase in  $V_{IN}$ , to 3.00V,  $I_{OUT}$  increases by about tenfold. For an additional increase in  $V_{IN}$  to 3.12V for the ALD910029 (3.14V for the ALD810029),  $I_{OUT}$  increases one hundredfold, to  $100\mu A$ . Conversely, for a 100mV decrease in  $V_{IN}$  to 2.80V,  $I_{OUT}$  decreases to one tenth of its previous value, to  $0.1\mu A$ . Another 100mV decrease in input voltage would reduce  $I_{OUT}$  to  $0.01\mu A$ . Hence, when an ALD810029/ALD910029 SAB MOSFET is connected across a supercapacitor that charges to less than 2.70V, it would dissipate essentially no power.

(Continued on next page)

**PRODUCT FAMILY SPECIFICATIONS**

For more information on supercapacitor balancing, how SAB MOSFETs achieve automatic supercapacitor balancing, the device characteristics of the SAB MOSFET family, product family product selection guide, applications, configurations, and package information, please download from [www.aldinc.com](http://www.aldinc.com) the document:

"ALD8100xx/ALD9100xx Family of Supercapacitor Auto Balancing (SAB™) MOSFET ARRAYS"

**ORDERING INFORMATION** ("L" suffix denotes lead-free (RoHS))

Package	Operating Temperature Range	
	0°C to +70°C (Commercial)	-40°C to +85°C (Industrial)
16-Pin SOIC	N/A	ALD810029SCLI
8-Pin SOIC	N/A	ALD910029SALI

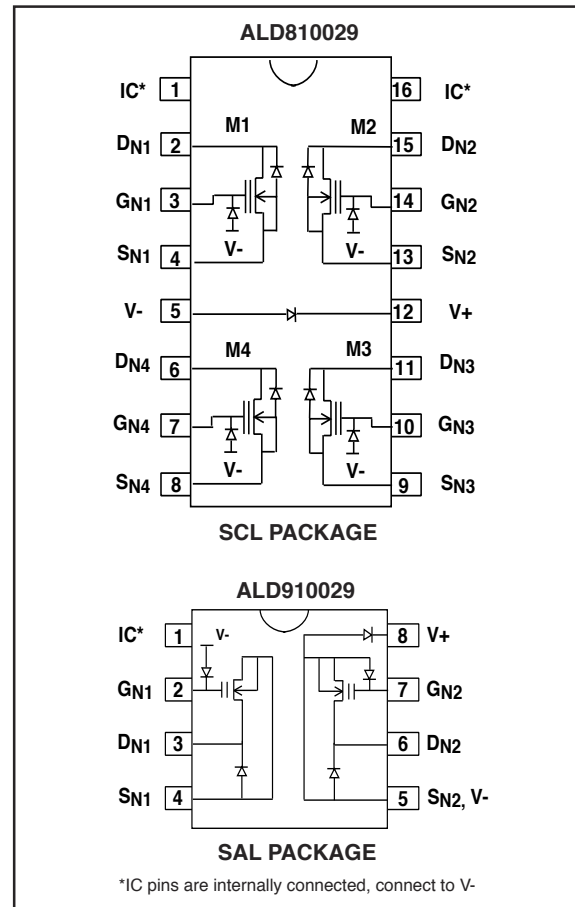
**FEATURES & BENEFITS**

- Simple and economical to use
- Precision factory trimmed
- Automatically regulates and balances leakage currents
- Effective for supercapacitor charge-balancing
- Balances up to 4 supercaps with a single IC package
- Balances 2-cell, 3-cell, 4-cell series-connected supercaps
- Scalable to larger supercap stacks and arrays
- Near zero additional leakage currents
- Zero leakage at 0.3V below rated voltages
- Balances series and/or parallel-connected supercaps
- Leakage currents are exponential function of cell voltages
- Active current ranges from  $<0.3nA$  to  $>1000\mu A$
- Always active, always fast response time
- Minimizes leakage currents and power dissipation

**APPLICATIONS**

- Series-connected supercapacitor cell leakage balancing
- Energy harvesting
- Long term backup battery with supercapacitor outputs
- Zero-power voltage divider at selected voltages
- Matched current mirrors and current sources
- Zero-power mode maximum voltage limiter
- Scaled supercapacitor stacks and arrays

**PIN CONFIGURATIONS**



**GENERAL DESCRIPTION (CONT.)**

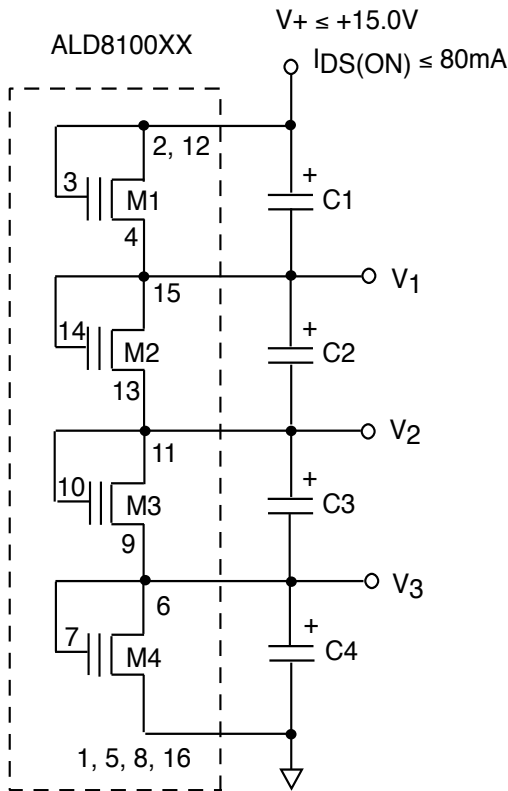
The voltage dependent characteristic of the ALD810029/ALD910029 on-resistance is effective in controlling excessive voltage rise across a supercapacitor when connected across it. In series-connected supercapacitor stacks, when one supercapacitor voltage rises, the voltage of the other supercapacitors drops, with the ones that have the highest leakage currents having the lowest supercapacitor voltages. The SAB MOSFETs connected across these supercapacitors would exhibit complementary opposing current levels, resulting in little additional leakage currents other than those caused by the supercapacitors themselves.

For technical assistance, please contact ALD technical support at [techsupport@aldinc.com](mailto:techsupport@aldinc.com).

**APPLYING THE ALD810029/ALD910029:**

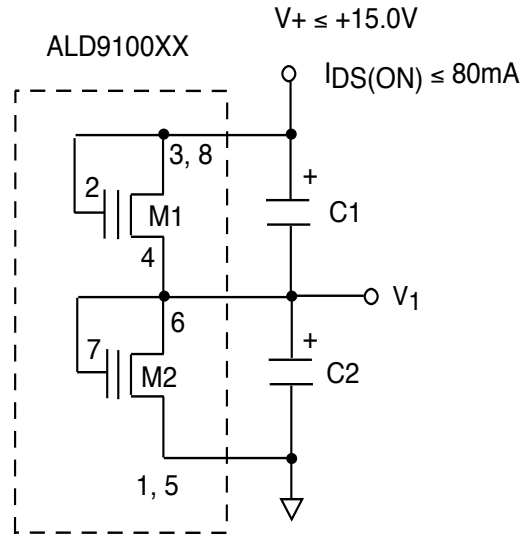
- 1) Select a maximum supercapacitor leakage current limit for any supercapacitor used in the stack. This is the same as output current,  $I_{OUT} = I_{DS(ON)}$ , of the ALD810029/ALD910029. Test that each supercapacitor leakage current meets this maximum current limit before use in the stack.
- 2) Determine whether the input voltage  $V_{IN}$  ( $V_{GS} = V_{DS}$ ) at that  $I_{OUT}$  is acceptable for the intended application. This voltage is the same voltage as the maximum desired operating voltage of the supercapacitor. For example, with the ALD810029,  $I_{OUT} = 1.0\mu A$  corresponds to  $V_{IN} = 2.90V$ .
- 3) Determine that the operating voltage margin, due to various tolerances and/or temperature effects, is adequate for the intended operating environment of the supercapacitor.

**SCHEMATIC DIAGRAM OF A TYPICAL CONNECTION FOR A FOUR-SUPERCAP STACK**



1-16 DENOTES PACKAGE PIN NUMBERS  
C1-C4 DENOTES SUPERCAPACITORS

**SCHEMATIC DIAGRAM OF A TYPICAL CONNECTION FOR A TWO-SUPERCAP STACK**



1-8 DENOTES PACKAGE PIN NUMBERS  
C1-C2 DENOTES SUPERCAPACITORS

## ABSOLUTE MAXIMUM RATINGS

V+ to V- voltage	15.0V
Drain-Source voltage, $V_{DS}$	10.6V
Gate-Source voltage, $V_{GS}$	10.6V
Operating Current	80mA
Power dissipation	500mW
Operating temperature range SCL	0°C to +70°C
Operating temperature range SCL1	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature, 10 seconds	+260°C

**CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.**

## OPERATING ELECTRICAL CHARACTERISTICS

V+ = +5V, V- = GND,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{GS} = V_{DS}$ ,  $I_{OUT} = I_{DS(ON)}$  unless otherwise specified

Parameter	Symbol	ALD810029			Unit	Test Conditions
		Min	Typ	Max		
Gate Threshold Voltage	$V_t$	2.88	2.90	2.92	V	$V_{GS} = V_{DS}$ ; $I_{DS(ON)} = 1\mu\text{A}$
Offset Voltage	$V_{OS}$		5	20	mV	$V_{t1} - V_{t2}$ or $V_{t3} - V_{t4}$
Offset Voltage Tempco	$TC_{VOS}$		5		$\mu\text{V}/\text{C}$	$V_{t1} - V_{t2}$ or $V_{t3} - V_{t4}$
Gate Threshold Voltage Tempco	$TC_{V_t}$		-2.2		mV/C	$V_{GS} = V_{DS}$ ; $I_{DS(ON)} = 1\mu\text{A}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		0.0001 25000		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.50\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		0.001 2600		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.60\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		0.01 270		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.70\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		0.1 28		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.80\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		1 2.9		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.90\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		10 0.30		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 3.00\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		100 31.4		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.14\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		300 10.8		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.24\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		1000 3.42		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.42\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		3000 1.24		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.72\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		10000 0.432		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 4.32\text{V}$
Drain Source Breakdown Voltage	$BV_{DSX}$	10.6			V	
Drain Source Leakage Current <sup>1</sup>	$I_{DS(OFF)}$		10	400	pA nA	$V_{IN} = V_{GS} = V_{DS} = V_t - 1.0$ $V_{IN} = V_{GS} = V_{DS} = V_t - 1.0$ , $T_A = +125^\circ\text{C}$
Gate Leakage Current <sup>1</sup>	$I_{GSS}$		5	200	pA nA	$V_{GS} = 5.0\text{V}$ , $V_{DS} = 0\text{V}$ $V_{GS} = 5.0\text{V}$ , $V_{DS} = 0\text{V}$ , $T_A = +125^\circ\text{C}$
Input Capacitance	$C_{ISS}$		15		pF	$V_{GS} = 0\text{V}$ , $V_{DS} = 5.0\text{V}$
Turn-on Delay Time	$t_{on}$		10		ns	
Turn-off Delay Time	$t_{off}$		10		ns	
Crosstalk			60		dB	$f = 100\text{KHz}$

## ABSOLUTE MAXIMUM RATINGS

V+ to V- voltage	15.0V
Drain-Source voltage, $V_{DS}$	10.6V
Gate-Source voltage, $V_{GS}$	10.6V
Operating Current	80mA
Power dissipation	500mW
Operating temperature range SAL	0°C to +70°C
Operating temperature range SALI	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Lead temperature, 10 seconds	+260°C

**CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.**

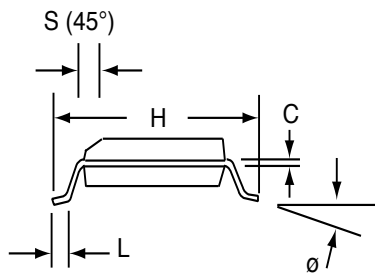
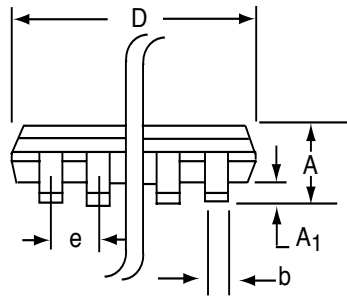
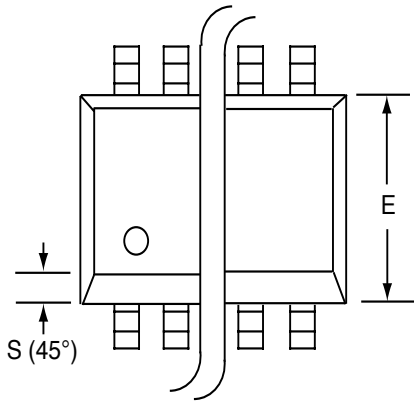
## OPERATING ELECTRICAL CHARACTERISTICS

V+ = +5V, V- = GND,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{GS} = V_{DS}$ ,  $I_{OUT} = I_{DS(ON)}$  unless otherwise specified

Parameter	Symbol	ALD910029			Unit	Test Conditions
		Min	Typ	Max		
Gate Threshold Voltage	$V_t$	2.88	2.90	2.92	V	$V_{GS} = V_{DS}$ ; $I_{DS(ON)} = 1\mu\text{A}$
Offset Voltage	$V_{OS}$		5	20	mV	$V_{t1} - V_{t2}$
Offset Voltage Tempco	$TC_{VOS}$		5		$\mu\text{V}/\text{C}$	$V_{t1} - V_{t2}$
Gate Threshold Voltage Tempco	$TC_{V_t}$		-2.2		mV/C	$V_{GS} = V_{DS}$ ; $I_{DS(ON)} = 1\mu\text{A}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		0.0001 25000		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.50\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		0.001 2600		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.60\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		0.01 270		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.70\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		0.1 28		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.80\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		1 2.9		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 2.90\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		10 0.30		$\mu\text{A}$ $\text{M}\Omega$	$V_{IN} = 3.00\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		100 31.2		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.12\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		300 10.7		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.20\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		1000 3.34		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.34\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		3000 1.13		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.40\text{V}$
Output Current Drain Source On Resistance	$I_{OUT}$ $R_{DS(ON)}$		10000 0.39		$\mu\text{A}$ $\text{K}\Omega$	$V_{IN} = 3.90\text{V}$
Drain Source Breakdown Voltage	$BV_{DSX}$	10.6			V	
Drain Source Leakage Current <sup>1</sup>	$I_{DS(OFF)}$		10	400	pA nA	$V_{IN} = V_{GS} = V_{DS} = V_t - 1.0$ $V_{IN} = V_{GS} = V_{DS} = V_t - 1.0$ , $T_A = +125^\circ\text{C}$
Gate Leakage Current <sup>1</sup>	$I_{GSS}$		5	200	pA nA	$V_{GS} = 5.0\text{V}$ , $V_{DS} = 0\text{V}$ $V_{GS} = 5.0\text{V}$ , $V_{DS} = 0\text{V}$ , $T_A = +125^\circ\text{C}$
Input Capacitance	$C_{ISS}$		30		pF	$V_{GS} = 0\text{V}$ , $V_{DS} = 5.0\text{V}$
Turn-on Delay Time	$t_{on}$		10		ns	
Turn-off Delay Time	$t_{off}$		10		ns	
Crosstalk			60		dB	$f = 100\text{KHz}$

# SOIC-16 PACKAGE DRAWING

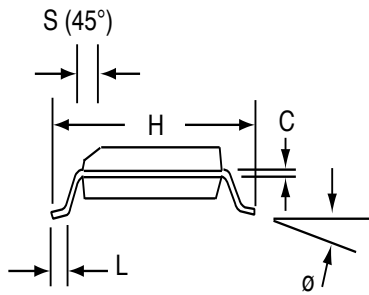
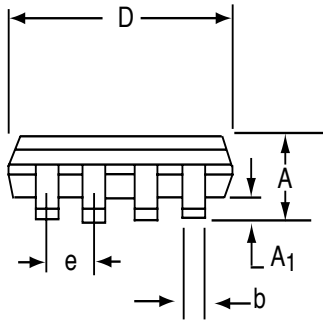
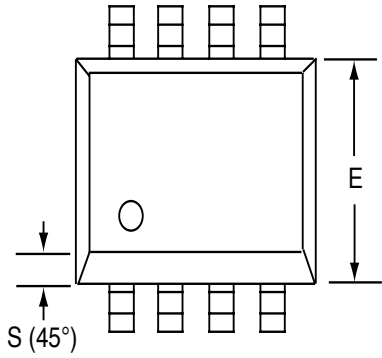
## 16 Pin Plastic SOIC Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	1.35	1.75	0.053	0.069
<b>A<sub>1</sub></b>	0.10	0.25	0.004	0.010
<b>b</b>	0.35	0.45	0.014	0.018
<b>C</b>	0.18	0.25	0.007	0.010
<b>D-16</b>	9.80	10.00	0.385	0.394
<b>E</b>	3.50	4.05	0.140	0.160
<b>e</b>	1.27 BSC		0.050 BSC	
<b>H</b>	5.70	6.30	0.224	0.248
<b>L</b>	0.60	0.937	0.024	0.037
<b>∅</b>	0°	8°	0°	8°
<b>S</b>	0.25	0.50	0.010	0.020

# SOIC-8 PACKAGE DRAWING

## 8 Pin Plastic SOIC Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	1.35	1.75	0.053	0.069
<b>A<sub>1</sub></b>	0.10	0.25	0.004	0.010
<b>b</b>	0.35	0.45	0.014	0.018
<b>C</b>	0.18	0.25	0.007	0.010
<b>D-8</b>	4.69	5.00	0.185	0.196
<b>E</b>	3.50	4.05	0.140	0.160
<b>e</b>	1.27 BSC		0.050 BSC	
<b>H</b>	5.70	6.30	0.224	0.248
<b>L</b>	0.60	0.937	0.024	0.037
<b>∅</b>	0°	8°	0°	8°
<b>S</b>	0.25	0.50	0.010	0.020