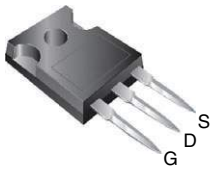
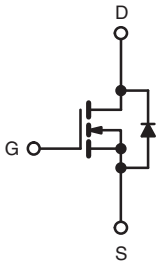
Power MOSFET

TO-247





N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{oss} Specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Two Transistor Forward
- Half Bridge, Full Bridge
- PFC Boost

PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.40
Q_g (Max.) (nC)	64	
Q_{gs} (nC)	16	
Q_{gd} (nC)	26	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-247
Lead (Pb)-free	IRFP450APbF

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	14	A
		T_C = 100 °C		8.7	
Pulsed Drain Current[a]			I_{DM}	56	
Linear Derating Factor				1.5	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	760	mJ
Repetitive Avalanche Current[a]			I_{AR}	14	A
Repetitive Avalanche Energy[a]			E_{AR}	19	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	190	W
Peak Diode Recovery dV/dt[c]			dV/dt	4.1	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	For 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Starting T_J = 25 °C, L = 7.8 mH, R_G = 25 Ω, I_{AS} = 14 A (see fig. 12)

c. I_{SD} ≤ 14 A, dI/dt ≤ 130 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C

d. 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.65	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.58	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 8.4 A[b]	-	-	0.40	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 8.4 A[b]	7.8	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	2038	-	pF
Output Capacitance	C_{oss}		-	307	-	
Reverse Transfer Capacitance	C_{rss}		-	10	-	
Output Capacitance	C_{oss}	V_{GS} = 0 V; V_{DS} = 1.0 V, f = 1.0 MHz		2859		
Output Capacitance	C_{oss}	V_{GS} = 0 V; V_{DS} = 400 V, f = 1.0 MHz		81		
Effective Output Capacitance	C_{oss} eff.	V_{GS} = 0 V; V_{DS} = 0 V to 400 V[c]		96		
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 14 A, V_{DS} = 400 V, see fig. 6 and 13[b]	-	-	64	nC
Gate-Source Charge	Q_{gs}		-	-	16	
Gate-Drain Charge	Q_{gd}		-	-	26	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 14 A, R_G = 6.2 Ω, R_D = 17 Ω, see fig. 10[b]	-	15	-	ns
Rise Time	t_r		-	36	-	
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	
Fall Time	t_f		-	29	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	56	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 14 A, V_{GS} = 0 V[b]	-	-	1.4	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 14 A, dI/dt = 100 A/µs[b]	-	487	731	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	3.9	5.8	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %

c. C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

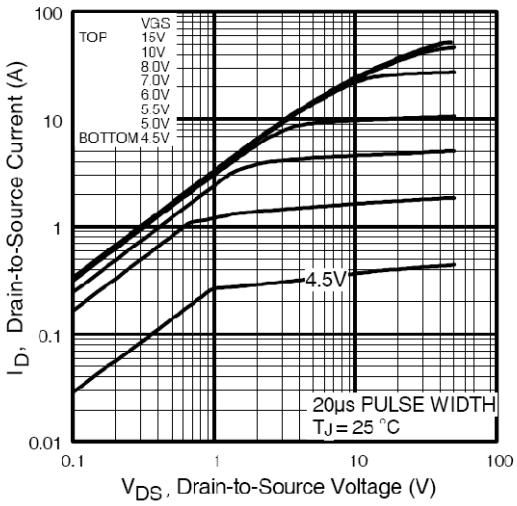


Fig. 1 - Typical Output Characteristics

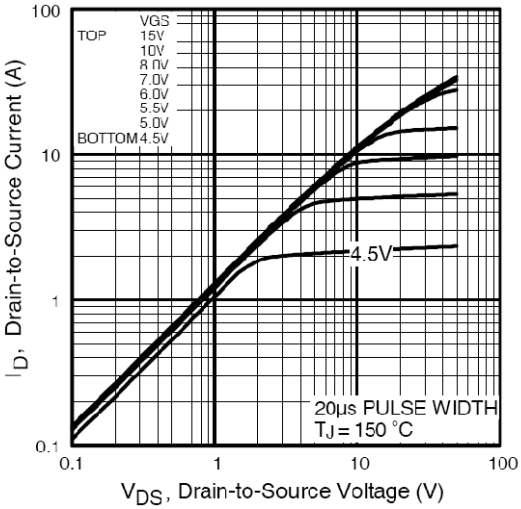


Fig. 2 - Typical Output Characteristics

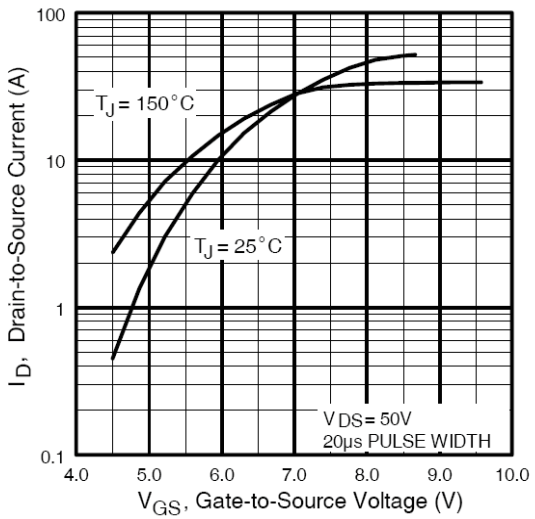


Fig. 3 - Typical Transfer Characteristics

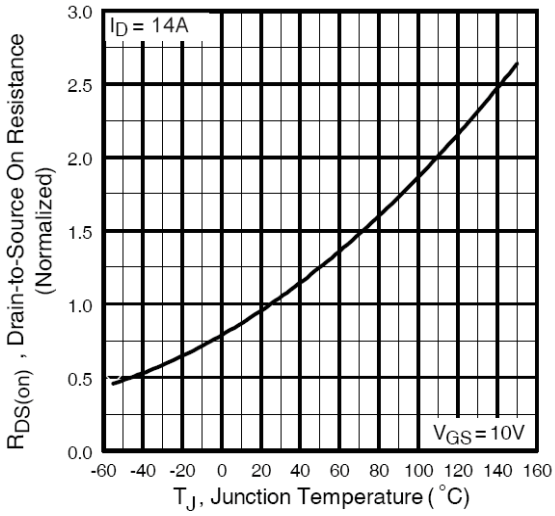


Fig. 4 - Normalized On-Resistance vs. Temperature

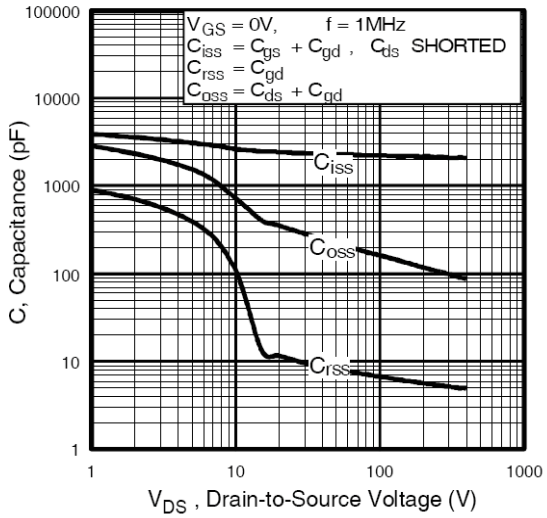


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

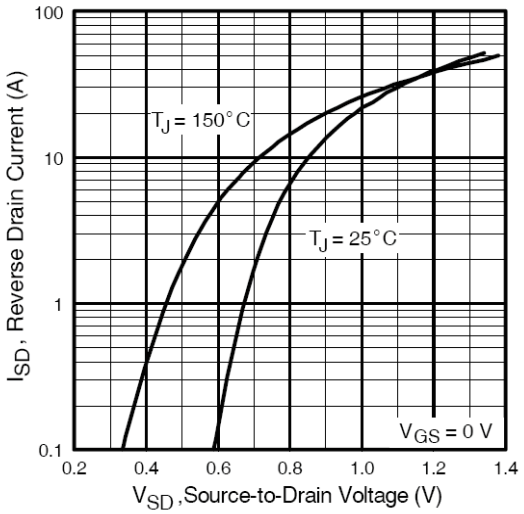


Fig. 7 - Typical Source-Drain Diode Forward Voltage

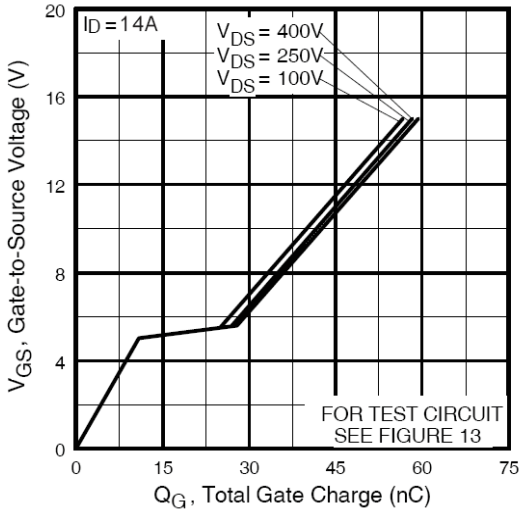


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

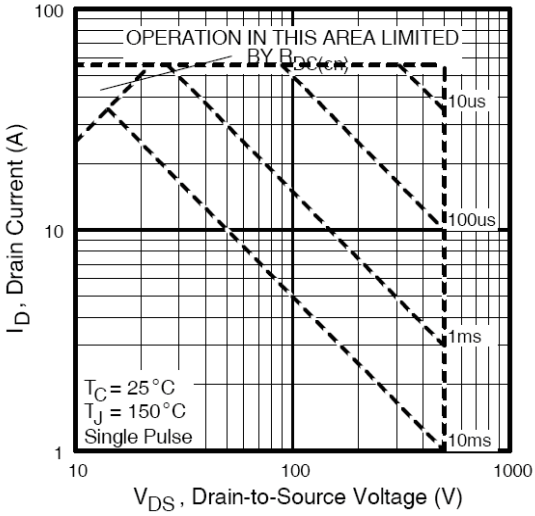


Fig. 8 - Maximum Safe Operating Area

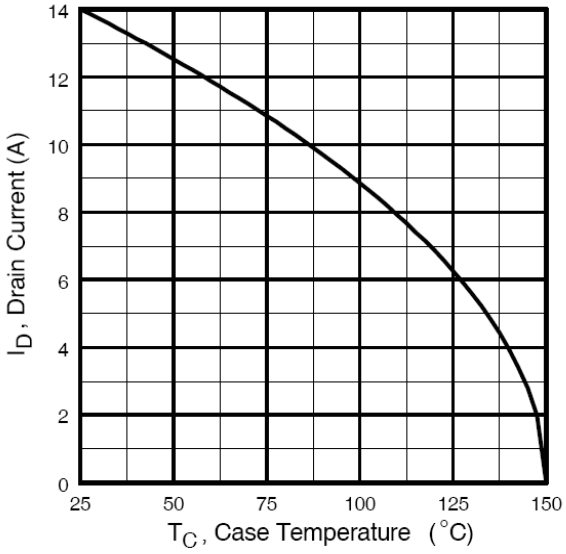


Fig. 9 - Maximum Drain Current vs. Case Temperature

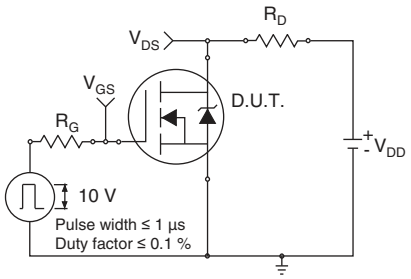


Fig. 10a - Switching Time Test Circuit

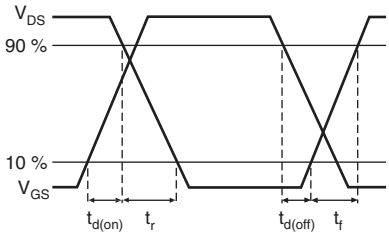


Fig. 10b - Switching Time Waveforms

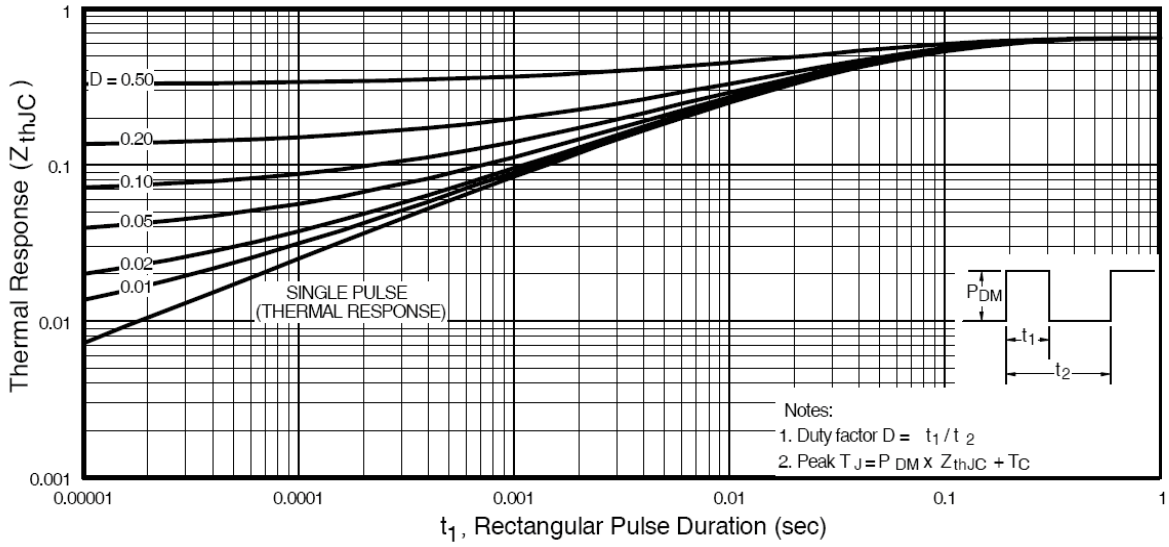


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

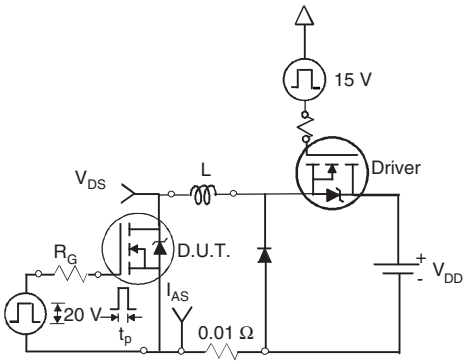


Fig. 12a - Unclamped Inductive Test Circuit

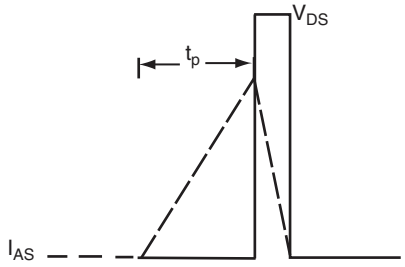


Fig. 12b - Unclamped Inductive Waveforms

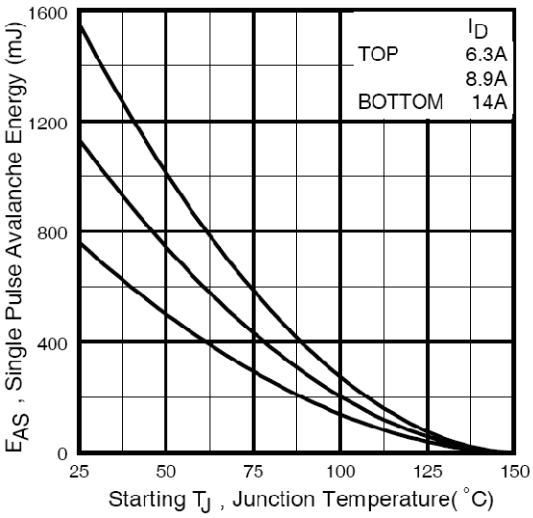


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

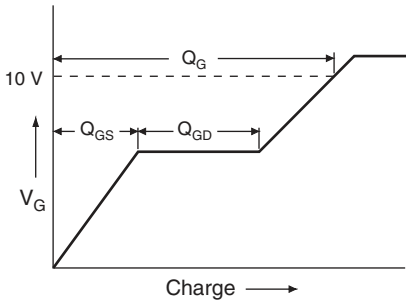


Fig. 13a - Basic Gate Charge Waveform

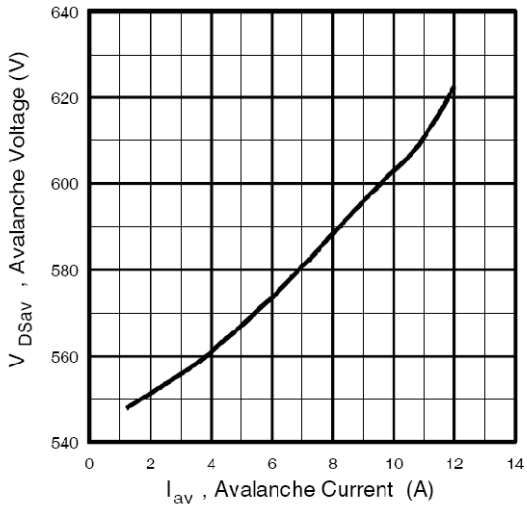


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

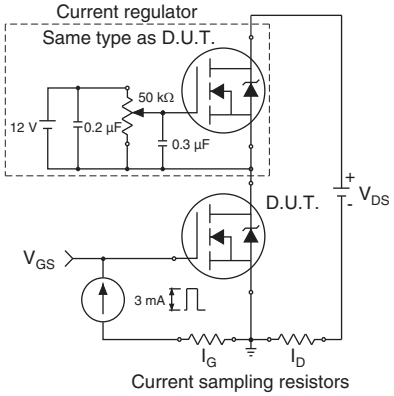
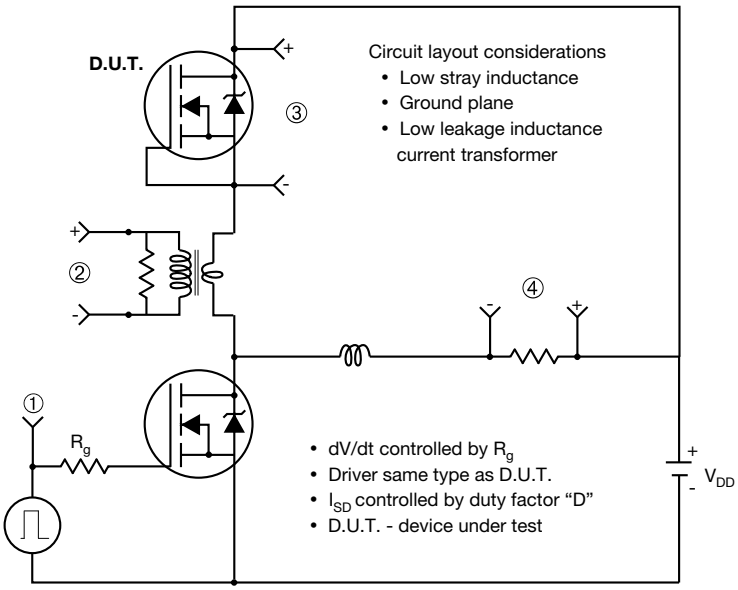
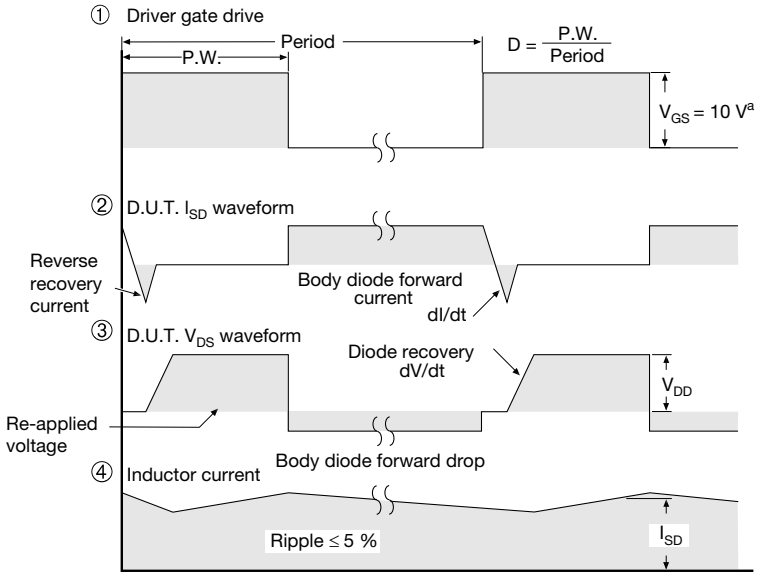


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

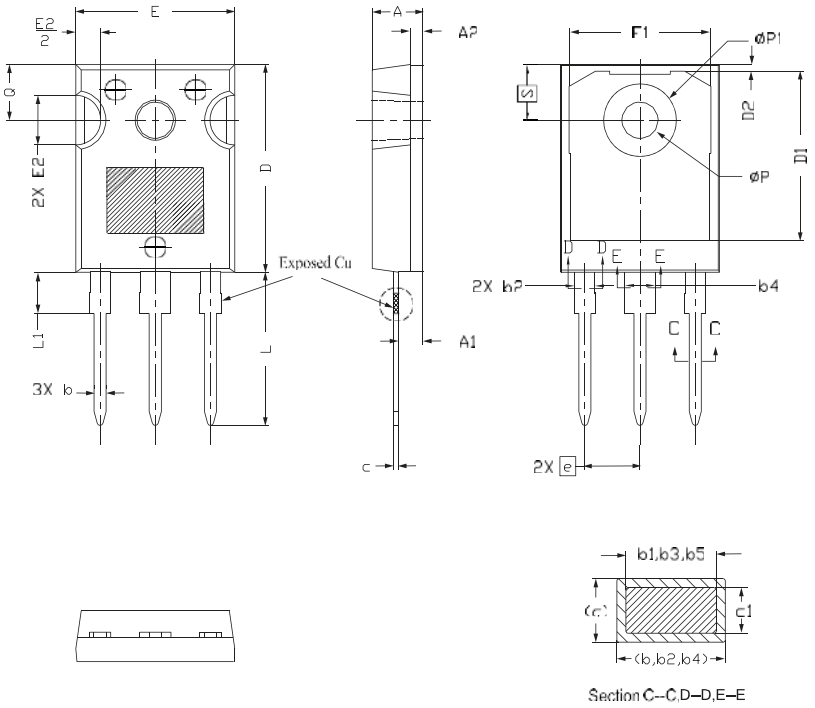
a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91230.

TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9



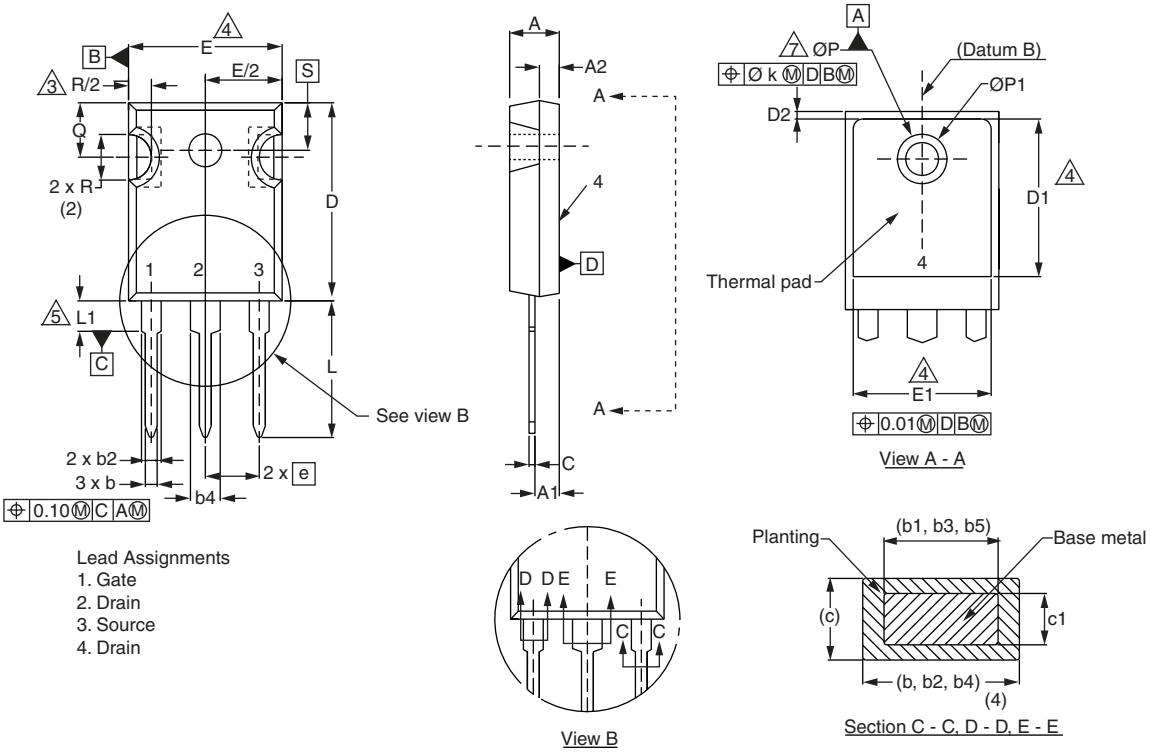
	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

	MILLIMETERS			
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

(1) Package reference: JEDEC® TO247, variation AC
(2) All dimensions are in mm
(3) Slot required, notch may be rounded
(4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
(5) Thermal pad contour optional with dimensions D1 and E1
(6) Lead finish uncontrolled in L1
(7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
(8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

VERSION 2: FACILITY CODE = Y



Lead Assignments
1. Gate
2. Drain
3. Source
4. Drain

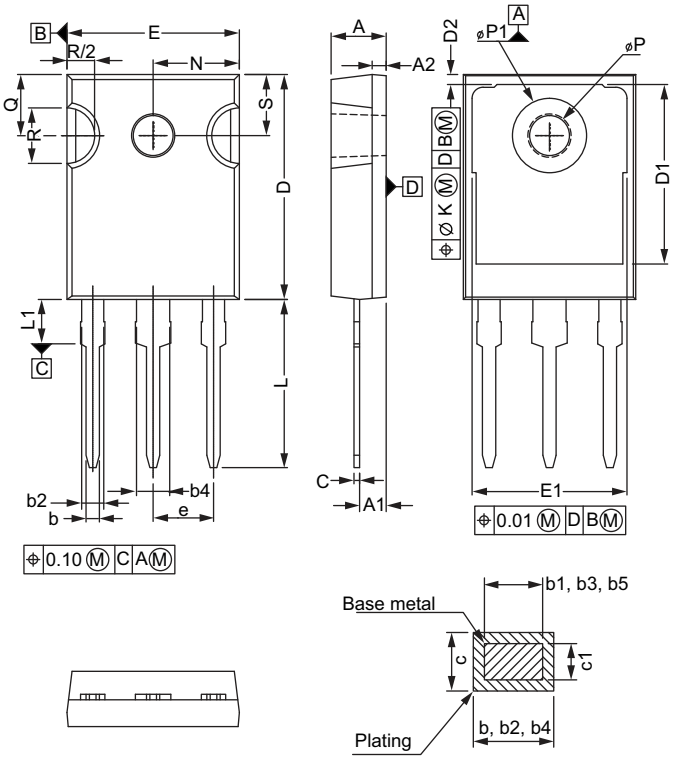
	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

(1) Dimensioning and tolerancing per ASME Y14.5M-1994
(2) Contour of slot optional
(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
(4) Thermal pad contour optional with dimensions D1 and E1
(5) Lead finish uncontrolled in L1
(6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
(7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

VERSION 3: FACILITY CODE = N



	MILLIMETERS	
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

	MILLIMETERS	
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
DWG: 5971

Notes

(1) Dimensioning and tolerancing per ASME Y14.5M-1994
(2) Contour of slot optional
(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
(4) Thermal pad contour optional with dimensions D1 and E1
(5) Lead finish uncontrolled in L1
(6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")

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