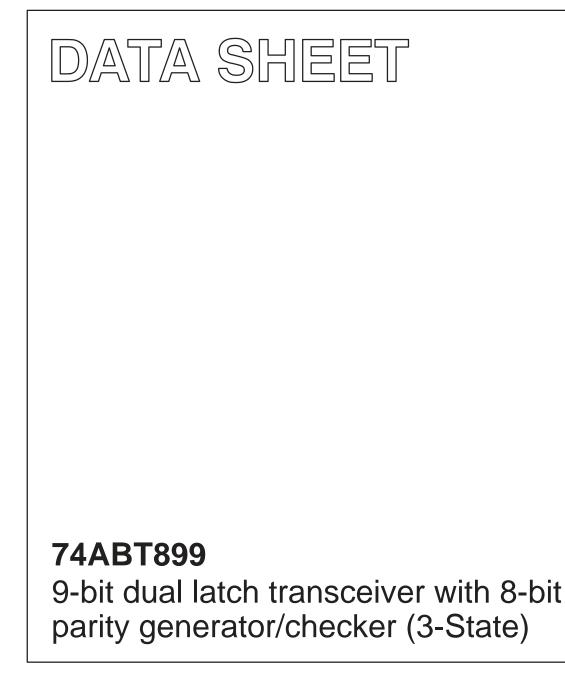
INTEGRATED CIRCUITS



Product specification Supersedes data of 1993 Oct 04 IC23 Data Handbook

1998 Jan 16





74ABT899

FEATURES

- Symmetrical (A and B bus functions are identical)
- Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions
- Independent transparent latches for A-to-B and B-to-A directions
- Selectable ODD/EVEN parity
- Continuously checks parity of both A bus and B bus latches as ERRA and ERRB
- Ability to simultaneously generate and check parity
- Can simultaneously read/latch A and B bus data
- Output capability: +64 mA/–32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power up 3-State
- Power-up reset
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT899 is a 9-bit to 9-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the $\overline{\text{SEL}}$ input.

Parity error checking of the A and B bus latches is continuously provided with ERRA and ERRB, even with both buses in 3-State.

The 74ABT899 features independent latch enables for the A and B bus latches, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION

The 74ABT899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:

Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEA and LEB are High and the Mode Select (\overline{SEL}) is Low, the parity generated from A0-A7 and B0-B7 can be checked and monitored by \overline{ERRA} and \overline{ERRB} . (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:

Bus A (B) communicates to Bus B (A) in a feed-through mode if SEL is High. Parity is still generated and checked as ERRA and ERRB and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed-through parity, Check A (and B) bus parity:

- Independent latch enables (LEA and LEB) allow other permutations of:
- Transparent latch / 1 bus latched / both buses latched
- Feed-through parity / generate parity
- Check in bus parity / check out bus parity / check in and out bus parity

QUICK REFERENCE DATA

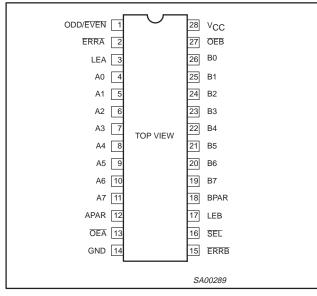
SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50 pF; V_{CC} = 5V$	2.9	ns
t _{PLH} t _{PHL}	Propagation delay An to ERRA	$C_L = 50 pF; V_{CC} = 5V$	6.1	ns
C _{IN}	Input capacitance	$V_I = 0V \text{ or } V_{CC}$	4	pF
C _{I/O}	Output capacitance	Outputs disabled; $V_O = 0V$ or V_{CC}	7	pF
I _{CCZ}	Total supply current	Outputs disabled; V _{CC} =5.5V	50	μΑ

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
28-Pin Plastic PLCC	–40°C to +85°C	74ABT899 A	74ABT899 A	SOT261-3
28-Pin Plastic SOP	–40°C to +85°C	74ABT899 D	74ABT899 D	SOT136-1
28-Pin Plastic SSOP	–40°C to +85°C	74ABT899 DB	74ABT899 DB	SOT341-1

74ABT899

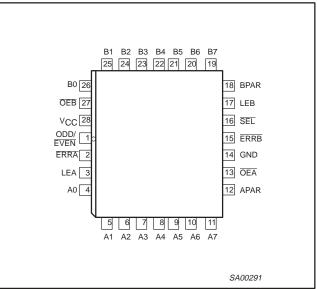
PIN CONFIGURATION



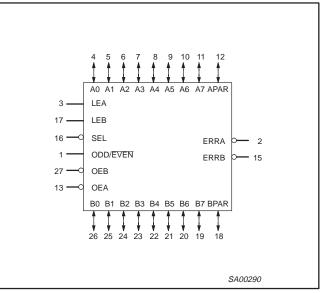
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
A0 - A7	4, 5, 6, 7, 8, 9, 10, 11	Latched A bus 3-State inputs/outputs
B0 - B7	19, 20, 21, 22, 23, 24, 25, 26	Latched B bus 3-State inputs/outputs
APAR	12	A bus parity 3-State input
BPAR	18	B bus parity 3-State input
ODD/ EVEN	1	Parity select input (Low for EVEN parity)
OEA, OEB	13, 27	Output enable inputs (gate A to B, B to A)
SEL	16	Mode select input (Low for generate)
LEA, LEB	3, 17	Latch enable inputs (transparent High)
ERRA, ERRB	2, 15	Error signal outputs (active-Low)
GND	14	Ground (0V)
V _{CC}	28	Positive supply voltage

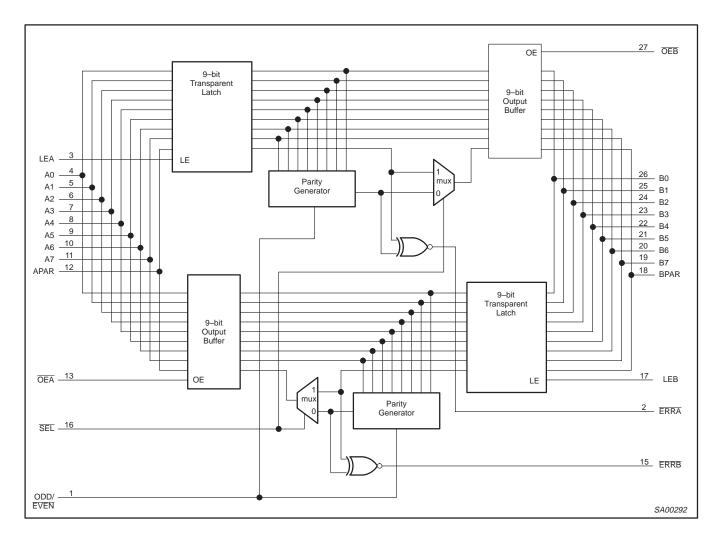
PLCC PIN CONFIGURATION



LOGIC SYMBOL



74ABT899



FUNCTION TABLE

	INPUTS			OPERATING MODE	
OEB	OEA	SEL	LEA LEB		
Н	Н	Х	Х	Х	3-State A bus and B bus (input A & B simultaneously)
Н	L	L	L	н	$B\toA,$ transparent B latch, generate parity from B0 - B7, check B bus parity
Н	L	L	Н	н	$B\toA,$ transparent A & B latch, generate parity from B0 - B7, check A & B bus parity
Н	L	L	Х	L	$B\toA,B$ bus latched, generate parity from latched B0 - B7 data, check B bus parity
Н	L	Н	Х	н	$B\toA,$ transparent B latch, parity feed-through, check B bus parity
Н	L	Н	н	н	$B\toA,$ transparent A & B latch, parity feed-through, check A & B bus parity
L	Н	L	н	Х	$A\toB,$ transparent A latch, generate parity from A0 - A7, check A bus parity
L	Н	L	н	н	$A \rightarrow B,$ transparent A & B latch, generate parity from A0 - A7, check A & B bus parity
L	Н	L	L	Х	$A \rightarrow B$, A bus latched, generate parity from latched A0 - A7 data, check A bus parity
L	Н	Н	н	L	$A \rightarrow B$, transparent A latch, parity feed-through, check A bus parity
L	Н	Н	н	н	$A \to B,$ transparent A & B latch, parity feed-through, check A & B bus parity
L	L	Х	Х	Х	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level

L = Low voltage level

X = Don't care

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PARITY AND ERROR FUNCTION TABLE

	INPU	TS			OUTPUTS			
SEL	ODD/EVEN	xPAR (A or B)	Σ of High Inputs	xPAR (B or A)	ERRt	ERRr*		PARITY MODES
н	н	н	Even Odd	H H	H L	H L	Odd	
н	н	L	Even Odd	L	L H	L H	Mode	Feed-through/check parity
н	L	Н	Even Odd	H	L H	L H	Even	
н	L	L	Even Odd	LL	H L	H L	Mode	
L	Н	н	Even Odd	H L	H L	H H	Odd	
L	Н	L	Even Odd	HL	L H	H H	Mode	Generate parity
L	L	н	Even Odd	L H	L H	H H	Even	
L	L	L	Even Odd	L H	H L	H H	Mode	

H = High voltage level

Low voltage level L =

t

= Transmit–if the data path is from $A \rightarrow B$ then ERRt is ERRA = Receive–if the data path is from $A \rightarrow B$ then ERRT is ERRB Blocked if latch is not transparent

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V ₁ < 0	-18	mA
VI	DC input voltage ³		-1.2 to +7.0	V
I _{ОК}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		–65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction 2. temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 1505C.

3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIM	ITS	UNIT
		Min	Max	
V _{CC}	DC supply voltage	4.5	5.5	V
VI	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level Input voltage		0.8	V
I _{ОН}	High-level output current		-32	mA
I _{OL}	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

						LIMITS			
SYMBOL	PARAM	ETER	TEST CONDITIONS	T _{amb} = +25°C			T _{amb} = to +8	–40°C 35°C	UNIT
			Min	Тур	Max	Min	Max		
V _{IK}	Input clamp volt	age	$V_{CC} = 4.5V; I_{IK} = -18mA$		-0.9	-1.2		-1.2	V
			V_{CC} = 4.5V; I_{OH} = –3mA; V_{I} = V_{IL} or V_{IH}	2.5	3.5		2.5		V
V _{OH}	High-level output	ut voltage	V_{CC} = 5.0V; I_{OH} = –3mA; V_{I} = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_{I} = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V _{OL}	Low-level output	t voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_{I} = V_{IL} or V_{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output voltage ³	t low	V_{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
l _l	Input leakage	Control pins	V_{CC} = 5.5V; V_{I} = GND or 5.5V		±0.01	±1.0		±1.0	μA
	current	Data pins	V_{CC} = 5.5V; V_{I} = GND or 5.5V		±5	±100		±100	μΑ
I _{OFF}	Power-off leaka	ge current	V_{CC} = 0.0V; V_{O} or $V_{I} \leq \ 4.5V$		±5.0	±100		±100	μΑ
I _{PU} /I _{PD}	Power-up/down output current ⁴	3-State	V_{CC} = 2.1V; V_{O} = 0.5V; V_{I} = GND or $V_{CC};$ V_{OE} = Don't care		±5.0	±50		±50	μΑ
I _{IH} + I _{OZH}	3-State output H	ligh current	V_{CC} = 5.5V; V_{O} = 2.7V; V_{I} = V_{IL} or V_{IH}		5.0	50		50	μΑ
$I_{IL} + I_{OZL}$	3-State output L	ow current	V_{CC} = 5.5V; V_{O} = 0.5V; V_{I} = V_{IL} or V_{IH}		-5.0	-50		-50	μΑ
I _{CEX}	Output High lea	kage current	V_{CC} = 5.5V; V_{O} = 5.5V; V_{I} = GND or V_{CC}		5.0	50		50	μA
Ι _Ο	Output current ¹		$V_{CC} = 5.5V; V_{O} = 2.5V$	-50	-80	-180	-50	-180	mA
I _{CCH}			V_{CC} = 5.5V; Outputs High, V_{I} = GND or V_{CC}		50	250		250	μA
I _{CCL}	Quiescent supp	ly current	V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		28	34		34	mA
I _{CCZ}]		V_{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		50	250		250	μA
ΔI_{CC}	Additional supp input pin ²	y current per	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		0.3	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

2. This is the increase in supply current for each input at 3.4V.

3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V \pm 10%, a transition time of up to 100µsec is permitted.

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AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500 Ω

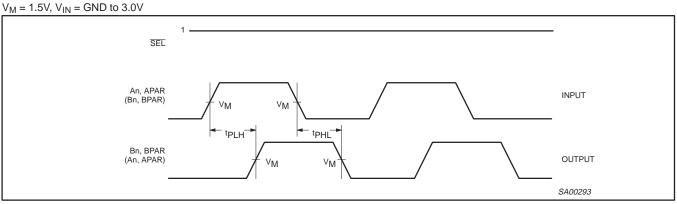
					LIMITS			
SYMBOL	PARAMETER	WAVEFORM	1	Γ _{amb} = +25° V _{CC} = +5.0\ C _L = 50pF R _L = 500Ω	/	V _{CC} = +5 C _L =	0 to +85°C 5.0V ±10% 50pF 500Ω	UNIT
			Min	Тур	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay An to Bn or Bn to An	1	1.0 1.0	3.2 2.7	4.5 4.1	1.0 1.0	4.9 4.6	ns
t _{PLH} t _{PHL}	Propagation delay An to BPAR or Bn to APAR	2	3.0 2.5	6.0 6.4	7.5 7.9	3.0 2.5	9.0 8.8	ns
t _{PLH} t _{PHL}	Propagation delay An to ERRA or Bn to ERRB	3	2.8 2.8	6.0 6.7	8.0 8.5	2.8 2.8	9.1 9.3	ns
t _{PLH} t _{PHL}	Propagation delay APAR to BPAR or BPAR to APAR	1	2.0 1.3	4.0 3.2	5.2 4.4	2.0 1.3	5.7 5.0	ns
t _{PLH} t _{PHL}	Propagation delay APAR to ERRA or BPAR to ERRB	6	1.5 1.5	4.2 4.0	5.4 5.4	1.5 1.5	6.0 6.1	ns
t _{PLH} t _{PHL}	Propagation delay ODD/EVEN to APAR or BPAR	5	2.6 2.5	5.5 5.3	6.8 6.7	2.6 2.5	8.1 7.8	ns
t _{PLH} t _{PHL}	Propagation delay ODD/EVEN to ERRA or ERRB	4	2.3 2.6	5.4 5.7	6.8 7.2	2.3 2.6	7.9 8.4	ns
t _{PLH} t _{PHL}	Propagation delay SEL to APAR or BPAR	8	1.3 1.4	4.1 4.1	5.2 5.3	1.3 1.4	6.0 5.9	ns
t _{PLH} t _{PHL}	Propagation delay SEL to ERRA or ERRB	8	3.7 5.1	6.8 8.3	8.3 9.7	3.7 5.1	9.8 11.0	ns
t _{PLH} t _{PHL}	Propagation delay LEA to Bn or LEB to An	9	1.0 1.0	3.2 3.1	4.4 4.5	1.0 1.0	4.9 5.0	ns
t _{PLH} t _{PHL}	Propagation delay LEA to BPAR or LEB to APAR	9	2.0 1.7	6.8 6.3	8.3 7.9	2.0 1.7	9.7 9.0	ns
t _{PLH} t _{PHL}	Propagation delay LEA to ERRA or LEB to ERRB	7	2.0 2.0	6.3 7.1	8.3 9.2	2.0 2.0	9.6 10.3	ns
t _{PZH} t _{PZL}	Output enable time OEA to An, APAR or OEB to Bn, BPAR	11, 12	1.0 1.0	3.0 3.4	4.3 4.8	1.0 1.0	5.1 5.4	ns
t _{PHZ} t _{PLZ}	Output disable time OEA to An, APAR or OEB to Bn, BPAR	11, 12	1.0 0.5	3.4 3.0	4.7 4.2	1.0 0.5	5.5 4.7	ns

AC SETUP REQUIREMENTS

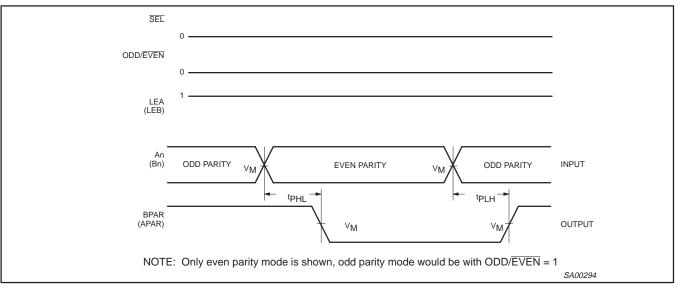
GND = 0V; t_R = t_F = 2.5ns; CL = 50pF, RL = 500 Ω

					LIMITS			
SYMBOL	PARAMETER	WAVEFORM	ſ	$ T_{amb} = +25^{\circ} $ $ V_{CC} = +5.0 V_{CL} = 50 pF$ $ R_L = 500 \Omega $		V _{CC} = +5 C _L =	0 to +85°C .0V ±10% 50pF 500Ω	UNIT
			Min	Тур	Max	Min	Max	
t _s (H) t _s (L)	Setup time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	2.0 1.5	0.4 0.0		2.0 1.5		ns
t _h (H) t _h (L)	Hold time, High or Low An, APAR to LEA or Bn, BPAR to LEB	10	1.5 1.0	0.0 0.2		1.5 1.0		ns
t _w (H)	Pulse width, High LEA or LEB	10	3.0	1.9		3.0		ns

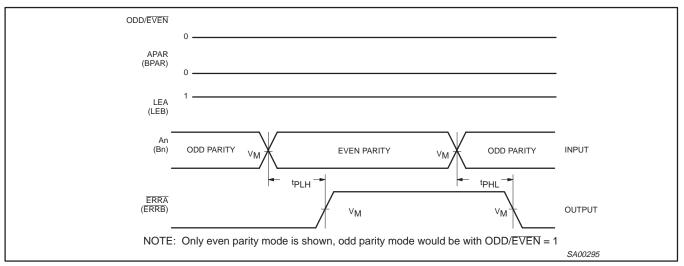
AC WAVEFORMS



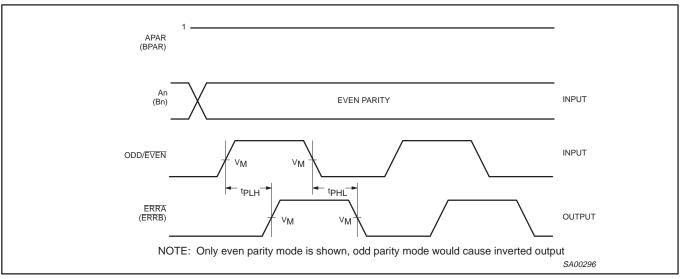
Waveform 1. Propagation Delay, An to Bn, Bn to An, APAR to BPAR, BPAR to APAR



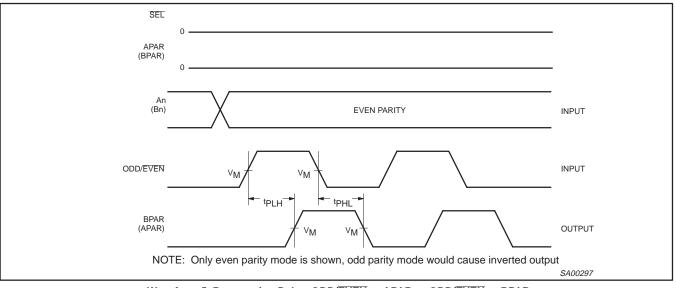
Waveform 2. Propagation Delay, An to BPAR or Bn to APAR



Waveform 3. Propagation Delay, An to ERRA or Bn to ERRB

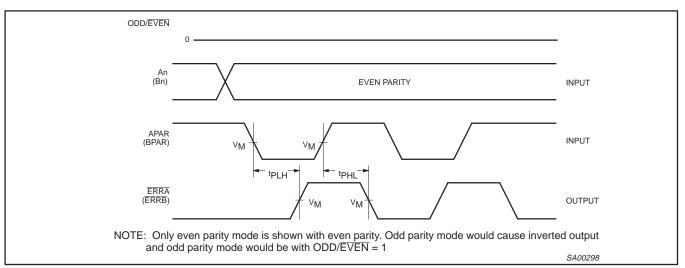


Waveform 4. Propagation Delay, ODD/EVEN to ERRA or ODD/EVEN to ERRB

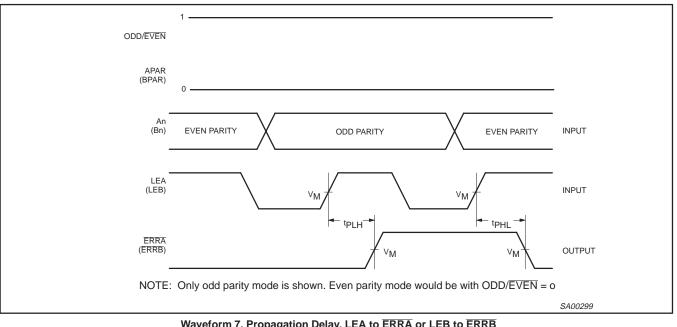


Waveform 5. Propagation Delay, ODD/EVEN to APAR or ODD/EVEN to BPAR

74ABT899

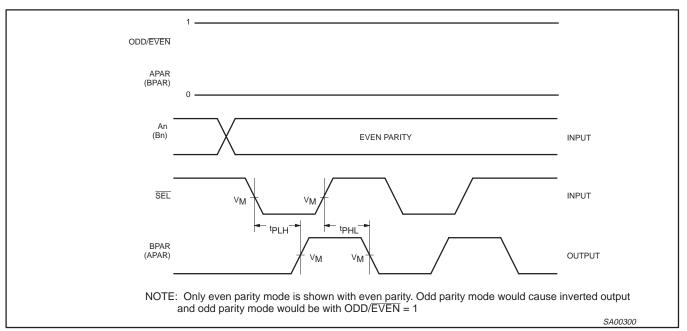


Waveform 6. Propagation Delay, APAR to ERRA or BPAR to ERRB

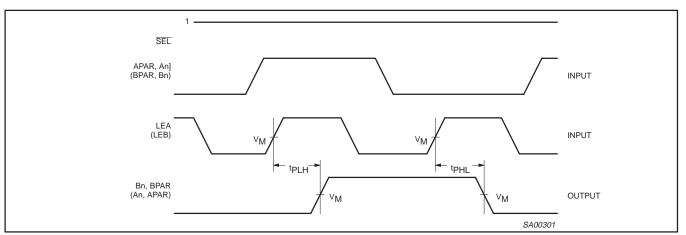


Waveform 7. Propagation Delay, LEA to ERRA or LEB to ERRB

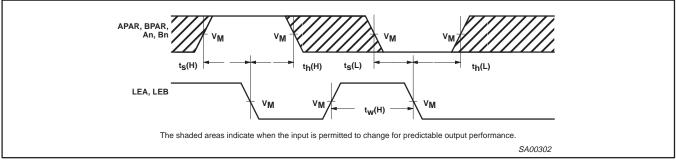
74ABT899



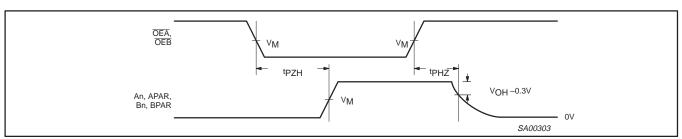
Waveform 8. Propagation Delay, $\overline{\text{SEL}}$ to BPAR or $\overline{\text{SEL}}$ to APAR

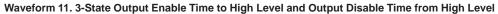


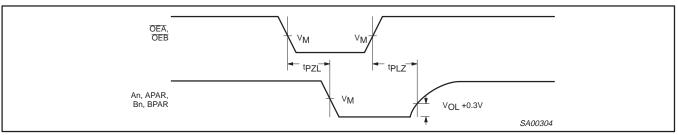
Waveform 9. Propagation Delay, LEA to BPAR or LEB to APAR, LEA to Bn or LEB to An



Waveform 10. Data Setup and Hold Times, Pulse Width High

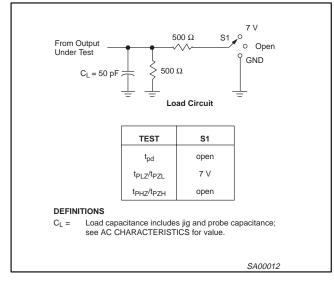




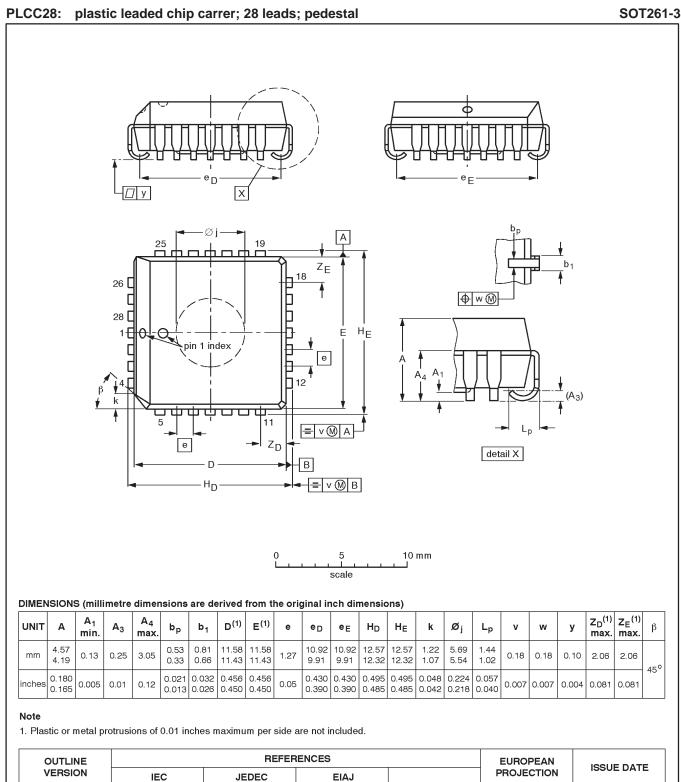


Waveform 12. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM

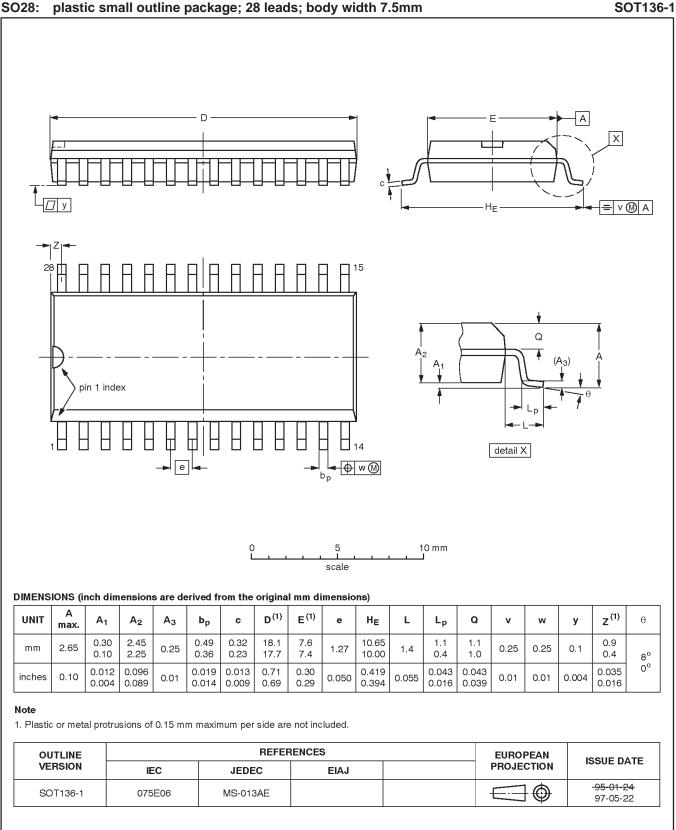


74ABT899



OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT261-3		MO-047AB				95-02-25 97-12-16

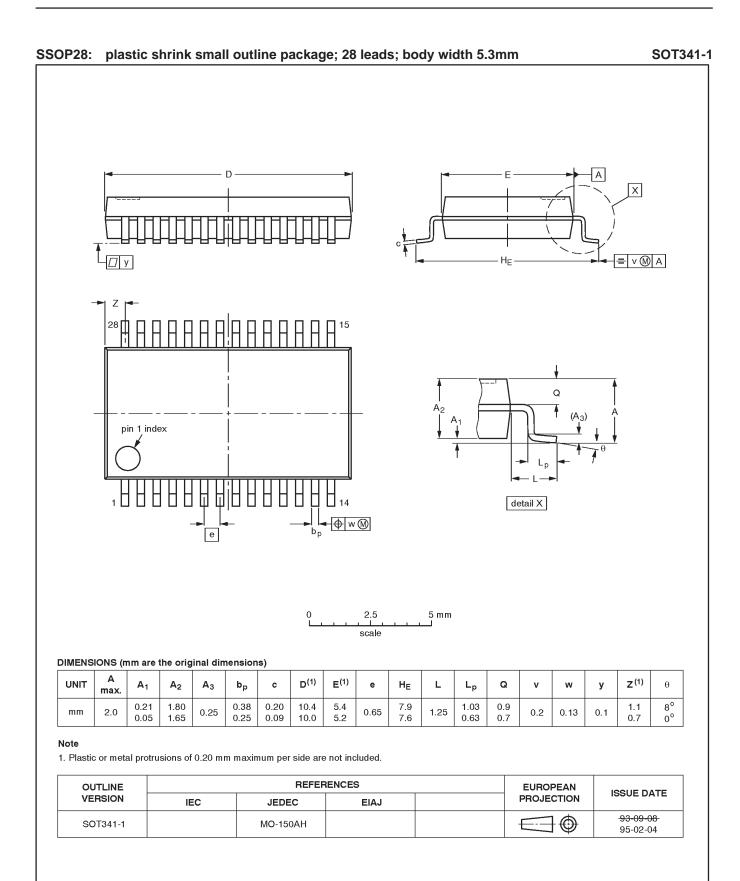
74ABT899



plastic small outline package; 28 leads; body width 7.5mm SO28:

74ABT899

Product specification



Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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