AK2

Request Samples 🕥

Check Inventory

2.50 x 2.0 x 1.0 mm RoHS/RoHS II Compliant MSL Level = N/A

Features

- Based on 3rd Overtone, Quartz Crystal Technology
- Ultra-low rms jitter; < 120fs typical @ 156.25MHz
- Lowest in-class power consumption (15mA max with LVDS)
- ±25ppm max & ±30ppm max stability over -20°C to +70°C and -40°C to +85°C respectively
- 3.3V, 2.5V & 1.8V supply voltage options
- LVPECL, LVDS and HCSL differential output options
- Output enabled (Active High standard default)

Key Electrical Specifications

Applications

- Optical Transceivers
- Optical Modules
- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH
- RF systems, base stations (BTS)
- Datacenter
- PCI Express

Parameters		Min.	Тур.	Max.	Unit	Notes
Frequency Range	100		200	MHz		
Standard Available Frequencies		100.00, 125.00, 148.50, 156.25 & 200.00		MHz	Contact Abracon for availability of frequencies not listed	
Supply Voltage (Vdd) ^[Note 1]		2.97	3.3	3.63		Option "A"
		2.37	2.5	2.62	V	Option "B"
		1.71	1.8	1.89		Option "C"
	LVPECL		30	50		@ 200MHz; @ Vdd=3.3V
Supply Current (Idd)	LVDS		10	15	mA	@ 200MHz; @ Vdd=3.3V
	HCSL		22	30		@ 200MHz; @ Vdd=3.3V
		-20		70	°C	Option "D"
Operating Temperature Range		-40		85	°C	Option "F"
Storage Temperature		-55		150	°C	
Frequency Accuracy (Initial Set-Tolerance, as received stand-alone measured frequency) at time of shipment (Pre-Reflow) $@$ +25°C		-10	<±5	+10	ppm	Relative to carrier frequency
Frequency Shift through Reflow		-2.00		+2.00	ppm	Relative to as received frequency
Frequency Stability over		-25		25		Option "D" (-20°C to +70°C)
Operating Temperature Range ^[Note 2]		-30		30	ppm	Option "F" (-40°C to +85°C)
First Year Aging		-3.00		+3.00	ppm	Maximum first year aging, ±2.00 ppm max. per year thereafter
Aging over 20 Year Product Life Note 3	i]	-15		+15	ppm	
All-Inclusive Frequency Accuracy (To	tal Stability)	-52		52		Option "D" (-20°C to +70°C)
over 20 Year Product Life [Notes 4]	• /	-57		57	ppm	Option "F" (-40°C to +85°C)
	LVPECL		0.3	0.6		@ Vdd=3.3V, RL=50Ω
Rise (Tr) / Fall (Tf) Time 20% to 80% Vpeak to peak	LVDS		0.3	0.5	ns	@ Vdd=3.3V, RL=100Ω
20% to 80% v peak to peak	HCSL		0.3	0.6	1	(a) Vdd=3.3V, RL=50 Ω to GND
Duty Cycle		45		55	%	
Start-up Time		< 2	5	ms		



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Parameters			Min.	Тур.	Max.	Unit	Notes	
	LVPECL	V _{OH}	V _{dd} -1.03		V _{dd} -0.88		D 5004 W 20W	
	LVPECL	Vol	V _{dd} -1.85		V _{dd} -1.60		$R_L=50\Omega$ to $V_{dd}=2.0V$	
Differential	LVDS	VOH		1.40	1.60	V	R = 1000 between both extracts	
Output High Voltage (VOH) Output Low Voltage (VOL)		V _{OL}	0.90	1.10		v	$R_L=100\Omega$ between both outputs	
1 5 ()	HCSL	Voh	0.40	0.74	0.85		$\mathbf{R} = 500$ to around on each output	
	nesl	Vol	-0.15	0.00	0.15		R_L =50 Ω to ground on each output	
			0.50				LVPECL	
Output Voltage Swing			0.250	0.350	0.450	V	LVDS	
			0.50				HCSL	
Output Enable & Disable Control			0.7*(V _{dd})			v	Output Enable or No Connect	
					0.3*(V _{dd})	v	Output Disable (High Impedance)	
Output Enable Time				< 2.00	5.00	ms		
Output Disable Time					0.2	μs		
Output Disable Current Consumption					< 10	μΑ	$OE \leq 0.3V$	
rms phase jitter (12kHz to 20MHz from Carrier)				< 200	500	fs	Vdd, RF output type and Carrier frequency dependent	
				<150	200	fs	@ 156.25MHz	

Note 1: Supply voltage (Vdd) = 1.8V option not available with LVPECL output.

Note 2: Relative to initial measured frequency @ +25°C, pre-reflow.

Note 3: Relative to post-reflow frequency.

Note 4: Includes post reflow frequency accuracy, temperature stability, load pulling, power supply variation, and 20-year aging.



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Phase Noise Test Setup

- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = Not omitted (Normalized in dBc/Hz)
- Specifed Spur Omission Function = Not enabled
- IF Gain = 20dB
- Correlation = 5
- Average = 3

Typical Values measured at 25°C ± 3°

Frequency	v (MHz)	100.00MHz								156.25MHz	
V _{DI})	1.8	3V		2.5V			3.3V		1.8V	2.5V
RF Ou	tput	LVDS	HCSL	LVDS	HCSL	LVPECL	LVDS	HCSL	LVPECL	LV	DS
rms Ph Jitter (1 12kHz-	fsec)	385.27	147.12	207.96	117.86	131.63	255.13	195.68	123.73	139.49	107.18
Phase	100Hz	-104.49	-86.91	-80.88	-75.50	-99.17	-87.89	-105.15	-102.40	-93.43	-93.21
Noise (dB _C /H _Z)	1KHz	-125.64	-120.54	-115.99	-115.89	-129.38	-120.80	-132.38	-132.55	-123.45	-125.31
(/	10KHz	-134.97	-144.63	-140.15	-147.34	-145.94	-143.61	-144.58	-146.61	-136.98	-139.61
	100KHz	-140.45	-152.42	-149.52	-457.05	-153.02	-146.87	-150.96	-152.79	-140.93	-149.12
	1MHz	-147.69	-155.94	-153.49	-153.53	-156.87	-148.30	-150.70	-156.98	-150.53	-154.70
	10MHz	-149.67	-157.06	-153.53	-159.42	-157.87	-153.04	-154.78	-158.59	-155.31	-156.40

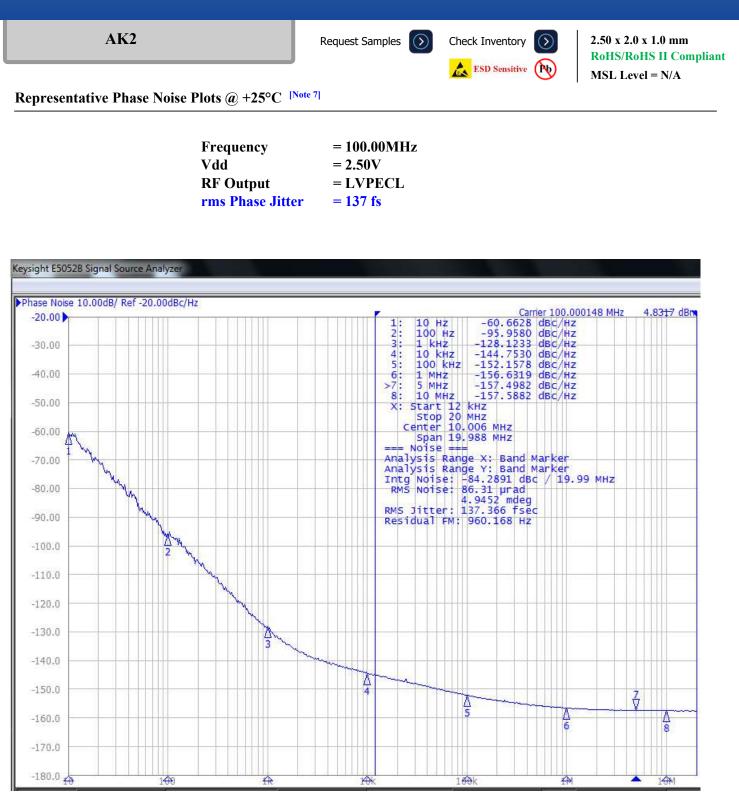
Note 5: Guaranteed by characterization; rms Phase Jitter specifications are inclusive of any spurs

Note 6: Phase jitter measured with Keysight E5052B Signal Source Analyzer at 25°C±3°C



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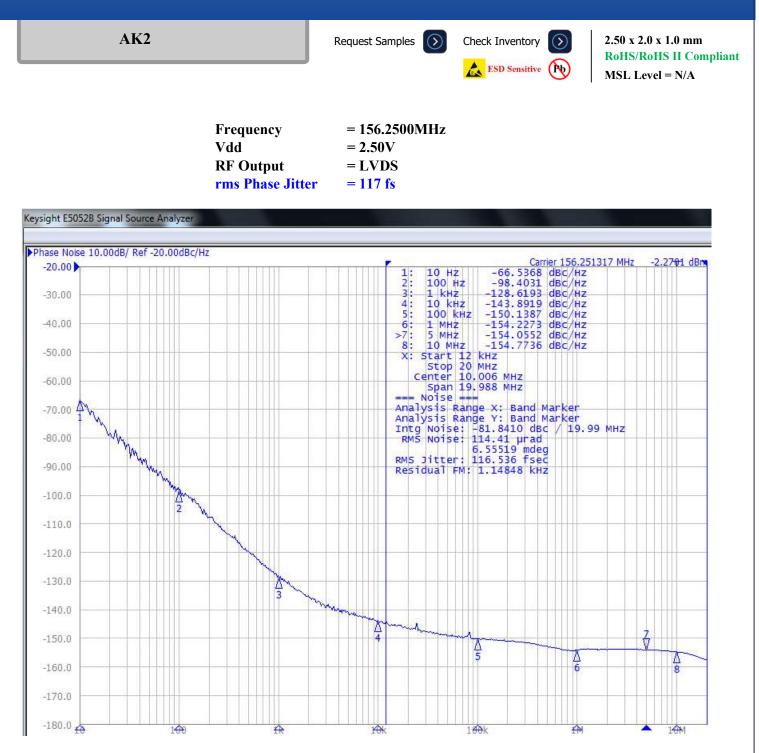
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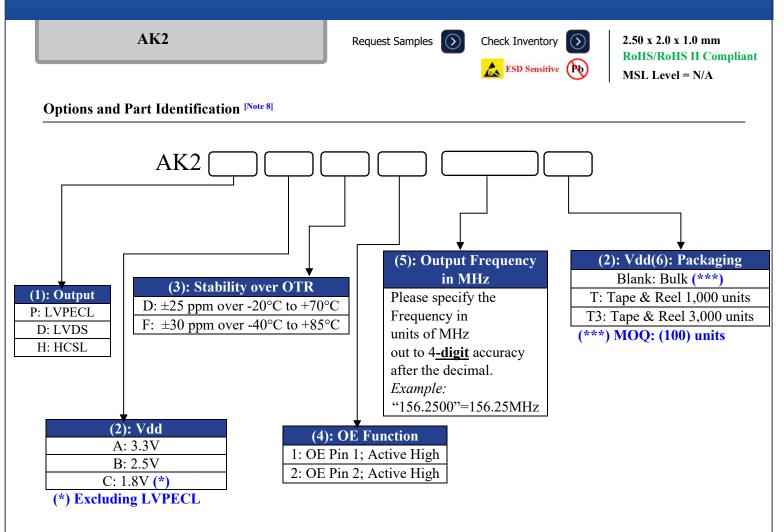


Note 7: Contact Abracon for phase noise plots at alternative supply voltage (V_{dd}) & differential output formats



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Part Number Example

- AK2PAF1-156.2500 [(100) units in Bulk]
- AK2PAF1-156.2500T [(1k) units on Tape & Reel]
- AK2PAF1-156.2500T3 [(3k) units on Tape & Reel]

Note 8: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal



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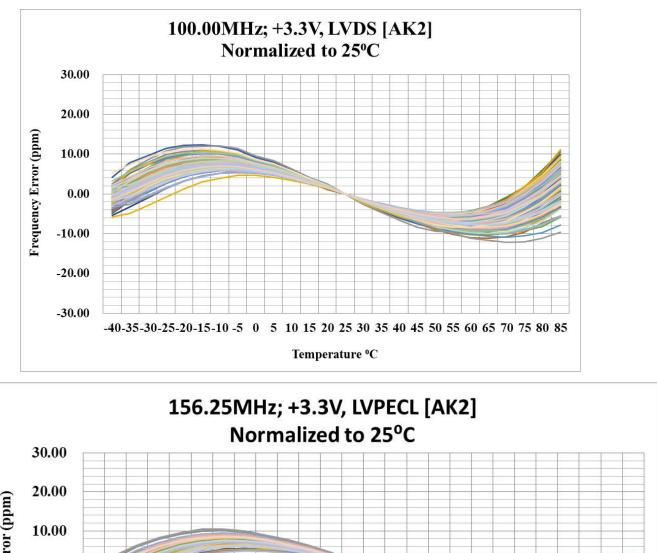
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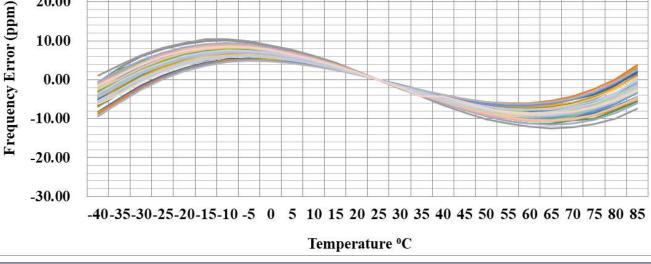
Check Inventory 🚫

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Typical Frequency vs. Temperature Characteristics

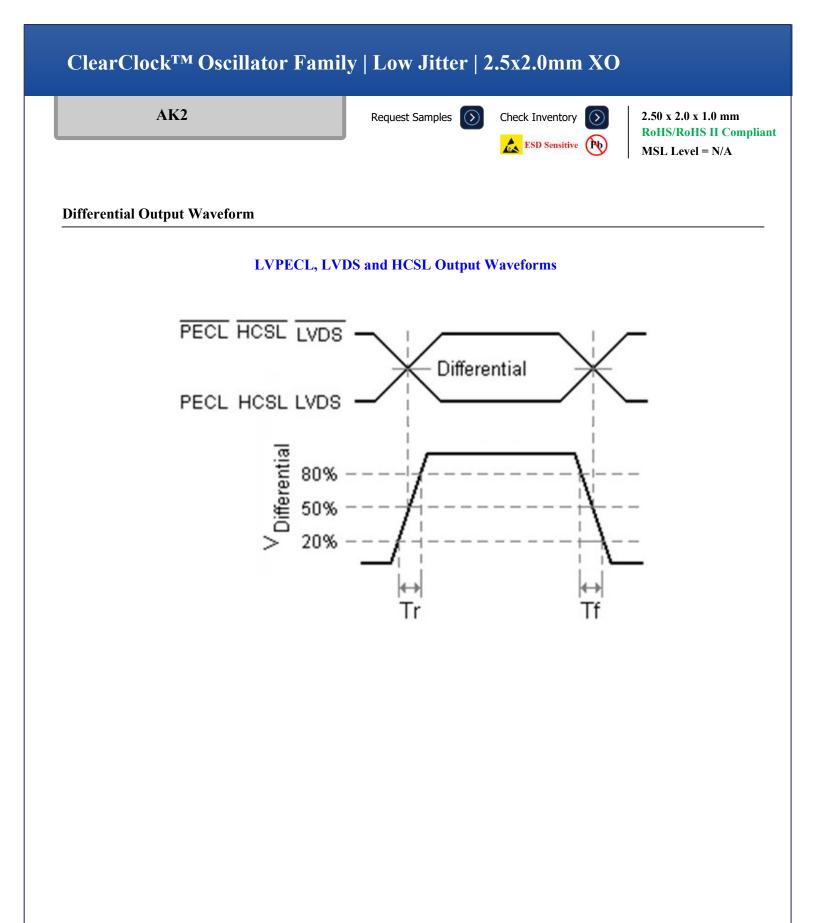
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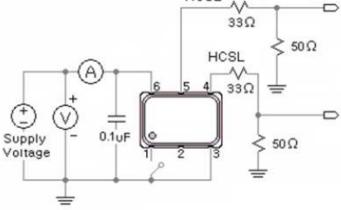




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ClearClockTM Oscillator Family | Low Jitter | 2.5x2.0mm XO AK2 Request Samples 🕥 Check Inventory 2.50 x 2.0 x 1.0 mm (\mathbf{b}) **RoHS/RoHS II Compliant** ESD Sensitive (Pb) MSL Level = N/A Recommended Test Circuit [Note 9] LVPECL LVDS Vai 0 < R1 LVDS PECL 100Ω Vat 5 4 R2 PECL 6 R3 0.1uF Supply 0.1uF Supply Voltage Voltage R4 < Vdd= 3.3V: R1=R3=127Ω; R2=R4=82.5Ω Vdd= 2.5V: R1=R3=250Ω; R2=R4=62.5Ω HCSL HCSL

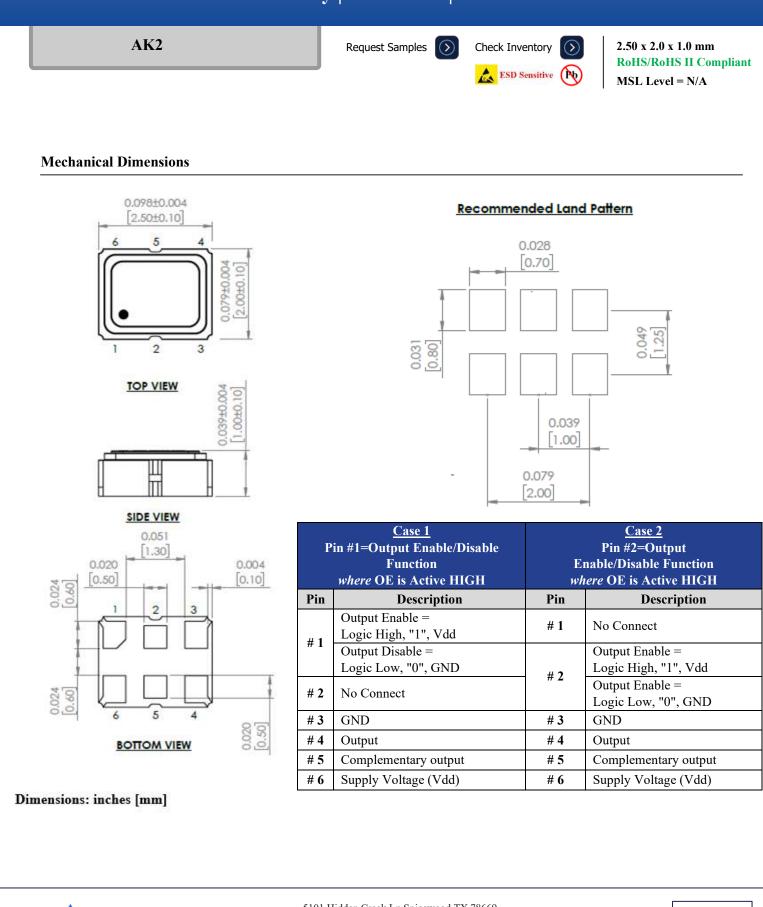


Note 9: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.



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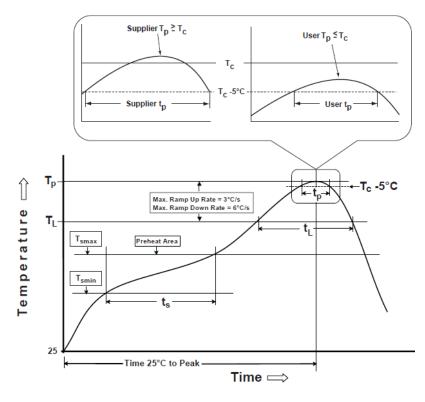


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2.50 x 2.0 x 1.0 mm RoHS/RoHS II Compliant MSL Level = N/A

Reflow Profile [JEDEC J-STD-020]



SnPb Eutectic Process Classification Temperatures (T _c)				
Package Thickness	Volume mm ³ <350	Volume mm ³ <u>></u> 350		
<2.5 mm	235 °C	220 °C		
>2.5 mm	220 °C	220 °C		

Classification Temperatures (T_c)

		• •	
Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T _{smin})	100°C	150°C
Temperature maximum (T _{smax})	150°C	200°C
Time (T _{smin} to T _{smax}) (t _s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T _{smax} to T _P)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T _L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T _P)*	see Table 1	see Table 2
Time $(t_p)^{**}$ within 5°C of the specified classification temperature (T_c)	20 sec.	30 sec.
Ramp-down rate (T _p to T _{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

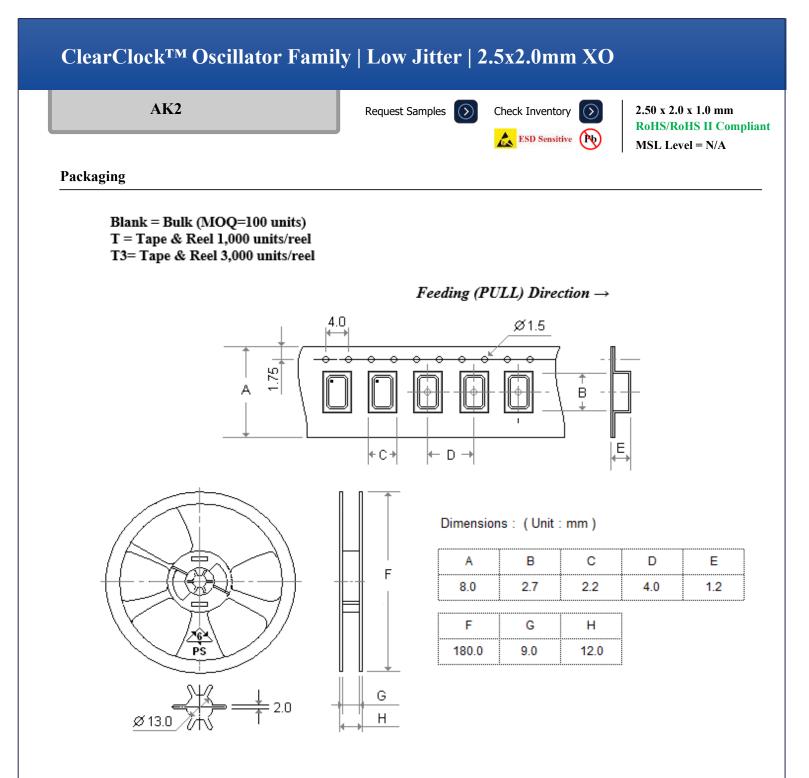
*Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature $\left(t_{p}\right)$ is defined as supplier minimum and a user maximum.



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- (10) sprocket hold pitch cumulative tolerance is ±0.10 mm
- "E" measured from a place on the inside bottom of the pocket to the top surface of the carrier

Dimensions: mm

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