Features

July 2011

- Meets jitter requirements of Telcordia GR-253-CORE for OC-192, OC-48, OC-12, and OC-3 rates
- Meets jitter requirements of ITU-T G.813 for STM-64, STM-16, STM-4 and STM-1 rates
- Provides four LVPECL differential output clocks at 622.08 MHz
- Provides a CML differential clock at 155.52 MHz
- Provides a single-ended CMOS clock at 19.44 MHz
- Lock Indicator
- Provides enable/disable control of output clocks
- Accepts a CMOS reference at 19.44 MHz
- 3.3 V supply

Applications

- SONET/SDH line cards
- Network Element timing cards

Ordering Information		
ZL30414QGG1	64 Pin TQFP*	Trays, Bake & Drypack
*Pb Free Matte Tin		
-40°C to +85°C		

Description

The ZL30414 is an analog phase-locked loop (APLL) designed to provide jitter attenuation and rate conversion for SDH (Synchronous Digital Hierarchy) and SONET (Synchronous Optical Network) networking equipment. The ZL30414 generates very low jitter clocks that meet the jitter requirements of Telcordia GR-253-CORE OC-192, OC-48, OC-12, OC-3 rates and ITU-T G.813 STM-64, STM-16, STM-4 and STM-1 rates.

The ZL30414 accepts a CMOS compatible reference at 19.44 MHz and generates four LVPECL differential output clocks at 622.08 MHz, a CML differential clock at 155.52 MHz and a single-ended CMOS clock at 19.44 MHz. The output clocks can be individually enabled or disabled. The ZL30414 provides a LOCK indication.

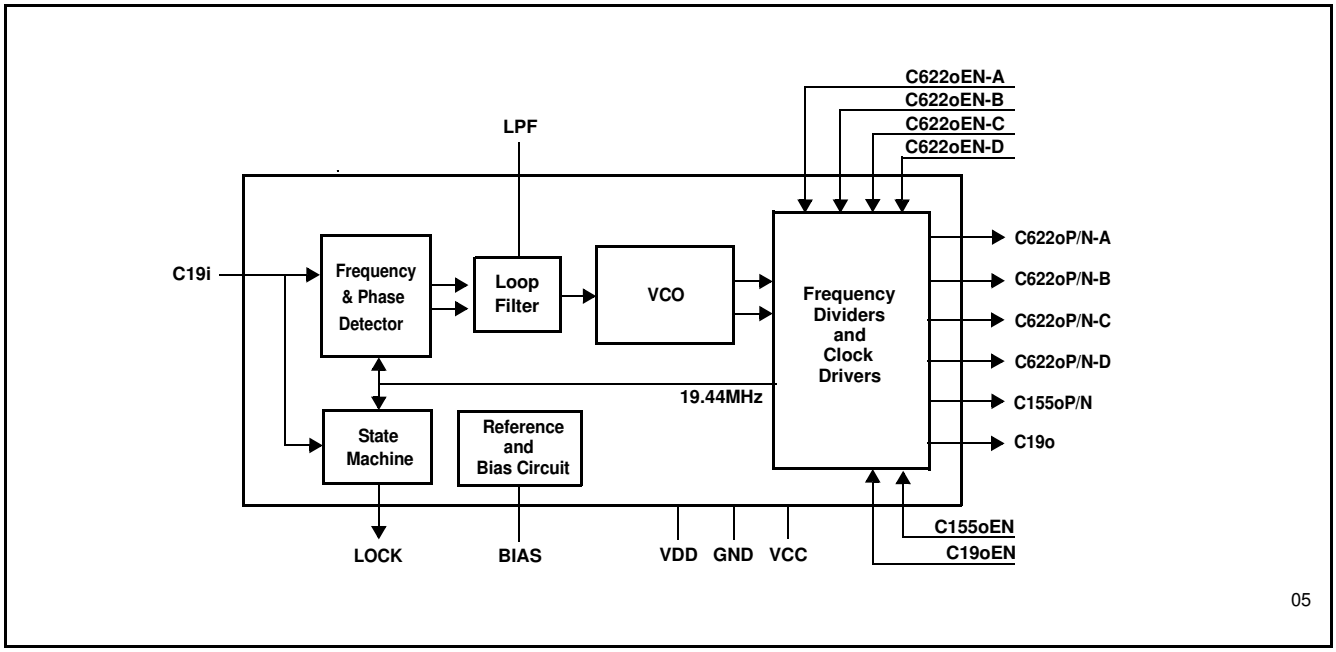


Figure 1 - Functional Block Diagram

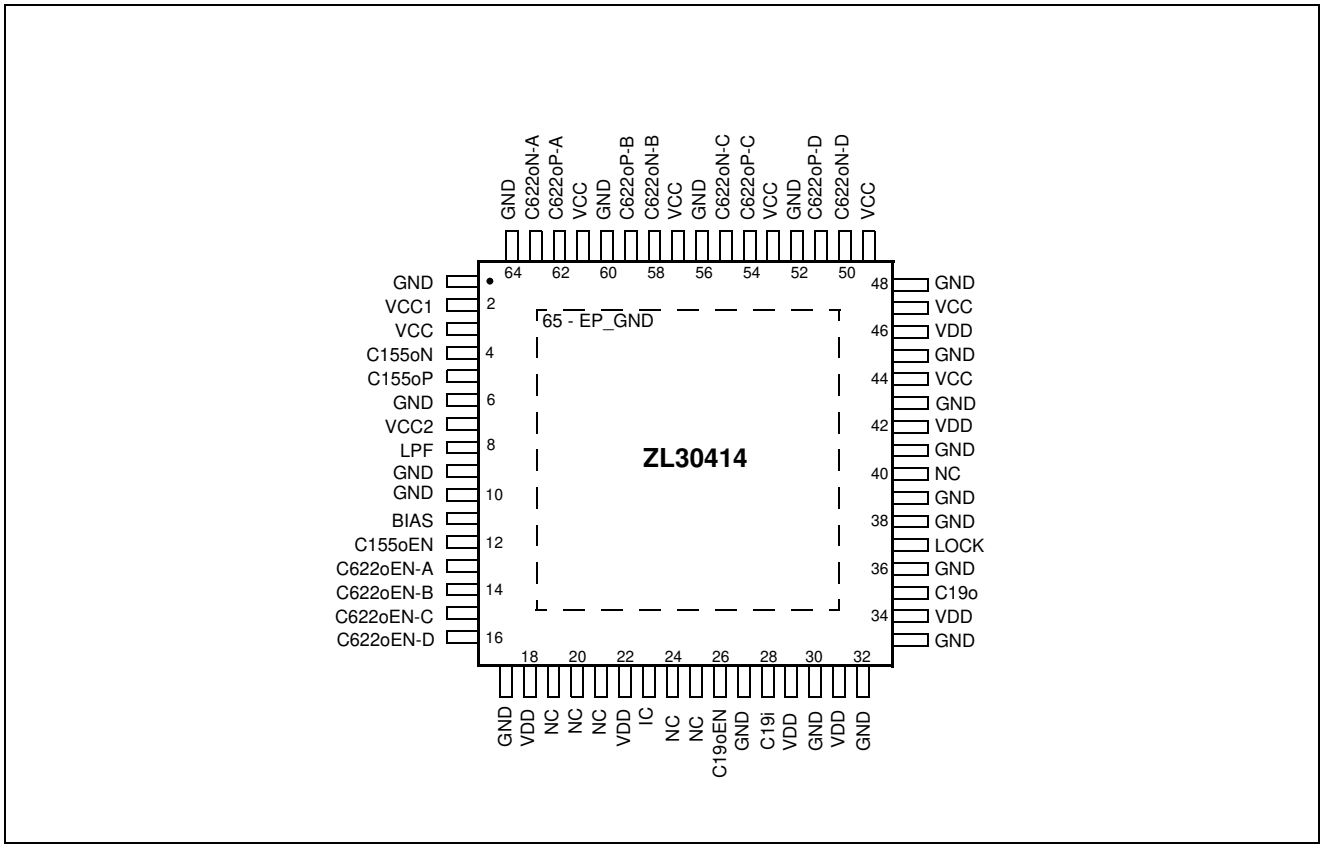


Figure 2 - TQFP 64 pin (Top View)

1.0 Change Summary

Changes from March 2006 Issue to July 2011 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Ordering Information	The ZL30414QGC has been obsoleted and replaced by the ZL30414QGG1.

Changes from February 2005 Issue to March 2006 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1		Updated Ordering Information

Pin Description

Pin #	Name	Description
1	GND	**Ground.** 0 volt
2	VCC1	**Positive Analog Power Supply.** +3.3 V ±10%.
3	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.
4 5	C155oN C155oP	**C155 Clock Output (CML).** These outputs provide a differential 155.52 MHz clock.
6	GND	**Ground.** 0 volt
7	VCC2	**Positive Analog Power Supply.** +3.3 V ±10%
8	LPF	**Low Pass Filter (Analog).** Connect to this pin external RC network (R_F and C_F) for the low pass filter.
9	GND	**Ground.** 0 volt
10	GND	**Ground.** 0 volt
11	BIAS	**Bias.** See Figure 13 for the recommended bias circuit.
12	C155oEN	**C155o Clock Enable (CMOS Input).** If tied high this control pin enables the C155oP/N differential driver. Pulling this input low disables the output clock and deactivates differential drivers.
13	C622oEN-A	**C622 Clock Output Enable A (CMOS Input).** If tied high this control pin enables the C622oP/N-A output clock. Pulling this input low disables the output clock without deactivating differential drivers.
14	C622oEN-B	**C622 Clock Output Enable B (CMOS Input).** If tied high this control pin enables the C622oP/N-B output clock. Pulling this input low disables the output clock without deactivating differential drivers.
15	C622oEN-C	**C622 Clock Output Enable C (CMOS Input).** If tied high this control pin enables the C622oP/N-C output clock.Pulling this input low disables the output clock without deactivating differential drivers.
16	C622oEN-D	**C622 Clock Output Enable D (CMOS Input).** If tied high this control pin enables the C622oP/N-D output clock.Pulling this input low disables the output clock without deactivating differential drivers.
17	GND	**Ground.** 0 volt
18	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
19	NC	**No internal bonding Connection.** Leave unconnected.
20	NC	**No internal bonding Connection.** Leave unconnected.
21	NC	**No internal bonding Connection.** Leave unconnected.

Pin #	Name	Description
22	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
23	IC	**Internal Connection.** Connect this pin to Ground (GND).
24	NC	**No internal bonding Connection.** Leave unconnected.
25	NC	**No internal bonding Connection.** Leave unconnected.
26	C19oEN	**C19o Output Enable (CMOS Input).** If tied high this control pin enables the C19o output clock. Pulling this pin low forces output driver into a high impedance state.
27	GND	**Ground.** 0 volt
28	C19i	**C19 Reference Input (CMOS Input).** This pin is a single-ended input reference source used for synchronization. This pin accepts 19.44 MHz.
29	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
30	GND	**Ground.** 0 volt
31	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
32	GND	**Ground.** 0 volt
33	GND	**Ground.** 0 volt
34	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
35	C19o	**C19 Clock Output (CMOS Output).** This pin provides a single-ended CMOS clock at 19.44 MHz.
36	GND	**Ground.** 0 volt
37	LOCK	**Lock Indicator (CMOS Output).** This output goes high when PLL is frequency locked to the input reference C19i.
38	GND	**Ground.** 0 volt
39	GND	**Ground.** 0 volt
40	NC	**No internal bonding Connection.** Leave unconnected.
41	GND	**Ground.** 0 volt
42	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
43	GND	**Ground.** 0 volt
44	VCC	**Positive Analog Power Supply.** +3.3 V ±10%
45	GND	**Ground.** 0 volt

Pin #	Name	Description
46	VDD	**Positive Digital Power Supply.** +3.3 V ±10%
47	VCC	**Positive Analog Power Supply.** +3.3 V ±10%
48	GND	**Ground.** 0 volt
49	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.
50 51	C622oN-D C622oP-D	**C622 Clock Output (LVPECL)**. These outputs provide a differential LVPECL clock at 622.08 MHz. Unused LVPECL port should be left unterminated to decrease supply current.
52	GND	**Ground.** 0 volt
53	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.
54 55	C622oP-C C622oN-C	**C622 Clock Output (LVPECL)**. These outputs provide a differential LVPECL clock at 622.08 MHz. Unused LVPECL port should be left unterminated to decrease supply current.
56	GND	**Ground.** 0 volt
57	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.
58 59	C622oN-B C622oP-B	**C622 Clock Output (LVPECL)**. These outputs provide a differential LVPECL clock at 622.08 MHz. Unused LVPECL port should be left unterminated to decrease supply current.
60	GND	**Ground.** 0 volt
61	VCC	**Positive Analog Power Supply.** +3.3 V ±10%.
62 63	C622oP-A C622oN-A	**C622 Clock Output (LVPECL)**. These outputs provide a differential LVPECL clock at 622.08 MHz. Unused LVPECL port should be left unterminated to decrease supply current.
64	GND	**Ground.** 0 volt
65	NC	No internal bonding Connection. Leave unconnected.

2.0 Functional Description

The ZL30414 is an analog phased-locked loop which provides rate conversion and jitter attenuation for SONET/SDH OC-192/STM-64, OC-48/STM-16, OC-12/STM-4 and OC-3/STM-1 applications. A functional block diagram of the ZL30414 is shown in Figure 1 and a brief description is presented in the following sections.

2.1 Frequency/Phase Detector

The Frequency/Phase Detector compares the frequency/phase of the input reference signal with the feedback signal from the Frequency Divider circuit and provides an error signal corresponding to the frequency/phase difference between the two. This error signal is passed to the Loop Filter circuit.

2.2 Lock Indicator

The ZL30414 has a built-in LOCK detector that measures frequency difference between input reference clock C19i and the VCO frequency. When the VCO frequency is less than ±300 ppm apart from the input reference frequency then the LOCK pin is set high. The LOCK pin is pulled low if the frequency difference exceeds ±1000 ppm.

2.3 Loop Filter

The Loop Filter is a low pass filter. This low pass filter ensures that the network jitter requirements are met for an input reference frequency of 19.44 MHz. The corner frequency of the Loop Filter is configurable with an external capacitor and resistor connected to the LPF pin and ground as shown in Figure 3.

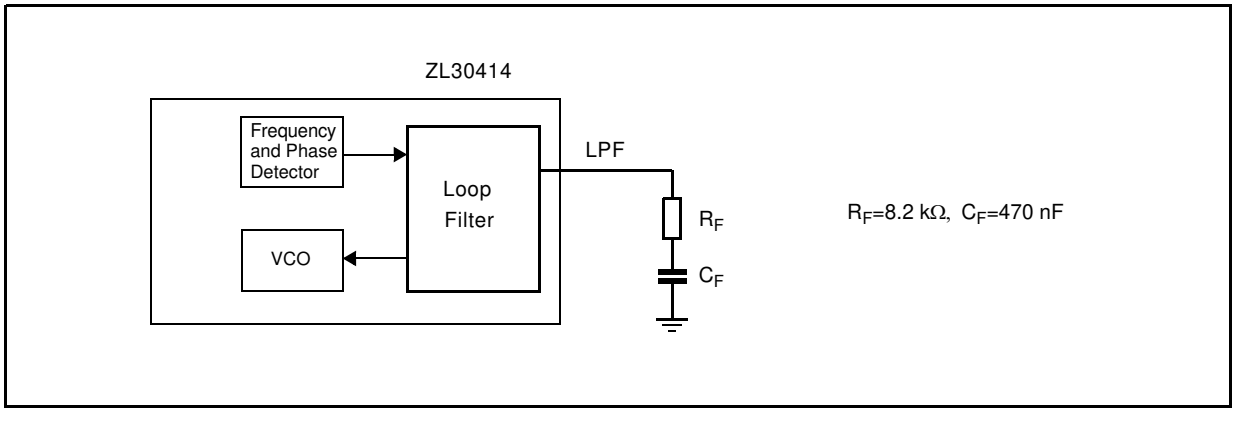


Figure 3 - Loop Filter Elements

2.4 VCO

The voltage-controlled oscillator (VCO) receives the filtered error signal from the Loop Filter, and based on the voltage of the error signal generates a primary frequency. The VCO output is connected to the "Frequency Dividers and Clock Drivers" block that divides VCO frequency and buffer generated clocks.

2.5 Output Interface Circuit

The output of the VCO is used by the Output Interface Circuit to provide four LVPECL differential clocks at 622.08 MHz, one CML differential clock at 155.52 MHz and a single-ended 19.44 MHz output clock. This block provides also a 19.44 MHz feedback clock that closes PLL loop. Each output clock can be enabled or disabled individually with the associated Output Enable pin.

Output Clocks	Output Enable Pins
C622oP/N-A	C622oEN-A
C622oP/N-B	C622oEN-B
C622oP/N-C	C622oEN-C
C622oP/N-D	C622oEN-D
C155oP/N	C155oEN
C19o	C19oEN

Table 1 - Output Enable Control

To reduce power consumption and achieve the lowest possible intrinsic jitter the unused output clocks must be disabled. If any of the LVPECL outputs are disabled they must be left open without any terminations.

3.0 ZL30414 Performance

The following are some of the ZL30414 performance indicators that complement results listed in the Characteristics section of this data sheet.

3.1 Input Jitter Tolerance

Jitter tolerance is a measure of the PLL's ability to operate properly (i.e., remain in lock and/or regain lock in the presence of large jitter magnitudes at various jitter frequencies) when jitter is applied to its input reference. The input jitter tolerance of the ZL30414 is shown in Figure 4. On this graph, the single line at the top represents measured input jitter tolerance and the three overlapping lines below represent minimum input jitter tolerance for OC-192, OC-48, and OC-12 network interfaces. The jitter tolerance is expressed in picoseconds (pk-pk) to accommodate requirements for interfaces operating at different rates.

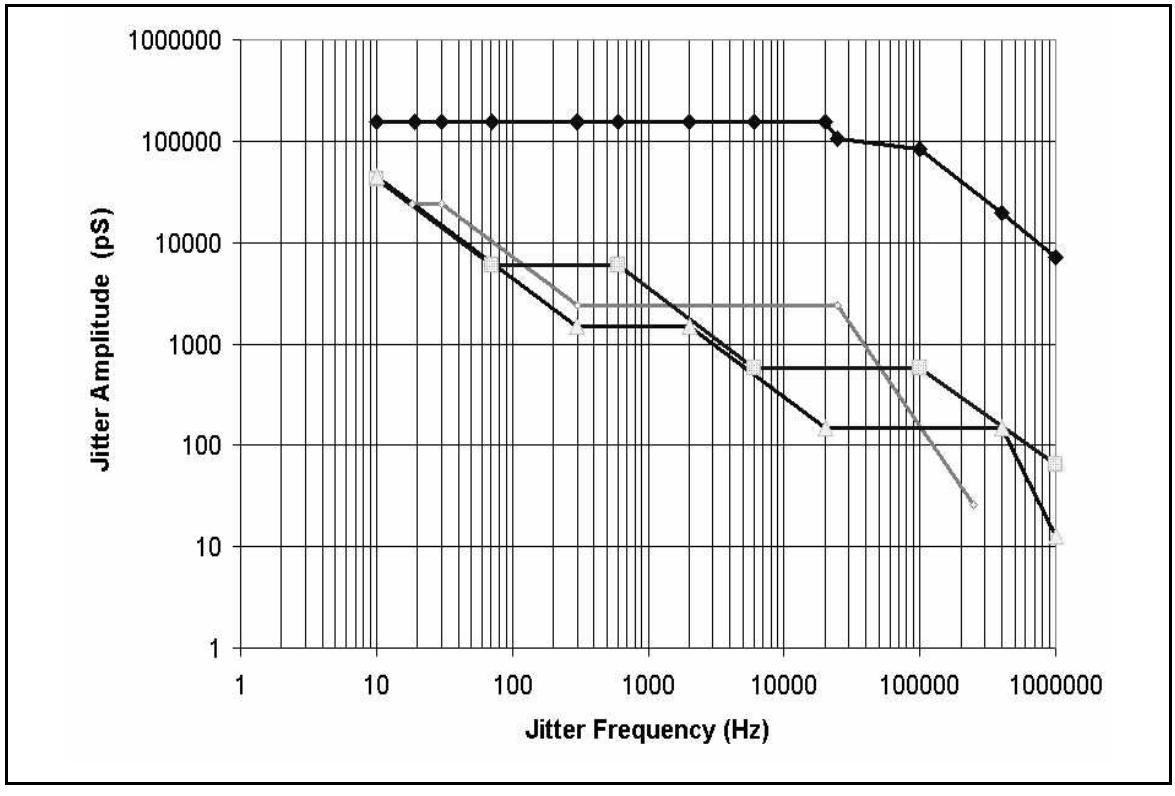


Figure 4 - Input Jitter Tolerance

3.2 Jitter Transfer Characteristic

Jitter Transfer Characteristic represents a ratio of the jitter at the output of a PLL to the jitter applied to the input of a PLL. This ratio is expressed in dB and it characterizes the PLLs ability to attenuate (filter) jitter. The jitter transfer characteristic for the ZL30414 configured with recommended loop filter components (R_F=8.2 kΩ, C_F=470 nF) is shown in Figure 5. The plotted curves represent jitter transfer characteristics over the recommended voltage (3.0 V to 3.6 V) and temperature (-40C to 85C) ranges.

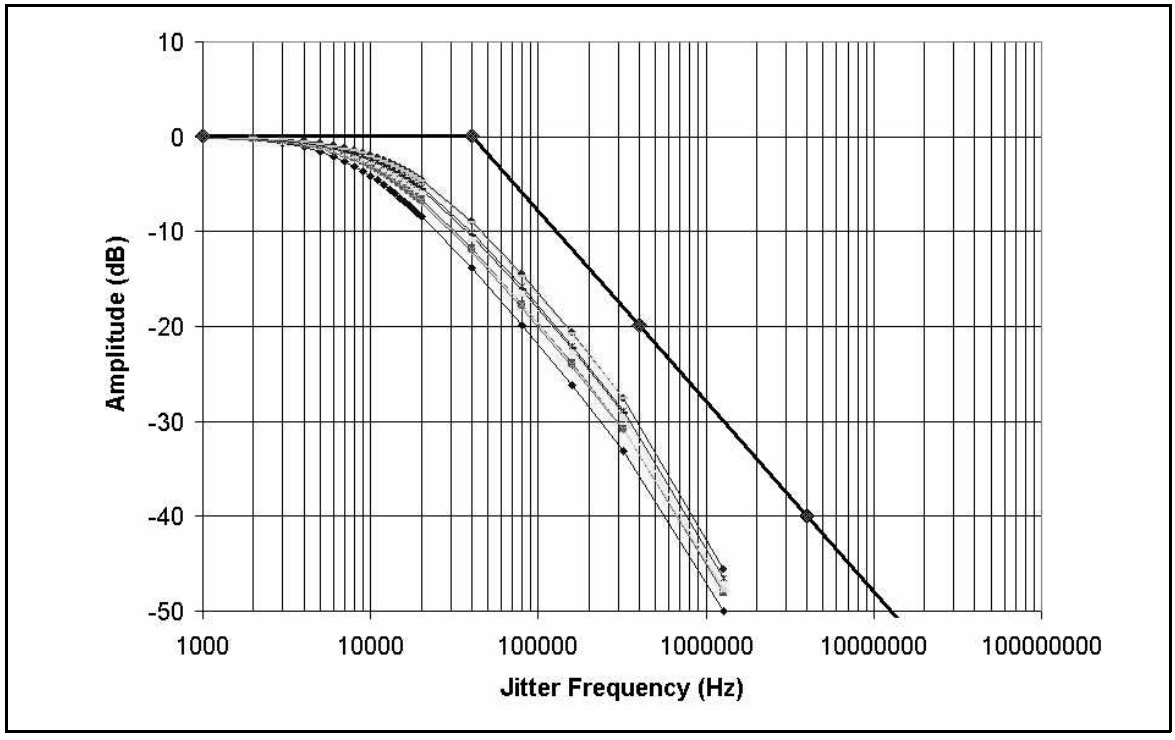


Figure 5 - Jitter Transfer Characteristic

4.0 Applications

4.1 Ultra-Low Jitter SONET/SDH Equipment Clocks

The ZL30414 functionality and performance complements the entire family of the Zarlink's advanced network synchronization PLLs. Its superior jitter filtering characteristics exceed requirements of SONET/SDH optical interfaces operating up to OC-192/STM-64 rate (10 Gbit/s). The ZL30414 in combination with the MT90401 or the ZL30407 (SONET/SDH Network Element PLLs) provides the core building blocks for high quality equipment clocks suitable for network synchronization (see Figure 6) .

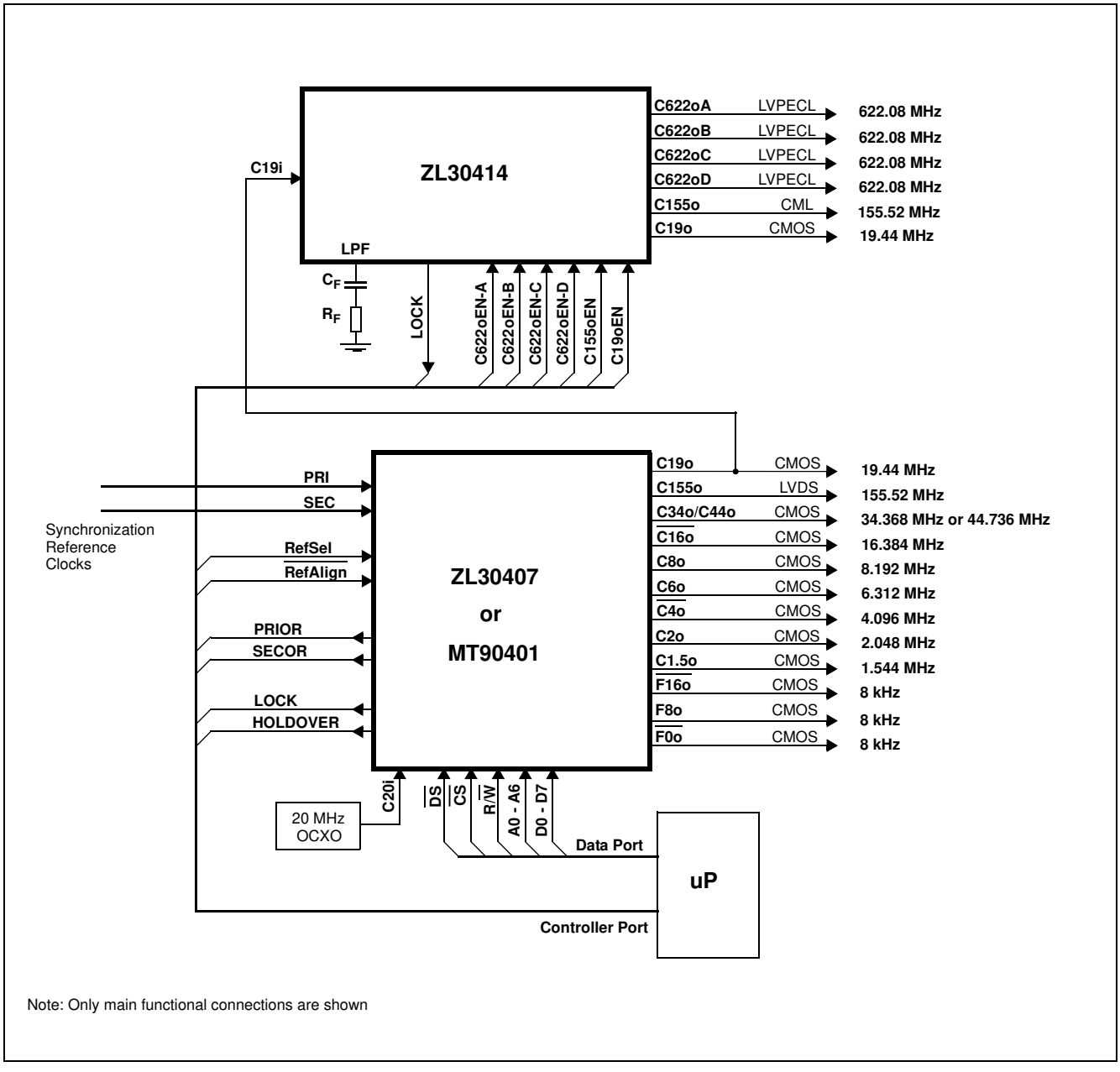


Figure 6 - SONET/SDH Equipment Clock

The ZL30414 in combination with the MT9046 provides an optimum solution for SONET/SDH line cards (see Figure 7).

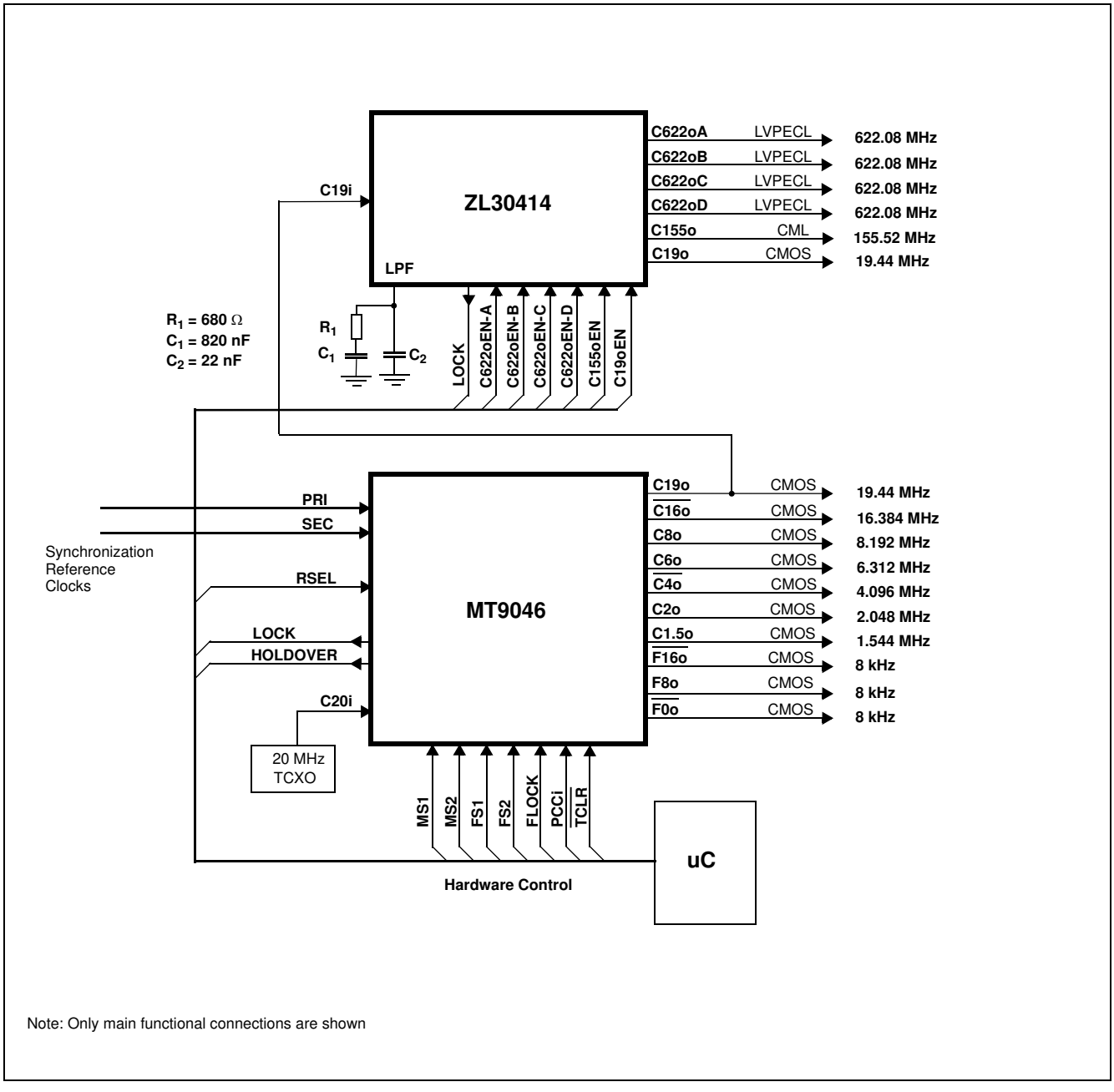


Figure 7 - SONET/SDH Line Card

4.2 Recommended Interface Circuit

4.2.1 LVPECL to LVPECL Interface

The C622oP/N-A, C622oP/N-B, C622oP/N-B, and C622oP/N-D outputs provide differential LVPECL clocks at 622.08 MHz. The LVPECL output drivers require a 50 Ω termination connected to the Vcc-2V source for each output terminal at the terminating end as shown below. The terminating resistors should be placed as close as possible to the LVPECL receiver.

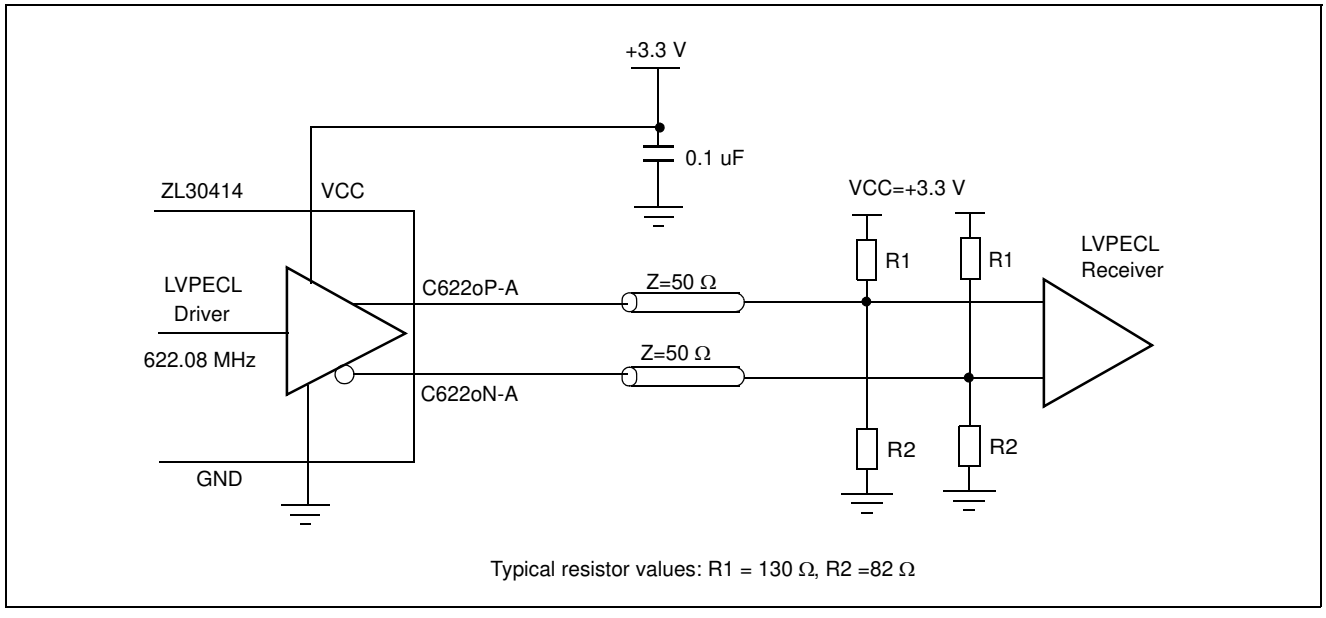


Figure 8 - LVPECL to LVPECL Interface

4.2.2 CML to CML Interface

The C155o output provides a differential CML/LVDS compatible clock at 155.52 MHz. The output drivers require a 50 Ω load at the terminating end if the receiver is CML type.

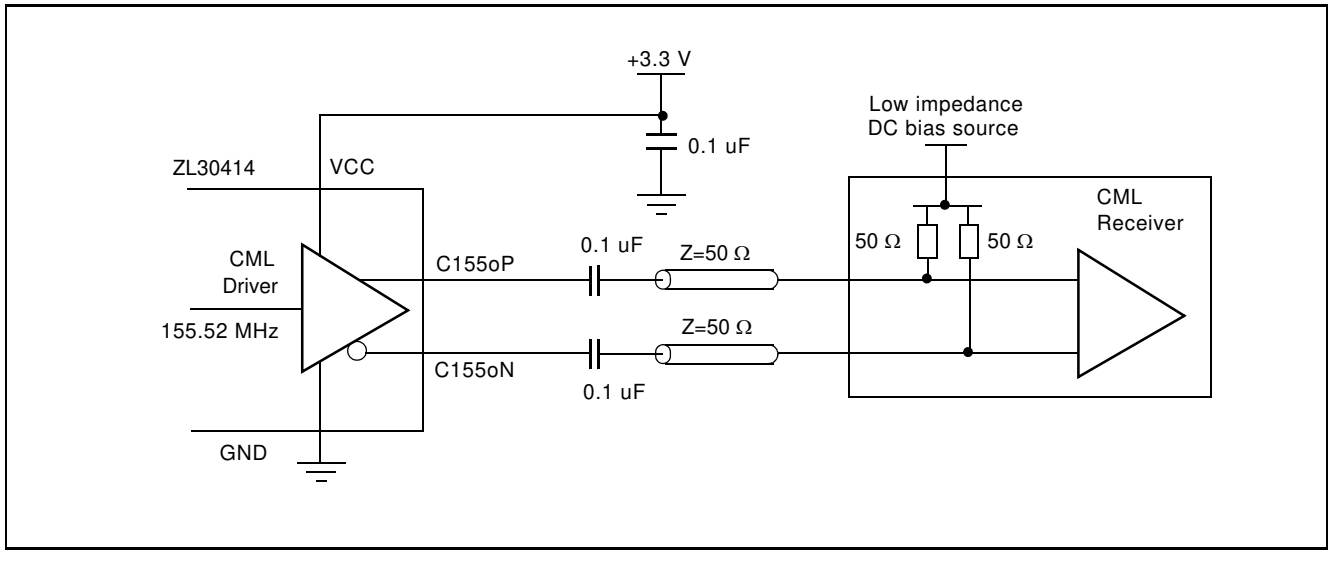


Figure 9 - CML to CML Interface

4.2.3 CML to LVDS Interface

To configure the driver as an LVDS driver, external biasing resistors are required to set up the common mode voltage as specified by ANSI/TIA/EIA-644 LVDS standard. The standard specifies the V_{CM} (common mode voltage) as minimum 1.125 V, typical 1.2 V, and maximum 1.375 V. The following figure provides a recommendation for LVDS applications.

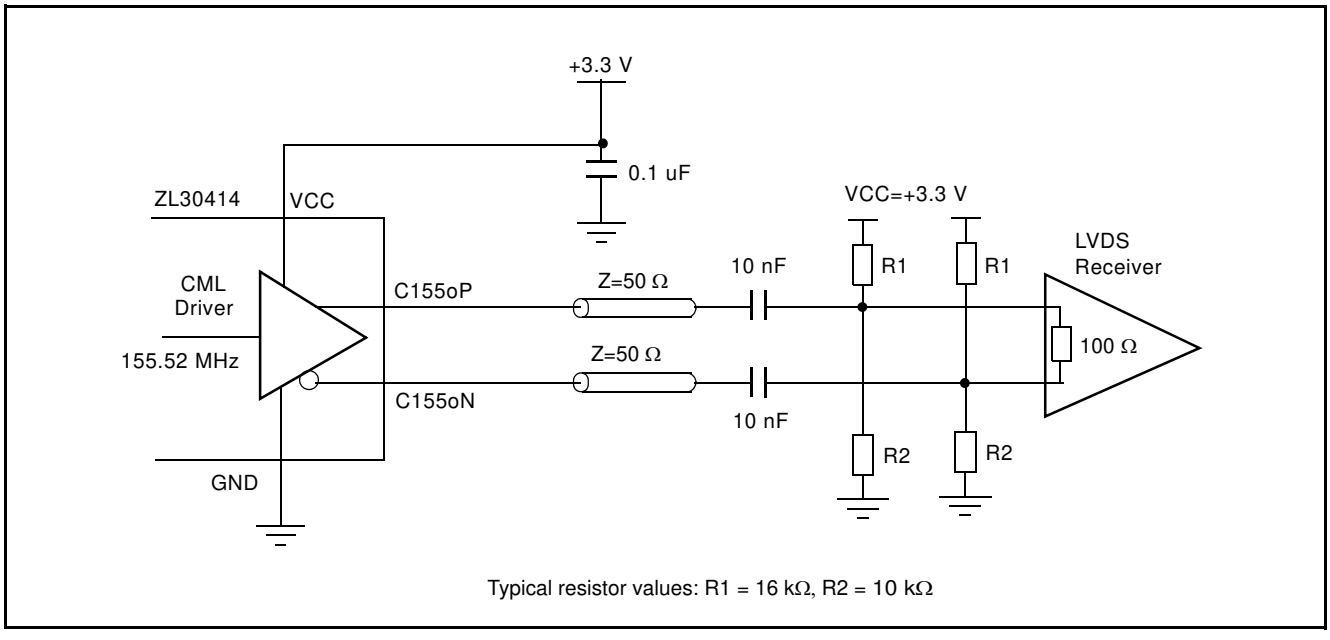


Figure 10 - LVDS Termination

4.2.4 CML to LVPECL Interface

The CML output can drive LVPECL input as is shown in Figure 11. The terminating resistors should be placed as close as possible to the LVPECL receiver.

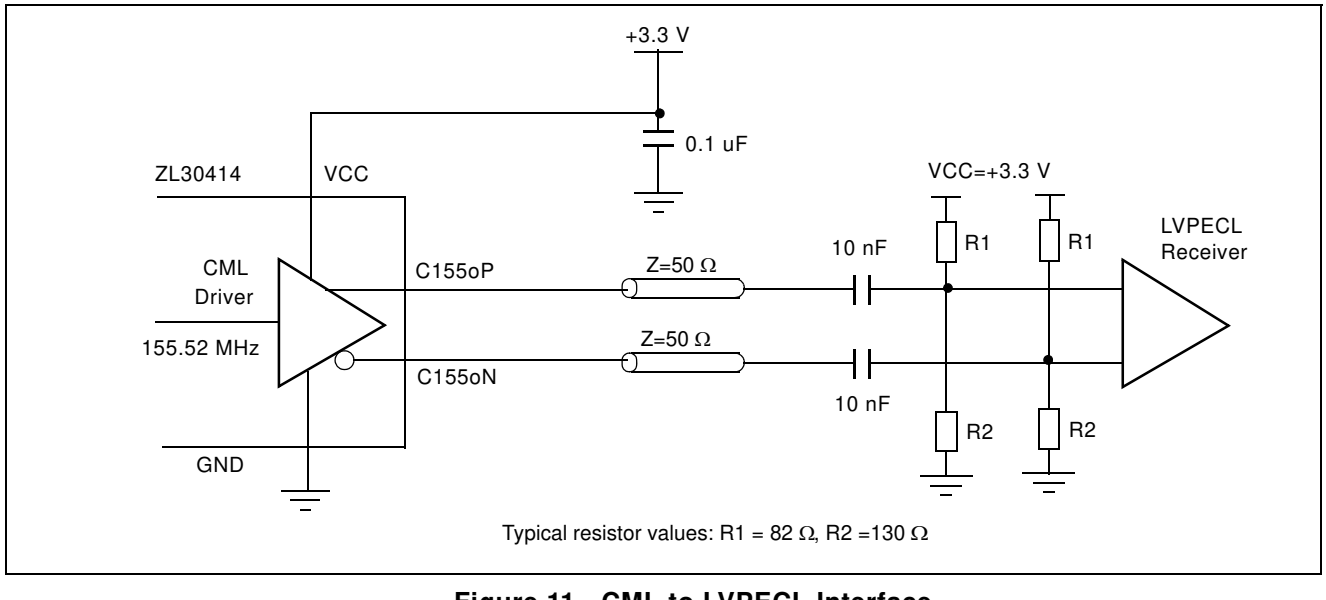


Figure 11 - CML to LVPECL Interface

4.3 Tristating LVPECL Outputs

The ZL30414 has four differential 622.08 MHz LVPECL outputs, which can be used to drive four different OC-3/OC-12/OC-48/OC-192 devices such as framers, mappers and SERDES. In the case where fewer than four clocks are required, a user can disable unused LVPECL outputs on the ZL30414 by pulling the corresponding enable pins low. When disabled, voltage at the both pins of the differential LVPECL output will be pulled up to Vcc - 0.7 V.

For applications requiring the LVPECL outputs to be in a tri-state mode, external AC coupling can be used as shown in Figure 12. Typically this might be required in hot swappable applications.

Resistors R1 and R2 are required for DC bias of the LVPECL driver. Capacitors C1 and C2 are used as AC coupling capacitors. During disable mode (C622oEN pin pulled low) those capacitors present infinite impedance to the DC signal and to the receiving device this looks like a tristated (High-Z) output. Resistors R3, R4, R5 and R6 are used to terminate the transmission line with 50 ohm impedance and to generate DC bias voltage for the LVPECL receiver. If the LVPECL receiver has an integrated 50 ohm termination and bias source, resistors R3, R4, R5 and R6 should not be populated.

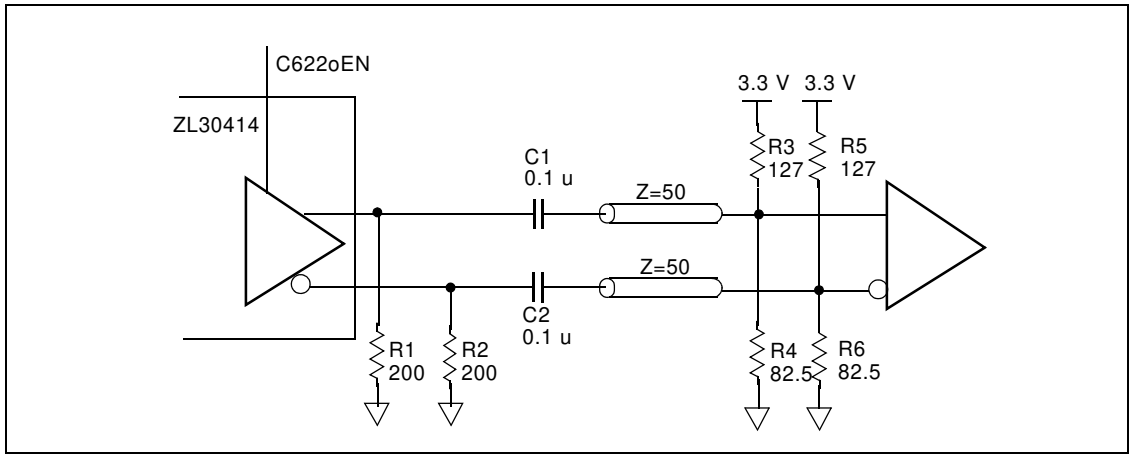
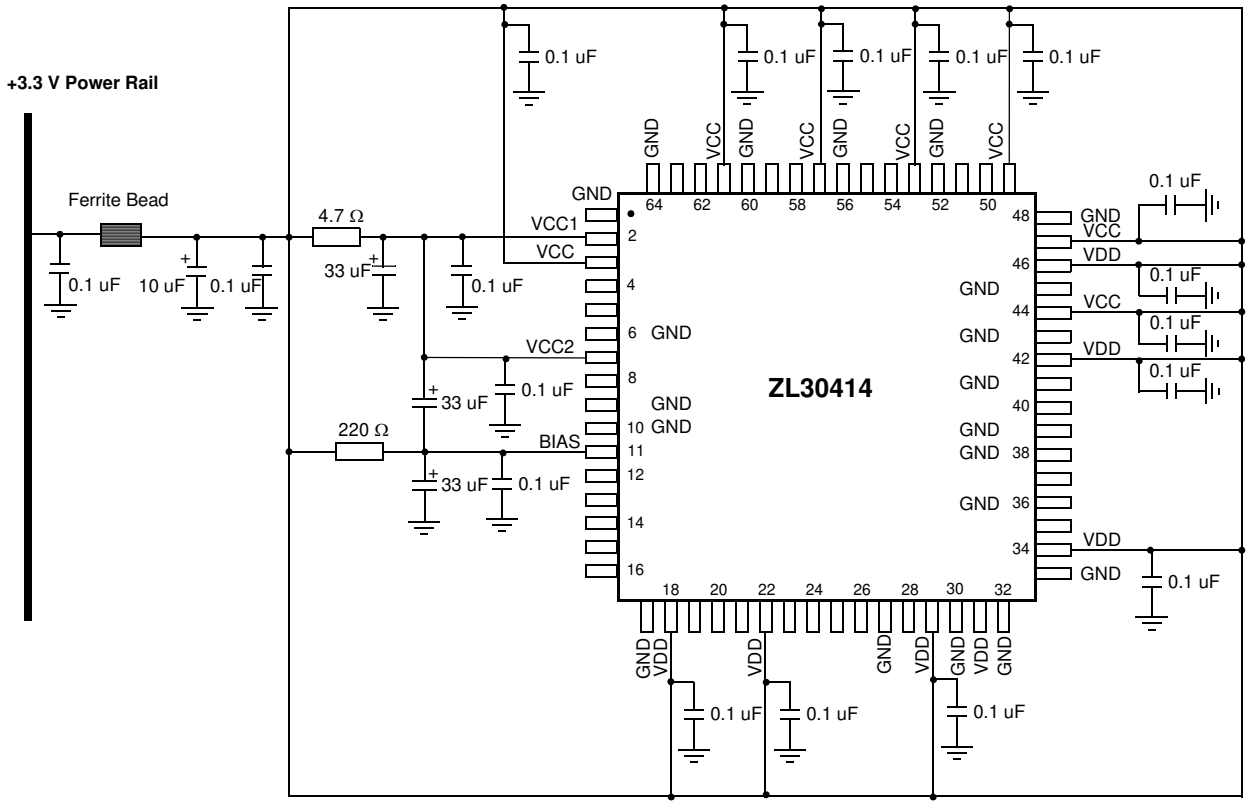


Figure 12 - Tristatable LVPECL Outputs

4.4 Power Supply and BIAS Circuit Filtering Recommendations

Figure 13 presents a complete filtering arrangement that is recommended for applications requiring maximum jitter performance. The level of required filtering is subject to further optimization and simplification. Please check Zarlink's web site for updates.



Notes:

1. All the ground pins (GND) and the Exposed die Pad (metal area at the back of the package) are connected to the same ground plane.
2. Select Ferrite Bead with I_{DC} > 400 mA and R_{DC} in a range from 0.10 Ω to 0.15 Ω

Figure 13 - Power Supply and BIAS Circuit Filtering

5.0 Characteristics

Absolute Maximum Ratings†

	Characteristics	Sym.	Min.‡	Max.‡	Units
1	Supply voltage	V_{DDR}, V_{CCR}	TBD	TBD	V
2	Voltage on any pin	V_{PIN}	-0.5	V_{CC} + 0.5 V_{DD} + 0.5	V
3	Current on any pin	I_{PIN}	-0.5	30	mA
4	ESD Rating	V_{ESD}		1250	V
5	Storage temperature	T_{ST}	-55	125	°C
6	Package power dissipation	P_{PD}		1.8	W

† Voltages are with respect to ground unless otherwise stated.

‡ Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Operating Temperature	T_{OP}	-40	25	+85	°C	
2	Positive Supply	V_{DD}, V_{CC}	3.0	3.3	3.6	V	

† Voltages are with respect to ground unless otherwise stated.

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics†

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	Supply Current	I_{DD}+I_{CC}		146		mA	LVPECL, CML drivers disabled and unterminated
2	Incremental Supply Current to single LVPECL driver (driver enabled and terminated, see Figure 8)	I_{LVPECL}		37		mA	Note 1 Note 2
3	Incremental Supply Current to CML driver (driver enabled and terminated, see Figure 9)	I_{CML}		26		mA	Note 3
4	CMOS: High-level input voltage	V_{IH}	0.7V_{DD}		V_{DD}	V	
5	CMOS: Low-level input voltage	V_{IL}	0		0.3V_{DD}	V	
6	CMOS: Input leakage current	I_{IL}		1	5	uA	V_I = V_{DD} or 0 V

DC Electrical Characteristics† (continued)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
7	CMOS: Input bias current for pulled-down inputs: C622oEN-A, C622oEN-C, C622oEN-D, OC-CLKoEN	I_{B-PU}		300		uA	$V_I = V_{DD}$
8	CMOS: Input bias current for pulled-up inputs: , C622oEN-B, C19oEN	I_{B-PD}		90		uA	V_I = 0V
9	CMOS: High-level output voltage	V_{OH}	2.4			V	I_{OH} = 8 mA
10	CMOS: Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
11	LOCK pin: High-level output voltage	V_{OH}	2.4				I_{OH} = 0.5 mA
12	LOCK pin: Low-level output voltage	V_{OL}			0.4		I_{OL} = 0.5 mA
13	CMOS: C19o output rise time	T_R		1.8	3.3	ns	18 pF load
14	CMOS: C19o output fall time	T_F		1.1	1.4	ns	18 pF load
15	LVPECL: Differential output voltage (622.08 MHz)	$IV_{OD\_LVPECL}I$		1.17		V	Note 2
16	LVPECL: Offset voltage (622.08 MHz)	V_{OS_LVPECL}	Vcc-1.31	Vcc-1.20	Vcc-1.09	V	Note 2
17	LVPECL: Output rise/fall times (622.08 MHz)	T_{RF}		170		ps	Note 2
18	CML: Differential output voltage (155.52 MHz)	$IV_{OD\_CML}I$		0.73		V	Note 3
19	CML: Offset voltage (155.52 MHz)	V_{OS_CML}	Vcc-0.58	Vcc-0.54	Vcc-0.50	V	Note 3
20	CML: Output rise/fall times (155.52 MHz)	T_{RF}		220		ps	Note 3

- †: Voltages are with respect to ground unless otherwise stated.
- ‡ :Typical figures are for design aid only: not guaranteed and not subject to production testing.
- Supply voltage and operating temperature are as per Recommended Operating Conditions
- Note 1: The I_{LVPECL} current is determined by the termination network connected to LVPECL outputs. More than 25% of this current flows outside the chip and it does not contribute to the internal power dissipation.
- Note 2: LVPECL outputs terminated with Z_T = 50 Ω resistors biased to V_{CC}-2V (see Figure 8)
- Note 3: CML outputs terminated with Z_T = 50 Ω resistors connected to low impedance DC bias voltage source (see Figure 9)

AC Electrical Characteristics† - Output Timing Parameters Measurement Voltage Levels

	Characteristics	Sym	CMOS	LVPECL	CML	Units
1	Threshold Voltage	$V_{T\text{-}CMOS}$ $V_{T\text{-}LVPECL}$ $V_{T\text{-}CML}$	$0.5V_{DD}$	$0.5V_{OD\_LVPECL}$	$0.5V_{OD\_CML}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.7V_{DD}$	$0.8V_{OD\_LVPECL}$	$0.8V_{OD\_CML}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.3V_{DD}$	$0.2V_{OD\_LVPECL}$	$0.2V_{OD\_CML}$	V

† Voltages are with respect to ground unless otherwise stated.

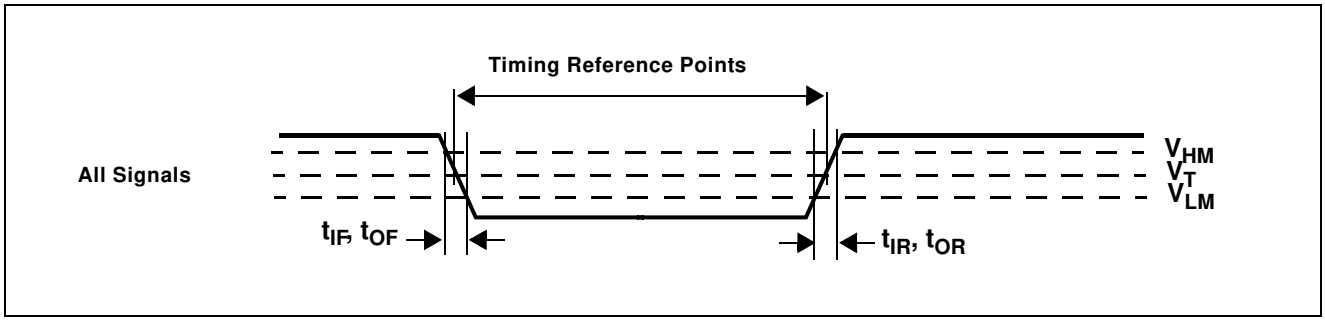


Figure 14 - Output Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics† - C19i Input to C19o, C155o and C622o Output Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C19i to C19o delay	t_{C19D}	6.2	7.2	8.2	ns	
2	C19i to C155o delay	tc_{155D}	3	4	5	ns	
3	C19i to C622oA delay	t_{C622D}	0	0.8	1.6	ns	
4	C155o duty cycle	d_{C155L}	48	50	52	%	
5	C622o duty cycle	d_{C622L}	48	50	52	%	

† Supply voltage and operating temperature are as per Recommended Operating Conditions

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.

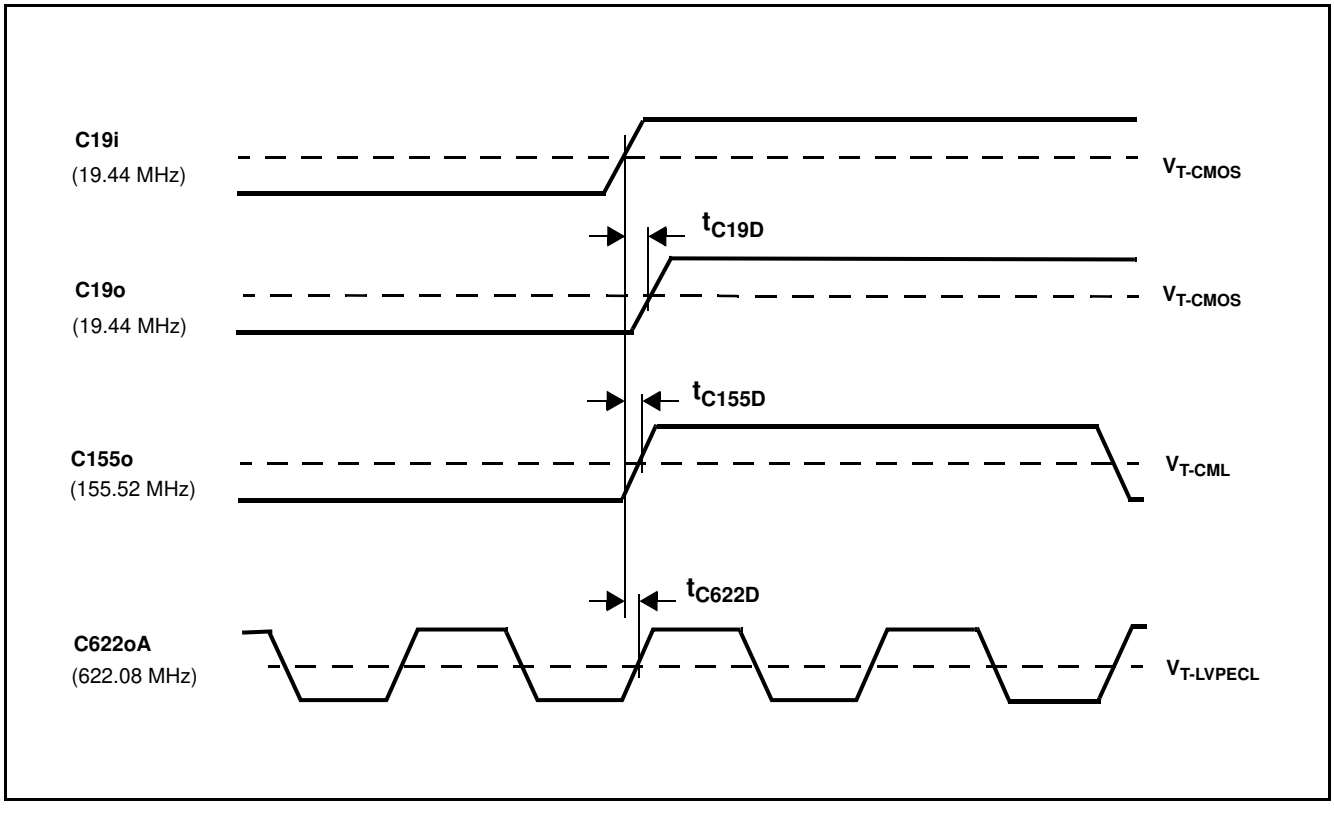


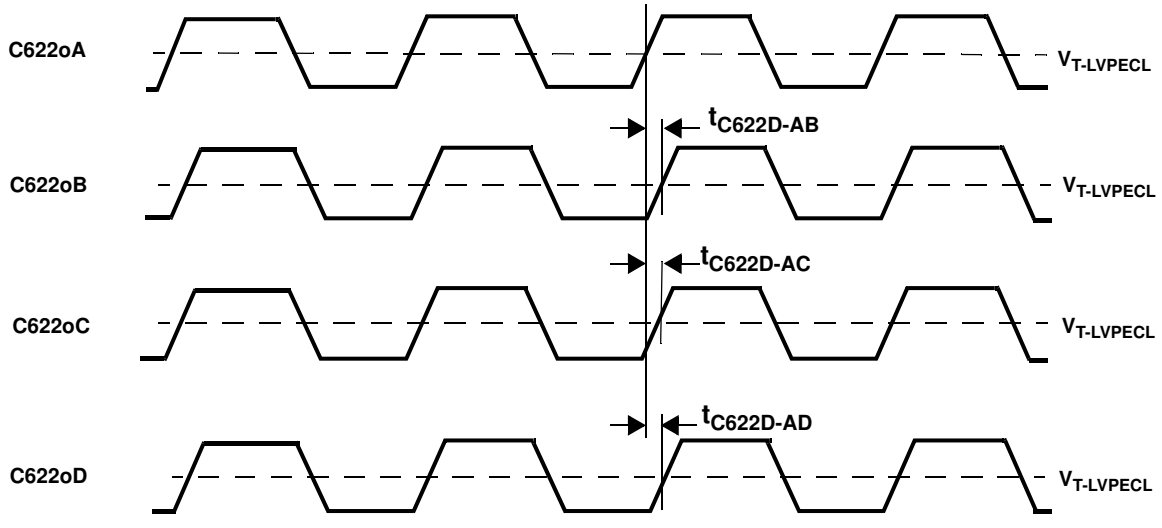
Figure 15 - C19i Input to C19o, C155o and C622o Output Timing

AC Electrical Characteristics† - C622 Clocks Output Timing

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes
1	C622oA to C622oB	$t_{C622D-AB}$	-50	0	+50	ps	
2	C622oA to C622oC	$t_{C622D-AC}$	-50	0	+50	ps	
3	C622oA to C622oD	$t_{C622D-AD}$	-50	0	+50	ps	

† Supply voltage and operating temperature are as per Recommended Operating Conditions

‡ Typical figures are for design aid only: not guaranteed and not subject to production testing.



Note: All output clocks have nominal 50% duty cycle.

Figure 16 - C622oB, C622oC, C622oD Outputs Timing

Performance Characteristics - Functional (V_{CC} = 3.3 V ±10%; T_A = -40 to 85°C)

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Pull-in range	±1000			ppm	At nominal input reference frequency C19i = 19.44 MHz
2	Lock Time			300	ms	

Performance Characteristics : Output Jitter Generation - GR-253-CORE conformance (V_{CC} = 3.3V ±10%; T_A = -40 to 85°C)

GR-253-CORE Jitter Generation Requirements					ZL30414 Jitter Generation Performance		
	Interface (Category II)	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**Typ.†**	**Max.‡**	**Units**
1	OC-192 STS-192	4 MHz to 80 MHz	0.1 UIpp	10.0	-	6.95	ps_{P-P}
					0.49	0.89	ps_{RMS}
		20 kHz to 80 MHz	0.3 UIpp	30.1	-	11.5	ps_{P-P}
					0.82	1.04	ps_{RMS}
2	OC-48 STS-48	12 kHz - 20 MHz	0.1 UI_{PP}	40.2	-	7.32	ps_{P-P}
			0.01 UI_{RMS}	4.02	0.58	0.83	ps_{RMS}
3	OC-12 STS-12	12 kHz - 5 MHz	0.1 UI_{PP}	161	-	4.37	ps_{P-P}
			0.01 UI_{RMS}	16.1	0.34	0.60	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

‡ Loop Filter components: R_F=8.2 kΩ, C_F=470 nF

Performance Characteristics : Output Jitter Generation - G.813 conformance (Option 1 and 2) (V_{CC} = 3.3V ±10%; T_A = -40 to 85°C)

G.813 Jitter Generation Requirements					ZL30414 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**Typ.†**	**Max.‡**	**Units**
Option 1							
1	STM-64	4 MHz to 80 MHz	0.1 UIpp	10.0	-	6.95	ps_{P-P}
					0.49	0.89	ps_{RMS}
		20 kHz to 80 MHz	0.5 UIpp	50.2	-	11.5	ps_{P-P}
					0.82	1.04	ps_{RMS}
2	STM-16	1 MHz to 20 MHz	0.1 UIpp	40.2	-	6.40	ps_{P-P}
					0.50	0.68	ps_{RMS}
		5 kHz to 20 MHz	0.5 UIpp	201	-	8.67	ps_{P-P}
					0.68	1.06	ps_{RMS}
3	STM-4	250 kHz to 5 MHz	0.1 UIpp	161	-	3.33	ps_{P-P}
					0.26	0.42	ps_{RMS}
		1 kHz to 5 MHz	0.5 UIpp	804	-	19.1	ps_{P-P}
					1.51	2.88	ps_{RMS}
Option 2							
5	STM-64	4 MHz to 80 MHz	0.1 UIpp	10.0	-	6.95	ps_{P-P}
					0.49	0.89	ps_{RMS}
		20 kHz to 80 MHz	0.3 UIpp	30.1	-	11.5	ps_{P-P}
					0.82	1.04	ps_{RMS}
6	STM-16	12 kHz - 20 MHz	0.1 UIpp	40.2	-	7.32	ps_{P-P}
					0.58	0.83	ps_{RMS}
7	STM-4	12 kHz - 5 MHz	0.1 UIpp	161	-	4.37	ps_{P-P}
					0.34	0.60	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

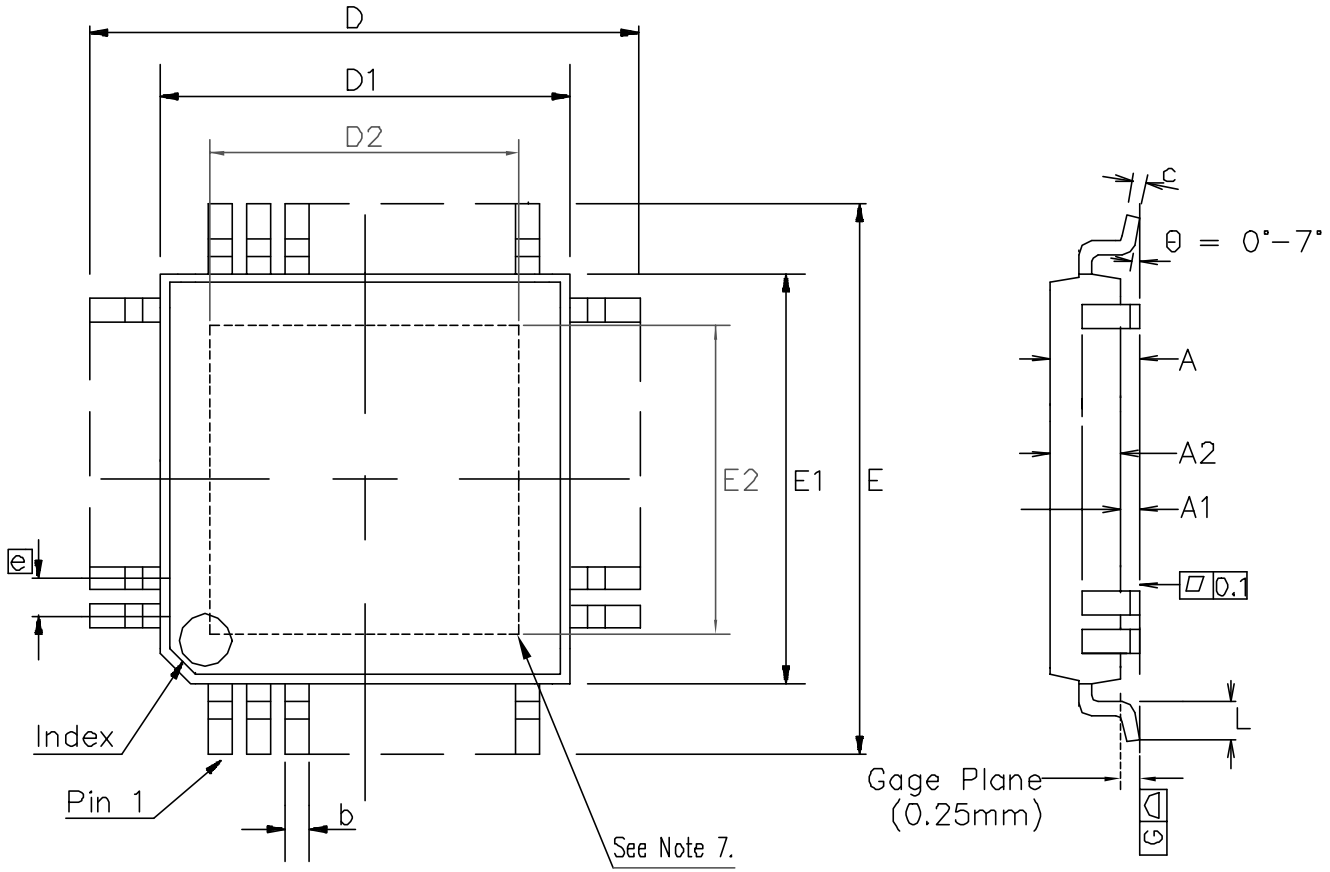
‡ Loop Filter components: R_F=8.2 kΩ, C_F=470 nF

Performance Characteristics : Output Jitter Generation - ETSI EN 300 462-7-1conformance (V_{CC} = 3.3V ±10%; T_A = -40 to 85°C)

EN 300 462-7-1 Jitter Generation Requirements					ZL30414 Jitter Generation Performance		
	Interface	**Jitter Measurement Filter**	**Limit in UI**	**Equivalent limit in time domain**	**Typ.†**	**Max.‡**	**Units**
1	STM-16	1 MHz to 20 MHz	0.1 UIpp	40.2	-	6.40	ps_{P-P}
					0.50	0.68	ps_{RMS}
		5 kHz to 20 MHz	0.5UIpp	201	-	8.67	ps_{P-P}
					0.68	1.06	ps_{RMS}
2	STM-4	250 kHz to 5 MHz	0.1 UIpp	161	-	3.33	ps_{P-P}
					0.26	0.42	ps_{RMS}
		1 kHz to 5 MHz	0.5 UIpp	804	-	19.1	ps_{P-P}
					1.51	2.88	ps_{RMS}

† Typical figures are for design aid only: not guaranteed and not subject to production testing.

‡ Loop Filter components: R_F=8.2 kΩ, C_F=470 nF



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.20		---	0.047
A1	0.05	0.15		0.002	0.006
A2	0.95	1.05		0.037	0.041
D	12.00 BSC			0.472 BSC	
D1	10.00 BSC			0.394 BSC	
D2	6.74	7.5		0.265	0.295
E	12.00 BSC			0.472 BSC	
E1	10.00 BSC			0.394 BSC	
E2	6.74	7.5		0.265	0.295
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	64				
ND	16				
NE	16				
NOTE	SQUARE				

Conforms to JEDEC MS-026 ACD Iss. C

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protrusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.
7. Dashed area represents exposed paddle.
   – Exposed pad is affected by mold flash, upto 30mils on straight edge, and upto 50mils at corner.

ISSUE	1			
ACN	CDCA			
DATE	15Aug05			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

N/A

Package Code QD/QG

Package Outline for 64 Lead e-Pad TQFP 10x10x1.0mm, +2.0mm (footprint) with 7.5mm DAP (Die Attach Pad)

113400

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www.zarlink.com