MIC2150/MIC2151

2-Phase Dual Output PWM Synchronous Buck Control IC

General Description

The MIC2150/1 are simple 2-phase dual-output synchronous buck control ICs featuring small size and high efficiency. The ICs implement PWM control at 500kHz (MIC2150) or 300kHz (MIC2151), with the outputs switching 180° out of phase. The result of the out-of-phase operation is 1MHz input ripple frequency with ripple current cancellation, minimizing the required input filter capacitance. A 1% output voltage tolerance allows the maximum level of system performance. Internal drivers with adaptive gate drive allow the highest efficiency with the minimum external components.

A dual threshold enable pin, matched soft-start pins, and a power good output are provided, allowing a high level of control.

The MIC2150/1 are available in the small size 4mm×4mm 24-pin MLF® package. The MIC2150/1 has a junction operating range from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

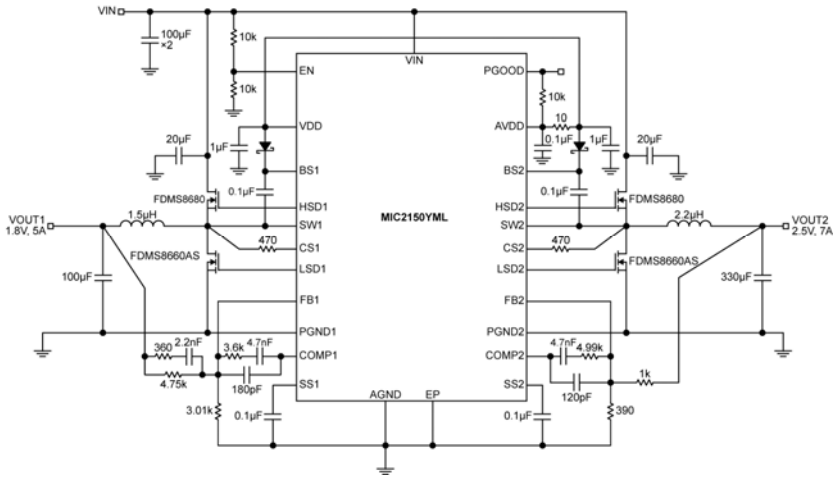
Applications

- Multi-output power supplies with sequencing
- DSP, FPGA, CPU and ASIC power supplies
- Telecom and Networking equipment
- Servers

Features

- Dual Synchronous Buck Control IC with outputs switching 180 degree out-of-phase
- 4.5V to 14.5V input voltage range
- Adjustable output voltages down to 0.7V
- 1% output voltage accuracy
- MIC2150: 500kHz PWM operation
- MIC2151: 300kHz PWM operation
- Adaptive gate drive allows efficiencies over 95%
- Adjustable current limit with no sense resistor
  - Senses low-side MOSFET current
- Internal drivers allow 20A per phase
- Power Good output allow simple sequencing
- Dual threshold enable pin
- Independent programmable soft-start pins
- Output over-voltage protection
- Input UVLO
- Works with ceramic output capacitors
- Tiny 4mm×4mm 24-Pin MLF® package
- Junction temperature range of -40°C to +125°C

Typical Application

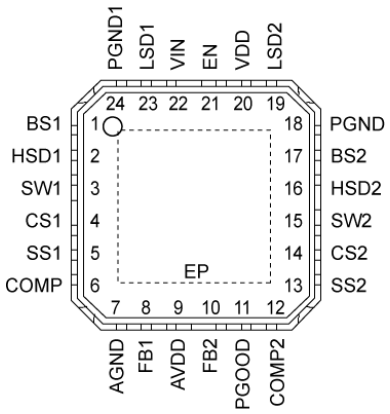


MicroLead Frame and MLF are registered trademarks of Amkor Technology, Inc.

Ordering Information

Part Number	Frequency	Voltage	Junction Temp. Range	Lead Finish	Package
MIC2150YML	500kHz	Adj.	–40°C to +125°C	Pb-Free	4mm×4mm 24-pin MLF®
MIC2151YML	300kHz	Adj.	–40°C to +125°C	Pb-Free	4mm×4mm 24-pin MLF®

Pin Configuration



24-Pin MLF® (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1	BS1	Boost 1(Input): Provides voltage for high-side MOSFET driver 1. The gate drive voltage is higher than the source voltage by V_{DD} minus a diode drop.
2	HSD1	High-Side Drive 1 (Output): High current output-driver for ext. high-side MOSFET.
3	SW1	Switch Node 1(Output): High current output driver return for HSD1.
4	CS1	Current Sense 1 (Input): Current-limit comparator non-inverting input. The current limit is sensed across the low-side FET during the ON-time. Current limit is set by the resistor in series with the CS1 pin.
5	SS1	Soft-start, Output 1(Input): Controls the turn-on time of the output voltage. Active at power-up, Enable and Current Limit recovery.
6	COMP1	Compensation 1 (Input): Pin for external compensation, Channel 1.
7	AGND	Analog Ground (Signal): Signal path return for FB, EN, PGOOD, AVDD, SS and COMP.
8	FB1	Feedback 1 (Input): Input to Channel 1 error amplifier. Regulates to 0.7V.
9	AVDD	Analog Supply Voltage (Input): Connect ext. bypass capacitor.
10	FB2	Feedback 2 (Input): Input to Channel 2 error amplifier. Regulates to 0.7V.
11	PGOOD	Power Good (Output): Indicates Channel 1 output AND Channel 2 output > 90% Nominal.
12	COMP2	Compensation 2 (Input): Pin for external compensation, Channel 2.

Pin Number	Pin Name	Pin Function
13	SS2	Soft-start, Output 2(Input): Controls the turn-on time of the output voltage. Active at power-up, Enable and Current Limit recovery.
14	CS2	Current Limit 2 (Input): Current-limit comparator non-inverting input. The current limit is sensed across the low-side FET during the ON time. Current limit is set by the resistor in series with the CS2 pin.
15	SW2	Switch node 2 (Output): High current output driver return for HSD2.
16	HSD2	High-Side Drive 2 (Output): High current output-driver for the high-side MOSFET.
17	BS2	Boost 2 (Input): Provides voltage for high-side MOSFET driver 2. The gate drive voltage is higher than the source voltage by V_{DD} minus a diode drop.
18	PGND2	Power Ground 2. High current return for low-side driver 2 & CS2.
19	LSD2	Low-Side Drive 2 (Output): High-current driver output for external MOSFET.
20	VDD	5V Internal Linear Regulator from V_{IN} (Output): V_{DD} is the ext. MOSFET gate drive supply voltage and an internal supply bus for the IC. When V_{IN} is <5V, this regulator operates in drop-out mode. Connect external bypass capacitor.
21	EN	Enable (Input): Dual threshold enable pin. Logic low turns the IC off. Exceeding lower threshold enables Channel 1, exceeding higher threshold then enables Channel 2. The dual threshold function allows the option of power up sequencing from a single EN pin. Both channels must be turned on and off together. The enable pin must be driven higher than 2.8V for proper operation.
22	VIN	Supply voltage Channel 1 (Input): 4.5V to 14V
23	LSD1	Low-Side Drive 1 (Output): High-current driver output for external MOSFET.
24	PGND1	Power Ground 1: High current return for low-side driver 1 & CS1.
EPAD	EP	Exposed Pad (Power): Must make a full connection to the GND plane to maximize thermal performance of the package.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) ..... –0.3V to 15V
Bootstrap Pin Voltage (BST & HSD) ..... V_{IN} + 6V
FB, COMP, SS, V_{DD}, LSD & A_{VDD} ..... –0.3V to 6V
CS, SW & EN ..... –0.3V to 15V
Power Good (P_{GOOD}) ..... AV_{DD} + 0.3V
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... 260°C
ESD Rating[3] ..... HBM = 2kV, MM = 200V, CDM = 2kV

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +4.5V to +14.5V
Output Voltage Range ..... 0.7V to 0.83×V_{IN}
Junction Temperature Range ..... –40°C ≤ T_J ≤ +125°C
Package Thermal Resistance
MLF® (θ_{JA}) ..... 60°C/W
MLF® (θ_{JC}) ..... 6°C/W

Electrical Characteristics[4]

T_J = 25°C; V_{EN} = V_{IN} = 12V; unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C

Parameter	Condition		Min	Typ	Max	Units
V_{IN} , V_{EN}, V_{DD} Supply						
Total Supply Current, PWM mode supply current	V_{FB} = 0.7V (both O/Ps) (Outputs switching but excluding external MOSFET gate current.)			4.2	**10**	mA
Shutdown Current	V_{EN} = 0V			50	**100**	µA
V_{IN} UVLO Start Voltage	V_{IN} rising		**1.5**	2.03	**2.4**	V
V_{IN} UVLO Stop Voltage	V_{IN} falling		**1.5**	2	**2.4**	V
V_{IN} UVLO Hysteresis				30		mV
V_{DD} UVLO Start Voltage	V_{DD} rising		**3.0**	3.3	**3.6**	V
V_{DD} UVLO Stop Voltage	V_{DD} falling		**2.8**	3.1	**3.4**	V
V_{IN} UVLO Hysteresis				200		mV
V_{EN} Threshold 1			**0.8**	1	**1.2**	V
V_{EN} Threshold 2			**1.7**	2	**2.3**	V
V_{EN} Hysteresis	(each threshold)			30		mV
Internal Bias Voltages (V_{DD})	IV_{DD} = -50mA		4.5	5	5.5	V
V_{DD} Load Current	V_{IN} = 6V to 14.5V				75	mA
	V_{IN} = 5.5V				50	mA
Oscillator / PWM Section						
PWM Frequency *See design note*	(Internal Oscillator = 2X PWM frequency)	MIC2150	450	500	550	kHz
		MIC2151	270	300	330	kHz
Maximum Duty Cycle (Each Channel)		MIC2150	**80**			%
		MIC2151	**83**			%
Minimum On-Time [5,6]	(Each Channel)			30	**50**	ns

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.
5. Minimum on-time before automatic cycle skipping begins. See applications section.
6. Guaranteed by design.

Parameter	Condition		Min	Typ	Max	Units
Regulation						
Feedback Voltage Reference	(Each Channel) 25°C (Each Channel) –40°C to +125°C		691 **686**	700	709 **714**	mV
Feedback Bias Current	(Each Channel)			35	**500**	nA
Output Voltage Line Regulation	(Each Channel)			0.03		% / V
Error Amplifier (Each Channel)						
DC Gain (6)				70		dB
Output Over voltage Protection (each channel)						
V_{FB} threshold	(Latches LSD High)		**110**	115	**120**	%Nom
Delay Blanking time				2		µs
Soft-Start						
Internal Soft-Start source current (each channel)	V_{SS} = 1V		1.25 **1**	2	2.75 **3**	µA
Soft-Start source current matching between channels			**–30**	0	**30**	%
Internal Soft-Start discharge current (each channel)	During Soft Current Limit			18		µA
Current Sense (Each Channel)						
CS Over Current Trip Point program current			170	200	230	µA
CS comparator sense threshold			–7	0	+7	mV
Power Good						
V_{FB} threshold			**86**	90	**93**	%Nom
PGOOD voltage low	V_{IN} = 4.5V, V_{FB} = 0 V; I_{PGOOD} = 1mA			0.1	**0.3**	V
Output Dynamic Correction Thresholds						
Upper Threshold, V_{FB_OVT} (6)	(relative to V_{FB}).			+6.5		%
Lower Threshold, V_{FB_UVT} (6)	(relative to V_{FB}).			–6.5		%
Gate Drivers						
Rise/Fall Time	Into 3000pF	Rise		23		ns
		Fall		16		ns
Low-Side Drive Resistance	V_{IN} = 5V	Source		1.5	3	Ω
		Sink		1.5	2	Ω
High-Side Drive Resistance	V_{IN} = 5V	Source		1.5	3	Ω
		Sink		1.5	2	Ω

Notes:

6. Guaranteed by design.

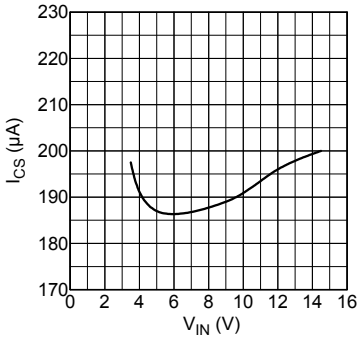
Parameter	Condition		Min	Typ	Max	Units
Driver non-overlap time (adaptive)[6]			**10**	20		ns
Driver non-overlap time between low-side off and high-side on[6]		MIC2150	**40**	60		ns
		MIC2151	**70**	100		ns

Notes:

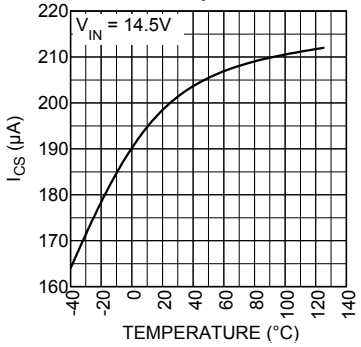
6. Guaranteed by design.

Typical Characteristics

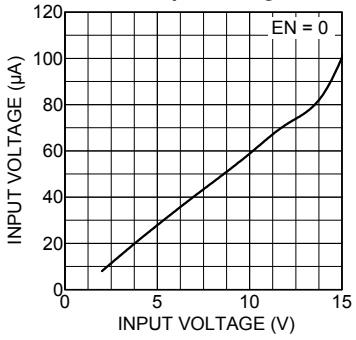
CS Pin Current Source vs V_{IN}



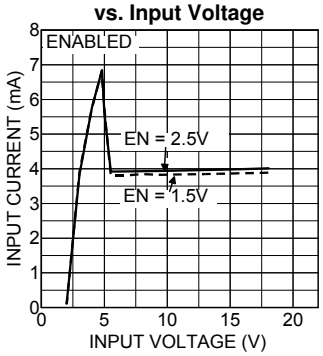
CS Pin Source Current vs Temperature



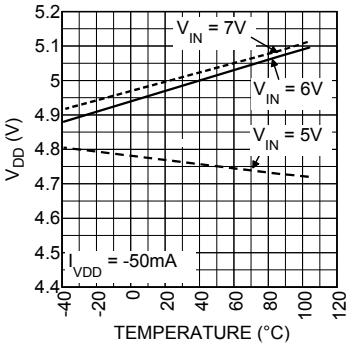
Input Current vs. Input Voltage



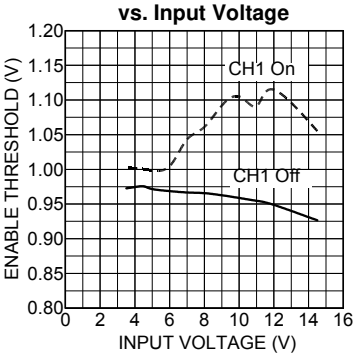
Input Current vs. Input Voltage



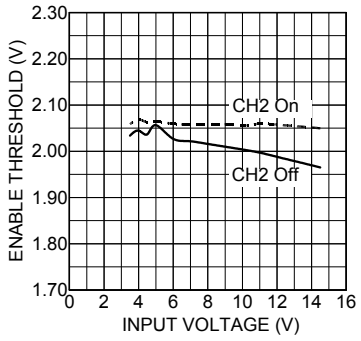
VDD Regulator vs. Temperature



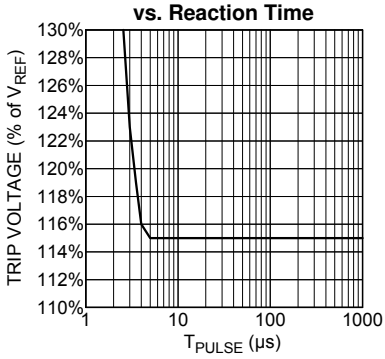
CH1 Enable Thresholds vs. Input Voltage



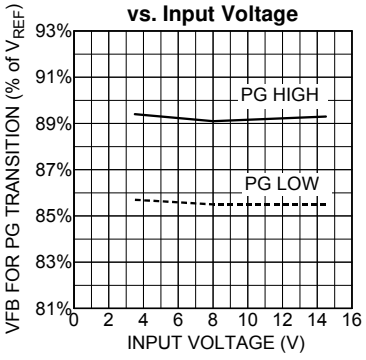
CH2 Enable Thresholds vs. Input Voltage



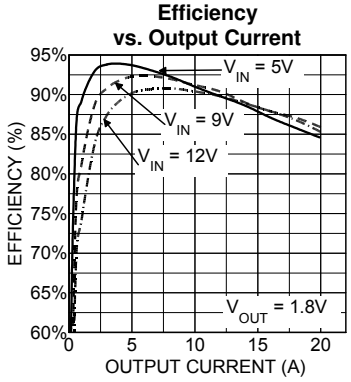
OVP Threshold vs. Reaction Time



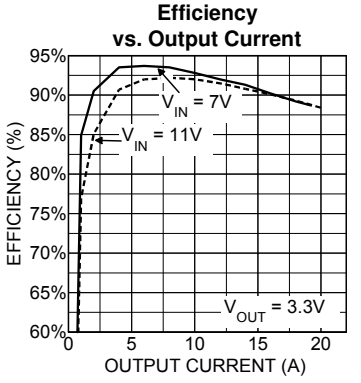
Power Good Thresholds vs. Input Voltage



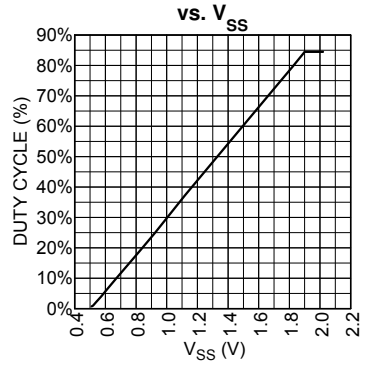
Efficiency vs. Output Current



Efficiency vs. Output Current

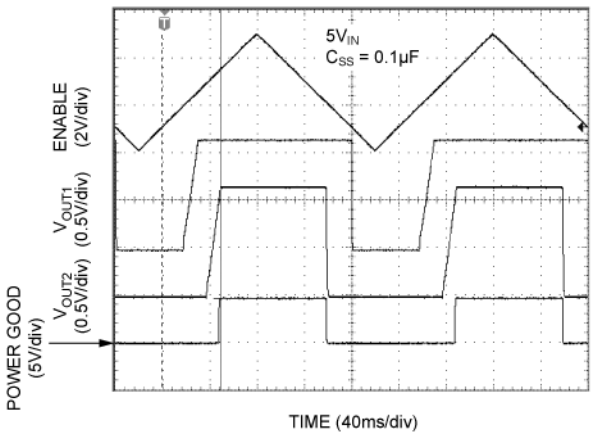


Max. Duty Cycle vs. V_{SS}

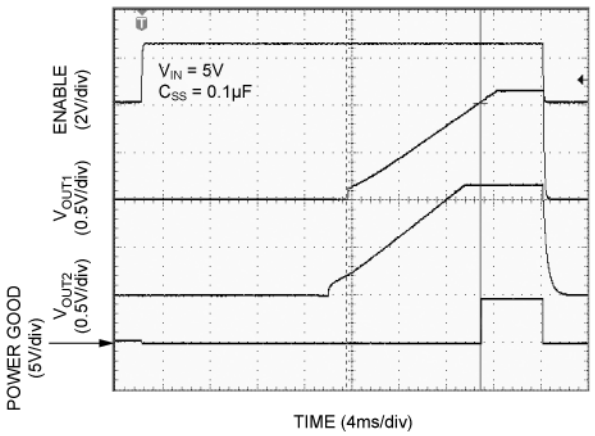


Functional Characteristics

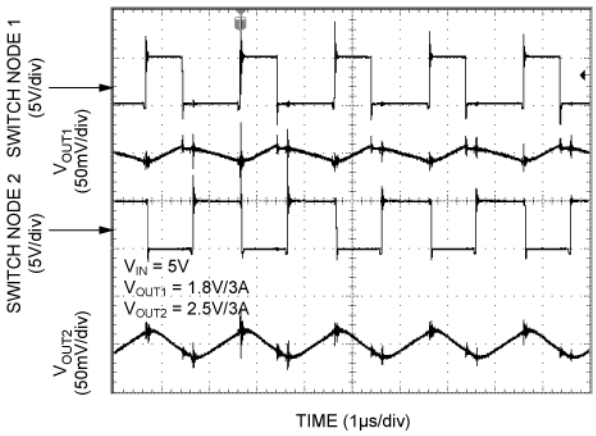
Output Sequencing



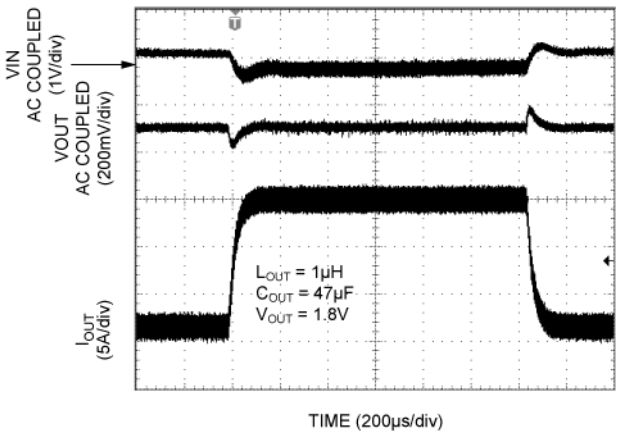
Output Turn-On and Turn-Off



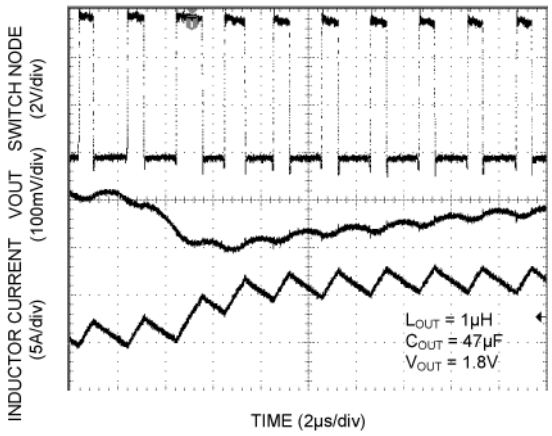
Output Ripple



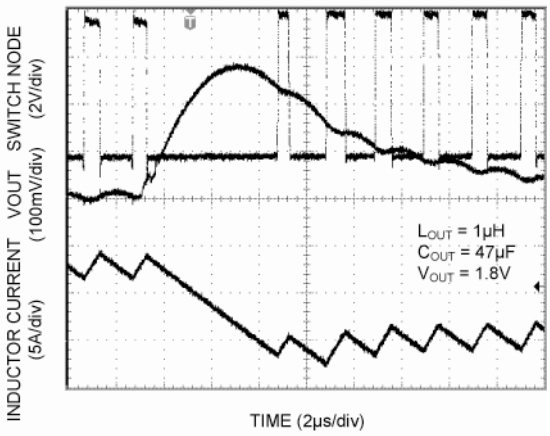
Output Load Transient Response



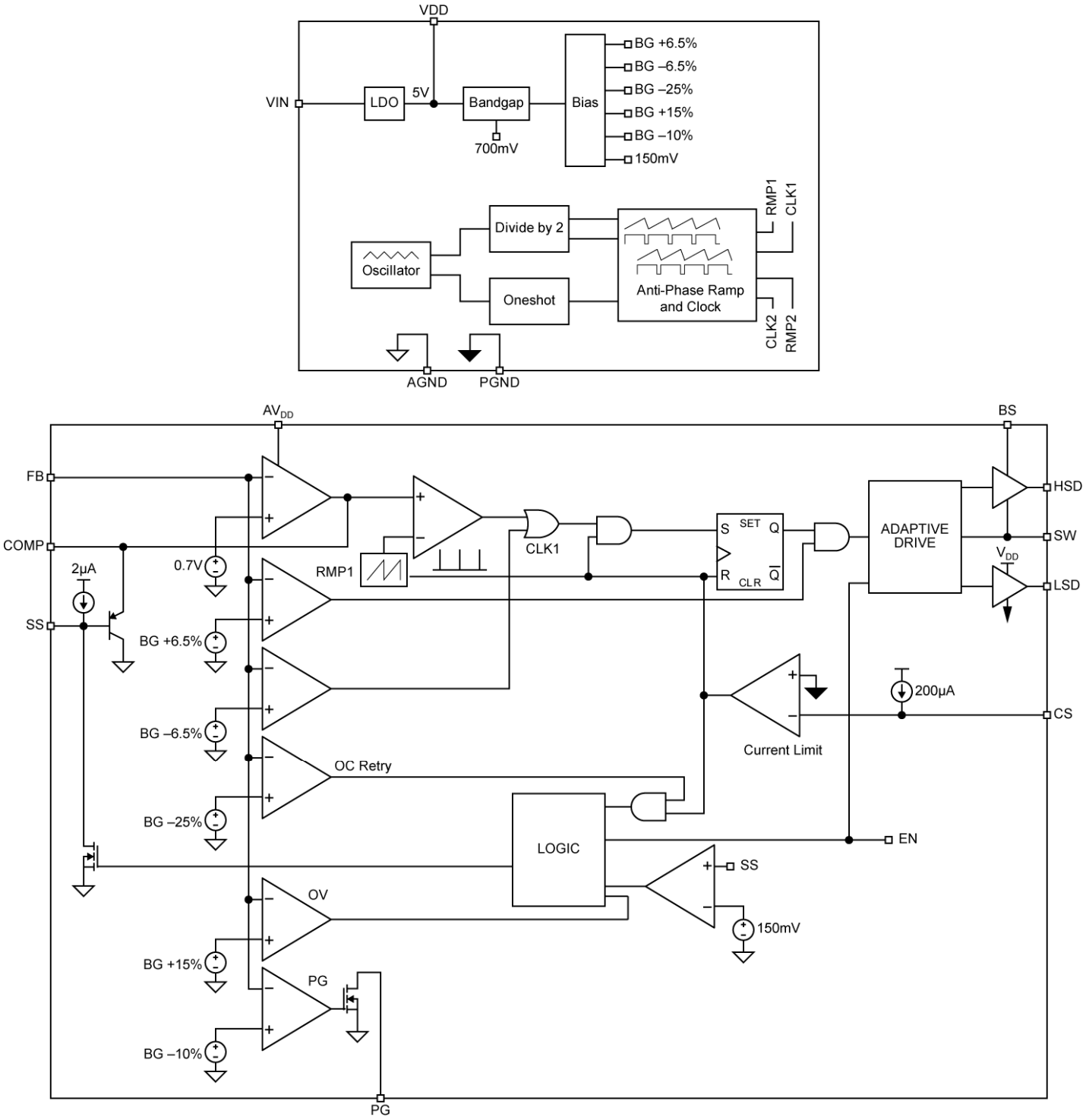
Hysteretic Response – Increasing Current

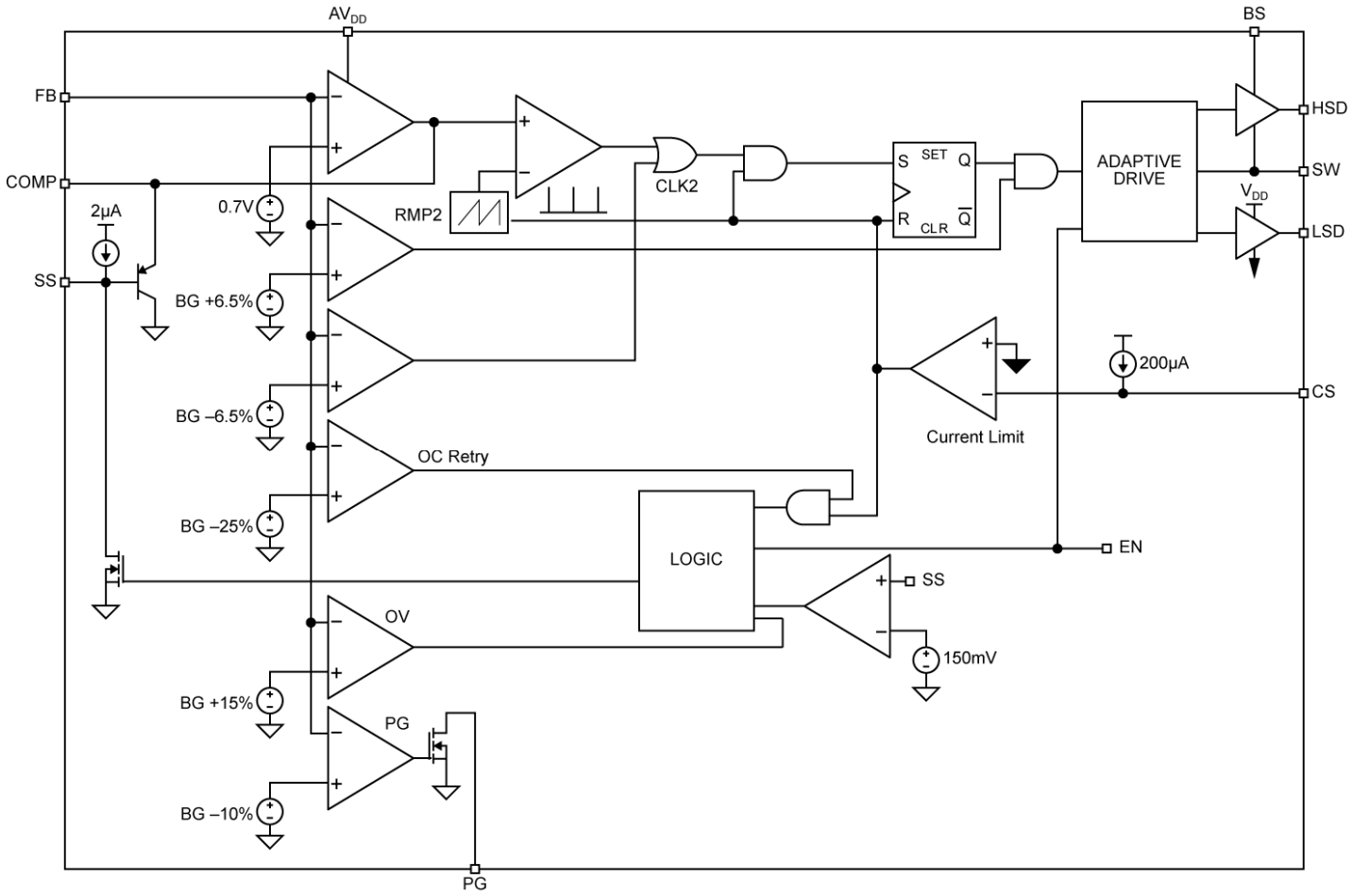


Hysteretic Response – Decreasing Current



Functional Diagram





Functional Description

The MIC2150 is a dual channel, synchronous buck controller built with the latest BiCMOS process for optimum speed and efficiency. Both PWM channels operate 180° out of phase with each other to minimize input capacitor ripple current and input noise. The control loop has two stages of regulation. During steady state to medium output disturbances, the loop operates in fixed frequency, PWM mode while, during a large voltage disturbance (~±6.5% nominal), the loop becomes hysteretic; meaning that for a short period, the switching MOSFETs are switched on continuously until the output voltage returns to its nominal level. This maximizes transient response for large load steps, while operating nominally in fixed frequency PWM mode. Voltage mode control is used to allow for maximum flexibility and maintain good transient regulation. The operating voltage range is 4.5V to 14.5V and the output voltage can be set down to 0.7V. Start-up surges are prevented using built in soft-start circuitry as well as resistor-less current sensing for overload protection. Other protection features include UVLO, dual level enable thresholds, over voltage latch off protection, power good signal and dual level over current protection.

Theory of Operation

The output voltage of the converter is sensed at the inverting input of the error amplifier. This is connected to V_{OUT} via the two feedback resistors. The non-inverting input is connected to the internal 0.7V reference and the two are compared to produce an error voltage. This error voltage is then fed into the non-inverting input of the PWM comparator and compared to the 1.5V voltage ramp to create the PWM pulses. The PWM pulses propagate through to the MOSFET drivers which drive the external MOSFETs and create the power switching waveform at the set DC (duty cycle). This is then filtered by a power inductor and low ESR capacitor to produce the output voltage where $V_{OUT} \approx DC \times V_{IN}$. As an example, due to a load increase or an input voltage drop, the output voltage will instantaneously drop. This will cause

the error voltage to rise, resulting in wider pulses at the output of the PWM comparator. The higher Duty Cycle power switching waveform will cause an associated rise in output voltage and will continue to rise until the feedback voltage is equal to the reference and the loop is again in equilibrium. It is necessary to reduce the bandwidth of this feedback loop in order to keep the system stable. This can result in relatively poor transient regulation performance. However, the MIC2150 has a further hysteretic feedback loop which operates during large transients to reduce this effect. Hysteretic mode is invoked when output voltage is detected to be ±6.5% of its nominal level. If the input voltage step or output load step is large enough to cause a 6.5% deviation in V_{OUT}, then the additional control loop functions to return the output voltage to its nominal set point in the fastest time possible. This is limited only by the time constant of the power inductor and output capacitor. This scheme is not used during normal operation because it creates a switching waveform whose frequency is dependant upon V_{IN}, passive component values and the load current. Due to its large noise spectrum, it is only used during surges to keep switching noise at a known, fixed frequency.

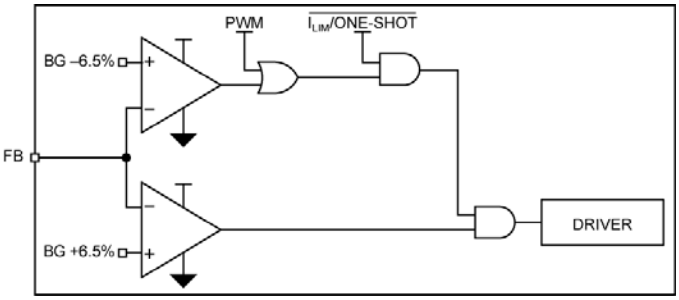


Figure 1. Hysteretic Block Diagram

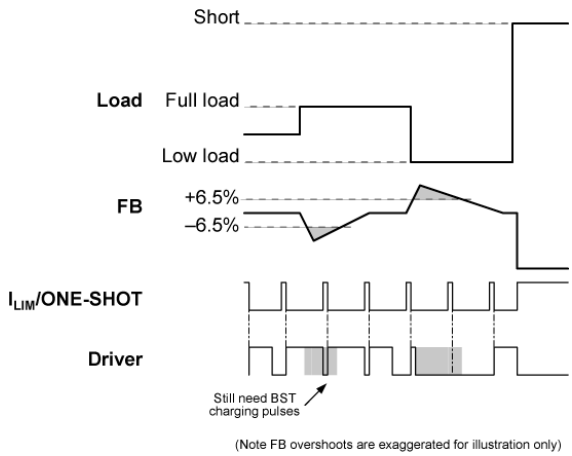


Figure 2. Hysteretic Waveforms

Soft-start

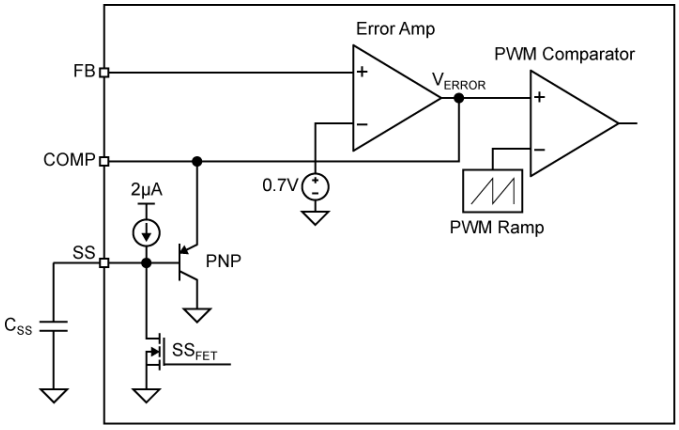


Figure 3. Soft-Start

At startup, the Soft-start MOSFET (SS_{FET}) is released and C_{SS} starts to charge at the rate $\frac{dV_{SS}}{dt} = \frac{2\mu A}{C_{SS}}$. The PNP transistor's emitter (COMP) starts to track V_{SS} at that rate until it reaches the lower end of the PWM ramp waveform. This is around 950mV and is where switching pulses will begin to drive the power MOSFETs. This ramp continues on the COMP pin until the loop reaches it's regulation point which is dependant upon the duty cycle required for regulation and can be anywhere from 1.4V to 2.9V. V_{SS} will however, continue to rise as the PNP base-emitter junction becomes reverse biased.

During large over current or short circuit conditions, i.e., where current limit is detected and V_{OUT} is <75% of nominal, the SS_{FET} is momentarily switched on. This discharges C_{SS} to ~150mV at which point, it re-starts the soft-start cycle once again. During soft-start, hysteretic comparators are disabled until the −6.5% comparator has been set.

Soft-start time = T1 + T2

Where T1 = $0.9 \times C_{SS}/2\mu A$

And T2 = $1.5 \times V_{OUT} \times C_{SS}/(V_{IN} \times 2\mu A)$

If the value of C_{COMP} is in the same magnitude as C_{SS}, then there may be an additional delay associated as the error amplifier charges the C_{COMP} capacitor.

Current Limit

The MIC2150 uses the R_{DSON} of the low-side MOSFET to sense over current conditions. The lower MOSFET is used as it displays much lower parasitic oscillations during switching then the upper MOSFET. Using the MOSFET R_{DSON} is not the most accurate method of current measurement, but is an adequate method for circuit protection without adding additional cost and board space that would be taken by discrete current sense resistors. Generally, the MIC2150 current limit

circuit acts to provide a fixed maximum output current until the resistance of the load is so low that the voltage across it is no longer within regulation limits. At this point (75% of nominal output voltage), Hiccup current mode is initiated to protect down-stream loads from excessive current during hard short circuits and also reduces overall power dissipation in the PWM converter components during a fault. Before hiccup current mode occurs, 'brick wall' current limiting is provided to prevent system shutdown or disturbance if the overload is only marginal.

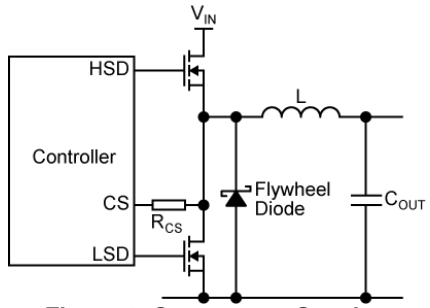


Figure 4. Overcurrent Sensing

During the normal operation of a synchronous Buck regulator, as the lower MOSFET is switched on, its drain voltage will become negative with respect to ground as the inductor current continues to flow from Source to Drain. This negative voltage is proportional to output load current, inductor ripple current and MOSFET R_{DSON}.

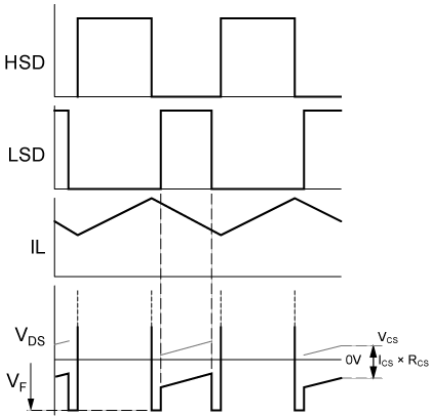


Figure 5. Current Sensing Waveforms

The larger inductor current, the more negative VDS becomes. This is utilized for the detection of over current by passing a known fixed current source (200µA) through a resistor R_{CS} which sets up an offset voltage ($I_{CS} \times R_{CS}$). When I_{SD} (Source to Drain current)$\times R_{DSON}$ is equal to this voltage, the MIC2150's over current trigger is set. This disables the next high-side gate drive pulse. After missing the high-side pulse, the over current (OC) trigger is reset. If, on the next low-side drive cycle, the current is still too high i.e., V_{CS} is ≤ 0V, another high-side pulse is missed and so on. Thus reducing the overall energy transferred to the output and V_{OUT} starts to fall. As this successive missing of pulses results in an effectively lower switching frequency, power inductor ripple currents can get very high if left unlimited. The MIC2150 therefore limits Duty Cycle during current limit to prevent currents building up in the power inductor and output capacitors.

Current-Limit Setting

The current limit circuit responds to the peak inductor current flowing through the low-side FET. The value of R_{CS} can be estimated with the "simple" method or can be more accurately calculated by taking the inductor ripple current into account.

The Simple Method

Current limit can be quickly estimated with the following equation:

$$R_{CS} = I_{OUT} \times R_{DSON(MAX)} / 200\mu A.$$

Where: R_{DSON} is the maximum on-resistance of the low side FET at the operating junction temperature

Accurate Method

For designs where ripple current is significant when compared to I_{OUT} or for low duty cycle operation, calculating the current setting resistor R_{CS} should take into account that one is sensing the peak inductor current and that there is a blanking delay of approximately 100ns.

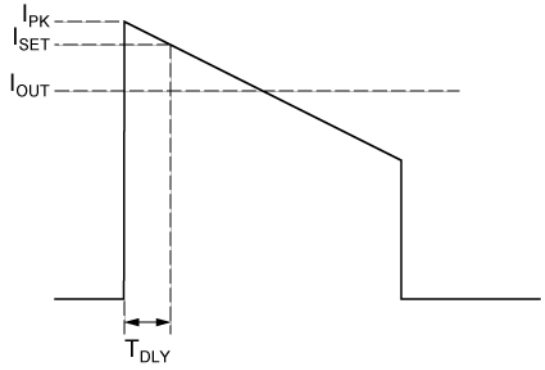


Figure 6. Overcurrent-Circuit Waveform

Calculate peak switch current

$$I_{PK} = I_{OUT} + \frac{I_{RIPPLE}}{2}$$

Where: $I_{RIPPLE} = \frac{V_{OUT} \times (1 - D)}{F_S \times L}$

Now calculate the actual set point to allow for the 100ns delay.

$$I_{SET} = I_{PK} - \frac{V_{OUT} \times T_{DLY}}{L}$$

Rcs can now be calculated using:

$$R_{CS} = \frac{I_{SET} \times R_{DSON(MAX)}}{I_{CS\,min}}$$

Where:

D = Duty Cycle

F_S = Switching Frequency

L = Power inductor value

T_{DLY} = Current limit blanking time ~ 100ns

$I_{CS(min)}$ = 180µA

Example

Consider a 12V to 3.3V @ 5A converter with 0.5µH power inductor and 90% efficiency at full load.

$$D \approx \frac{V_{OUT}}{V_{IN} \times Efficiency} = \frac{3.3V}{12V \times 0.9} = 31\%$$

$$I_{RIPPLE} = \frac{3.3V \times (1 - 0.31)}{500kHz \times 0.5\mu H} = 9.11A$$

$$I_{PK} = 5 + \frac{9.11}{2} = 9.55A$$

$$I_{SET} = 9.55A - \frac{3.3v \times 100ns}{0.5\mu H} = 8.89A$$

$$R_{CS} = \frac{8.89 \times 10m\Omega}{180\mu A} = 494\Omega$$

Using the simple method here would result in a current limit point much lower than expected.

This equation sets the minimum current limit point of the converter, but maximum will depend on the actual inductor value and R_{DSON} of the MOSFET under current limit conditions. This could be in the region of 50% higher and should be considered to ensure that all the power components are within their thermal limits unless thermal protection is implemented separately.

It is recommended to connect a 22pF capacitor from CS to AGND close to the pins of the IC to prevent adjacent channel switching noise from affecting the current limit behavior.

Over Voltage Protection

If the voltage at the FB pin is detected to be 15% higher than nominal for >2µs, the channel is stopped from switching immediately and latched off. Switching can be re-started by taking EN below the channel's enable threshold and re-enabling or re-cycling power to the IC.

Power Good Output

The power good output (PG) will go high only when both Channel outputs are above 90% of their nominal set output voltage. If CH2 is disabled (EN<2V), then PG will be low regardless of the state of CH1. If PG functionality is required for CH1 only, FB2 can be driven externally above 90% V_{REF} to enable PG to operate on CH1 only.

Enable

Sometimes, at high currents, it is possible to see relatively large ground current peaks. These, in turn, can create voltage differentials between AGND points. In order to prevent these from affecting the converter operation, it is good practice to drive enable 0.5V higher than its maximum threshold i.e., >2.8V for both channels.

V_{DD} Regulator

The internal regulator provides a regulated 5V for supplying the analogue circuit power (AV_{DD}) and the MOSFET driver power from the input supply (V_{IN}). While this is designed to operate in dropout at input voltages down to 3V, driver current will be limited while the V_{DD} regulator is in dropout. It is therefore recommended that for V_{IN} ranges 5V to 7V, MOSFET gate current should be kept to less than 50mA.

The AV_{DD} supply should be connected to V_{DD} through an RC filter to provide decoupling of the switching noise generated by the MOSFET drivers taking large current steps from the V_{DD} regulator.

Gate Drivers

The MIC2150 is designed to drive both high-side and low-side N-Channel MOSFETs to enable high switching speeds and the lowest possible losses. The high-side MOSFET driver is supplied by bootstrapping the switching voltage at the Drain of the lower MOSFET to V_{DD}. This provides the high-side MOSFET with a constant VGS drive voltage equal to V_{DD}.

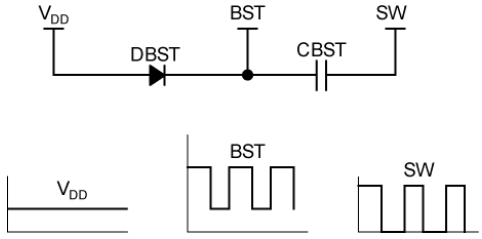


Figure 7. High-Side Gate Drive Circuit and Waveform

When HSD goes high, this turns on the high-side MOSFET and the SW node rises sharply. This is coupled through the bootstrap capacitor C_{BST} and Diode D_{BST} becomes reverse biased. The MOSFET Gate is held at V_{DD} - 0.5V above the Source for as long as C_{BST} remains charged. The bias current of the high-side driver is <10mA so 100nF is sufficient to hold the gate voltage with minimal droop for the power stroke (High-side

switching) cycle.

i.e., Δ_{BST} = 10mA×1.6µs / 100nF = 160mV. For most applications, 220nF should be used to achieve an improved, lower droop. When the low-side driver turns on every switching cycle, any lost charge from C_{BST} is replaced via D_{BST} as it becomes forward biased. Therefore minimum BST voltage is V_{DD} – 0.5V.

The Low-side driver is supplied directly from V_{DD} at nominal 5V.

Adaptive Gate Drive

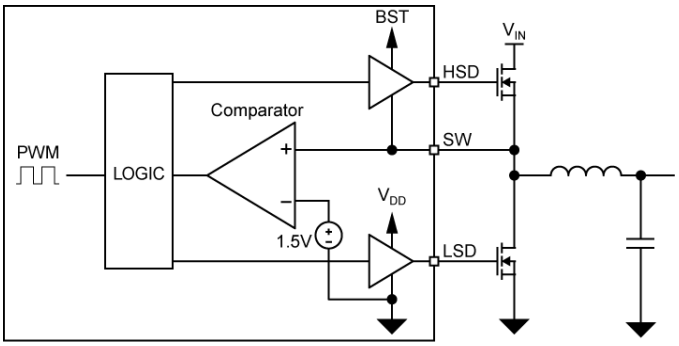


Figure 8. Adaptive Gate Drive Diagram

There is a period when both driver outputs are held off ('dead time') to prevent shoot-through current flowing. Shoot-through current flows if both MOSFETS are on momentarily as the cycle's crossover. This dead time must be kept to a minimum to reduce losses in the catch diode which could either be an external Schottky diode placed across the lower MOSFET or the internal Schottky diode implemented in some MOSFETs. It is not recommended for high current designs, to rely on the intrinsic body diode of the power MOSFET; these typically have large V_F values and a slow reverse recovery characteristic which will add significant losses to the regulator. Dependent on the MOSFETs used, the dead time could be required to be 150ns or 20ns. The MIC2150 solves this variability issue by using an adaptive gate-drive scheme:

When the high-side driver is turned off, naturally the inductor forces the voltage at the switching node (low-side MOSFET drain) towards ground to keep current flowing. When the SW pin is detected to have reached 1.5V, the top MOSFET can be assumed to be off and the low-side driver output is immediately turned on. There is also a short delay between the low-side drive turning off and the high-side driver turning on. This is fixed at ~60ns to 100ns to allow for large gate charge MOSFETs to be used.

Application Information

Passive Component Selection Guide

Inductor Selection

The inductor value is responsible for the ripple current which causes some proportion of the resistive losses in the power components. These losses are proportional to I_{RIPPLE}^2. Minimizing inductor ripple current can therefore reduce the RMS current flowing in the power components and generally improve efficiency; this is achieved by choosing a larger value inductor. Having said this, the actual value of inductance is realistically defined by space limitations, RMS rating (I_{RMS}) and saturation current (I_{SAT}) of available inductors. If one looks at the newer flat wire inductors for example, these typically have higher I_{SAT} ratings than the I_{RMS} for lower values. Also, as inductance value increases, these figures tend to get closer in value. This mirrors what happens in the converter with I_{SAT} analogous to the maximum peak switch current and I_{RMS} analogous to output current. As inductance increases, so $I_{SWITCH(PK)}$ tends towards I_{OUT}. This is a characteristic that makes these types of inductor optimal for use with high power buck converters such as MIC2150.

To determine the I_{SAT} and I_{RMS} rating of the inductor, we should start with a nominal value of ripple current. This should typically be no more than $I_{OUT(MAX)}/2$ to minimize MOSFET losses due to ripple current mentioned earlier. Therefore:

$$L_{MIN} \sim 2 \times \frac{V_{OUT}}{I_{OUT} \times F_S} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \text{Efficiency}}\right)$$

$I_{LRMS} > 1.04 \times I_{OUT(MAX)}$

$I_{LSAT} > 1.25 \times I_{OUT(MAX)}$

Any value chosen above L_{MIN} will ensure these ratings are not exceeded.

In considering the actual value to choose, one needs to look at the effect of ripple on the other components in the circuit. The chosen inductor value will have a ripple current of:

$$I_{RIPPLE} \sim \frac{(1-D)}{F_S} \times \frac{V_{OUT}}{L}$$

This value should ideally be kept to a minimum, within the cost and size constraints of the design, to reduce unnecessary heat dissipation.

Output Capacitor Selection

The output capacitor (C_{OUT}) will have the full inductor ripple current $I_{RIPPLERMS}$ flowing through it. This creates the output switching noise which consists of two main components:

$$VOUT_{PK-PK} \approx I_{RIPPLE} \times ESR + \frac{I_{RIPPLE} \times t_{ON}}{2 \times C_{OUT}}$$

If therefore, the need is for low output voltage noise (e.g., in low output voltage converters), V_{OUT} ripple can be directly reduced by increasing inductor value, output capacitor value or reducing ESR.

For tantalum capacitors, ESR is typically >40mΩ which usually makes loop stabilization easier by utilizing a pole-zero (type II) compensator.

Due to many advantages of multi-layer ceramic capacitors, among them, cost, size, ripple rating and ESR, it can be useful to choose these in many cases. However, one disadvantage is the CV product. This is lower than tantalum. A mixture of one tantalum and one ceramic can be a good compromise which can still utilize the simple type II compensator.

With ceramic output capacitors only, a double-pole, double-zero (type III) compensator is required to ensure system stability. Loop compensation is described in more detail later in the data sheet.

Ensure the RMS ripple current rating of the capacitor is above $I_{RIPPLE} \times 0.6$ to improve reliability.

Input Capacitor Selection

C_{IN} ripple rating for a single phase converter is typically $I_{OUT}/2$ under worst case duty cycle conditions of 50%. This increases ~10% for a ripple current of $I_{OUT}/2$.

When both cycles are switching 180° out of phase, the ripple can reduce at DC <50% to:

$$I_{RMSCIN} = \sqrt{I_1^2 \times D_1 \times (1-D_1) + I_2^2 \times D_2 \times (1-D_2) - 2 \times I_1 \times I_2 \times D_1 \times D_2}$$

It is however, also advisable to closely decouple the Power MOSFETs with 2×10µF ceramic capacitors to reduce ringing and prevent noise related issues from causing problems in the layout of the regulator. The ripple rating of C_{IN} may therefore, be satisfied by these decoupling capacitors; allowing the use of perhaps one more ceramic or tantalum input capacitor at the input voltage node to decouple input noise and localize high di/dt signals to the regulator input.

Power MOSFET Selection

The MIC2150 drives N-Channel MOSFETs in both the upper and lower positions. This is because the switching speed for a given R_{DSON} in the N-Channel device is superior to the P-Channel device.

There are different criteria for choosing the upper and lower MOSFETs and these criteria are more marked at lower duty cycles such as 12V to 1.8V conversion. In such an application, the upper MOSFET is required to switch as quickly as possible to minimize transition

losses (power dissipated during rise and fall times). Conversely, the lower MOSFET can switch slower, but must handle larger RMS currents. When duty cycle approaches 50%, then the current carrying capability of the upper MOSFET starts to become critical also and can sometimes benefit from external high current drivers to achieve the necessary switching speeds.

MOSFET loss = Static loss + Transition loss

Static loss (P_S) = $I_{FETRMS}^2 \times R_{DSON}$

Transition loss (P_T) = $I_{OUT} \times (tr + tf) \times V_{DSOFF} \times F_S/2$

Where:

tr + tf = Rise time + Fall time

Due to the worst case driver currents of the MIC2150, the value of tr + tf simplifies to:

tr + tf (ns) = ΔQg (nC)

ΔQg can be found in the MOSFET characteristic curves

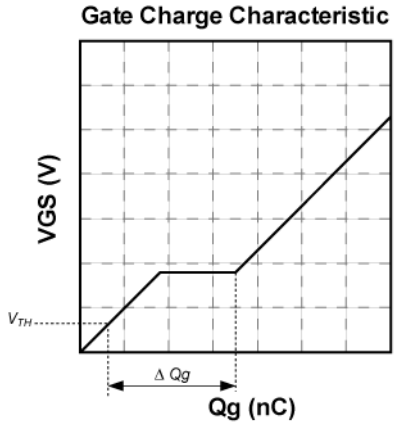


Figure 9. MOSFET Gate Charge Characteristic

V_{DSOFF} = Voltage across MOSFET when it is off

$$I_{FETRMS} = \sqrt{D \times \frac{\left(Ix^2 + Ix \times Iy + Iy^2\right)}{3}}$$

$Ix = I_{OUT} - I_{RIPPLE}/2$

$Iy = I_{OUT} + I_{RIPPLE}/2$

$D = T_{ON} \times F_S$

D is not duty cycle (DC ~$1.1 \times V_{OUT}/V_{IN}$) since it changes depending upon which MOSFET one is calculating losses for.

Upper FET $T_{ON} = DC/F_S$

The lower MOSFET is not on for the whole time that the upper MOSFET is off due to the fixed 80ns high-side driver delay. Therefore, there is an 80ns term subtracted from the lower FET on time equation.

Lower FET $T_{ON} = (1 - DC)/F_S - 80ns$

There are many MOSFET packages available which have various values of thermal resistance and therefore, can dissipate more power if there is sufficient airflow or heat sink externally to remove the heat. However, for this exercise, one can assume a maximum dissipation of 1.2W per MOSFET package. This can be altered if the final design has higher allowable package dissipation.

Look at lower MOSFET first:

$1.2W = P_S + P_T$

For the low-side FET, P_T is small because VDS_{OFF} is clamped to the forward voltage drop of the Schottky diode. Therefore:

$R_{DSON(MAX)} \sim 1.2 / I_{FETRMS}^2$

E.g. For 12V to 1.8V @ 10A

$R_{DSON(MAX)} < 14m\Omega$

It is important to remember to use the $R_{DSON(MAX)}$ figure for the MOSFET at the maximum temperature to help prevent thermal runaway (as the temperature increases, the R_{DSON} increases).

ΔQgmax should be limited so that the low-side MOSFET is off within the fixed 80ns delay before the high-side driver turns on.

High-side MOSFET:

For the high-side FET, the losses should ideally be evenly spread between transition and static losses. Use the center of the V_{IN} range to balance the losses.

$P_T = 0.6 = I_{OUT} \times \Delta Qg \times VIN_{MID} \times F_S/2$

Therefore:

$\Delta Qgmax < 0.6 \times 2 / (I_{OUT} \times VIN_{MID} \times F_S)$

R_{DSON} is calculated similarly for the high-side MOSFET:

$R_{DSON(MAX)} \sim 0.6 / I_{FETRMS}^2$

Using previous example:

$\Delta Qgmax < 20nC$

$R_{DSON(MAX)} < 35m\Omega$

Note that these are maximum figures based upon thermal limits and are not targeted at the highest efficiency. Selection of lower values is recommended to achieve higher efficiency designs.

Limits to watch out for:

Qg_{TOTAL} <1500 nC/V_{IN}

(<2500nC/V_{IN} for MIC2151)

- Total of both high-side and low-side MOSFET Qg values at V_{GS} = 5V for both channels.
- E.g. @ $V_{IN(MAX)}$ = 13.2V:
  Qg_{TOTAL} < 1500 / 13.2 = 114nC
  ΔQg_{LOW} <120nC (Per LSD output)

- Maximum turn on gate charge for each separate low-side MOSFET to ensure proper turn off before high-side MOSFET is switched on.

Output Voltage Setting

The internal reference of the MIC2150 is 0.7V nominal. Therefore:

$V_{OUT} = 0.7 \times (R1 + R2)/R2$

By setting R2 at <10k

$R1 = R2 \times (V_{OUT} - 0.7)/0.7$

The FB pin input offset current can be up to 500nA. It is therefore recommended to use resistor values of less than 10k to improve output accuracy

Schottky Diode and Snubbing Components

When the high-side switch turns on, there is usually an overshoot and ringing associated with this fast edge. This is induced by perturbation of the tank circuit made up of a combination of trace and lead inductances and MOSFET Drain and other parasitic capacitances. This can cause unwanted EMI and stress the driver circuitry if left un-damped. Snubbing is recommended to reduce this ringing and acts to critically damp the natural ringing frequency of the tank circuit. Technically, this can be achieved using a single resistance to dissipate the ringing energy. However, in practical terms, this would cause a DC power loss. Therefore a series RC is used to act only on the edges of the waveform. There are several methods of calculating the ideal values for the RC. The approach presented here is to estimate a value of C then calculate the R. This is best left until the final layout and components are available as it then accounts for all the parasitic contributors that cause the rising edge ringing.

Estimating C:

With no snubbing, measure the frequency of ringing. This is Fo. Now add a capacitor that results in a ring frequency of Fo/2. This is C_{SNUB}.

Calculating R:

$R_{SNUB} = 1/\pi \times C_{SNUB} \times Fo$

Loop compensation

The loop of a voltage mode, PWM buck converter contains 3 main blocks to be considered; the modulator, the power stage and the compensator.

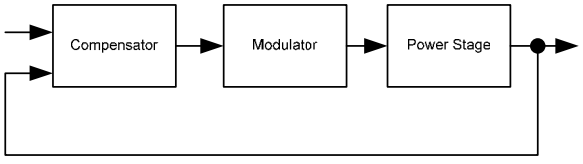


Figure 10. Loop Compensation Block Diagram

Modulator

This section turns the error signal from the error amplifier into a low impedance square wave with a pulse width proportional to the input. This section therefore includes the ramp, PWM comparator, drivers and MOSFETs. Usually, at the moderate frequencies of the control loop, the delays which appear as a phase lag between the error amplifier output and the power stage are small, but significant in allowing a loop to become unstable. The average gain of this stage can therefore be assumed to be linear with a gain of V_{IN}/Ramp and a phase shift less than 10 degrees.

Power Stage

This section is essentially the inductor, output capacitors and load resistance. Unlike the Modulator, in the frequency range of the loop, this is a complex system and contains two poles (i.e., a –40dB/decade gain fall at $1/2.\pi\sqrt{LC}$ and a total 180° phase lag) and a zero (i.e., a +20dB/Decade gain rise at $1/2\pi C.ESR$ and a total 90 degree phase lead). If the zero created by the output capacitor's ESR is too high to affect the two poles of the LC, then it is possible to have the conditions for an unstable loop without compensation. In general, there are two types of compensators that give a good transient response (the measure of how fast the regulation loop responds to a load step and brings the output voltage back to its steady state voltage):

1. If $1/2\pi \times C_{OUT} \times ESR > ½ F_S$
   Use a Double pole-Double Zero, PID or Type III compensator. This is typically used for low ESR ceramic output capacitor designs.
2. If $1/2\pi \times C_{OUT} \times ESR < Fco < ½ F_S$.
   Use a Pole Zero pair, PI or Type II compensator. This is typically used for Tantalum or electrolytic output capacitor designs.

Compensator

This section consists of the feedback resistors, error amplifier, compensation network and reference. It acts to sample the output voltage and create a frequency compensated error signal proportional to the difference between the output voltage and the reference. As this is a negative feedback system, this stage introduces a DC phase shift of 180 degrees. The output of the compensator is then fed into the modulator.

What is meant by frequency compensated is that it adds phase and gain where it is lost in the power stage and also acts to ensure gain is low at high frequencies to reduce susceptibility to switching noise.

The goal of the compensation network is to achieve a closed loop system that has sufficient phase margin and/or gain margin to ensure system stability across all

operating conditions. The detailed analysis for achieving this is covered in other texts and will not be covered here. The following is a method for calculating the correct values for stability.

Ceramic Output Capacitor Designs

The closed loop Bode plot response for a correctly compensated ceramic output capacitor design is shown below.

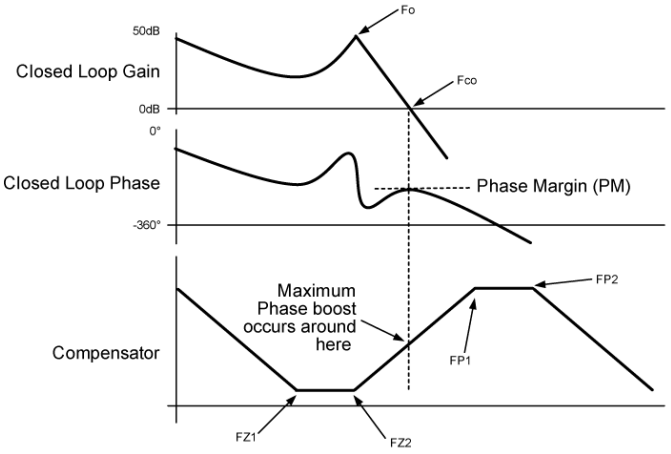


Figure 11. Ceramic Output Capacitor Bode Plot

The power inductor and output capacitor create the resonant frequency at Fo. It is preferred to make the desired crossover frequency (loop bandwidth) greater than this at Fco with a phase margin (PM) of typically 50 degrees. The maximum phase boost, on a log scale, occurs approximately half way between the highest zero (FZ2) and the lowest pole (FP1). To be precise, it is at $\sqrt{FZ2 \times FP1}$. The required compensation network for this is a double pole, double zero or type III network shown in Figure 12.

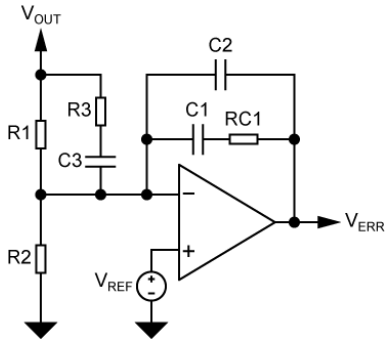


Figure 12. Type III Compensation Network

Placement of the 2 Poles and 2 Zeros

Choose a loop bandwidth/crossover frequency (Fco) at less than one fifth switching frequency and a phase margin (typically 50 degrees will ensure system stability over all conditions).

Fco < Fs/5

PM = 50 degrees

Place the two phase boost break frequencies such that our maximum phase boost occurs at the desired crossover frequency Fco.

$$FZ2 = Fco \times \sqrt{\frac{1 - Sin(PM)}{1 + Sin(PM)}}$$

$$FP1 = Fco \times \sqrt{\frac{1 + Sin(PM)}{1 - Sin(PM)}}$$

FZ1 must be somewhere below or equal to FZ2. Placing it at one half FZ2 helps to spread the frequency range of the phase boost.

$$FZ1 = FZ2 / 2$$

Finally, place the noise suppression pole at one half the switching frequency.

$$FP2 = \frac{F_S}{2}$$

The calculation of the required components to achieve FP1, FP2, FZ1 and FZ2 for this circuit is ideal for a spreadsheet which is available on the Micrel website. However, they can also be calculated using the following method:

Collect All Known Circuit Parameters

L:	Inductor value
C_{OUT}:	Output capacitor value
ESR:	Output capacitor ESR.
Fco:	Desired crossover frequency
V_{RAMP}:	Internal ramp voltage = 1.5V
V_{REF}:	Internal reference voltage = 0.7V
V_{IN}:	Maximum input voltage of the converter

Calculating Network Values

$$Fo = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

Choose RC1 value:

This can be any reasonable value up to 10kΩ, but in order to keep the values of R1 and C2 within practical limits, this 'factor' can be useful.

Rc1 = 25k/Fo

$$C1 = \frac{1}{2 \times \pi \times RC1 \times FZ1}$$

$$C2 = \frac{1}{2 \times \pi \times RC1 \times FP2}$$

$$C3 = \frac{2 \times \pi \times Fco \times L \times C_{OUT}}{RC1} \times \frac{V_{IN}}{V_{RAMP}}$$

$$R3 = \frac{1}{2 \times \pi \times C3 \times FP1}$$

$$R2 = \frac{R1 \times V_{REF}}{V_{OUT} - V_{REF}}$$

$$R1 = \frac{1}{2 \times \pi \times C3 \times FZ2} - R3$$

Tantalum/Electrolytic Output Capacitor Designs

The closed loop bode plot response of the higher ESR capacitor design looks something like the figure below.

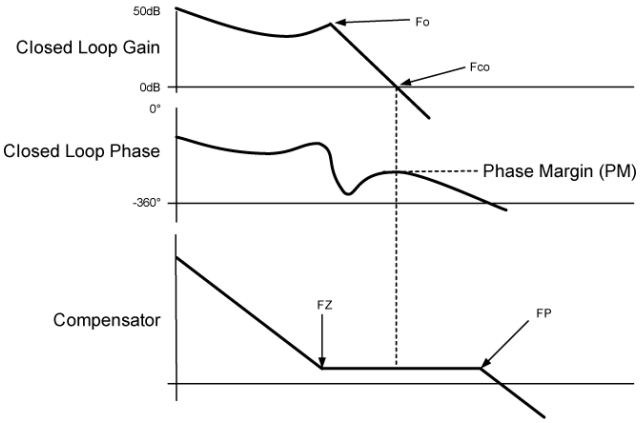


Figure 13. Tantalum Output Capacitor Bode Plot

Due to the output capacitor ESR creating a zero within the range of the desired crossover frequency (Fco), this design only requires that one adds one zero and one associated pole. The phase boost in this case occurs between the zero (FZ) and the pole (FP) of the compensator. Therefore, the zero gain crossover frequency (Fco) will be between these two points. The zero is created by RC1 and C1. The pole should be set at ≤one half switching frequency to reduce noise sensitivity. The plateau gain (gain between FZ and FP) is set by RC1 and R1, $Av_{PLATEAU}$ = RC1/R1, this should be set to a modest gain of five-to-ten to improve transient response. This compensation network is shown in Figure 14.

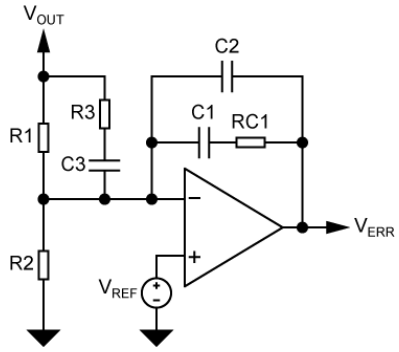


Figure 14. Type II Compensation Network

Pole and Zero Positioning

$$Fo = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

To introduce a boost in phase at and beyond the resonance of the output LC filter (Fo), FZ can be placed at Fo.

FZ = Fo

Together with phase boost associated with the output capacitor ESR zero, this will achieve up to 45 degrees Phase margin. The noise suppression pole can be set to one half switching frequency.

$$FP = \frac{F_S}{2}$$

Calculating Network Values

Choose R1 <10k to reduce susceptibility to noise and inaccuracies induced by the error amplifier bias current.

R1 = 1k

To set output voltage, set R2:

$$R2 = \frac{R1 \times V_{REF}}{V_{OUT} - V_{REF}}$$

For a plateau gain of 5

$$RC1 = R1 \times 5$$

$$C1 = \frac{1}{2 \times \pi \times RC1 \times FZ}$$

Assuming FZ<<FP, C2 can be approximated to:

$$C2 \approx \frac{1}{2 \times \pi \times RC1 \times FP}$$

Design and PCB Layout Guideline

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC2150 and MIC2151 converters.

IC (Integrated Circuit)

- Place the IC and MOSFETs close to the point-of-load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.
- The exposed pad (EP) on the bottom of the IC must be connected to the PGND and AGND pins of the IC.
- Place the feedback network close to the IC and keep the high impedance feedback trace short. Then route the V_{OUT} trace to the output.
- The V_{DD} capacitor must be placed close to the VDD pin and preferably connected directly to the pin and not through a via. The capacitor must be located right at the IC. The VDD terminal is very noise sensitive and placement of the capacitor is very critical. Connections must be made with wide trace.

Input Capacitor

- Place the V_{IN} input capacitors on the same side of the board and as close to the MOSFETs as possible.
- Keep both the V_{IN} and power GND connections short.
- Place several vias to the ground plane close to the V_{IN} input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.
- An additional Tantalum or Electrolytic bypass input capacitor of 22µF or higher is required at the input power connection.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Make sure stability calculations and done at the minimum and maximum tolerance values of ESR for the capacitor.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

MOSFETs

- Low gate charge MOSFETs should be used to maximize efficiency, especially at when operating at lower output current.

RC Snubber

- An RC snubber from each switch node-to-ground is recommended to reduce ringing and noise on the output and minimize component stress.

Schottky Diode (Optional)

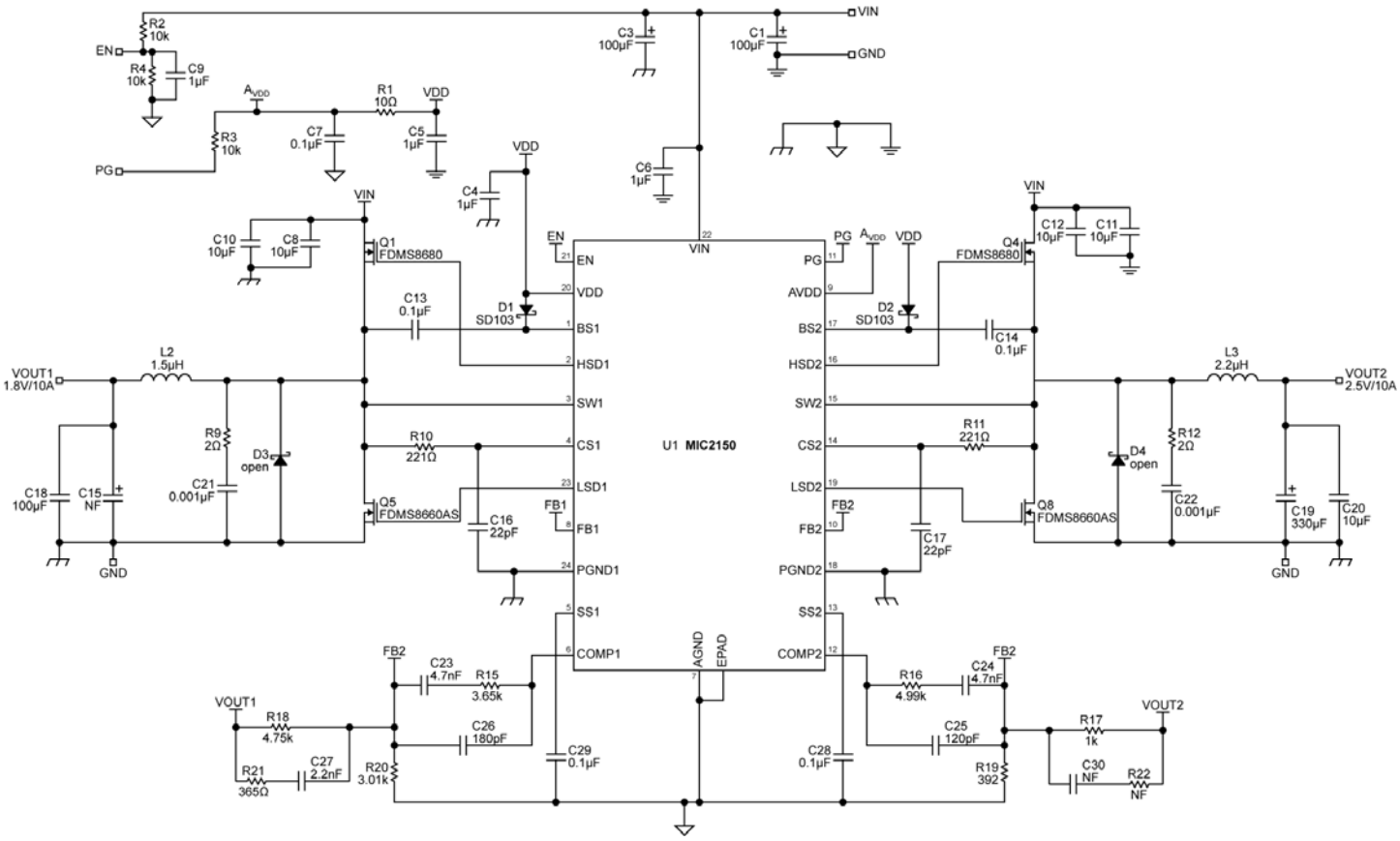
- Place the Schottky diode on the same side of the board as the MOSFETs and V_{IN} input capacitor.
- The connection from the Schottky diode’s Anode to the input capacitors ground terminal must be as short as possible.
- The diode’s Cathode connection to the switch node (SW) must be keep as short as possible.

Others

- Connect the current limiting resistor directly to the drain of low-side MOSFET.

- The output voltage feedback resistors should be placed close to the FB pin. The top side of the upper resistor should connect directly to the output node. Run this trace away from the switch node traces and inductor. The bottom side of the lower voltage divider resistor should connect to the GND pin of the control IC.
- The compensation resistor and capacitors should be placed right next to the COMP pin and the other side should connect directly to the GND pin on the control IC rather than going to the ground plane.
- Add placeholders for gate resistors on the top-side MOSFET gate drives. If necessary, gate resistors of 10Ω or less should be used.

MIC2150 Evaluation Board Schematic



Bill of Materials

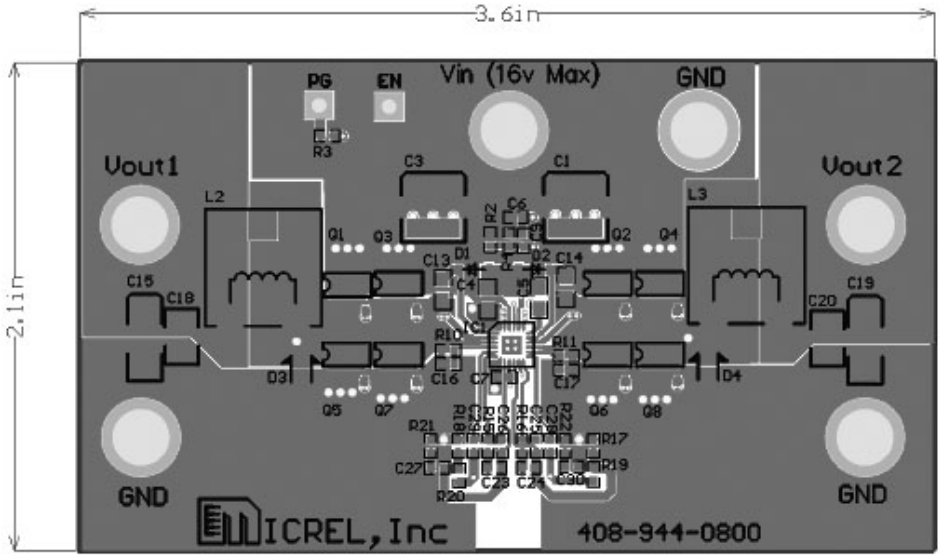
Item	Part Number	Manufacturer	Description	Qty.
C1,C3	TR3D107K016C0100	Vishay[1]	100µF/16V, D case	2
C8,C10,C11, C12,C20	GRM21BR61C106KE15L	Murata[2]	10µF/16V, 1210, X5R	5
or	VJ0805Y106KXXAT	Vishay[1]		
or	0805YD106K	AVX[3]		
C13,C14	VJ0805Y104KXXAT	Vishay[1]	100nF/16V, 0805	2
C7,C28,C29	VJ0603Y104KXXAT	Vishay[1]	100nF/16V, 0603	3
C6,C9	VJ0603Y105KXXAT	Vishay[1]	1µF/16V, 0603	2
C4,C5	VJ0805Y105KXXAT	Vishay[1]	1µF/16V, 0805	2
C18	C3225X5R0J107M	TDK[4]	100µF/6.3V, 1210	1
or	12106D107KAT2A	AVX[3]		
C15	OPEN		OPEN, NF	1
C19	TR3D337K6R3C0100	Vishay[1]	330µF/6.3V, D case	1
or	TPSD337K006R0045	AVX[3]		
C21,C22	VJ0805Y102KXXAT	Vishay[1]	1nF/16V, 0805	2
C26	VJ0603A181KXXAT	Vishay[1]	180pF/16V, 0603	1
C25	VJ0603A121KXXAT	Vishay[1]	120pF/16V, 0603	1
C23,C24	VJ0603Y472KXXAT	Vishay[1]	4.7nF/16V, 0603	2
C16,C17	VJ0603A220KXXAT	Vishay[1]	22pF/16V, 0603	2
C27	VJ0603Y222KXXAT	Vishay[1]	2.2nF/16V, 0603	1
C30	OPEN		OPEN, NF	1
D1,D2	SD103BWS-V-GS08	Vishay[1]	SD103BWS	2
D3,D4	DFLS220L-7(Not Fitted)	Diodes Inc.[5]	DFLS220L-7	2
L2	HC5-1R5	Cooper[6]	1.5µH,17A	1
L3	HC5-2R2	Cooper[6]	2.2µH,14A	1
Q1,Q4	FDMS8680	Fairchild[7]	20A HS FET	2
or	SiR462DP	Vishay[1]		
Q5,Q8	FDMS8660AS	Fairchild[7]	20A LS FET	2
or	Si7636DP	Vishay[1]		
Q3, Q2	Not Fitted		20A HS FET	0
Q7, Q6	Not Fitted		20A LS FET	0
R2,R3,R4	CRCW06031002FKEA	Vishay[1]	10K , 0603	3
R18	CRCW06034751FKEA	Vishay[1]	4.75k, 0603	1
R17	CRCW06031001FKEA	Vishay[1]	1k, 0603	1
R10,R11	CRCW06032210FKEA	Vishay[1]	221 ohm, 0603	2
R9,R12	CRCW12062R00FKEA	Vishay[1]	2 ohms, 1206	2
R20	CRCW06033011FKEA	Vishay[1]	3.01k, 0603	1
R19	CRCW06033920FKEA	Vishay[1]	392 ohms, 0603	1
R15	CRCW06033651FKEA	Vishay[1]	3.65k, 0603	1

Item	Part Number	Manufacturer	Description	Qty.
R16	CRCW06034991FKEA	Vishay[1]	4.99k, 0603	1
R1	CRCW060310R0FKEA	Vishay[1]	10 ohms, 0603	1
R21	CRCW06033650FKEA	Vishay[1]	365 ohms , 0603	1
R22	OPEN		OPEN, NF	1
U1	**MIC2150YML**	**Micrel Semiconductor [8]**	**MIC2150 2-Phase Dual Output PWM Synchronous Buck Control IC**	1

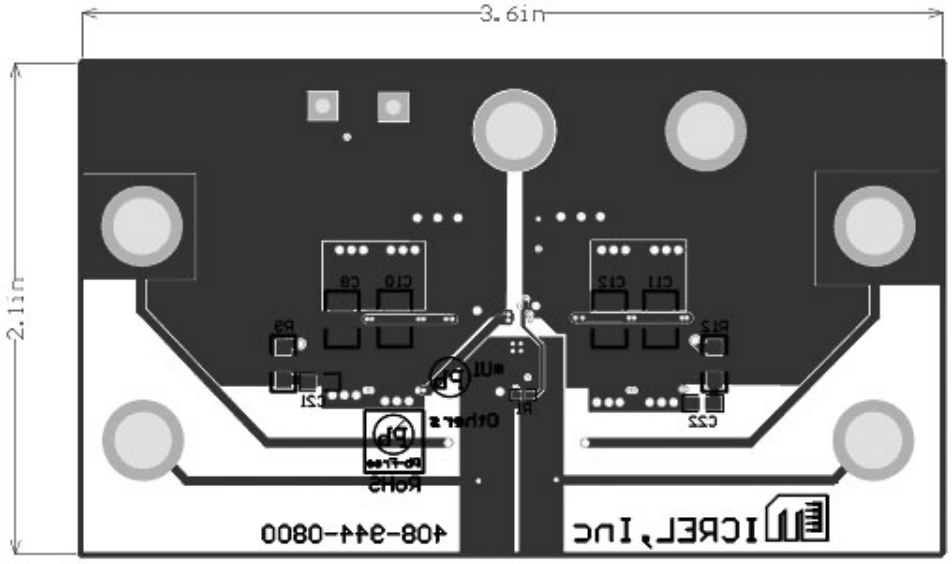
Notes:

1. Vishay.: www.vishay.com
2. Murata: www.murata.com
3. AVX: www.avx.com
4. TDK: www.tdk.com
5. Diodes Inc.: www.diodes.com
6. Cooper Electronics: www.cooperet.com
7. Fairchild Semiconductor: www.fairchildsemi.com
8. **Micrel, Inc.:** www.micrel.com

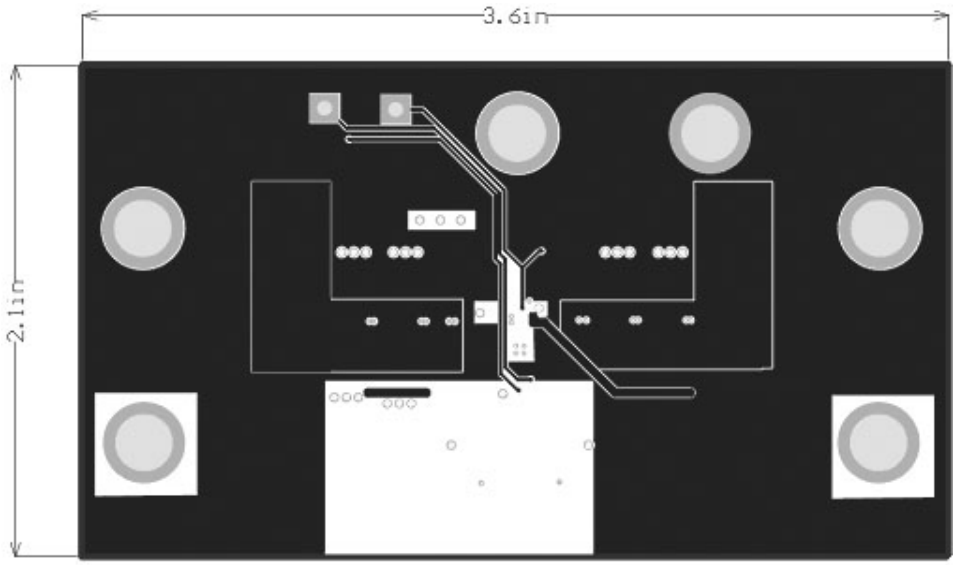
Recommended Layout



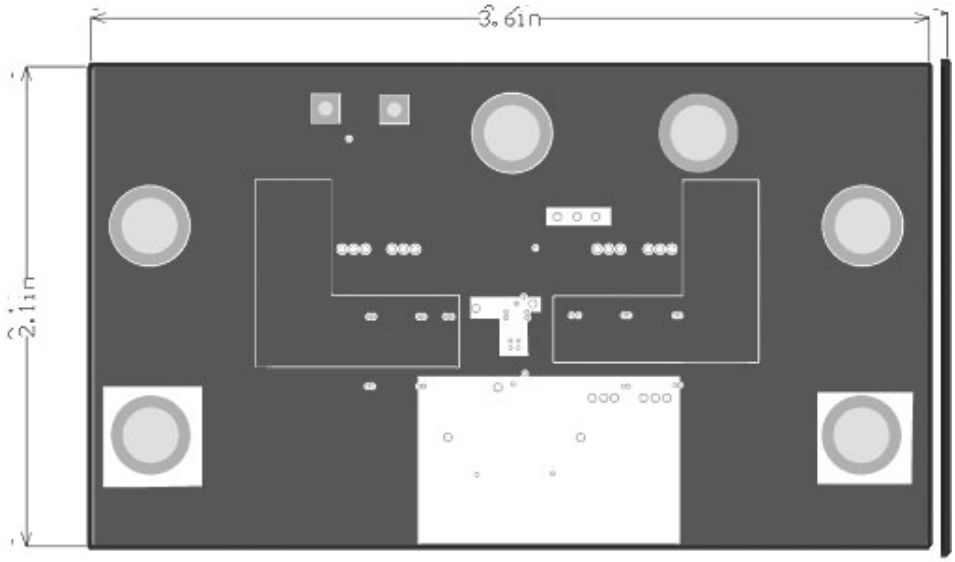
Top Copper



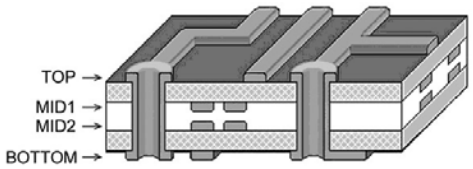
Bottom Copper



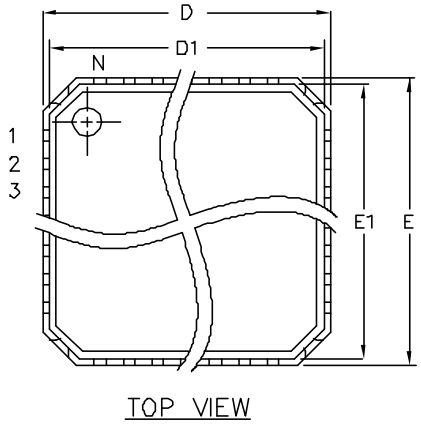
Mid Layer 1

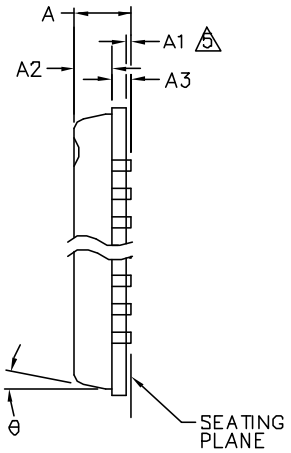


Mid Layer 2

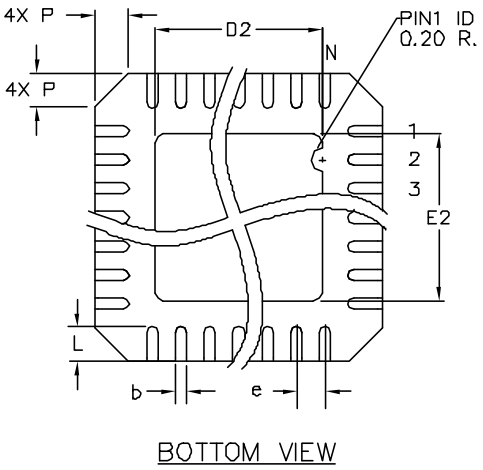


Package Information





	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	–	0.85	1.00
A1	0.00	0.01	0.05
A2	–	0.65	0.80
A3		0.20 REF.	
D		4.00 BSC	
D1		3.75 BSC	
D2	2.19	2.34	2.49
E		4.00 BSC	
E1		3.75 BSC	
E2	2.19	2.34	2.49
θ			12°
P	0.24	0.42	0.60
e		0.50 BSC	
N		24	
L	0.30	0.40	0.50
b	0.18	0.23	0.30



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE NUMBER OF TERMINALS.
   THE NUMBER OF TERMINALS PER SIDE IS N/4.
3. THE PIN#1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. PACKAGE WARPAGE MAX 0.05mm.
5. APPLIED FOR EXPOSED PAD AND TERMINALS.

24-Lead MLF (ML)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com