SCP51460

LDO Regulator - High Accuracy, Low Noise

20 mA

The SCP51460 is a low cost, low power, high accuracy LDO voltage regulator. This device will supply output current up to 20 mA at fixed output voltage 3.3 V with excellent regulation characteristics, making it ideal for precision regulator applications. It is designed to be stable without output capacitor. This is an important feature, when fast rise times and PCB space are in concern. The protective features include Short Circuit Current and Reverse Voltage Protection. The SCP51460 is packaged in 3 leads surface mount SOT−23 package.

Features

- Fixed Output Voltage 3.3 V
- V_{OUT} Accuracy 1% over 0 to +100°C
- Wide Input Voltage Range up to 28 V
- Low Quiescent Current
- Low Noise
- Reverse Battery Protection
- Stable Without Output Capacitor
- Available in 3 leads SOT−23 Package
- This Device is Pb−Free and is RoHS Compliant

Typical Applications

- Handheld Instruments
- Precision Regulators
- Data Acquisition Systems
- High Accuracy Micropower Supplies

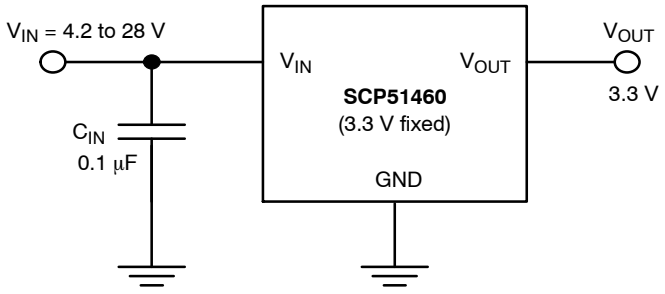

Figure 1. Typical Application Schematics

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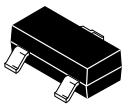
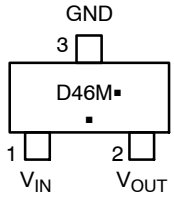


SOT−23−3
SN1 SUFFIX
CASE 318

MARKING DIAGRAM AND PIN ASSIGNMENT



(Top View)

D46 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{IN}	Positive Input Voltage
2	V_{OUT}	Regulated Output Voltage
3	GND	Power Supply Ground; Device Substrate

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	30	V
Reverse Input Voltage	V_{IN}	−15	V
Output Short Circuit Duration (Note 2)	I_{OUT}	∞	sec
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	1000	V
ESD Capability, Machine Model (Note 3)	ESD_{MM}	100	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. With the Input Voltage ≤ 28 V the SCP51460 is able to withstand an infinitely long time under Short Circuit Condition.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latch up Current Maximum Rating: tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT23−3 package Thermal Resistance, Junction−to−Ambient (Note 4)	$R_{\theta JA}$	246	°C/W

4. Soldered on 1 oz 50 mm^2 FR4 copper area.

Table 4. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Operating Input Voltage (Note 5)	V_{IN}	V_{OUT} + 0.9	28	V
Operating Ambient Temperature Range	T_A	0	100	°C

5. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS (V_{IN} = V_{OUT} + 2.5 V, I_{OUT} = 0, C_{IN} = 0.1 μF, C_{OUT} = 0 μF; For typical values T_A = 25°C, for min/max values 0°C ≤ T_A ≤ 100°C unless otherwise noted.) (Note 6).

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Output Voltage		V_{OUT}	3.267 (−1 %)	3.3	3.333 (+1 %)	V
Line Regulation	V_{IN} = V_{OUT} + 0.9 V to 2.5 V V_{IN} = V_{OUT} + 2.5 V to 20 V	Reg_{LINE}	– –	120 75	1000 130	ppm/V
Load Regulation	I_{OUT} = 100 μA, T_A = 25°C I_{OUT} = 10 mA, T_A = 25°C I_{OUT} = 20 mA, T_A = 25°C	Reg_{LOAD}	– – –	1200 210 180	3000 300 300	ppm/mA
Load Regulation	I_{OUT} = 100 μA, 0°C ≤ T_A ≤ 100°C I_{OUT} = 10 mA, 0°C ≤ T_A ≤ 100°C	Reg_{LOAD}	– –	1500 260	4000 300	ppm/mA
Dropout Voltage	Measured at V_{OUT} − 2% I_{OUT} = 0 mA I_{OUT} = 10 mA	V_{DO}	 – –	 0.65 0.94	 0.9 1.4	V
Quiescent Current	I_{OUT} = 0 mA, T_A = 25°C I_{OUT} = 0 mA, 0°C ≤ T_A ≤ 100°C	I_Q	– –	150	180 220	μA
Output Short Circuit Current	V_{OUT} = 0 V, T_A = 25°C	I_{SC}	–	40	–	mA
Reverse Leakage	V_{IN} = − 15 V, T_A = 25°C	I_{LEAK}	–	0.1	10	μA
Output Noise Voltage (Note 7)	f = 0.1 Hz to 10 Hz f = 10 Hz to 1 kHz	V_N	–	13.2 13.2	–	μV_{PP} μV_{rms}

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Peak−to−peak noise is measured with a single pole high pass filter at 0.1 Hz and 2−pole low pass filter at 10 Hz. The unit is enclosed into still−air environment to eliminate thermocouple effects. The test time is set to 10 sec.

TYPICAL CHARACTERISTICS

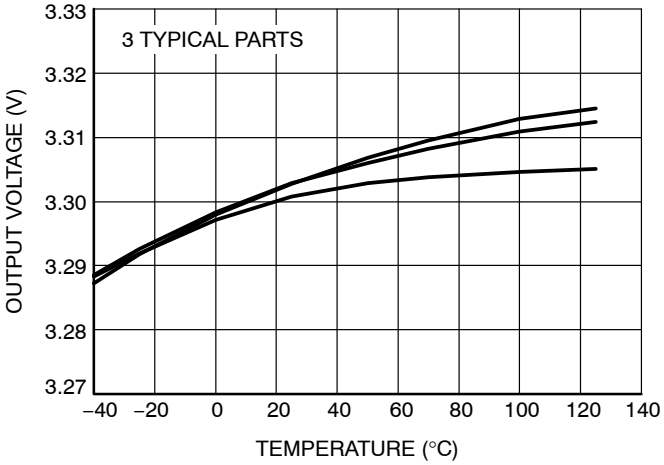


Figure 2. Output Voltage vs. Temperature

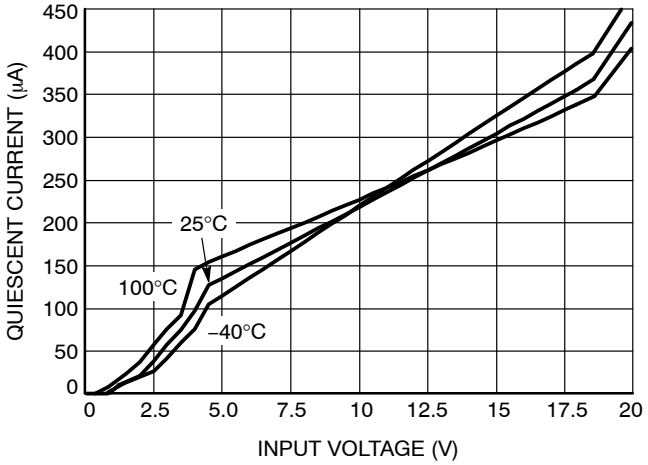


Figure 3. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTICS

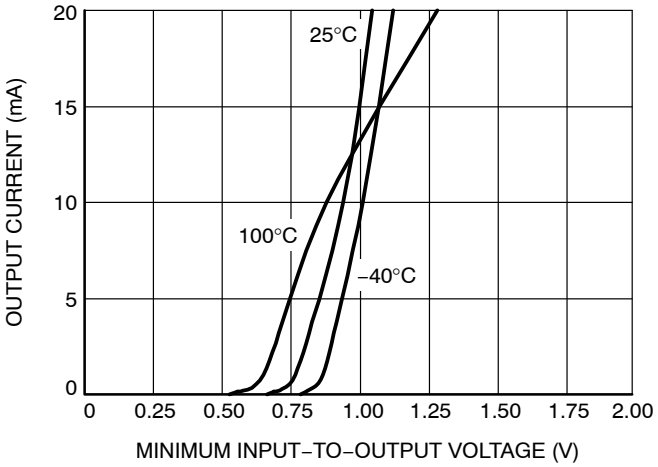


Figure 4. Dropout Voltage vs. Output Current

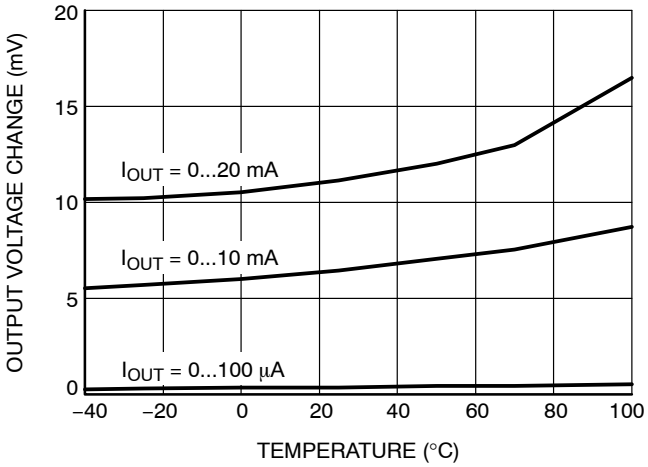


Figure 5. Output Voltage Change vs. Temperature

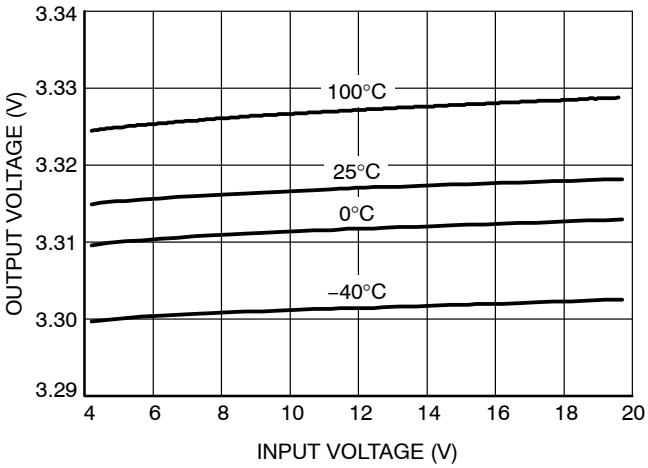


Figure 6. Output Voltage vs. Input Voltage

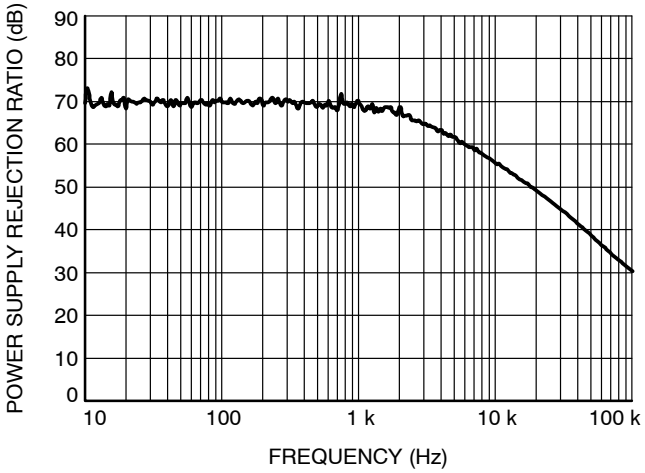


Figure 7. PSRR vs. Frequency

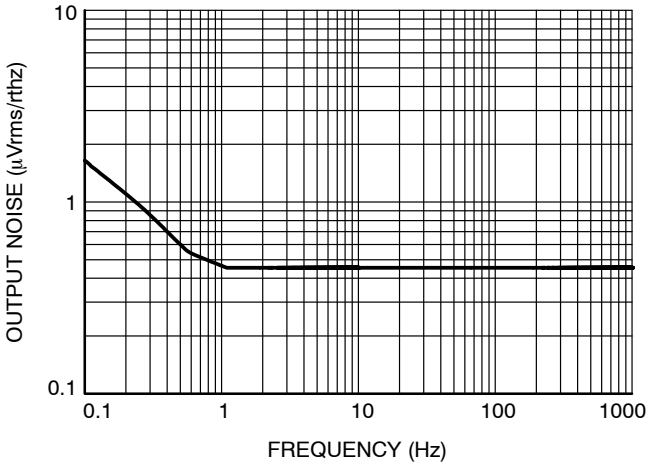


Figure 8. Output Voltage Noise 0.1 Hz – 1 kHz

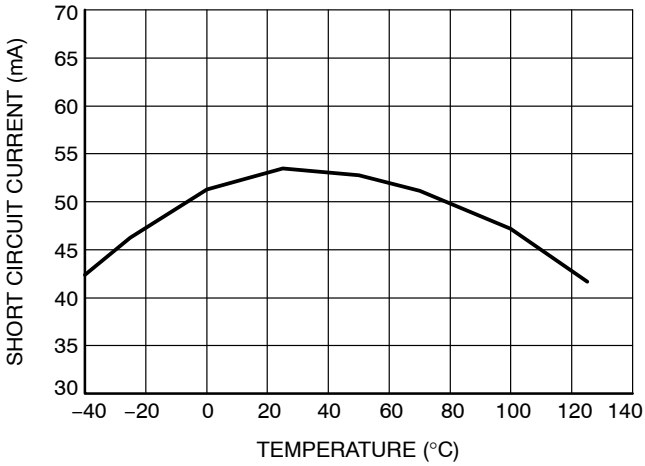


Figure 9. Short Circuit Current vs. Temperature

APPLICATIONS INFORMATION

Input Decoupling Capacitor (C_{IN})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the SCP51460 package. Higher capacitance and lower ESR will improve the overall line transient response.

Output Decoupling Capacitor (C_{OUT})

The SCP51460 does not require any output capacitance to be stable. With no capacitor at the output the device will have faster V_{OUT} rise time and will occupy less PCB space. In some applications however the output capacitor could be added. This will improve the overall transient response. During the transients capacitors with low ESR (e.g. Ceramic capacitors) will cause more ringing than the Tantalum or Aluminum Capacitors.

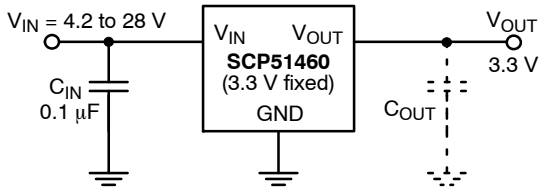


Table 6 shows the maximum capacitance of C_{OUT} for various load currents to avoid instability.

Table 6.

I_{OUT} = 100 μA	I_{OUT} = 1 mA	I_{OUT} = 10 mA	I_{OUT} = 20 mA
>10 μF	>10 μF	1 μF	0.68 μF

Thermal Characteristics

As power dissipation in the SCP51460 increases, it may become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. The board material and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the SCP51460 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

Since T_J is not recommended to exceed 100°C ($T_{J(MAX)}$), then the SCP51460 can dissipate up to 305 mW when the ambient temperature (T_A) is 25°C.

The power dissipated by the SCP51460 can be calculated from the following equations:

$$P_D \approx V_{in}(I_{GND}@I_{out}) + I_{out}(V_{in} - V_{out}) \quad \text{(eq. 2)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + (V_{out} \cdot I_{out})}{I_{out} + I_{GND}} \quad \text{(eq. 3)}$$

Hints

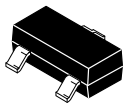
V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the SCP51460, and make traces as short as possible.

ORDERING INFORMATION

Device	Device Code	Package	Shipping†
SCP51460SN33T1G	D46	SOT23−3 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

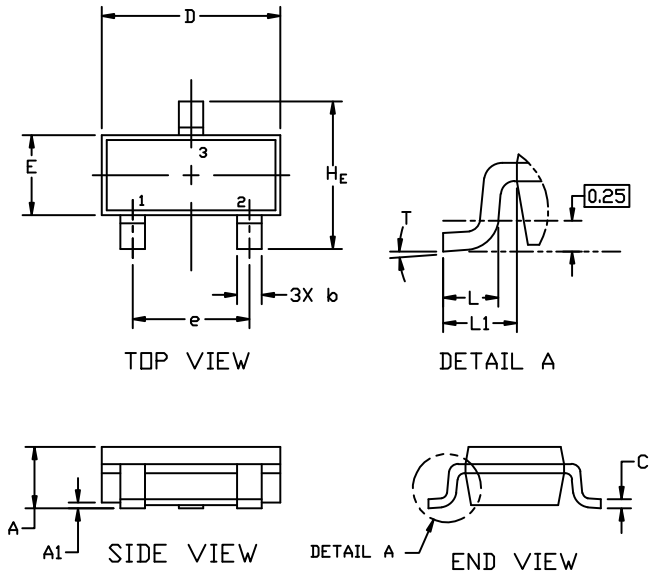
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 4:1

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

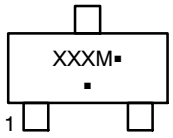


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

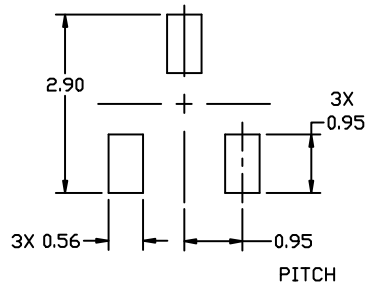
	MILLIMETERS			INCHES		
DIM	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42226B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23 (TO−236)**		**PAGE 1 OF 2**

SOT−23 (TO−236)
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

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