Crystal or Differential to Differential Clock Fanout Buffer

IDT8T3910I

PRELIMINARY DATA SHEET

General Description

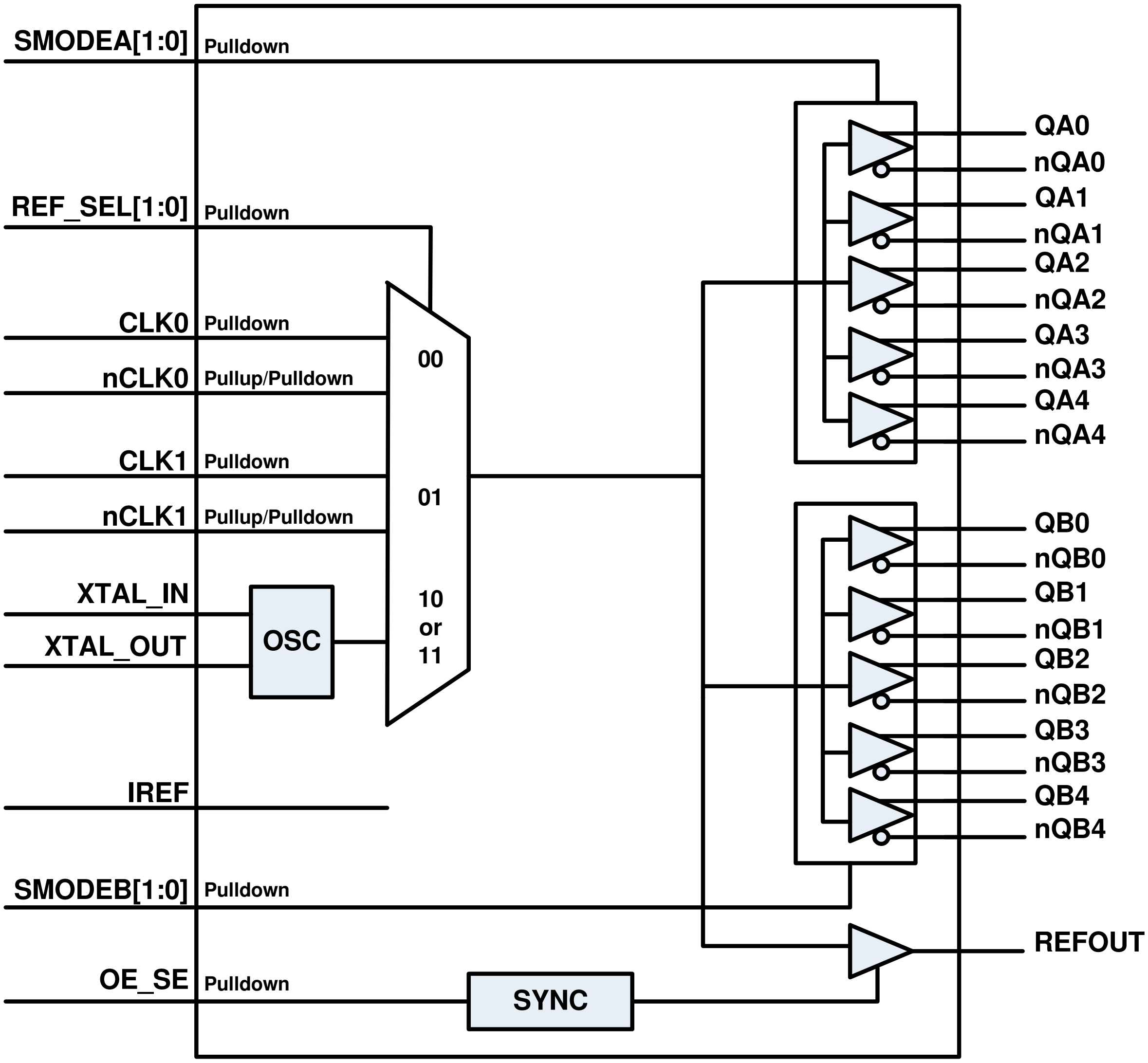
The IDT8T3910I is a high-performance clock fanout buffer. The input clock can be selected from two differential inputs or one crystal input. The internal oscillator circuit is automatically disabled if the crystal input is not selected. The selected signal is distributed to ten differential outputs which can be configured as LVPECL, LVDS or HSCL outputs. In addition, an LVCMOS output is provided. The user should always turn off this LVCMOS output when (the) clock is over 200MHz. The differential outputs can be disabled into an high-impedance state. The device is designed for signal fanout of high-frequency, low phase-noise clock and data signal. The outputs are at a defined level when inputs are open or shorted. It's designed to operate from a 3.3V core power supply, and either a 3.3V or 2.5V output operating supply.

Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 40MHz
- Two banks, each has five differential output pairs that can be configured as LVPECL or LVDS or HCSL
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: (Bank A and Bank B at the same output level) 32ps (typical)
- Part-to-part skew: 200ps (typical)
- Additive RMS phase jitter: 0.22ps (typical)
- Power supply modes:
- Output supply voltage modes:
  V_{CC}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Block Diagram



Pin Assignment

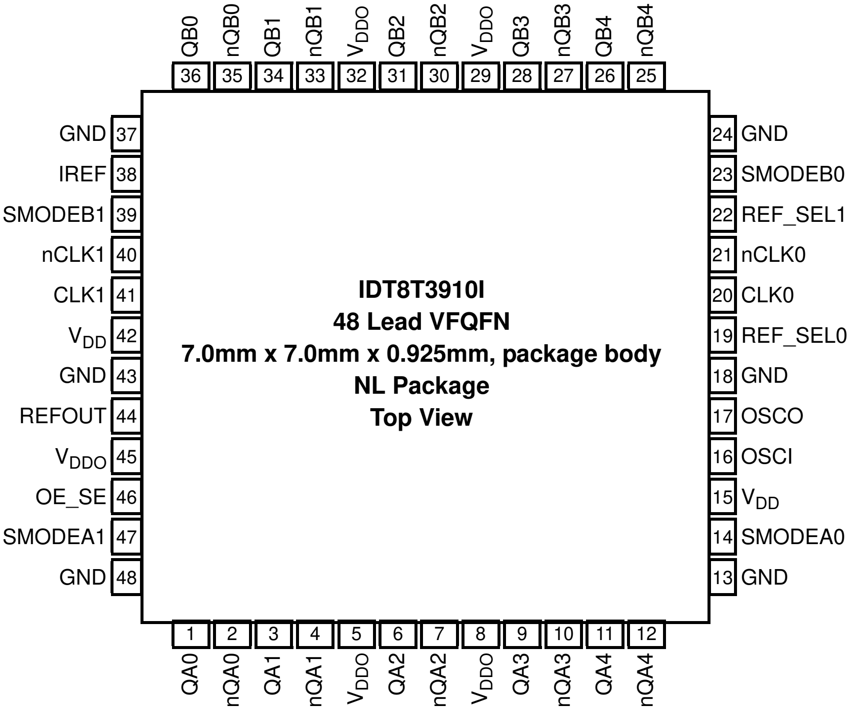


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
3, 4	QA1, nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5, 8, 29, 32, 45	V_{DDO}	Power		Output supply pins.
6, 7	QA2, nQA2	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
9, 10	QA3, nQA3	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
11, 12	QA4, nQA4	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
13, 18, 24, 37, 43, 48	GND	Power		Power supply ground.
14, 47	SMODEA0, SMODEA1	Input	Pulldown	Output driver select for Bank A outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
15, 42	V_{DD}	Power		Power supply pins.
16, 17	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
19, 22	REF_SEL0, REF_SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3A for function.
20	CLK0	Input	Pulldown	Non-inverting differential clock.
21	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to $V_{DD}/2$.
23, 39	SMODEB0, SMODEB1	Input	Pulldown	Output driver select for Bank B outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
25, 26	nQB4, QB4	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
27, 28	nQB3, QB3	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
30, 31	nQB2, QB2	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
33, 34	nQB1, QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
35, 36	nQB0, QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
38	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QXx, nQXx clock outputs.
40	nCLK1	Input	Pullup/ Pulldown	Non-inverting differential clock. Internal resistor bias to $V_{DD}/2$.
41	CLK1	Input	Pulldown	Inverting differential clock.
44	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels
46	OE_SE	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels. See Table 3B.

NOTE: *Pulldown and Pullup* refer to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance	V_{DDO} = 3.3V		10		pF
		V_{DDO} = 2.5V		9		pF
R_{OUT}	Output Impedance	V_{DDO} = 3.3V		15		Ω
		V_{DDO} = 2.5V		18		Ω

Function Tables

Table 3A. REF_SELx Function Table

Control Input	
REF_SEL[1:0]	**Selected Input Reference Clock**
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
10	XTAL
11	XTAL

Table 3B. OE_SE Function Table

OE_SE	REF_OUT
0 (default)	High-Impedance
1	Enabled

NOTE: Synchronous output enable to avoid clock glitch.

Table 3C. Input/Output Operation Table, OE_SE

Input Status			Output State
OE_SE	REF_SEL [1:0]	CLKx and nCLKx	REFOUT
0	Not care	Don’t Care	High Impedance
1	10 or 11	Don’t Care	Fanout crystal oscillator
1	00	CLK0 and nCLK0 are both open circuit	Logic low
		CLK0 and nCLK0 are tied to ground	Logic low
		CLK0 is high, nCLK0 is low	Logic High
		CLK0 is low, nCLK0 is high	Logic Low
1	01	CLK1 and nCLK1 are both open circuit	Logic low
		CLK1 and nCLK1 are tied to ground	Logic low
		CLK1 is high, nCLK1 is low	Logic High
		CLK1 is low, nCLK1 is high	Logic Low

NOTE: The device output should support differential input being driven by a single-ended signal.

Table 3D. Input/Output Operation Table, SMODEA

Input Status			Output State
SMODEA[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QA[4:0], nQA[4:0]
11	Not care	Don’t Care	High Impedance
00,01,or 10	10 or 11	Don’t Care	Fanout crystal oscillator
00,01,or 10	00	CLK0 and nCLK0 are both open circuit	QA[4:0]=Low nQA4:0]=High
		CLK0 and nCLK0 are tied to ground	QA[4:0]=Low nQA[4:0]=High
		CLK0 is high, nCLK0 is low	QA[4:0]=High nQA[4:0]=Low
		CLK0 is low, nCLK0 is high	QA[4:0]=Low nQA[4:0]=High
00,01,or 10	01	CLK1 and nCLK1 are both open circuit	QA[4:0]=Low nQA4:0]=High
		CLK1 and CLK1 are tied to ground.	QA[4:0]=Low nQA[4:0]=High
		CLK1 is high, nCLK1 is low	QA[4:0]=High nQA[4:0]=Low
		CLK1 is low, nCLK1 is high	QA[4:0]=Low nQA4:0]=High

NOTE: The device output should support differential input being driven by a single-ended signal.

Table 3E. Input/Output Operation Table, SMODEB

Input Status			Output State
SMODEB[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QB[4:0], nQB[4:0]
11	Not care	Don't Care	High Impedance
00,01,or 10	10 or 11	Don't Care	Fanout crystal oscillator
00,01,or 10	00	CLK0 and nCLK0 are both open circuit	QB[4:0]=Low nQB4:0]=High
		CLK0 and nCLK0 are tied to ground	QB[4:0]=Low nQB[4:0]=High
		CLK0 is high, nCLK0 is low	QB[4:0]=High nQB[4:0]=Low
		CLK0 is low, nCLK0 is high	QB[4:0]=Low nQB[4:0]=High
00,01,or 10	01	CLK1 and nCLK1 are both open circuit	QB[4:0]=Low nQB[4:0]=High
		CLK1 and nCLK1 are tied to ground	QB[4:0]=Low nQB[4:0]=High
		CLK1 is high, nCLK1 is low	QB[4:0]=High nQB[4:0]=Low
		CLK1 is low, nCLK1 is high	QB[4:0]=Low nQB[4:0]=High

NOTE: The device output should support differential input being driven by a single-ended signal.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O, (HCSL, LVCMOS)	-0.5V to V_{DD} + 0.5V
Outputs, I_O, (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O, (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	29°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±5\%$, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01		67		mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01		264		mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)		165		mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10		80		mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10		22		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01		67		mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01		263		mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)		164		mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10		80		mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10		18		mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% or 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V±5%	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V±5%	-0.3		0.8	V
I_{IH}	Input High Current	REF_SEL, SMODEA, SMODEB, OE_SE	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	OE_SE	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	REFOUT	V_{DDO} = 3.3V±5%	2.6			V
		REFOUT	V_{DDO} = 2.5V±5%	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	REFOUT	V_{DDO} = 3.3V±5% or 2.5V±5%			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

Table 4D. Differential DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% or 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[0:1], nCLK[0:1]	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK[0:1]	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK[0:1]	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as V_{IH}.

Table 4E. LVPECL DC Characteristics, V_{DD} = V_{DDO} = 3.3V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} – 1.4		V_{DDO} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} – 2.0		V_{DDO} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{DDO} – 2V.

Table 4F. LVPECL DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} – 1.4		V_{DDO} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} – 2.0		V_{DDO} – 1.4	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs termination with 50Ω to V_{DDO} – 2V.

Table 4G. LVDS DC Characteristics, $V_{DD} = V_{DDO} = 3.3V±5\%$, GND = 0V, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			405		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.26		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 4H. LVDS DC Characteristics, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, GND = 0V, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			405		mV
ΔV_{OD}	V_{OD} Magnitude Change			50		mV
V_{OS}	Offset Voltage			1.26		V
ΔV_{OS}	V_{OS} Magnitude Change			50		mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal	10		40	MHz
		LVDS, LVPECL output		500		MHz
		HCSL output			250	MHz
		LVCMOS output			200	MHz
tjit	Additive Phase Jitter:156.25MHz Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01	SMODEA/B[1:0] = 00		0.185		ps
		SMODEA/B[1:0] = 01		0.20		ps
		SMODEA/B[1:0] = 10		0.22		ps
tjit	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz	REF_SEL[1:0] = 10 or 11		0.375		ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1	SMODEA/B[1:0] = 00		1.72		ns
		SMODEA/B[1:0] = 01		1.77		ns
		SMODEA/B[1:0] = 10		2.88		ns
*t*sk(o)	Output Skew; NOTE 2, 3			32		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			200		ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs	-100		100	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs			1150	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs	-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs	250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs			140	mV
	Rise/Fall Edge Rate; NOTE 7, 13	HCSL Outputs; Measured between 150mV to +150mV	0.6		4.0	V/ns
t_R / t_F	Output Rise/Fall Time	SMODEA/B[1:0] = 00; 20% to 80%		430		ps
		SMODEA/B[1:0] = 01; 20% to 80%		515		
$MUX_{\_ISOLATION}$	MUX Isolation	156.25MHz		83		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: Measurement taken from differential waveform.

NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.

NOTE 7: Measurement taken from single-ended waveform.

NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

Notes continued on next page.

NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
Notes continue on next page.
NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Table 6B. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C to 85°C

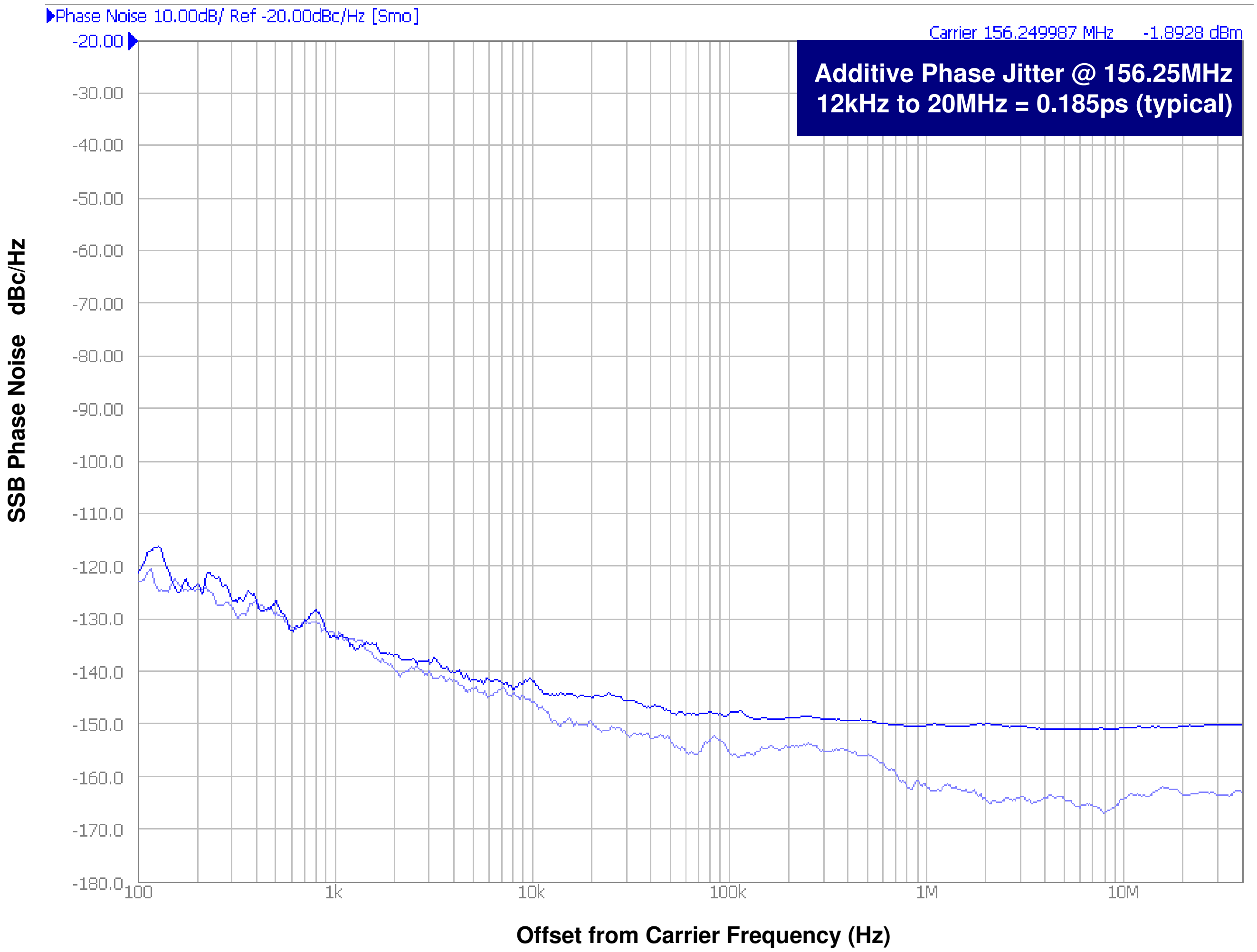
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal	10		40	MHz
		LVDS, LVPECL output		500		MHz
		HCSL output			250	MHz
		LVCMOS output			200	MHz
tjit	Additive Phase Jitter: 156.25 MHz Integration Range: 12kHz - 20 MHz REF_SEL[1:0] = 00 or 10					
		SMODEA/B[1:0] = 00		0.185		ps
		SMODEA/B[1:0] = 01		0.20		ps
		SMODEA/B[1:0] = 10		0.22		ps
tjit	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz	REF_SEL[1:0] = 10 or 11		0.375		ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1	SMODEA/B[1:0] = 00		1.72		ns
		SMODEA/B[1:0] = 01		1.77		ns
		SMODEA/B[1:0] = 10		2.88		ns
*t*sk(o)	Output Skew; NOTE 2, 3			32		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			200		ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs	-100		100	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs			1150	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs	-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs	250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs			140	mV
	Rise/Fall Edge Rate; NOTE 7, 13	HCSL Outputs; Measured between 150mV to +150mV	0.6		4.0	V/ns
t_R / t_F	Output Rise/Fall Time	SMODEA/B[1:0] = 00; 20% to 80%		430		ps
		SMODEA/B[1:0] = 01; 20% to 80%		570		
MUX$_{\_ISOLATION}$	MUX Isolation	156.25MHz		83		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
Notes continued on next page.

NOTE 5: Measurement taken from differential waveform.
NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
NOTE 7: Measurement taken from single-ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Additive Phase Jitter (LVPECL)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

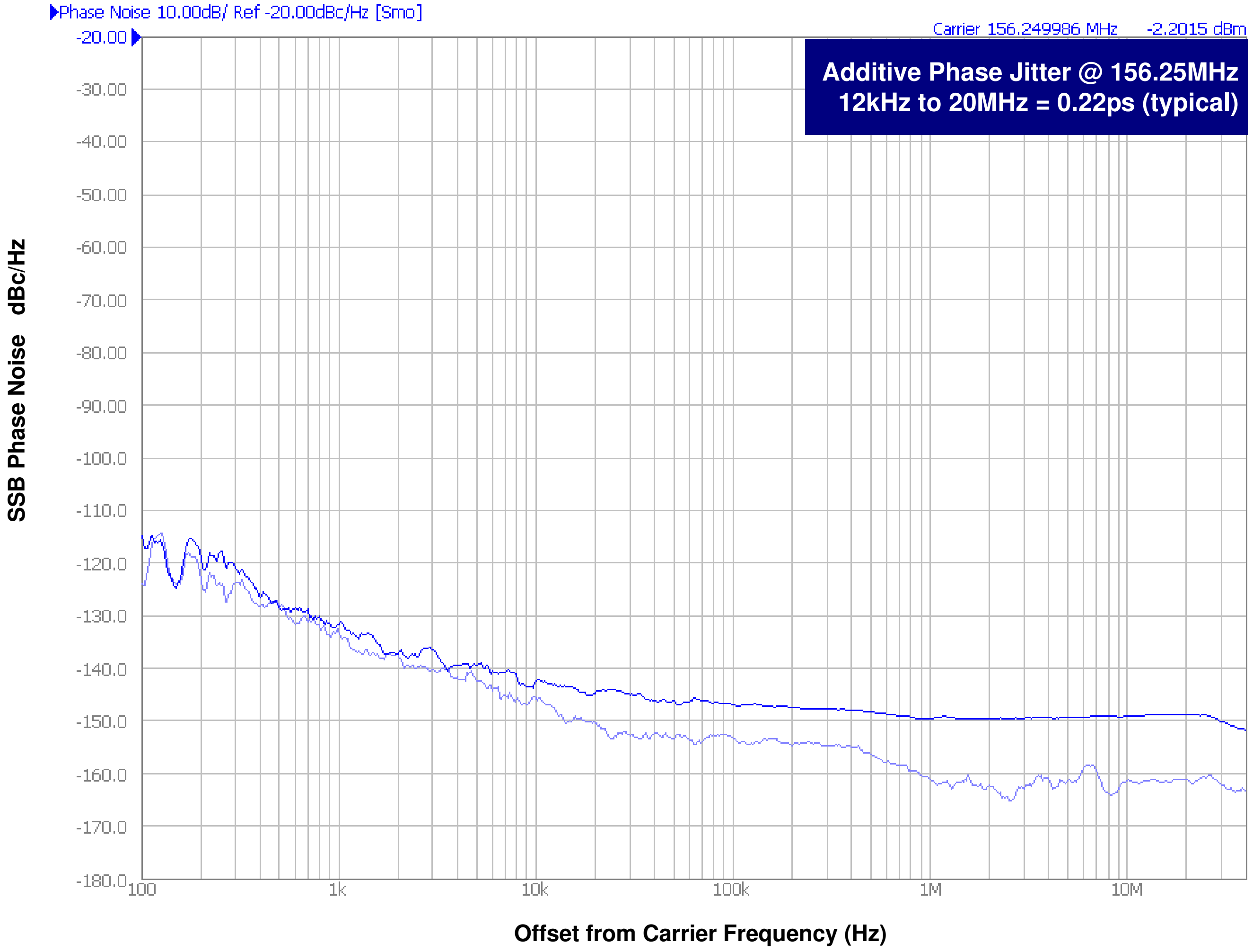


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

The above plot was measured using a Rohde & Schwarz SMA100A as the input source.

Additive Phase Jitter (HCSL)

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

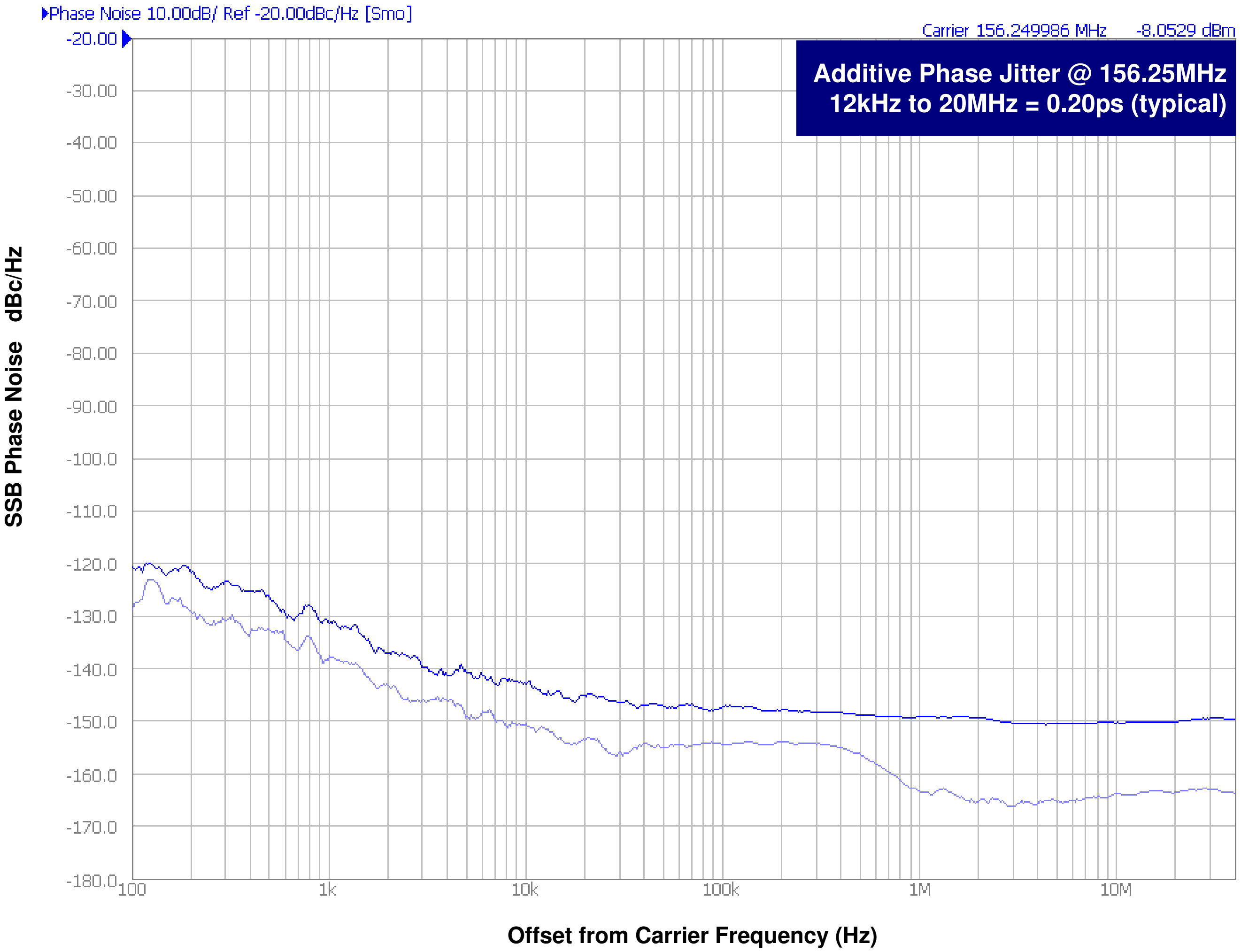


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

The above plot was measured using a Rohde & Schwarz SMA100A as the input source.

Additive Phase Jitter (LVDS)

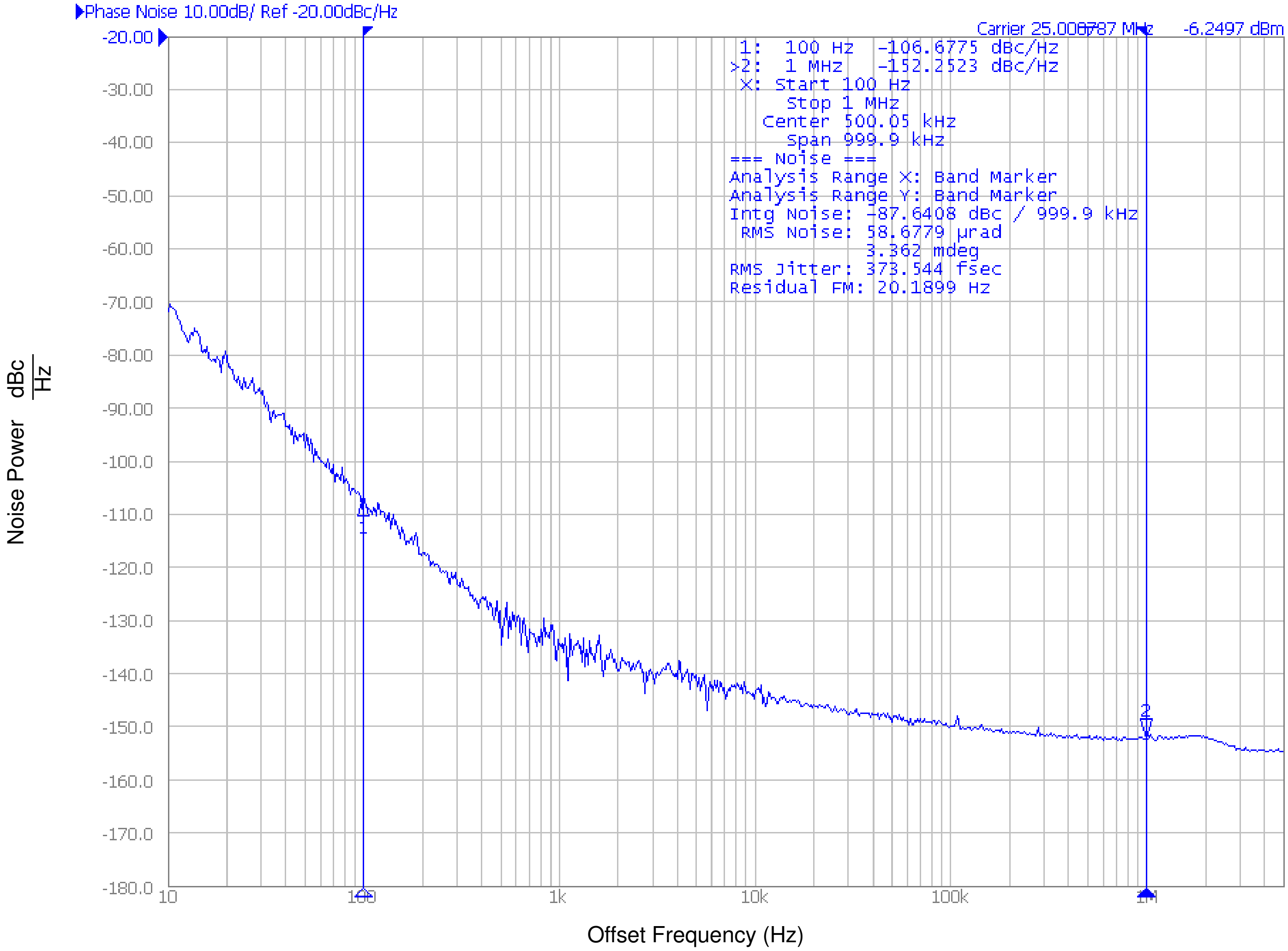
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. The additive phase jitter is dependent on the input source and measurement equipment.

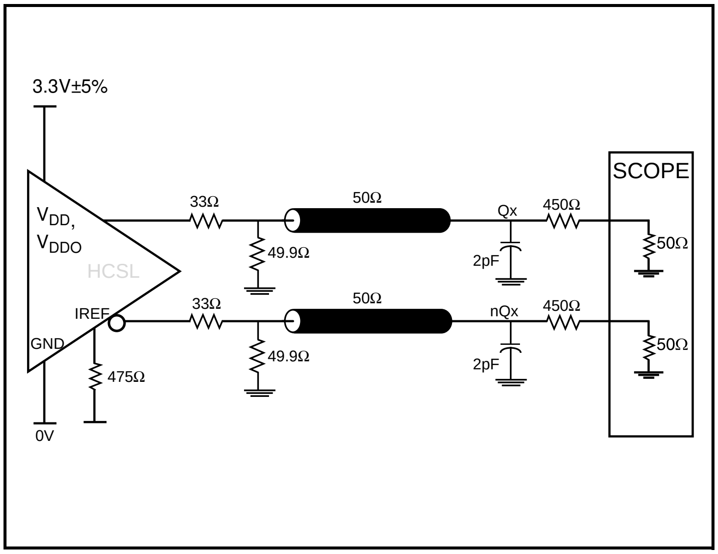
The above plot was measured using a Rohde & Schwarz SMA100A as the input source.

Typical Phase Noise at 25MHz Integration Range: 100Hz - 1MHz

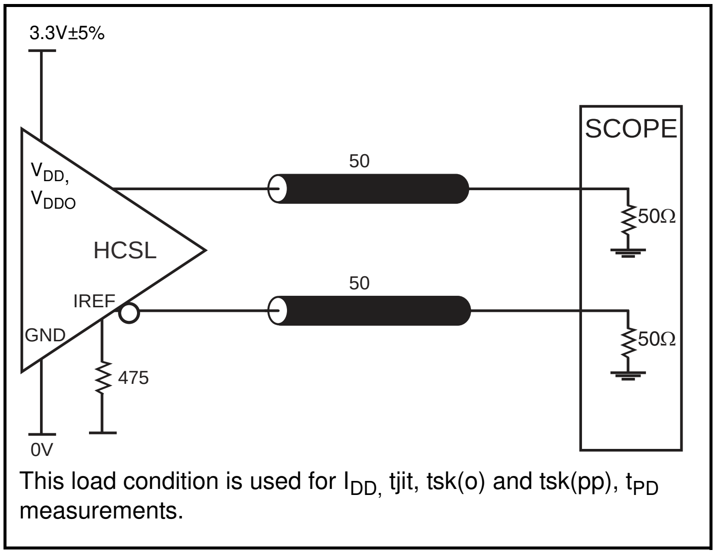


```
 1:  100 Hz  -106.6775 dBc/Hz
>2:  1 MHz   -152.2523 dBc/Hz
 X: Start 100 Hz
      Stop 1 MHz
    Center 500.05 kHz
      Span 999.9 kHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -87.6408 dBc / 999.9 kHz
 RMS Noise: 58.6779 µrad
             3.362 mdeg
RMS Jitter: 373.544 fsec
Residual FM: 20.1899 Hz
```

Parameter Measurement Information

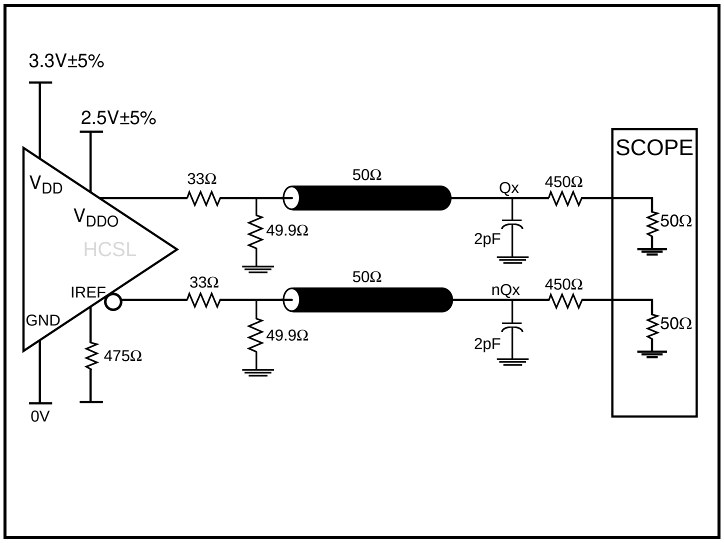


3.3V Core/3.3V HCSL Output Load AC Test Circuit

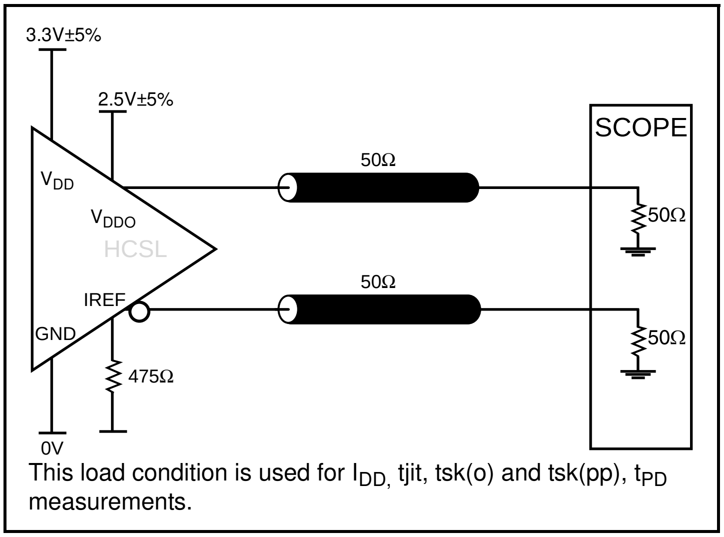


This load condition is used for $I_{DD,}$ tjit, tsk(o) and tsk(pp), t_{PD} measurements.

3.3V Core/3.3V HCSL Output Load AC Test Circuit

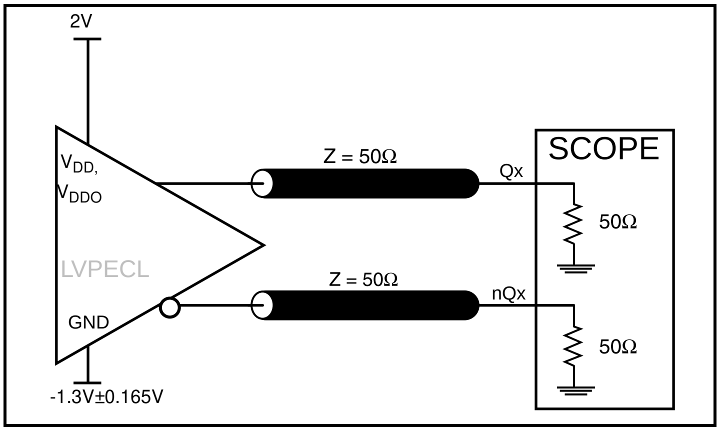


3.3V Core/2.5V HCSL Output Load AC Test Circuit

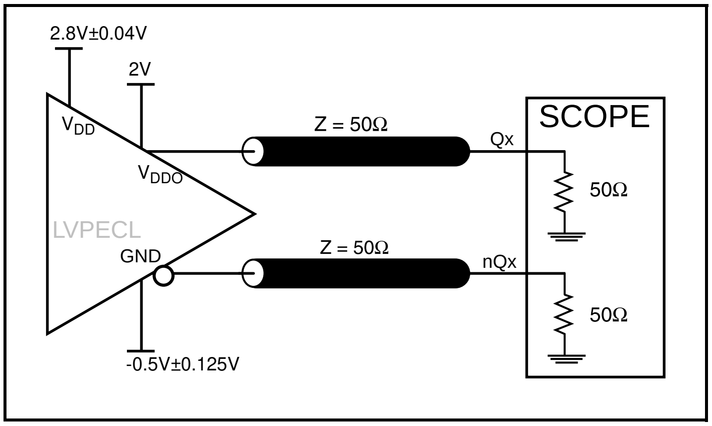


This load condition is used for $I_{DD,}$ tjit, tsk(o) and tsk(pp), t_{PD} measurements.

3.3V Core/2.5V HCSL Output Load AC Test Circuit

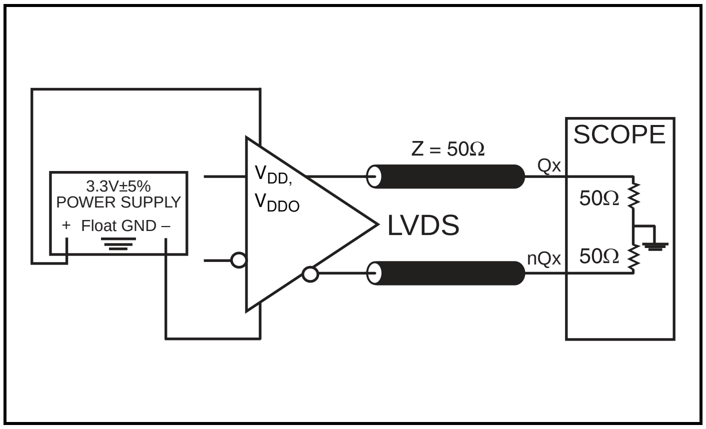


3.3V Core/3.3V LVPECL Output Load AC Test Circuit

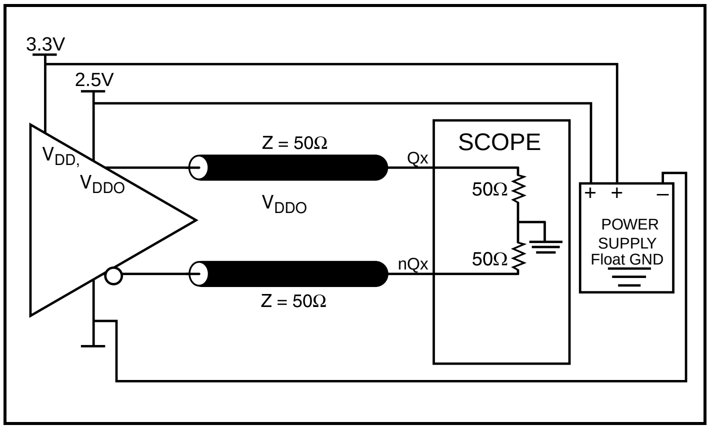


3.3V Core/2.5V LVPECL Output Load AC Test Circuit

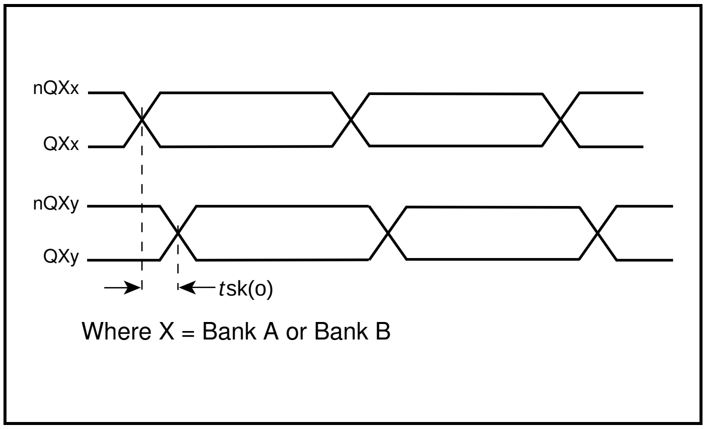
Parameter Measurement Information, continued



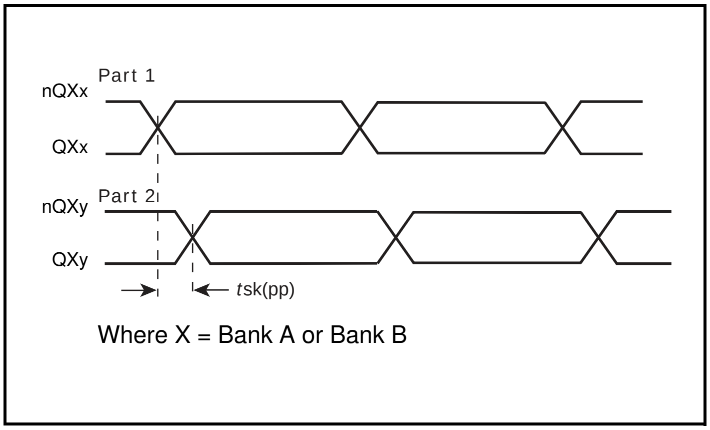
3.3V Core/3.3V LVDS Output Load AC Test Circuit



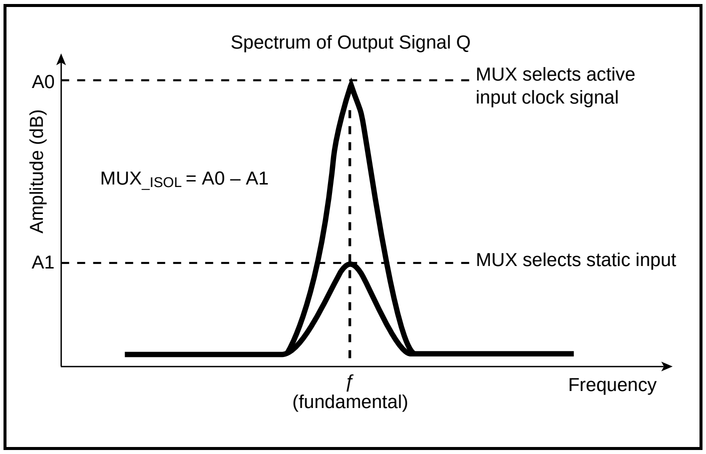
2.5V Core/2.5V LVDS Output Load AC Test Circuit



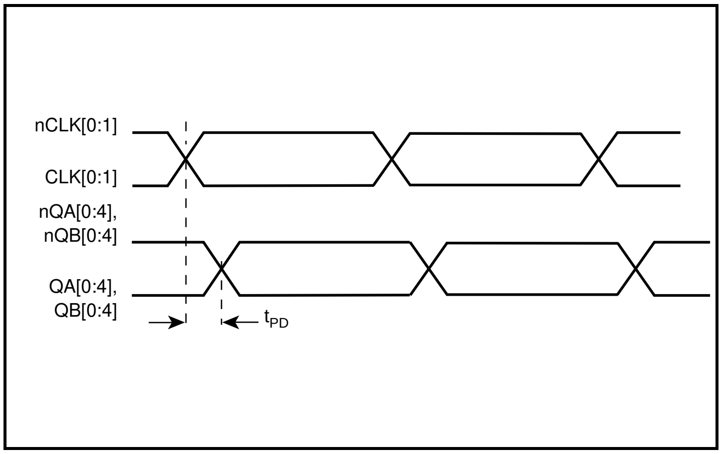
Output Skew



Part-to-Part Skew

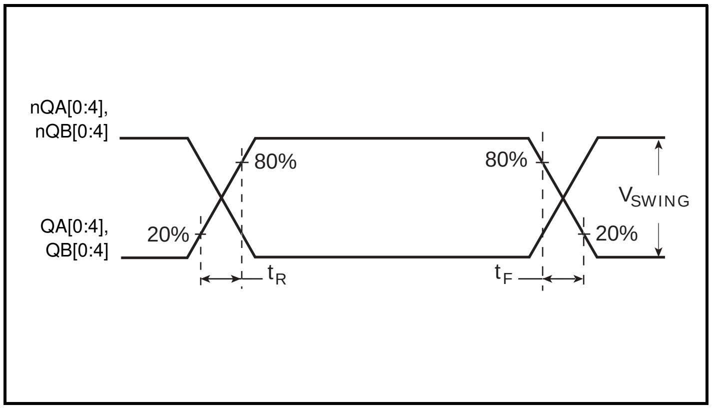


MUX Isolation

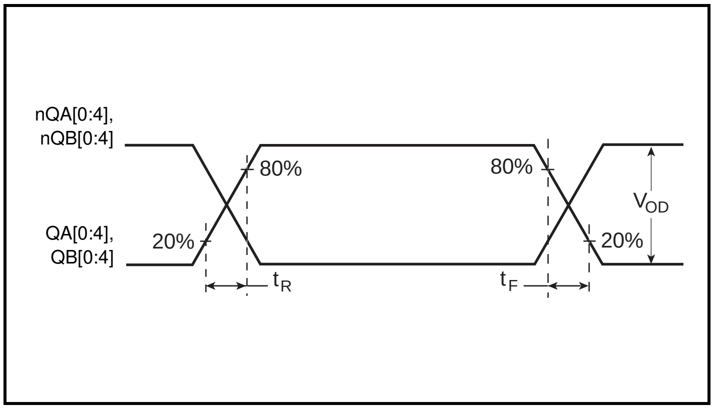


Propagation Delay

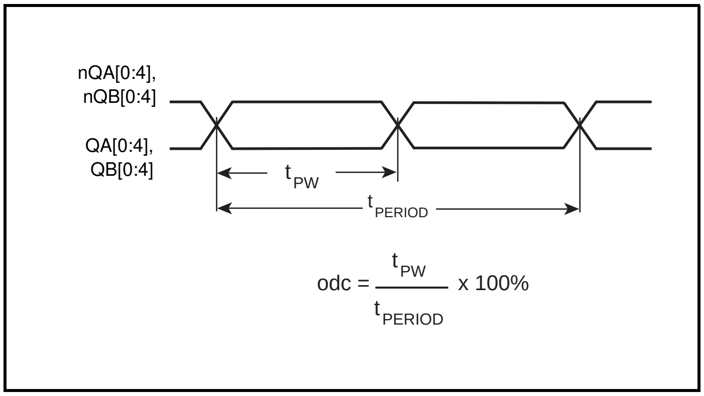
Parameter Measurement Information, continued



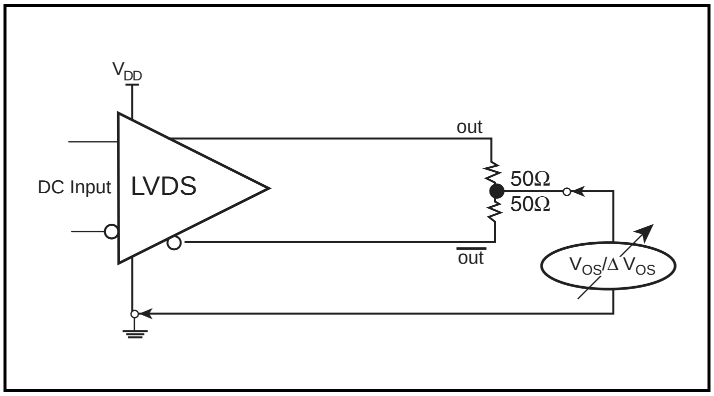
LVPECL Output Rise/Fall Time



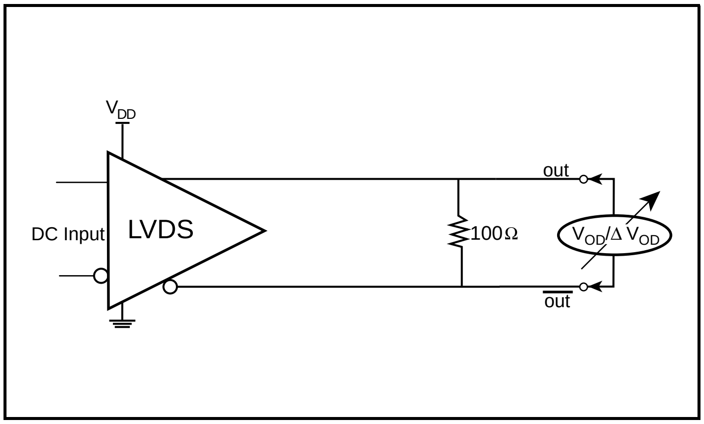
LVDS Output Rise/Fall Time



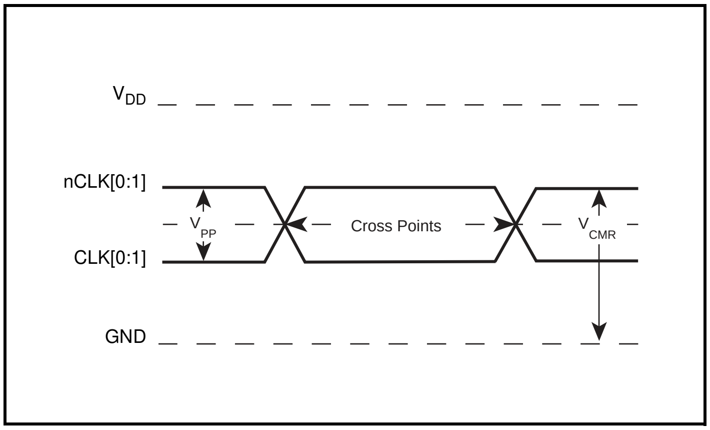
Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup

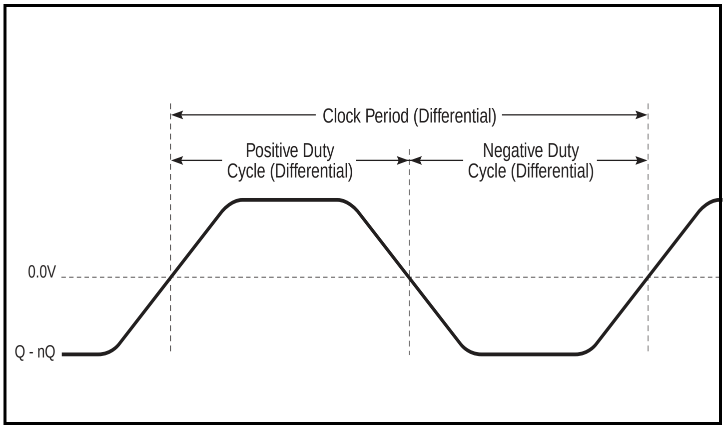


Differential Output Voltage Setup

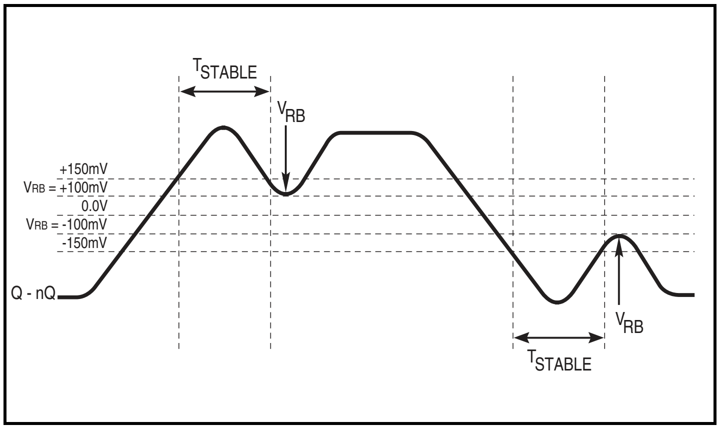


Differential Input Level

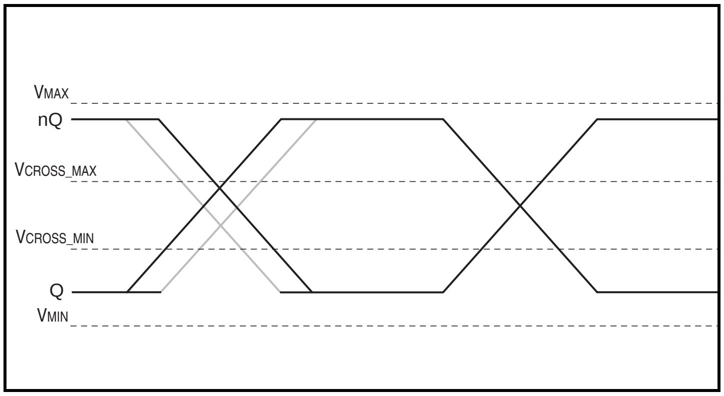
Parameter Measurement Information, continued



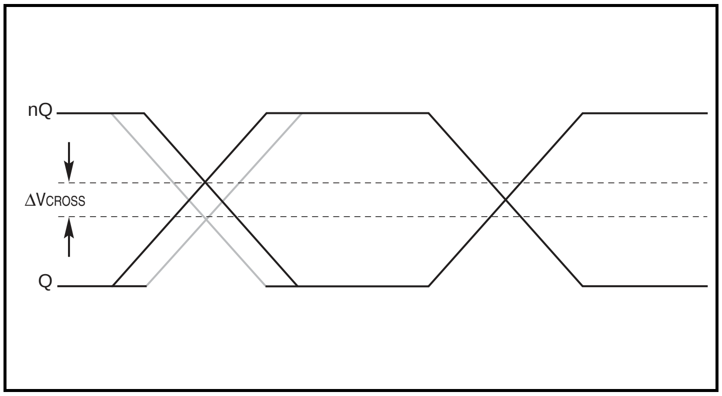
Differential Measurement Points for Duty Cycle/Period



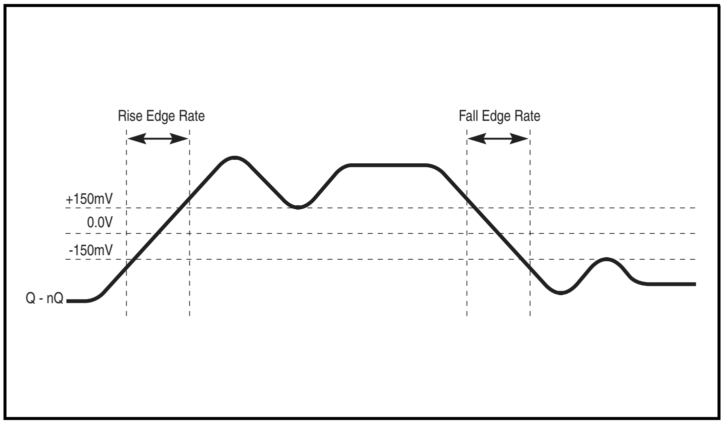
Differential Measurement Points for Ringback



Single-ended Measurement Points for Absolute Cross Point/Swing



Single-ended Measurement Points for Delta Cross Point



Differential Measurement Points for Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating We recommend that there is no trace attached.

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage V_1= V_{DD}/2 is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

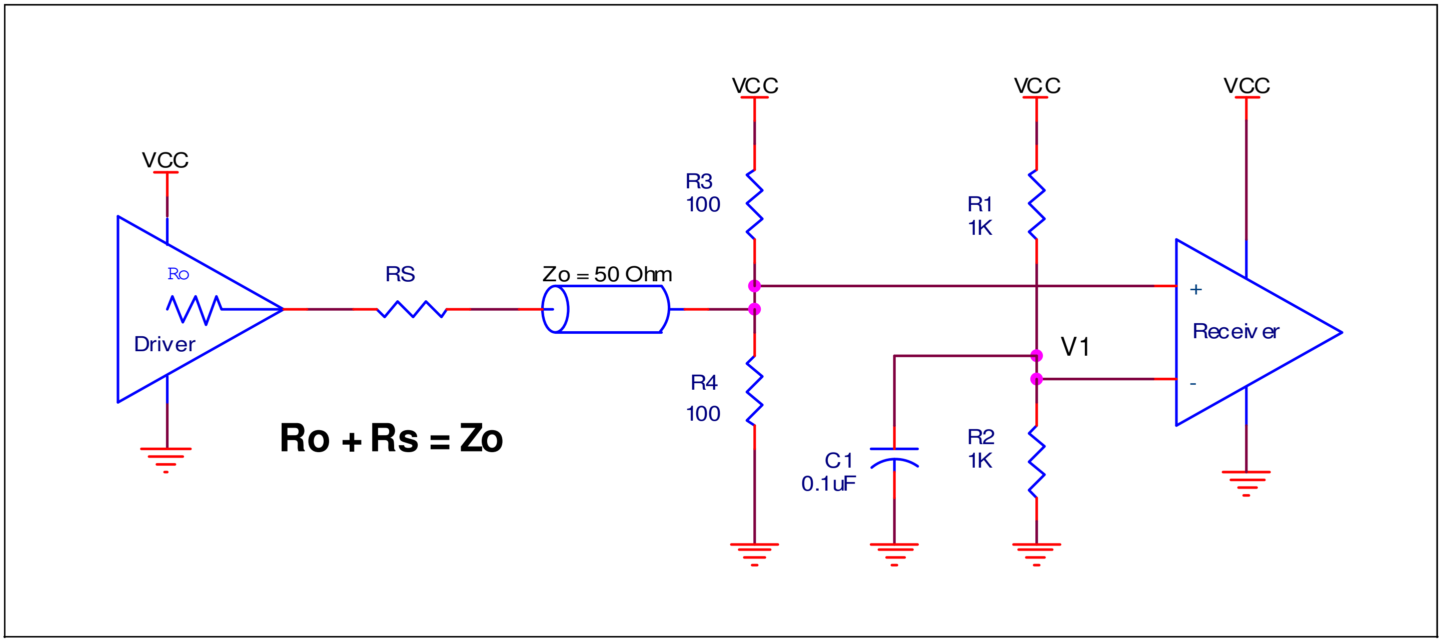


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Crystal Input Interface

The IDT8T3910I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

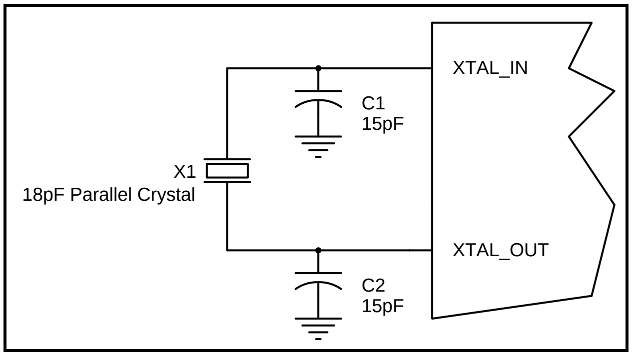


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

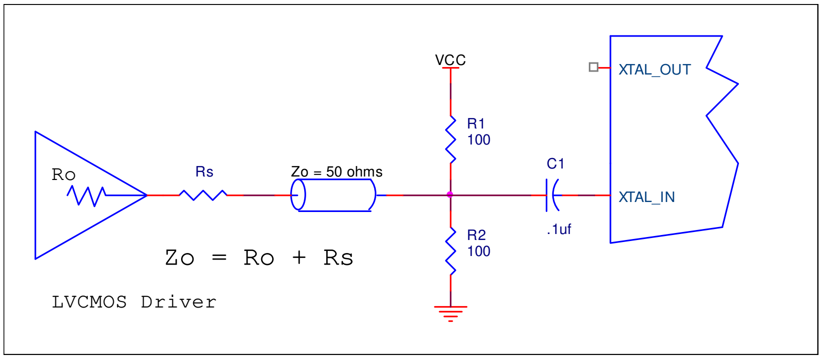


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

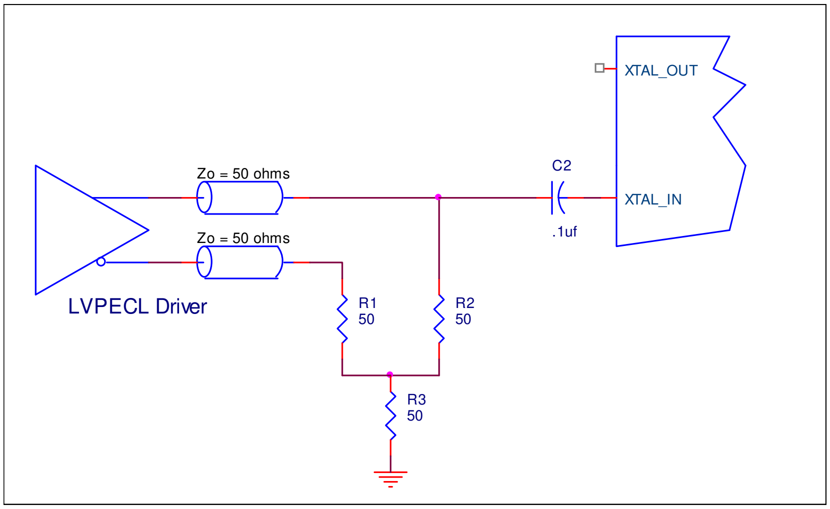


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the CLK /nCLK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

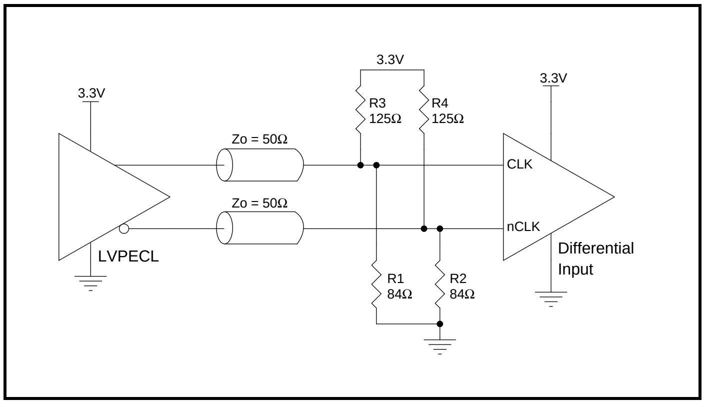


Figure 4A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

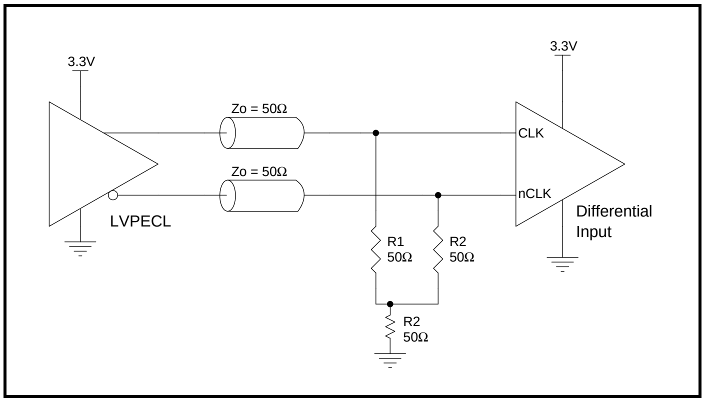


Figure 4B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

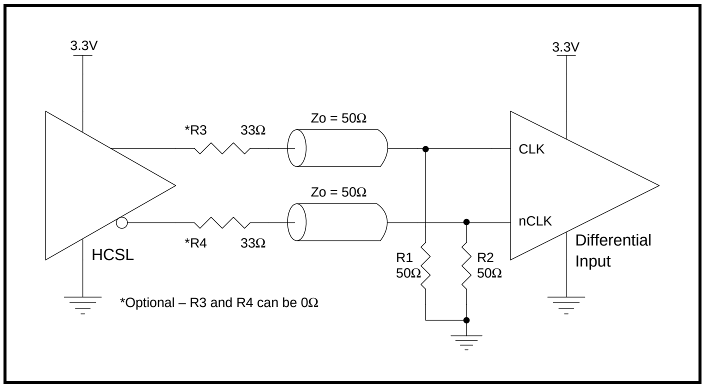


Figure 4C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

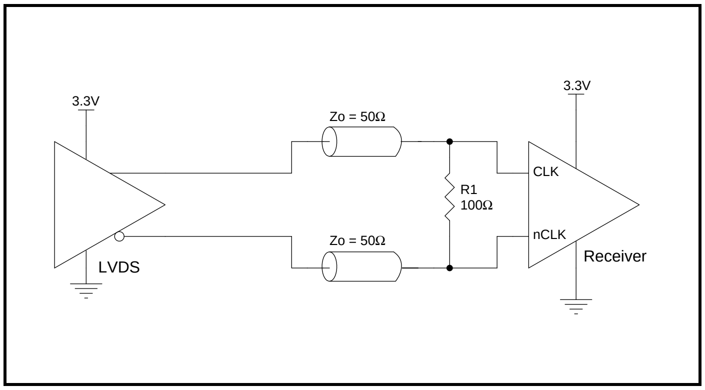


Figure 4D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

Recommended Termination

Figure 5A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

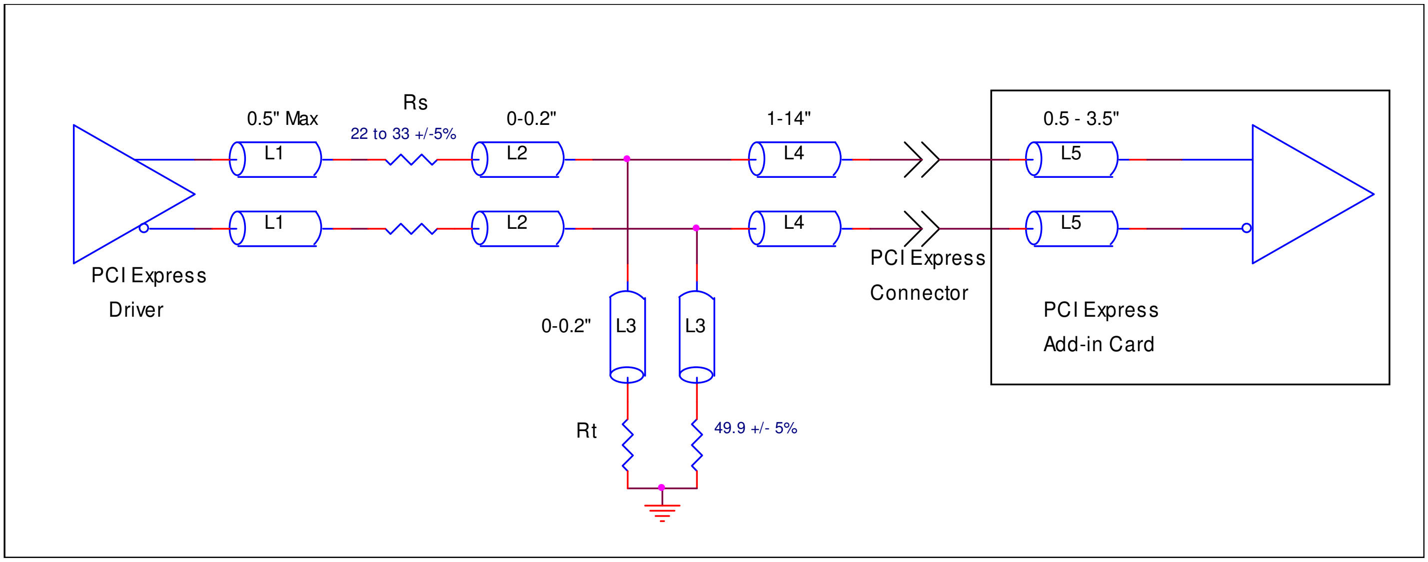


Figure 5A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 5B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

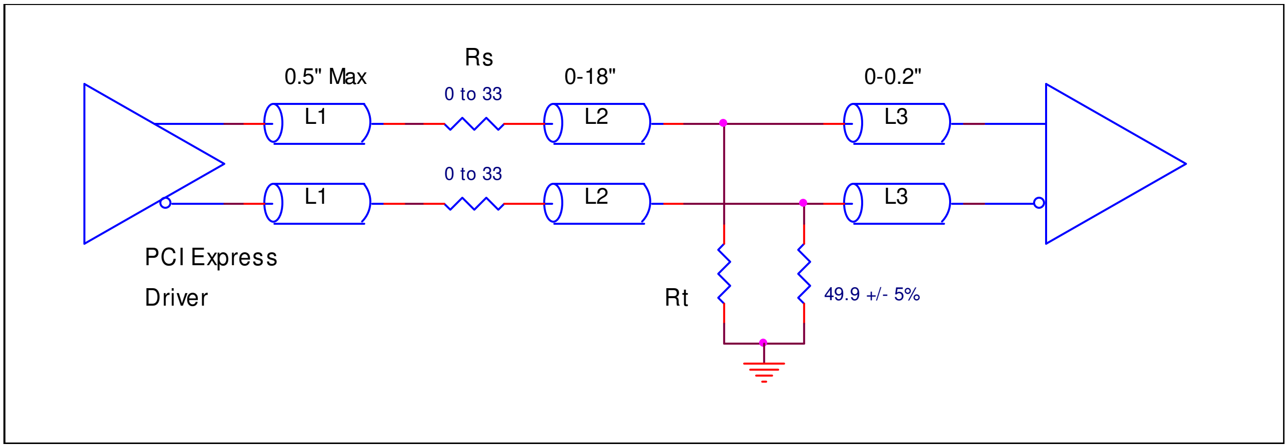


Figure 5B. Recommended Termination (where a point-to-point connection can be used)

LVDS Driver Termination

A general LVDS interface is shown in *Figure 6.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 6 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

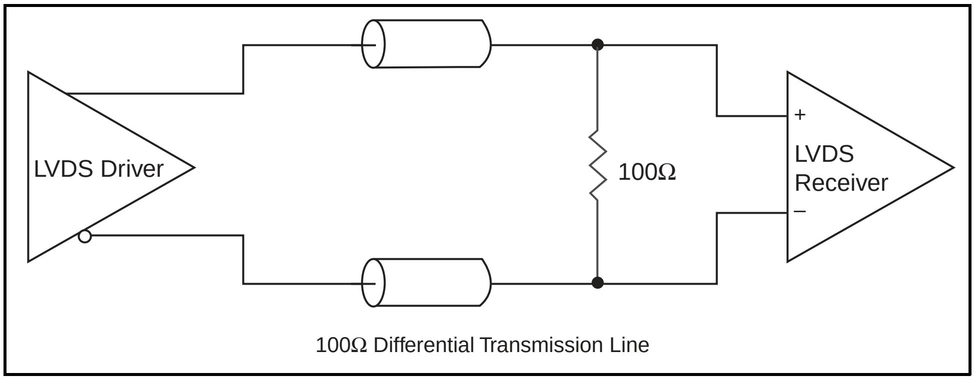


Figure 6. Typical LVDS Driver Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 7A and 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

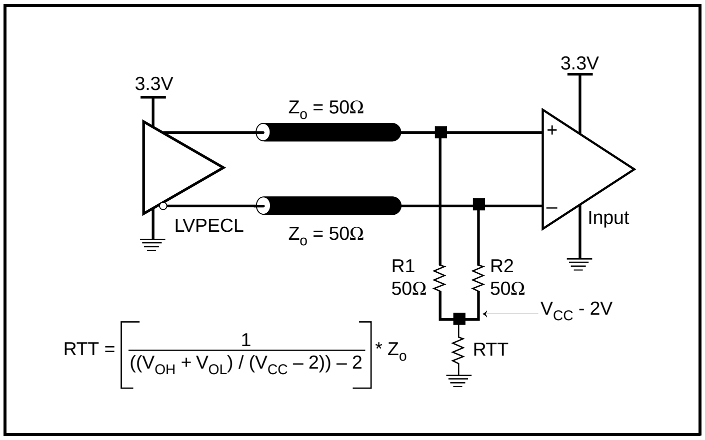


Figure 7A. 3.3V LVPECL Output Termination

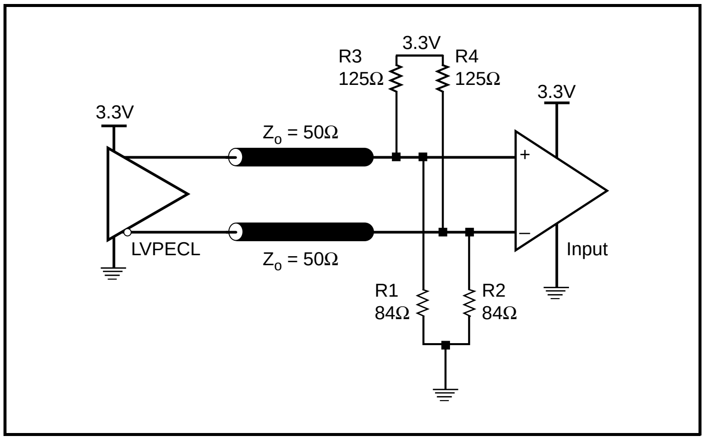


Figure 7B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 8A and *Figure 8B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DD} – 2V. For V_{DDO} = 2.5V, the V_{DDO} – 2V is very close to ground level. The R3 in Figure 8B can be eliminated and the termination is shown in *Figure 8C.*

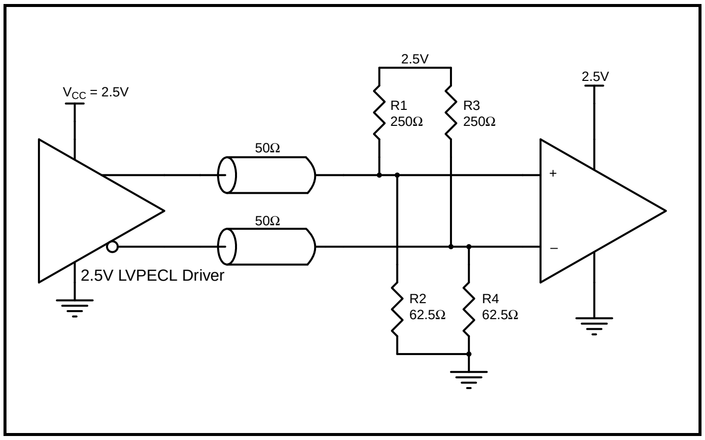


Figure 8A. 2.5V LVPECL Driver Termination Example

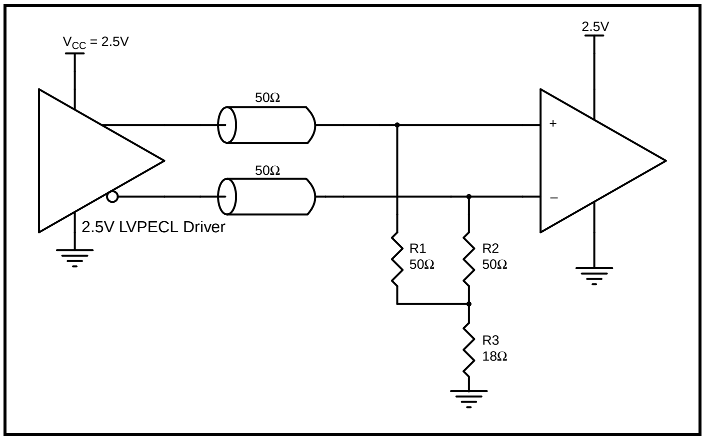


Figure 8B. 2.5V LVPECL Driver Termination Example

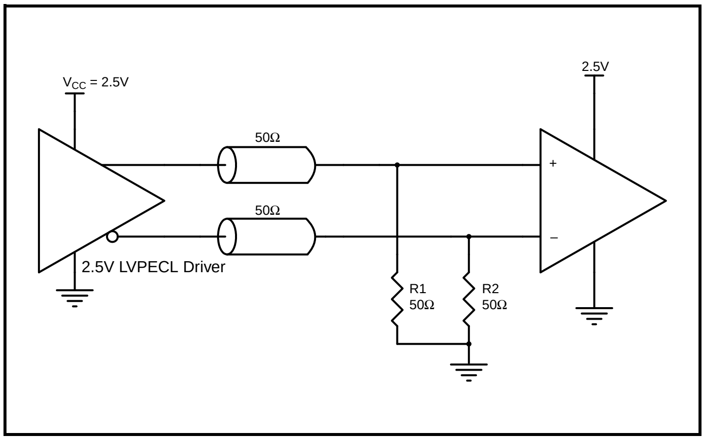


Figure 8C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 9.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

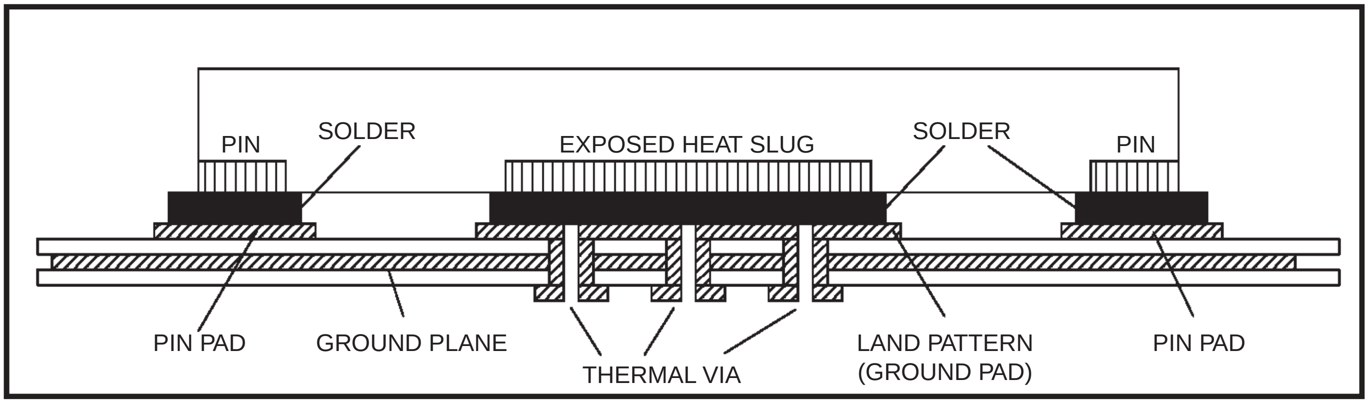


Figure 9. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T39101.
Equations and example calculations are also provided.

LVPECL Power Considerations

1. Power Dissipation.

The total power dissipation for the IDT8T39101 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V+5% = 3.465, which gives worst case results.

The Maximum current at 85°C is as follows
I_{EE_MAX} = 189mA

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = I_{EE\_MAX} * V_{DD\_MAX}$ = 3.465V * 189mA = 655**mW**
- Power $(outputs)_{MAX}$ = **30.0mW/Loaded Output pair**
  If all outputs are loaded, the total power is 10 * 30.0mW = **300mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to loading 50Ω to $V_{DDO}/2$ Output Current:

  $I_{OUT} = V_{DDO}$_MAX / [2 * $(R_{LOAD} + R_{OUT})$] = 3.465V / [2 * (50Ω + 15Ω] = **26.654mA**
- Power Dissipation on ROUT per LVCMOS output:

  Power (R_{OUT}) = ROUT * I_{OUT}^2 = 15Ω * $(26.654mA)^2$ = **10.656mW**
- Dynamic Power Dissipation at 200MHz, (REFOUT)
- Power (200MHz) = C_{PD} * Frequency * V_{DDO}^2 = 10pF * 200MHz * 3.465^2 = **24.012mW**
- Total Power (200MHz) = 24.012mW * 1 = **24.012mW**

Total Power_Max = 655mW + 300mW + 10.656mW + 24.012mW = **989.67mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 40.2°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.99 W * 29.0°C/W = 113.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 48 Lead VQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	25.4°C/W	22.8°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 10.*

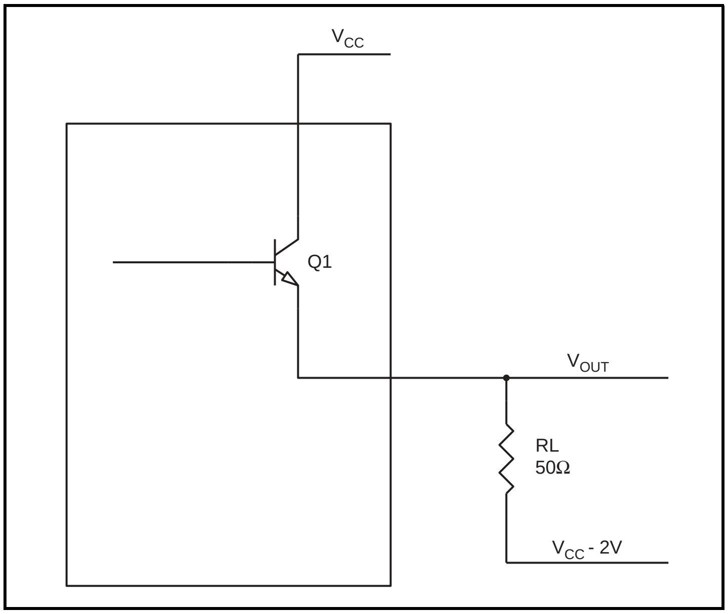


Figure 10. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{DD} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DD\_MAX} – 0.90V}$
  $(V_{DD\_MAX} – V_{OH\_MAX}) = \mathbf{0.90V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{DD\_MAX} – V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.mW**

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T39101.
Equations and example calculations are also provided.

HCSL Power Considerations

1. Power Dissipation.

The total power dissipation for the IDT8T39101 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V+5% = 3.465, which gives worst case results.

The Maximum current at 85°C is as follows
I_{DD_MAX} = 92mA

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 92mA = 319**mW**
- Power $(outputs)_{MAX}$ = 44.5**mW/Loaded Output pair**
  If all outputs are loaded, the total power is 10 * 44.5mW = **445mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to loading 50Ω to V_{DDO}/2 Output Current:

  I_{OUT} = V_{DDO}_MAX / [2 * (R_{LOAD} + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω] = **26.654mA**
- Power Dissipation on ROUT per LVCMOS output:

  Power (R_{OUT}) = ROUT * I_{OUT}^2 = 15Ω * (26.654mA)^2 = **10.656mW**
- Dynamic Power Dissipation at 200MHz, (REFOUT)
- Power (200MHz) = C_{PD} * Frequency * V_{DDO}^2 = 10pF * 200MHz * 3.465^2 = **24.012mW**
- Total Power (200MHz) = 24.012mW * 1 = **24.012mW**
- Total Power_Max = 319mW + 445mW + 10.656mW + 24.012mW = **798.67mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 40.2°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.799 W * 29.0°C/W = 108.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance θ_{JA} for 48 Lead VQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	25.4°C/W	22.8°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

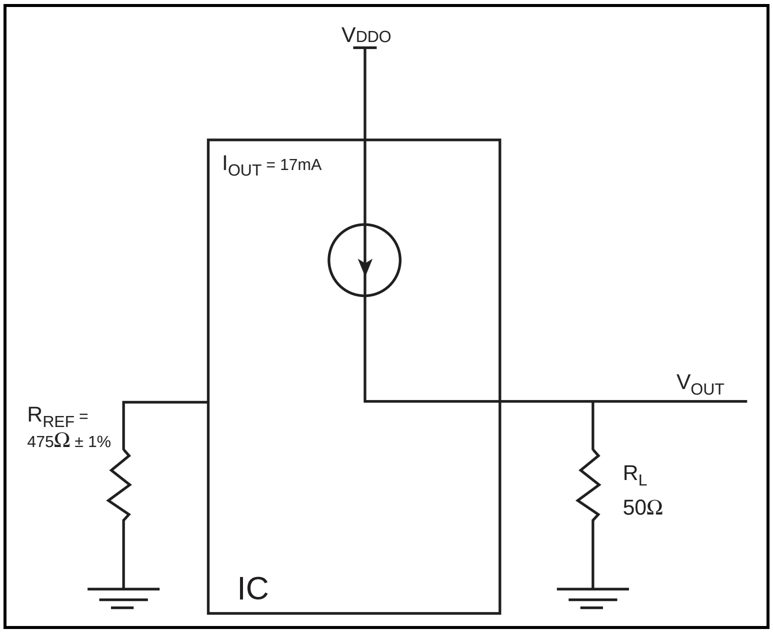


Figure 11. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DDO_MAX}.

Power $= (V_{DDO\_MAX} – V_{OUT}) * I_{OUT}$,
since $V_{OUT} – I_{OUT} * R_L$

$= (V_{DDO\_MAX} – I_{OUT} * R_L) * I_{OUT}$

$= (3.465V – 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T39101.
Equations and example calculations are also provided.

LVDS Power Considerations

1. Power Dissipation.

The total power dissipation for the IDT8T39101 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V+5% = 3.465, which gives worst case results.

The Maximum current at 85°C is as follows
I_{DD_MAX} = 76mA

I_{DDO_MAX} = 303mA

Power (core) Max = V_{DD_MAX} *(I_{DD_MAX} + I_{DDO_MAX}) = 3.465 * (76mA + 303mA) = **1313.235mW**.

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to loading 50Ω to V_{DDO}/2 Output Current:

  I_{OUT} = V_{DDO}_MAX / [2 * (R_{LOAD} + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω] = **26.654mA**
- Power Dissipation on ROUT per LVCMOS output:

  Power (R_{OUT}) = ROUT * I_{OUT}^2 = 15Ω * (26.654mA)^2 = **10.656mW**
- Dynamic Power Dissipation at 200MHz, (REFOUT)
- Power (200MHz) = C_{PD} * Frequency * V_{DDO}^2 = 10pF * 200MHz * 3.465^2 = **24.012mW**
- Total Power (200MHz) = 24.012mW * 1 = **24.012mW**
- Total Power_Max = 1313.235mW + 10.656 + 24.012 = **1347.903mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 40.2°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.344W * 29.0°C/W = 124.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 9. Thermal Resistance θ_{JA} for 48 Lead VQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	25.4°C/W	22.8°C/W

Reliability Information

Table10. θ_{JA} vs. Air Flow Table for a 48 Lead VFQFN

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	29.0°C/W	25.4°C/W	22.8°C/W

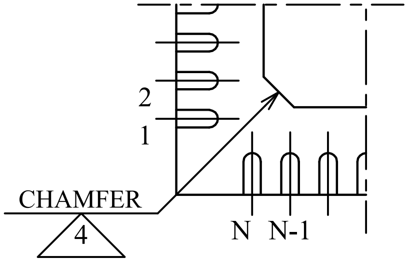
Transistor Count

The transistor count for IDT8T3910I is: 19,425

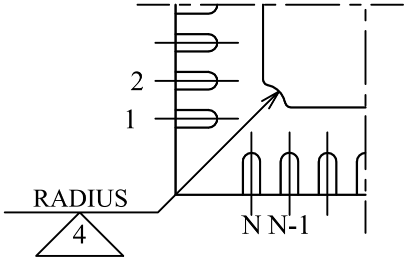
Package Outline and Package Dimensions

Package Outline NL Suffix for 48 Lead VFQFN

Bottom View w/Type A ID



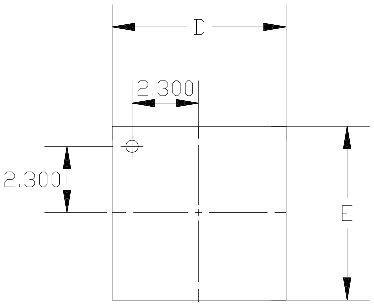
Bottom View w/Type C ID



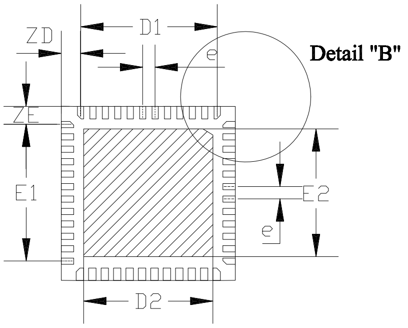
There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

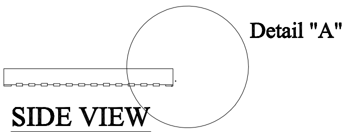
FOR REFERENCE ONLY



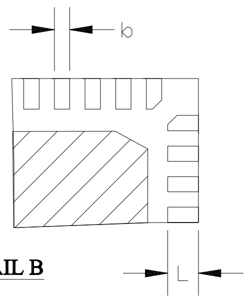
TOP VIEW



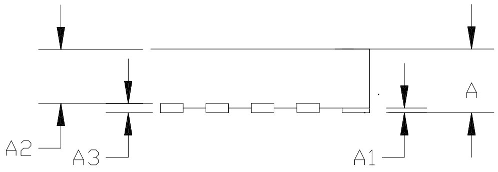
BOTTOM VIEW



SIDE VIEW



DETAIL B



DETAIL A

Table 11. Package Dimensions for 48 Lead VFQFN

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N	48		
A		0.8	0.9
A1	0	0.02	0.05
A3	0.2 Ref.		
b	0.18	0.25	0.30
D & E	7.00 Basic		
D1 & E1	5.50 Basic		
D2 & E2	5.50	5.65	5.80
e	0.50 Basic		
R	0.20~0.25		
ZD & ZE	0.75 Basic		
L	0.35	0.40	0.45

Reference Document: IDT Drawing #PSC-420

Ordering Information

Table 12. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T3910BNLGI	IDT8T3910BNLGI	Lead-Free, 48 Lead VFQFN	Tray	-40°C to 85°C
8T3910BNLGI8	IDT8T3910BNLGI	Lead-Free, 48 Lead VFQFN	1500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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