

## CMOS HPL™ Harris Programmable Logic

### Features

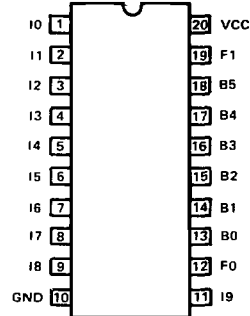
- Pin & Function Compatible with the Bipolar 16L8 and 16P8
- Scaled SAJI IV CMOS Process
- Fast Access (Input to Output) ..... 125ns Max.
- Ultra-low Standby Power ..... ICCSB = 150 $\mu$ A
- Low Operating Power ..... ICCOP = 6mA/MHz
- Wide Operating Temperature Ranges:
  - ▶ HPL-16LC8-5 ..... 0 $^{\circ}$ C to +75 $^{\circ}$ C
  - ▶ HPL-16LC8-9 ..... -40 $^{\circ}$ C to +85 $^{\circ}$ C
  - ▶ HPL-16LC8-8 ..... -55 $^{\circ}$ C to +125 $^{\circ}$ C
- Programmable Output Polarity
- 20-pin Slimline DIP
- Security Fuse for Pattern Protection
- TTL/CMOS Compatible Inputs/Outputs for Mixed System Compatibility
- Logic Paths Tested to Insure Functionality

### Applications

- Random Logic Replacement
- Code Converters
- Address Decoding
- Fault Detectors
- Boolean Function Generators
- Digital Multiplexers
- Parity Generators
- Pattern Recognition
- ROM Patching

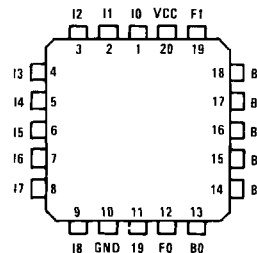
### Pinouts

TOP VIEW



LCC

TOP VIEW



### Description

The HPL-16LC8 is a CMOS Programmable Logic Device designed to provide a high performance, low power alternative to the industry standard 16L8 and 16P8 programmable logic devices.

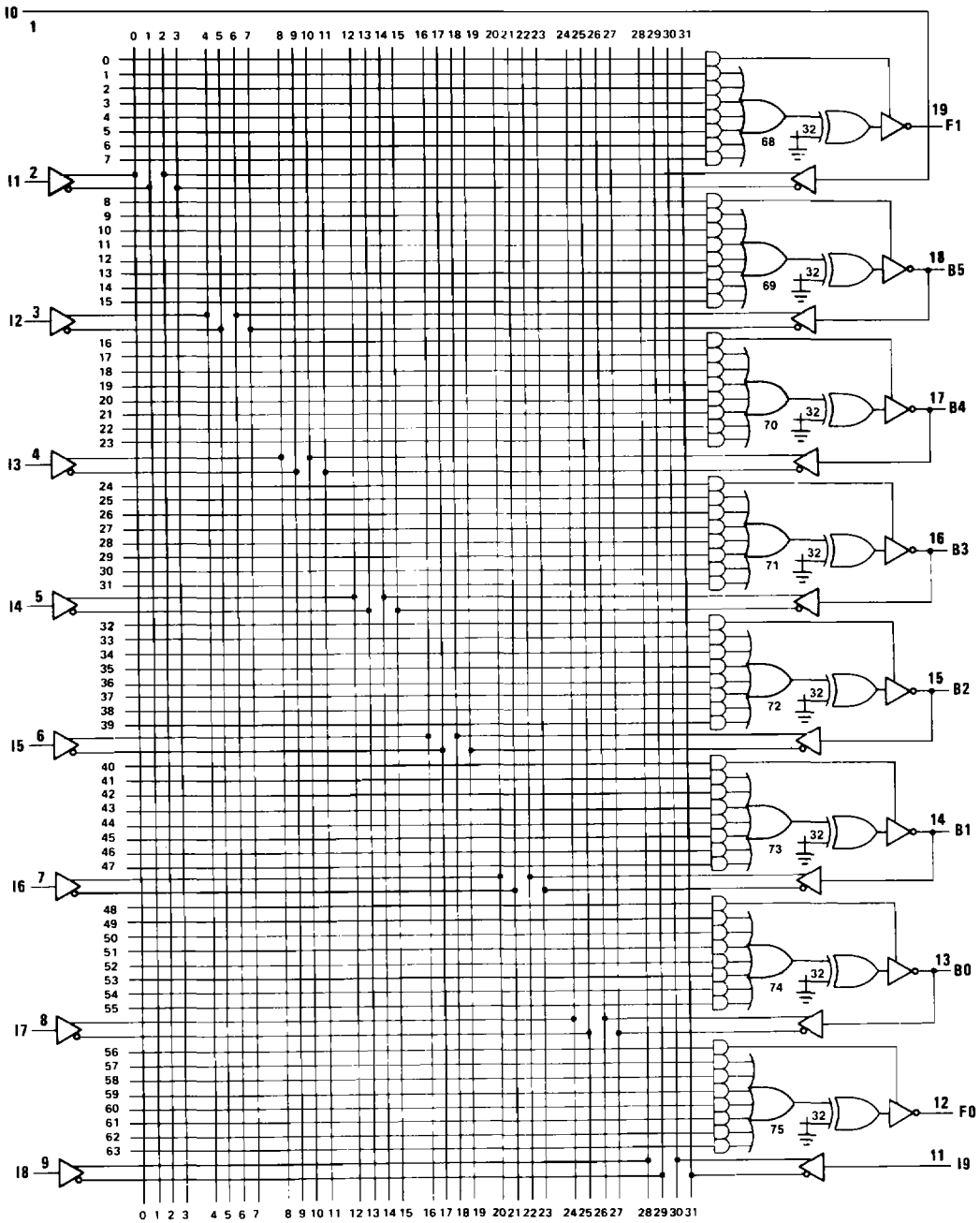
In addition to the low power advantage of this device over its bipolar counterparts the HPL-16LC8 contains programmable output polarity, allowing the user to individually select each output as either active-high or active-low. When all output polarity fuses are left intact, all active outputs are active-low.

The Harris fuse link technology provides a permanent fuse with stable storage characteristics over the full temperature ranges of 0 $^{\circ}$ C to +75 $^{\circ}$ C, -40 $^{\circ}$ C to +85 $^{\circ}$ C and -55 $^{\circ}$ C to +125 $^{\circ}$ C. Like all Harris Programmable Logic (HPL), this device contains unique test circuitry developed by Harris which allows AC, DC and functional testing before programming.

On-chip automatic power-down circuitry places internal circuitry into an ultra-low ICCSB power mode after output data becomes valid.

# HPL-16LC8

## Functional Diagram



HPL-16LC8

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## Specifications HPL-16LC8

### Absolute Maximum Ratings

Supply Voltage	+7.0 Volts
Input, Output or I/O Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1 Watt
$\theta_{JC}$	16°C/W (CERDIP Package), 19°C/W (LCC Package)
$\theta_{JA}$	70°C/W (CERDIP Package), 76°C/W (LCC Package)
Gate Count	1500 Gates
Junction Temperature	+150°C
Lead Temperature (Soldering, Ten Seconds)	+275°C

**CAUTION.** Stresses above those listed in the 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

### Operating Conditions

Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	
HPL-16LC8-5	0°C to +70°C
HPL-16LC8-9	-40°C to +85°C
HPL-16LC8-8	-55°C to +125°C

### D.C. Electrical Specifications

(Operating)

HPL-16LC8-5	(VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-16LC8-9	(VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-16LC8-8	(VCC = 5.0V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS ①
I <sub>IH</sub> I <sub>IL</sub>	Dedicated input Current	-1 0	+1	μA	V <sub>IH</sub> = VCC MAX V <sub>IL</sub> = 0V VCC = VCC MAX
I <sub>FZH</sub> I <sub>FZL</sub>	Output Current Hi-Z State	-1 0	+10	μA	V <sub>FH</sub> = VCC MAX V <sub>FL</sub> = 0V VCC = VCC MAX
I <sub>IBZH</sub> I <sub>IBZL</sub>	Bidirectional Hi-Z Current	-1 0	+10	μA	V <sub>BH</sub> = VCC MAX V <sub>BL</sub> = 0V VCC = VCC MAX
V <sub>IH</sub> V <sub>IL</sub>	Input Threshold Voltage ②	-1 0	20	V	VCC = VCC MAX VCC = VCC MIN
V <sub>OH1</sub> V <sub>OH2</sub>	Output Voltage ③	-1 1	30 VCC-04	V	I <sub>OH1</sub> = -50 mA I <sub>OH2</sub> = -10 mA VCC MIN, V <sub>IL</sub> MAX, V <sub>IH</sub> MIN
V <sub>OL</sub>	Output Voltage	0	04	V	I <sub>OL</sub> = +50 mA
I <sub>CCSB</sub>	Standby Power Supply Current		150	μA	V <sub>I</sub> = VCC or GND I <sub>F</sub> = 0.00 μA VCC = VCC MAX
I <sub>CCOP</sub>	Operating Power Supply Current		6	mA/MHz	V <sub>I</sub> = VCC or GND I <sub>F</sub> = 0.00 μA VCC = VCC MAX

① These specifications apply to both Input (I) and Bidirectional (B) Pins

② These specifications apply to both Output (F) and Bidirectional (B) Pins.

③ All DC parameters tested under worst case conditions.

### A.C. Switching Specifications

(Operating)

HPL-16LC8-5	(VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-16LC8-9	(VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-16LC8-8	(VCC = 5.0V ± 10%, TA = -55°C to +125°C)

JEDEC STANDARD	SYMBOL	PARAMETER	HPL-16LC8-5		HPL-16LC8-9		HPL-16LC8-8		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
TDVQH1 (1)	TPD	Propagation delay I or B to Output High	-	125	-	125	-	125	ns
TDVOL1 (2)	TPD	Propagation delay I or B to Output Low	-	125	-	125	-	125	ns
TDVQH2 (3)	TPZX	Enable Access Time to Output High ④	TDVQZ1	125	TDVQZ1	125	TDVQZ1	125	ns
TDVOL2 (4)	TPZX	Enable Access Time to Output Low ④	TDVQZ2	125	TDVQZ2	125	TDVQZ2	125	ns
TDVQZ1 (5)	TPXZ	Disable Access Time from Output High	-	125	-	125	-	125	ns
TDVQZ2 (6)	TPXZ	Disable Access Time from Output Low	-	125	-	125	-	125	ns

④ Enable access time is guaranteed to be greater than disable access time to avoid device contention

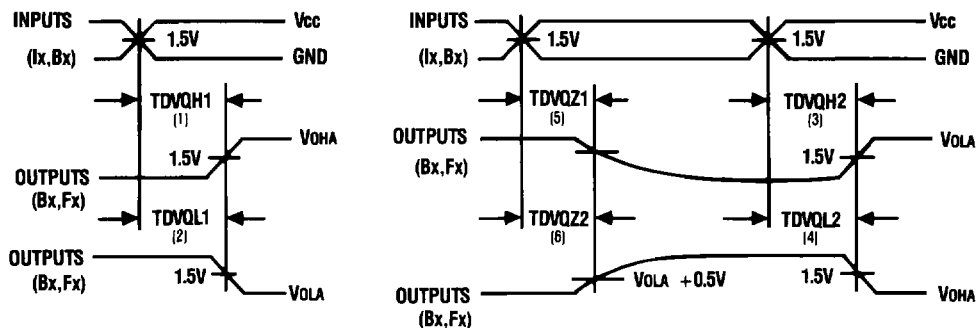
## Specifications HPL-16LC8

HPL-16LC8

**Capacitance:**  $T_A = +25^{\circ}\text{C}$  (NOTE: Sampled and guaranteed - but not 100% tested.)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	$V_I = V_{CC}$ or GND $f = 1$ MHz
CF	Output Capacitance	10	pF	$V_F = V_{CC}$ or GND $f = 1$ MHz
CB	Bidirectional Capacitance	12	pF	$V_B = V_{CC}$ or GND $f = 1$ MHz

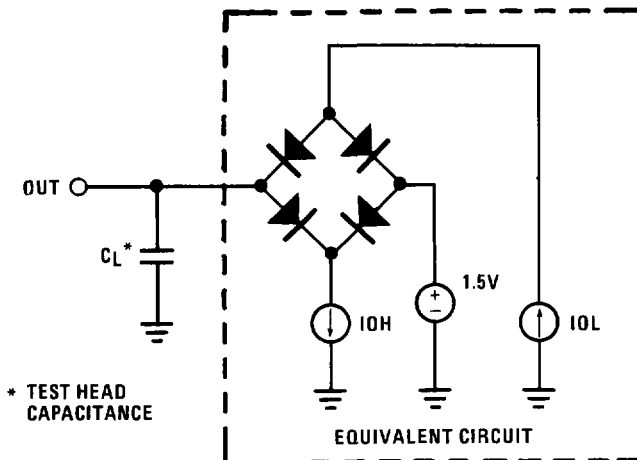
### Switching Time Definitions



INPUT CONDITIONS:  $t_r, t_f = 5\text{ns}$  (10% to 90%)

NOTE: Disable access time is the time taken for the output to reach a high impedance state when the three-state product term drives the output inactive. The high impedance state is defined as a point on the waveform equal to a  $\Delta V$  of 0.5V from  $VoHA$  or  $VoLA$ , the active output level.

### A.C. Test Load



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## Programming

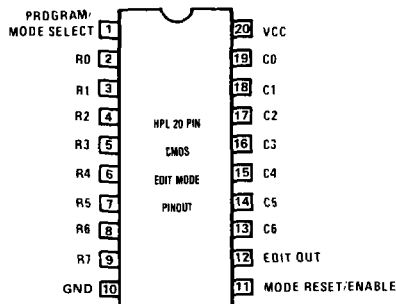
Following is the programming procedure which is used for the HPL-16LC8 programmable logic device. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One

may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

**TABLE 1**  
**PROGRAMMING SPECIFICATIONS**

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	ICC Limit During Programming			100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-5.00	-5.00	-7.00	V
INEG	Edit Enable & Mode Select Current				-5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	verify ①	VCCV-2	VCCV	VCCV	V
VIHP	Input Voltage High	programming ①	VCCP-2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V		0	1	μA
IILHV	Input Current High	verify		0	1	μA
IILHP	Input Current High	programming		0	1	μA
VSI	Verify voltage	Intact Fuse	3.00	3.30		V
VSP	Verify voltage	Programmed Fuse		0.00	0.50	V
TV	Verify Pulse Delay		500	750	1000	μsec
PWP	Programming Width		4.5	5.1	5.5	msec
td	Pulse Seq. Delay		1	1	—	μsec
tr	Signal Rise Time	10% to 90%	0.01	0.1	1	μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
INEG	Mode Select Width		1	1	5	μsec
TPP	Programming Period			5.2		msec
FL	Fuse Attempts/Link		1	1	2	cycles

① Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC Pin.



**FIGURE 1**  
**EDIT MODE PINOUT**  
**HPL-16LC8**

NOTES. \* While programming the CMOS HPL device, no pins should be left floating. EDIT OUT appears as an open drain output during programming. It should be tied to GND through a 1M-ohm resistor.

\* CMOS HPL outputs are not put into a high impedance state (suitable for row and column address application) until the device is reset and put into the edit mode. For this reason it is recommended that the outputs be left floating until the edit mode is enabled or that the outputs be driven thru a 2k-ohm resistor.

\* It is suggested that a 0.01 μf capacitor be put between VCC and GND to minimize VCC voltage spikes. Also, particular care should be exercised in regards to transients on the MODE SELECT and MODE RESET pins which could place the device in the incorrect mode.

**Programming Procedure**

① Set-Up:

NOTE: Refer to the Figure 1 for the pin definitions, Table 1 for the timing and level definitions, Tables 3 & 4 for the address decoding.

- a. During programming, no pins should be left floating.
- b. EDIT OUT (Pin 12) should be terminated with a 1 M-ohm ( $\pm 1\%$ ) resistor to GND and stray capacitances on this pin should be  $\leq 50$  pf.
- c. Set GND to 0.00 volts.
- d. Outputs are only in a high impedance state (and available for addressing of edit mode rows and columns) while in Edit Modes 1 thru 4. Do not apply signals to these pins until a valid Edit Mode is entered.
- e. All input and bi-directional pins should be at zero volts nominal with a maximum of 0.3 volts applied.
- f. Apply VCCV to the part. No input should ever exceed the level on the VCC PIN.

② Mode Reset/Edit Enable:

- a. Wait  $t_d$  and reset the edit control logic by pulsing the MODE RESET PIN to VNEG for  $t_{NEG}$ .
- b. Wait  $t_d$  and enable Edit mode by applying VNEG to the EDIT ENABLE PIN.

③ Mode Select:

- a. Wait  $t_d$  and select EDIT MODE 1 by pulsing the MODE SELECT PIN to VNEG for  $t_{NEG}$ . Subsequent pulses will increment the mode to 2, 3 and 4 sequentially (sequencing the device beyond mode 4 will result in unpredictable results—if in doubt, return to STEP 2).
- b. Verify entry into the proper mode by addressing column 64 and the row indicated in Table 2, waiting  $t_V$  and monitoring the EDIT OUT PIN for the proper data.
- c. Address column 65 and the row indicated in Table 2, wait  $t_V$  and monitor the EDIT OUT PIN for the proper data. If both Steps 3b & 3c are correct, then the proper mode has been selected.
- d. To re-enter a mode lower than the current mode, return to Step 2. Mode 1 can only be (re-)entered from Step 2.

④ Fuse Select:

NOTE: The voltage for a logical "1" (VIHP) must not exceed VCCP and must track VCCP as it rises from VCCV in Step 5.

- a. Wait  $t_d$  and select a row by applying the appropriate address from Table 3.
- b. Select a column by applying the appropriate address from Table 4.

⑤ Verify Intact Fuse:

NOTE: Skip this step for post-programming verify.

b. If EDIT OUT has indicated less than VSI, the fuse is not intact. Reject this device for a non-blank matrix.

⑥ Program the Fuse:

NOTE: The PROTECT and POLARITY fuses can be accessed from either mode 1 or mode 3 by applying the addresses indicated in Tables 3 & 4.

THE 'PROTECT' FUSE SHOULD NOT BE PROGRAMMED UNTIL ALL OTHER FUSES HAVE BEEN PROGRAMMED AND VERIFIED AS PROGRAMMING THIS FUSE DEFEATS ALL FURTHER VERIFICATION!

- a. Wait  $t_d$  and raise the VCC PIN to VCCP (allow VIHP to track this rise).
- b. Wait  $t_d$  and pulse the PROGRAM PIN (Pin 1) to VIHP for a duration of PWP.
- c. Wait  $t_d$  and lower the VCC PIN to VCCV (allow VIHP to track this fall).

⑦ Verify Fuse:

- a. Wait  $t_V$  and monitor EDIT OUT for VSP (or VSI if verifying an intact fuse).
- b. If EDIT OUT has indicated greater than VSP for an attempted programmed fuse, repeat Step 6 so that the fuse receives a maximum of FL fusing attempts.

① Repeat Steps 4 through 7 for all addresses in a given mode.

③ Repeat Steps 3 through 8 for all modes.

**Programming Waveforms**

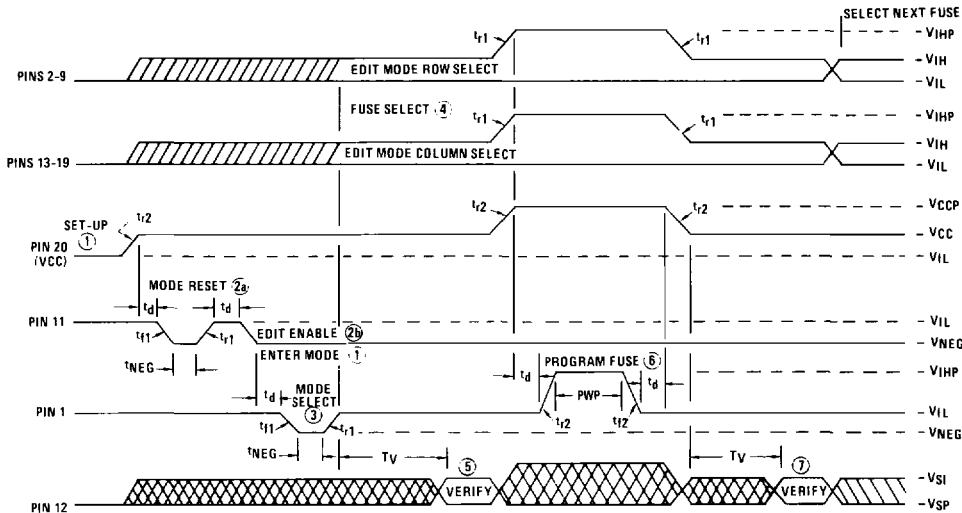


FIGURE 2

NOTE: Pins 13-19 are not necessarily three-state and available for application of column address input signals until a valid edit mode is entered. Refer to the edit mode pinout (Figure 1) for further details.

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## Programming Procedure

**Mode Verification**  
Table 2

MODE	COLUMN NUMBER	ROW NUMBER	EDIT OUT (PIN 12) LOGICAL LEVEL
1	64	0	0
	65	0	0
2	64	1	0
	65	1	1
3	64	2	1
	65	2	0
4	64	3	1
	65	3	1

NOTES: \* At least two addresses must be checked to verify the proper edit mode.  
† The conversion from the decimal column and row addresses in the table above to the actual pin levels can be made in Tables 3 and 4.

**Edit Mode Column Select**  
Table 4

COLUMN NUMBER	C6	C5	C4	C3	C2	C1	C0	MODE VERIFY
	Pin 13	Pin 14	Pin 15	Pin 16	Pin 17	Pin 18	Pin 19	
0	L	L	L	L	L	L	L	
1	L	L	L	L	L	L	L	
2	L	L	L	L	L	H	L	
3	L	L	L	L	L	H	H	
4	L	L	L	L	H	L	L	
5	L	L	L	L	H	H	L	
6	L	L	L	L	H	H	H	
7	L	L	L	L	H	L	H	
8	L	L	L	H	L	L	H	
9	L	L	L	H	L	L	H	
10	L	L	L	H	L	H	L	
11	L	L	L	H	L	H	H	
12	L	L	L	H	H	L	L	
13	L	L	L	H	H	L	H	
14	L	L	L	H	H	H	L	
15	L	L	L	H	H	H	H	
16	L	L	H	L	L	L	L	
17	L	L	H	L	L	L	H	
18	L	L	H	L	L	H	H	
19	L	L	H	L	L	H	H	
20	L	L	H	L	H	L	H	
21	L	L	H	L	H	H	L	
22	L	L	H	L	H	H	L	
23	L	L	H	L	H	H	L	
24	L	L	H	H	L	L	L	
25	L	L	H	H	L	L	H	
26	L	L	H	H	L	H	L	
27	L	L	H	H	L	H	H	
28	L	L	H	H	H	L	L	
29	L	L	H	H	H	L	H	
30	L	L	H	H	H	H	L	
31	L	L	H	H	H	H	L	
32	L	H	L	L	L	L	L	
33	L	H	L	L	L	L	H	
34	L	H	L	L	L	L	H	
35	L	H	L	L	L	L	H	
36	L	H	L	L	L	L	L	
37	L	H	L	L	H	L	L	
38	L	H	L	L	H	H	L	
39	L	H	L	L	H	H	H	
40	L	H	L	L	H	L	L	
41	L	H	L	L	H	L	L	
42	L	H	L	L	H	L	H	
43	L	H	L	L	H	L	H	
44	L	H	L	L	H	L	L	
45	L	H	L	L	H	H	L	
46	L	H	L	L	H	H	L	
47	L	H	L	L	H	H	L	
48	L	H	L	L	L	L	L	
49	L	H	L	L	L	L	L	
50	L	H	L	L	L	L	H	
51	L	H	L	L	L	L	H	
52	L	H	L	L	L	H	L	
53	L	H	L	L	L	H	L	
54	L	H	L	L	L	H	L	
55	L	H	L	L	L	H	H	
56	L	H	L	L	H	L	L	
57	L	H	L	L	H	L	L	
58	L	H	L	L	H	L	L	
59	L	H	L	L	H	L	H	
60	L	H	L	L	H	L	L	
61	L	H	L	L	H	L	L	
62	L	H	L	L	H	H	L	
63	L	H	L	L	H	H	L	
64	H	L	L	L	L	L	L	
65	H	L	L	L	L	L	H	
68	H	L	L	L	L	L	L	Pin 19
69	H	L	L	L	L	H	L	Pin 18
70	H	L	L	L	L	H	L	Pin 17
71	H	L	L	L	L	H	H	Pin 16
72	H	L	L	L	H	L	L	Pin 15
73	H	L	L	L	L	L	H	Pin 14
74	H	L	L	L	L	L	H	Pin 13
75	H	L	L	L	L	L	H	Pin 12
76	H	L	L	H	H	L	L	PROTECT

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**Edit Mode Row Select**  
Table 3

PROG. MODE	ROW NUMBER	R7	R6	R5	R4	R3	R2	R1	R0	VARIABLE
		Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	
1	0	H	H	H	H	H	H	L	H	/1
	4	H	H	H	H	H	H	L	H	/2
	8	H	H	H	H	H	L	H	H	/3
	12	H	H	H	H	L	H	H	H	/4
	16	H	H	H	L	L	H	H	H	/5
2	20	H	L	L	L	H	H	H	H	/6
	24	H	L	L	L	H	H	H	H	/7
	28	L	H	H	H	H	H	H	H	/8
	1	L	L	L	L	L	L	L	H	/11
	5	L	L	L	L	L	L	L	H	/12
3	9	L	L	L	L	L	L	L	L	/13
	13	L	L	L	L	L	L	L	L	/14
	17	L	L	L	L	L	L	L	L	/15
	21	L	L	L	L	L	L	L	L	/16
	25	L	L	L	L	L	L	L	L	/17
4	29	L	L	L	L	L	L	L	L	/18
	2	H	H	H	H	H	H	L	L	/10
	6	H	H	H	H	H	H	L	H	/B5
	10	H	H	H	H	H	L	H	H	/B4
	14	H	H	H	H	L	H	H	H	/B3
1 or 3	18	H	H	H	L	H	H	H	H	/B2
	22	H	H	L	H	H	H	H	H	/B1
	26	H	L	H	H	H	H	H	H	/B0
	30	L	L	H	H	H	H	H	H	/19
	32	H	H	H	H	H	H	H	H	CONFIGURE

NOTE: The configuration row can be selected while in either mode 1 or mode 3.

LEGEND: L = Logic Low, H = Logic High.