EVALZ-ADN2905/EVALZ-ADN2913/ EVALZ-ADN2915/EVALZ-ADN2917 User Guide

UG-877

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ADN2905/ADN2913/ADN2915/ADN2917 Evaluation Board Setup and Applications

FEATURES

Full featured evaluation board for the ADN2905/ADN2913/ADN2915/ADN2917
Configurable as PRBS generator or PRBS error detector
Locked to any rate, continuous mode, up to 11.3 Gbps input signal

EVALUATION KIT CONTENTS

One evaluation board with device under test (DUT): ADN2905, ADN2913, ADN2915, or ADN2917
USB-to-I²C adaptor board
USB cable
Software CD

GENERAL DESCRIPTION

The ADN29xx (ADN2905, ADN2913, ADN2915, and ADN2917) provide the receiver functions of quantization, signal level detect, and clock/data recovery for a continuous signal data rate range from 6.5 Mbps to 11.3 Gbps (see Table 1). The ADN29xx automatically lock to such a data signal without referring to an external clock or extra programming. All SONET/SDH jitter requirements are exceeded, including jitter transfer, jitter generation, and jitter tolerance. All specifications are quoted for the −40°C to +85°C temperature range, unless otherwise noted.

For the best input signal detection, the ADN29xx input circuitry can be configured as a limiting amplifier, an equalizer, or a 0 dB equalizer. Additionally, the ADN29xx provide manual control of sampling phase and slice level adjust to optimize the incoming data eye detection.

The loss of signal (LOS) is available in limiting amplifier input mode only. The asserted LOS indicates that the input signal level has fallen below a preset threshold. The LOS detect circuit provides a typical 6.0 dB hysteresis to prevent LOS output chatter.

The asserted loss of lock (LOL) indicates when incoming signal rate shifts more than 1000 ppm away from the CDR VCO frequency.

The ADN29xx are available in a compact 4 mm × 4 mm, 24-lead chip scale package (LFCSP).

Table 1. ADN29xx Register IDs and Supported Data Range

Device	Register 0x20H	Register 0x21H	Data Rate (Mbps)	Comments
ADN2905	0xAD	0x63	614 to 10,312	CPRI/10GE CDR
ADN2913	0xA8	0x00	6.5 to 8,500	Lower rate, any rate CDR
ADN2915	0x00	0x00	6.5 to 11,300	Full feature, any rate CDR
ADN2917	0xFF	0xA6	8,500 to 11,300	Low cost, limited rate range CDR

Full specifications on the ADN2905/ADN2913/ADN2915/ ADN2917 are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.

The ADN2905, ADN2913, ADN2915, and ADN2917 are pin-to-pin compatible devices and share the same evaluation board. Each EVALZ-ADN29xx evaluation board is populated by a different DUT: ADN2905 on the EVALZ-ADN2905, ADN2913 on the EVALZ-ADN2913, ADN2915 on the EVALZ-ADN2915, and ADN2917 on the EVALZ-ADN2917.

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REVISION HISTORY

8/15—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

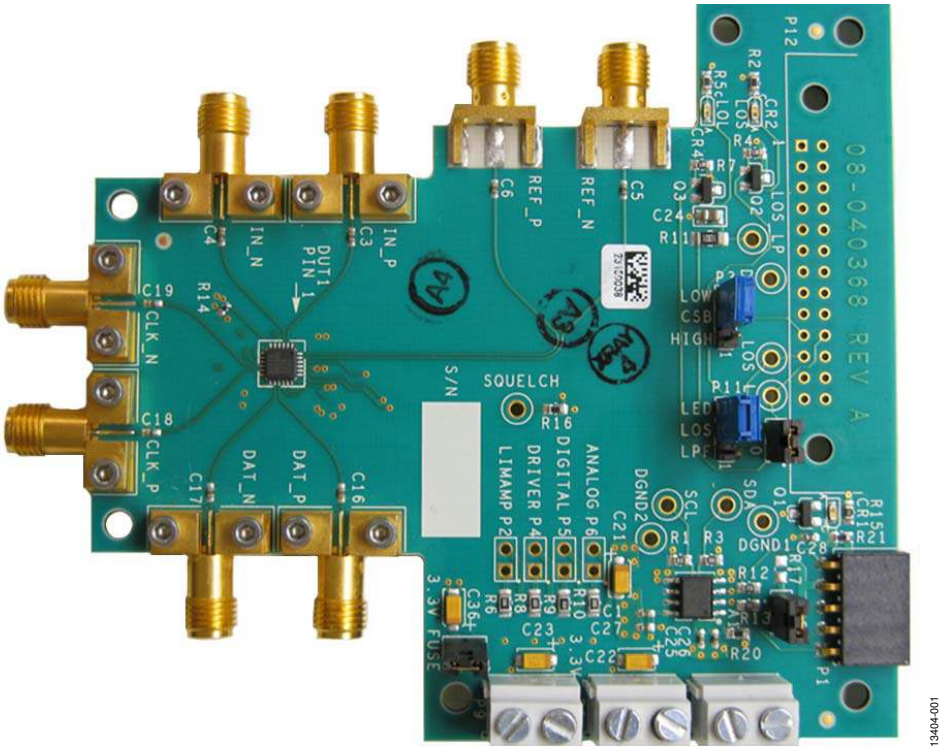

Figure 1. EVALZ-ADN29xx Evaluation Board

QUICK START GUIDE

ADAPTOR

To set up the USB-to-I²C adaptor, connect a USB cable from P2 of the adaptor (circled in yellow, in Figure 2) to a PC. The adaptor has two LEDs: CR1 and CR2 (circled in yellow, in Figure 2), which blink alternately when the adaptor connects to a USB source properly.

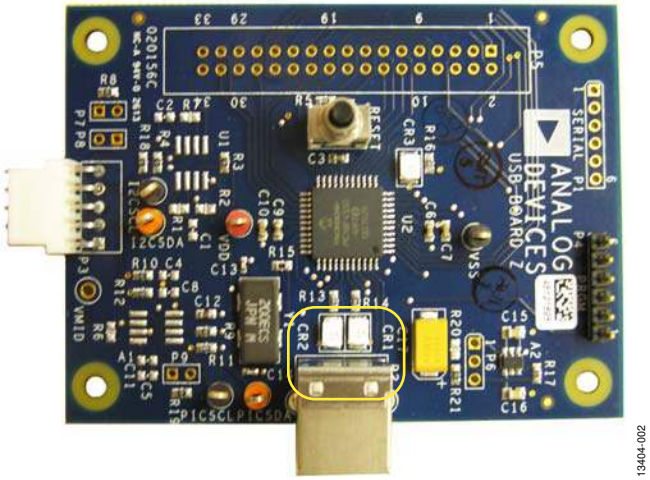

Figure 2. Adaptor

EVALUATION BOARD

The evaluation board has SMA connector for all the inputs: IN_P, IN_N, REF_P, and REF_N. Only the IN_P and IN_N inputs are required to operate the ADN29xx device. The evaluation board also has SMA connectors for all the DUT outputs: DAT_P, DAT_N, CLK_P, and CLK_N.

The evaluation board is set to a factory default mode: lock to data (LTD) mode.

The adaptor is required to configure the evaluation board in a proper working mode (other than the factory default mode). For further details, see the ADN2905/ADN2913/ADN2915/ADN2917 data sheet.

To set up the evaluation kit, take the following steps:

1. Place jumpers on the evaluation board as follows:
   - P3, LOW to CSB
   - P11, LOS to LED
   - P10
   - P14
2. Connect supply rails (shown in Figure 3) to the evaluation board as follows:
   - P7: 1.2 V (0.6 A maximum compliant current)
   - P8: 1.8 V (0.1 A maximum compliant current)
   - P9: 3.3 V (0.05 A maximum compliant current)

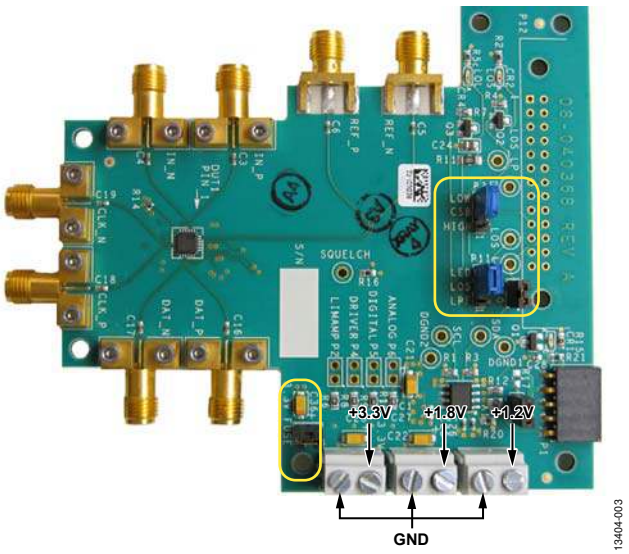

Figure 3. Evaluation Board, Jumper P14, Jumper P10, Jumper P11, Jumper P3 (Marked in Yellow), and Supply Rails

3. Connect P3 of the adaptor board to P1 of the evaluation board directly, as shown in Figure 4 (circled in yellow).

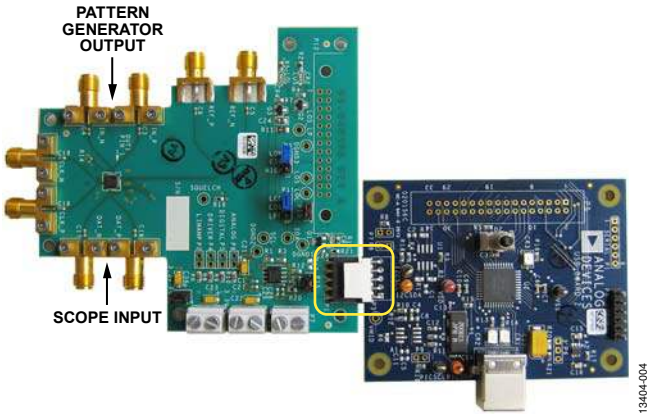

Figure 4. Connect the Evaluation Board and the Adaptor

4. Connect a pattern generator output to the evaluation board IN_P and IN_N connectors (see Figure 4).
5. Connect a scope to the evaluation board DAT_P and DAT_N connectors (see Figure 4).
6. Make sure to double check the evaluation setup before turning on the supplies.
7. After powering up the evaluation board, the CR1 LED is on when the evaluation board is properly connected to adaptor and the adaptor is correctly connected to a USB source.

ADDITIONAL SETUP INFORMATION

Scope

If the scope vertical input range is limited to 100 mV only, place a high frequency 12 dB attenuator (such as a PicoSeconds Lab model 5510K 40 GHz attenuator) on each of the scope inputs.

Coaxial Cables

All coaxial cables to and from the evaluation board must be as short as possible and be of very high quality and high bandwidth, such that the chosen coaxial cable allows a 40 GHz signal to be attenuated no more than 3 dB as seen at the end of the length of cable used. This is necessary for viewing and transporting the 10 Gbps signal from the evaluation board to the scope. See the Scope Shots section for example scope shots at 8.5 Gbps and 9.95328 Gbps.

Note that if the pattern generator, when connected directly to the scope, cannot produce quality signals as good or better than the eye plot shown in Figure 5, it means that the bandwidth of the scope or cables or the quality of the pattern generator is insufficient to view rates around 10 Gbps.

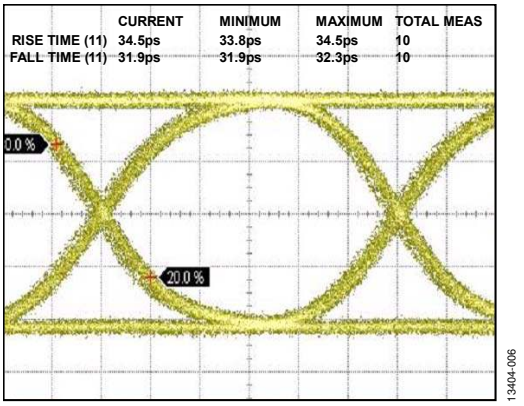

Figure 5. A Reference Eye at 9.953 Gbps

Set the pattern generator to 500 Mbps with a PRBS pattern of 7, and set the data amplitude to 500 mV. Turn on the 3.3 V, 1.2 V and 1.8 V supplies. The current draws should be initially approximately 10 mA for 3.3 V, 250 mA for 1.2 V, and 20 mA for 1.8 V

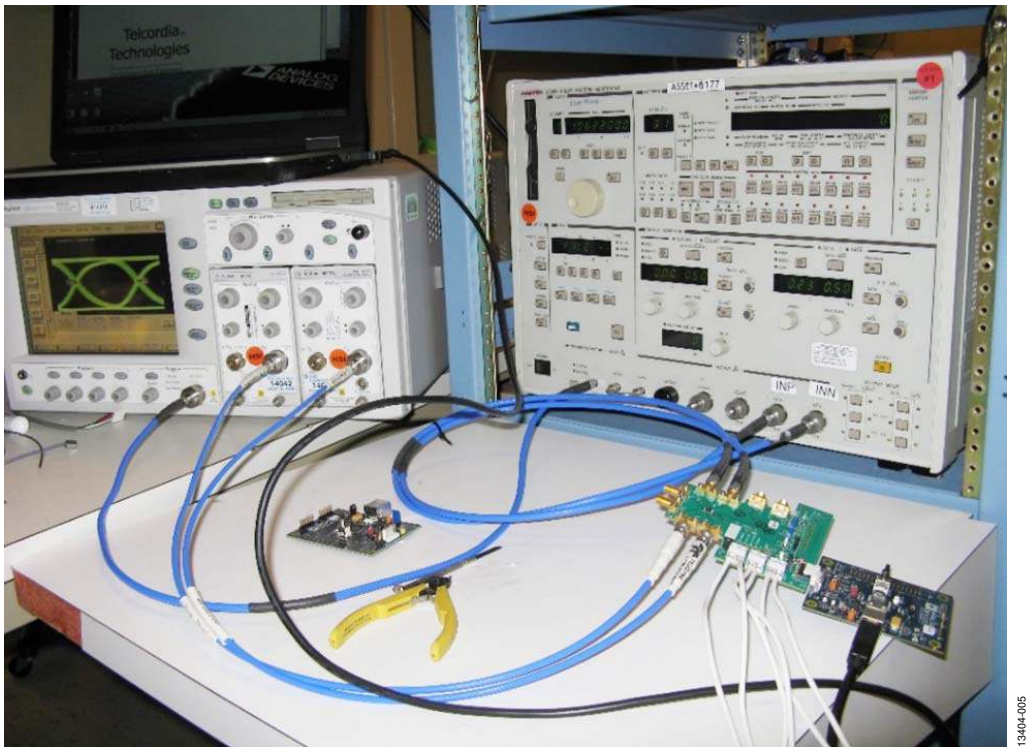

Figure 6. Test Kit Setup

POWER ON

When the input signal is a PRBS7 pattern at 500 Mbps, turn on the 3.3 V, 1.8 V, and 1.2 V supplies. The ADN29xx typically draws a current of 10 mA from the 3.3 V supply, 20 mA from the 1.8 V supply, and 250 mA from the 1.2 V supply. At different input rates, each supply current can be data rate dependent.

SOFTWARE INSTALLATION

Install the adaptor software:

1. Insert the software CD (included in the evaluation kit) into your PC.
2. From the CD drive, double-click **BasicI2C.zip** and load the **BasicI2C.exe** onto your PC.
3. Double-click **BasicI2C.exe**, and a dialog box appears as shown in Figure 7.

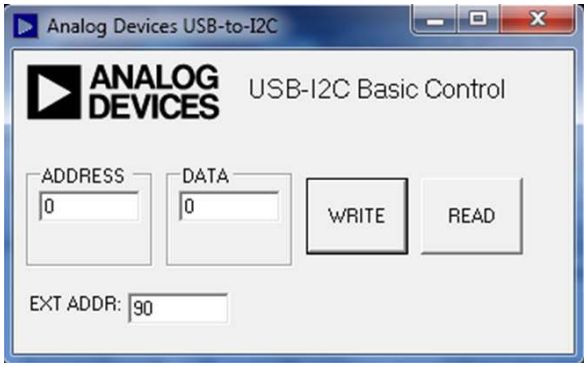

Figure 7. USB-to-I²C Dialog Box

4. Check the communication link from the PC to the adaptor and to the evaluation board:
   a. The default I²C address of the evaluation board is 0x80H.
   b. The released ADN29xx device revision number, at Register Address 0x48, is 54.
   c. Write the register addresses in the dialog box, as shown in Figure 8, and then click **READ**.

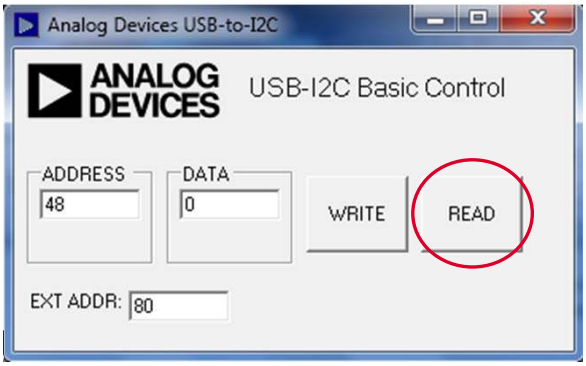

*Figure 8. **READ** Button*

   d. If the communication setup between the PC and the evaluation board is correct, the **DATA** field content changes to 54.

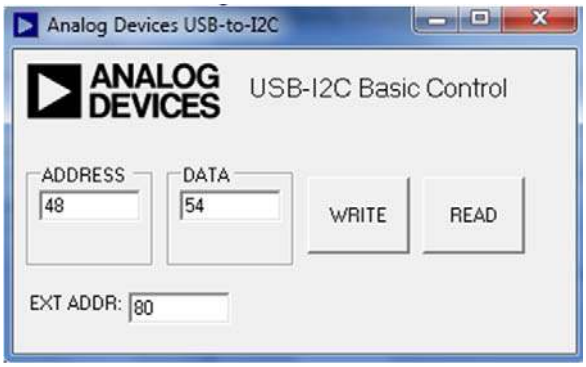

*Figure 9. **DATA** Field Update*

   e. If the **DATA** field does not update, or feedback errors, the link is not set up correctly. Double check the link and software installation, and repeat Step A to Step C, or contact Analog Devices for help.

EVALUATION BOARD APPLICATIONS

PRBS GENERATOR

To operate the ADN29xx as a PRBS generator, the evaluation board needs a clock signal to the inputs at an appropriate frequency.

In LTD mode, a data input signal can work as the necessary clock input. For example, a 5 Gbps input signal can be used as the recovered clock source, and then a 5 Gbps PRBS pattern can be built up by this recovered clock. The example configuration is shown in Figure 10.

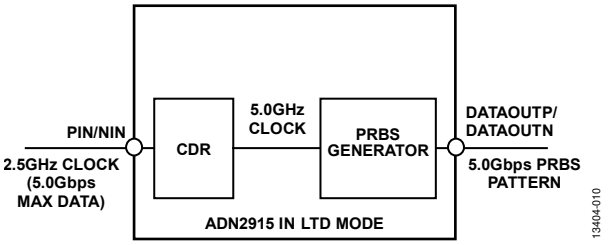

Figure 10. LTD Mode Configuration

Configure the ADN29xx in LTD mode using the commands shown in Table 2.

Table 2. LTD Mode I²C Writes

Functions	Register Address	Content	Comments
I²C Write	0x08	0x00	CDR_MODES = 000. Place DUT into LTD mode.
I²C Write	0x0A	0x05	REFCLK_PD = 1. Disable reference clock buffer.

In LTD mode, the PRBS generator limitation is that it needs a high speed clock source to produce a high speed PRBS pattern.

In LTR mode, the CDR can work as a frequency multiplier, allowing high frequency PRBS patterns to be produced with lower frequency reference clocks. The example configuration is shown in Figure 11.

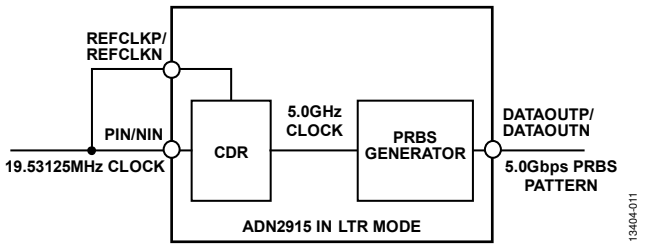

Figure 11. LTR Mode Configuration

A low frequency reference clock is applied to the ADN29xx as both the reference clock and data inputs. Both signals are required because the CDR locks to the reference clock signal in LTR mode, but requires a valid signal on the data inputs to maintain lock.

Configure the ADN29xx in LTR mode using the commands shown in Table 3.

Table 3. LTR Mode I²C Writes

Functions	Register Address	Content	Comments
I²C Write	0x08	0x20	CDR_Modes = 010. Place DUT into LTR mode.
I²C Write	0x0A	0x01	REFCLK_PD = 0. Enable reference clock buffer.
I²C Write	0x0F	Case dependent	Set FREF_RANGE and DATA_TO_REF_RATIO to desired values.

By writing to Register 0x0F over I²C, the user can configure the ADN29xx to lock to any binary multiple of the reference clock. The relationship between the data rate and the reference clock is shown in the following equation:

$$Data\ Rate/2^{(LTR\_MODE[3:0]-1)} = REFCLK/2^{LTR\_MODE[5:4]}$$

The LTR_MODE[5:4] is based the frequency range of the input reference clock according to Table 4.

Table 4. LTR_MODE[5:4]

LTR_MODE[5:4]	Range (MHz)	LTR_MODE[3:0]	Ratio
0	11.05 to 22.1	0000	2^{-1}
1	22.1 to 44.2	0001	20
10	44.2 to 88.4	n	2^{n-1}
11	88.4 to 176.8	1010	29

Figure 11 shows an example of how to produce a 5.0 Gbps PRBS pattern in LTR mode. Note that a 19.53125 MHz clock is necessary.

In this case, setting LTR_MODE[5:4] = 0x00b and LTR_MODE[3:0] = 0x1001b sets the ADN29xx lock to 5.0 Gbps. The CDR clock then clocks the internal PRBS generator, producing a 5.0 Gbps PRBS pattern on the data outputs.

Note that if a 39.0625 MHz, 78.125MHz, or 156.25 MHz reference clock was used instead, LTR_MODE[5:4] must be set to 1, 2, or 3, respectively. However, LTR_MODE[3:0] is still 9, because the ratio remains the same between the desired data rate and the divided down reference clock, not the input reference clock (only) as shown in the previous equation.

Using the same 19.53125 MHz clock, the ADN29xx can produce frequencies shown in Table 5.

Table 5. ADN29xx Output Frequencies

LTR_ MODE[3:0]	Multiply By	Output Frequency
0	$2^{(0-1)} = ½$	19.53125 MHz × ½ = 9.76525 MHz
1	$2^{(1-1)} = 1$	19.53125 MHz × 1 = 19.53125 MHz
2	$2^{(2-1)} = 2$	19.53125 MHz × 2 = 39.0625 MHz
3	$2^{(3-1)} = 4$	19.53125 MHz × 4 = 78.125 MHz
4	$2^{(4-1)} = 8$	19.53125 MHz × 8 = 156.258 MHz
5	$2^{(5-1)} = 16$	19.53125 MHz × 16 = 312.5 MHz
6	$2^{(6-1)} = 32$	19.53125 MHz × 32 = 625 MHz
7	$2^{(7-1)} = 64$	19.53125 MHz × 64 = 1250 MHz
8	$2^{(8-1)} = 128$	19.53125 MHz × 128 = 2500 MHz
9	$2^{(9-1)} = 256$	19.53125 MHz × 256 = 5000 MHz
10	$2^{(10-1)} = 512$	19.53125 MHz × 512 = 10,000 MHz

This technique can be applied to produce PRBS patterns at other frequencies, simply by adjusting the reference clock frequency accordingly.

Finally, enable the PRBS generator and program the correct PRBS pattern. For example, if selecting PRBS7, perform the write as shown in Table 6.

Table 6. PRBS I²C Write

Function	Register Address	Content	Comments
I²C Write	0x39	0x04	Enable the PRBS generation and the PRBS 7

See the PRBGS Generator/Receiver section in the ADN2905/ADN2913/ADN2915/ADN2917 data sheet for details.

ERROR DETECTOR

Only I²C commands are required to operate the PRBS detector on the ADN29xx, because the CDR automatically locks to the incoming data in lock to data (LTD) mode.

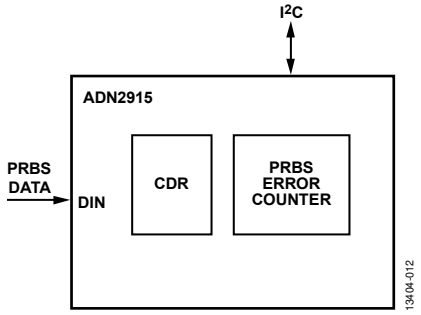

Figure 12.

The following steps configure the PRBS detector:

1. Set DATA_RECEIVER_ENABLE (Register PRBS Rec 1, Bit 2) to 1, and also set DATA_RECEIVER_MODE[1:0] (Register PRBS Rec 1, Bits[1:0]) according to the desired PRBS pattern (0 for PRBS7, 1 for PRBS15, 2 for PRBS31).
2. Setting DATA_RECEIVER_MODE[1:0] to 3 leads to a one-shot sampling of recovered data into DATA_LOADED[15:0].
3. Set DATA_RECEIVER_CLEAR (Register PRBS Rec 1, Bit 3) to 1 followed by 0 to clear PRBS_ERROR and PRBS_ERROR_COUNT.
4. The states of PRBS_ERROR (Register PRBS Rec 3, Bit 1) and PRBS_ERROR_COUNT[7:0] (Register PRBS Rec 2, Bits[7:0]) can be frozen by setting DATA_RECEIVER_ ENABLE (Register PRBS Rec 1, Bit 2) to 0.

For example, to detect a PRBS7 pattern, set up the registers as shown in Table 7.

The PRBS error detector registers are shown in Table 8.

Table 7. Detecting a PRBS7 Pattern

Function	Register Address	Content	Comments
I²C Write	0x3F	0x04	Enable the PRBS detector, look for PRBS7.
I²C Write	0x3F	0x0C	Clear both PRBS error counter at Address 0x40 and PRBS_ERROR bit while keeping the DATA_RECEIVER and DATA_RECEIVER_MODE[1:0] bit settings unchanged.
I²C Write	0x3F	0x04	Restart the PRBS detector, look for PRBS7.
I²C Read	0x41		Monitor if PRBS_ERROR bit = 1, if yes.
I²C Read	0x40		Obtain the error counts.
I²C Write	0x3F	0x00	Disable the PRBS detector, preserve the values of PRBS error count and PRBS error bit.

Table 8. PRBS Error Detector Registers

Register Name	R/W	Address (Hex)	Default (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
PRBS Rec 1	R/W	0x3F	0x00	0	0	0	0	DATA_ RECEIVER_ CLEAR	DATA_ RECEIVER_ ENABLE	DATA_ RECEIVER_ MODE[1:0]	
PRBS Rec 2	R	0x40	0x00	PRBS_ERROR_COUNT[7:0]							
PRBS Rec 3	R	0x41	0x00								PRBS_ERROR
PRBS Rec 4	R	0x42	N/A	DATA_LOADED[7:0]							
PRBS Rec 5	R	0x43	N/A	DATA_LOADED[15:8]							
PRBS Rec 6	R	0x44	N/A	DATA_LOADED[23:16]							
PRBS Rec 7	R	0x45	N/A	DATA_LOADED[31:24]							

PRBS PATTERNS

In PRBS generation mode, the PRBS pattern is determined by DATA_GEN_MODE[1:0], as shown in Table 9.

Table 9. PRBS Generation Mode Settings

PRBS Pattern	DATA_GEN_MODE[1:0]	PRBS Polynomial
PRBS7	0x00	$1 + x^6 + x^7$
PRBS15	0x01	$1 + x^{14} + x^{15}$
PRBS31	0x10	$1 + x^{28} + x^{31}$
PROG_DATA[31:0]	0x11	Not applicable

In PRBS detection mode, the PRBS pattern is set by DATA_RECEIVER_MODE[1:0], as shown in Table 10.

Table 10. PRBS Detection Mode Settings

PRBS Pattern	DATA_RECEIVER_MODE[1:0]	PRBS Polynomial
PRBS7	0x00	$1 + x^6 + x^7$
PRBS15	0x01	$1 + x^{14} + x^{15}$
PRBS31	0x10	$1 + x^{28} + x^{31}$
PROG_DATA[31:0]	0x11	Not applicable

The DATA_GEN_MODE[1:0] bits are defined in Register 0x39. The DATA_RECEIVER_MODE[1:0] bits are defined in Register 0x3F.

Table 11. PRBS Gen 1 Register

Register Name	R/W	Address (Hex)	Default (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
PRBS Gen 1	R/W	0x39	0x00	0	0	DATA_CID_BIT	DATA_CID_EN	0	DATA_GEN_ENABLE	DATA_GEN_MODE[1:0]	

Table 12. PRBS Rec 1 Register

Register Name	R/W	Address (Hex)	Default (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
PRBS Rec 1	R/W	0x3F	0x00	0	0	0	0	DATA_RECEIVER_CLEAR	DATA_RECEIVER_ENABLE	DATA_RECEIVER_MODE[1:0]	

SCOPE SHOTS

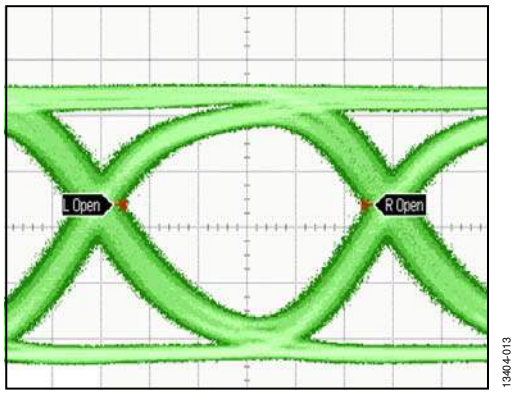

Figure 13. 1000 Waveforms and Persist Mode at 11.3 Gbps

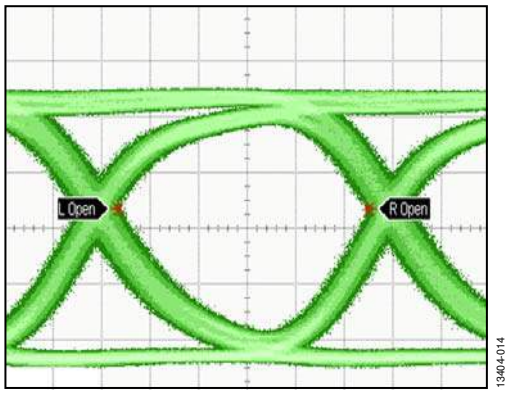

Figure 14. 1000 Waveforms and Persist Mode at 10.3 Gbps

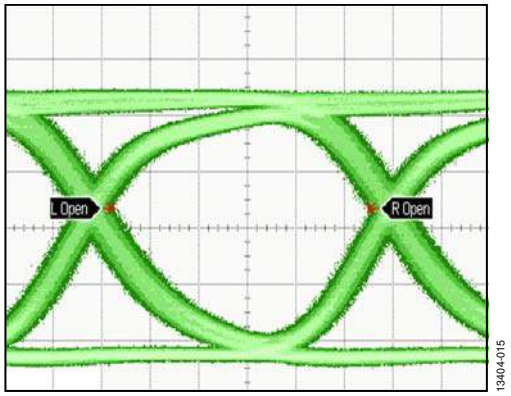

Figure 15. 1000 Waveforms and Persist Mode at 9.953 Gbps

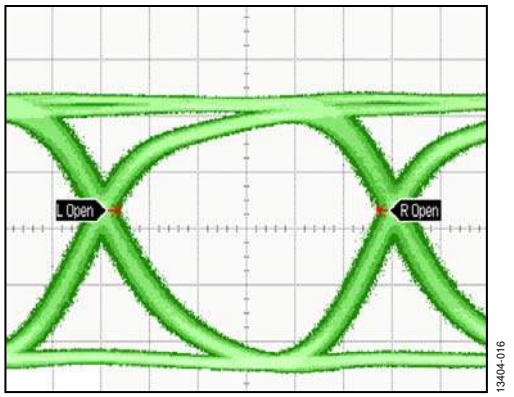

Figure 16. 1000 Waveforms and Persist Mode at 8.5 Gbps

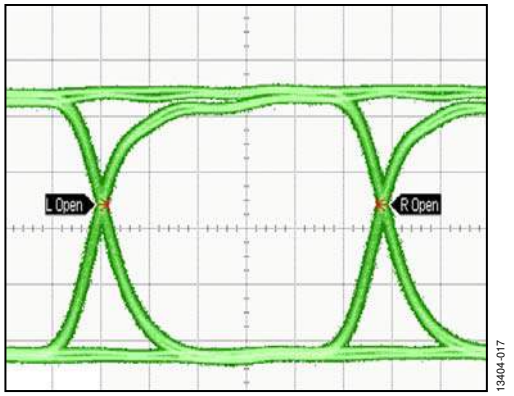

Figure 17. 1000 Waveforms and Persist Mode at 4.25 Gbps

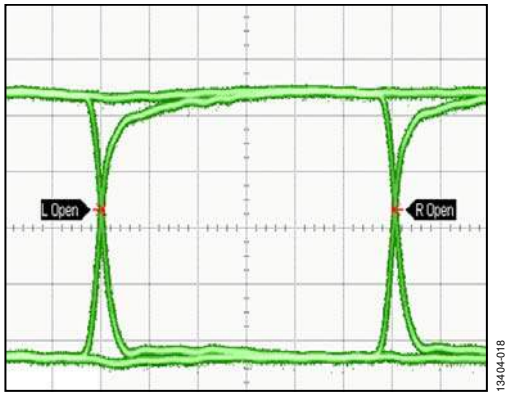

Figure 18. 1000 Waveforms and Persist Mode at 1.25 Gbps

EVALUATION BOARD BILL OF MATERIALS

Table 13.

Qty	Reference Designator	Description	Manufacturer	Part No.
1		PCB	Analog Devices	08_040368a
1	A1	IC, swappable dual isolator	Analog Devices	ADUM1250ARZ
2	C1, C25	Capacitor, ceramic, chip, X7R, 0402	TDK	C1005X7R1E103K
17	C3 to C6, C8 to C11, C13 to C19, C34, C35	Capacitor, ultra-broadband	ATC	545L104KT10
8	C2, C7, C12, C20 to C23, C36	Capacitor, tantalum	AVX	TAJA106K010RNJ
1	C24	Capacitor, ceramic, 0805, X7R	Murata	GRM21BR71H105KA12L
2	C26,C27	Capacitor, ceramic, X7R, 0402	Murata	GRM155R71C104KA88D
1	C28	Capacitor, ceramic, X7R	Murata	GRM155R71C333KA01D
6	IN_N, IN_P, CLK_N, CLK_P, DAT_N, DAT_P	Connector, PCB, SMA, RA jack	Rosenberger	32K243-40ML5
3	CR1, CR2, CR4	LED, red, surface mount	ROHM	SML-310LTT86
1	DUT1	IC, clock and data recovery	Analog Devices	ADN2905ACPZ/ ADN2913ACPZ/ ADN2915ACPZ/ ADN2917ACPZ
1	P1	Connector, PCB, receptacle, 0.100 in, 5-position, RA	Samtec	SSW-105-02-G-S-RA
3	P10, P14, P15	Connector, PCB, header, 2-position	Samtec	TSW-102-08-G-S
2	P3,P11	Connector, PCB, Berg, HDR, ST, male, 3P	Samtec	TSW-103-08-G-S
3	P7-P9	Connector, PCB, term, black, 2P, ST	Lumberg	KRM2 02
1	Q1	Transistor, N-channel FET, enhancement mode	Fairchild Semiconductor	FDV303N
2	Q2,Q3	Transistor, MMBT3904, NPN, SOT-23	Fairchild	MMBT3904
4	R1, R3, R12, R13	Resistor, film, SMD, 0603	Phycomp (Yageo)	9C06031A2001FKHFT
4	R6, R8 to R10	Resistor, thick film chip	Panasonic	ERJ-6GEY0R00V
1	R11	Resistor, film, SMD, 1206	Phycomp (Yageo)	9C12063A1001FKHFT
1	R14	Resistor, chip, SMD, jumper	Panasonic	ERJ-2GE0R00X
1	R15	Resistor, thick film chip	Bourns	CR0603-FX-1101ELF
1	R16	Resistor, precision, thick film chip	Panasonic	ERJ-3EKF1003V
2	R2, R5	Resistor, precision, thick film chip, R0603	Panasonic	ERJ-3EKF1181V
1	R20	Resistor, chip, SMD, 0603	Panasonic	ERJ-3EKF2000V
1	R21	Resistor, metal, film, high reliability	Panasonic	ERA-3AEB5621V
2	R4, R7	Resistor, precision, thick film chip, R0603	Panasonic	ERJ-3EKF3481V
2	REF_N, REF_P	Connector, PCB, coaxial, SMA, end launch	Johnson	142-0701-851

EVALUATION BOARD SCHEMATIC

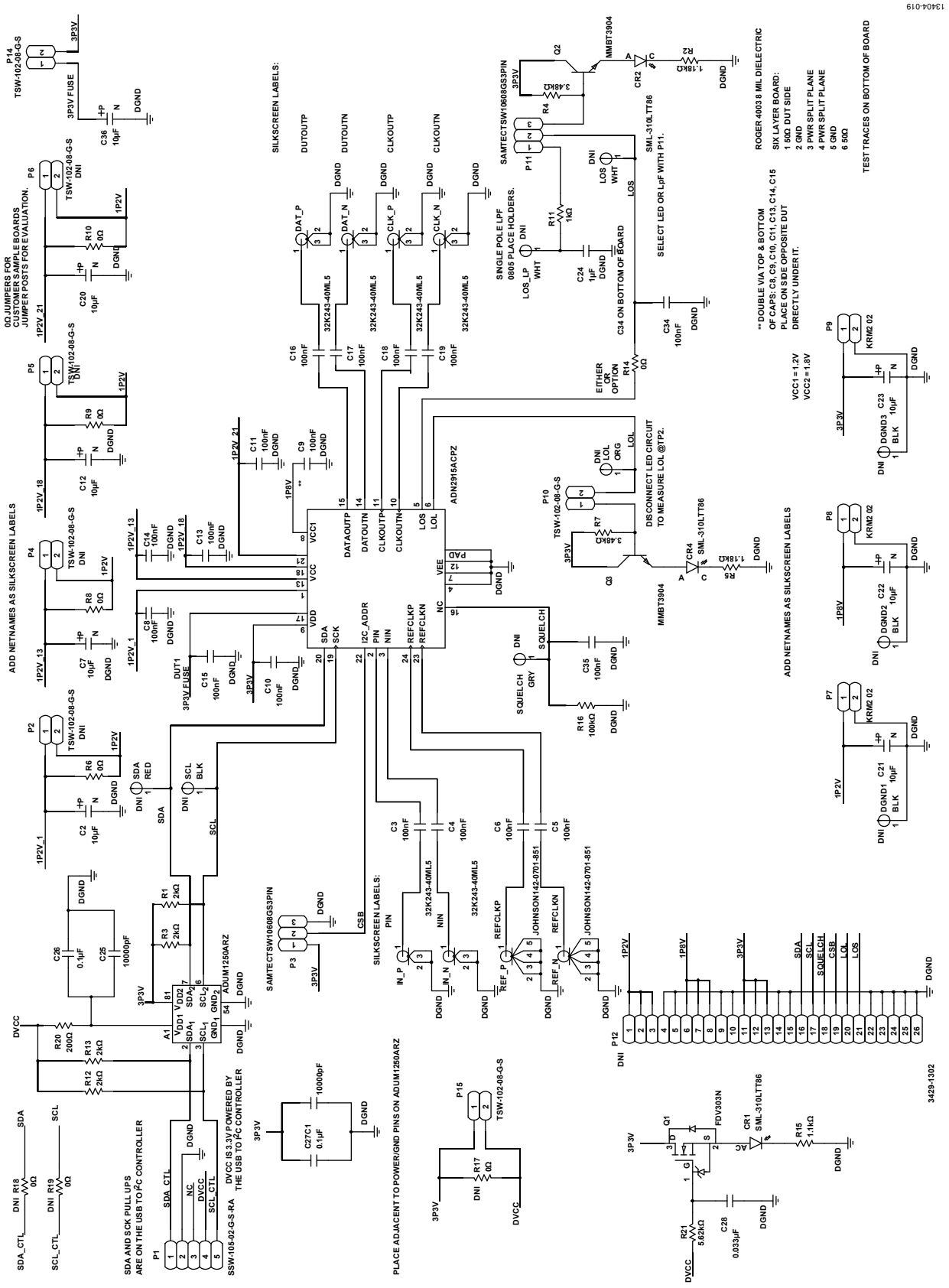

Figure 19. Evaluation Board Schematic

USB-TO-I²C ADAPTOR BOARD SCHEMATIC AND BILL OF MATERIALS

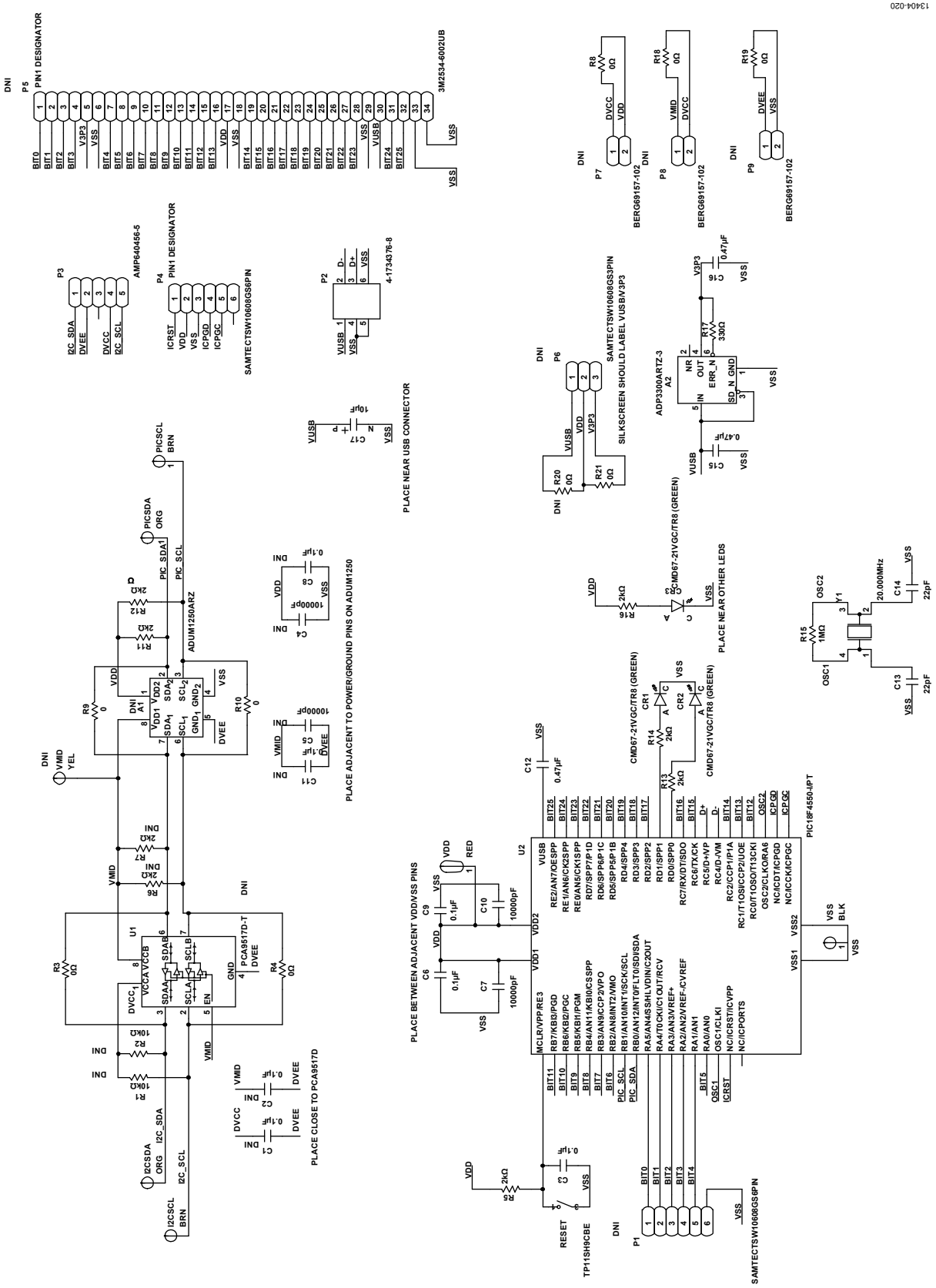

Figure 20. USB-to-I²C Adaptor Board Schematic

Table 14. USB-to-I²C Adaptor Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part No.
1	A2	IC, high accuracy, anyCAP®, 50 mA, LDO linear regulator	Analog Devices	ADP3300ARTZ-3-RL7
2	C7, C10	Capacitor, monolithic, ceramic, X7R, 0603	Murata	GRM188R71E103KA01D
1	C12	Capacitor, chip, ceramic, X7R, 0603	Murata	GCM188R71C474KA55D
2	C13, C14	Capacitor, ceramic	Phycomp (Yageo)	0402CG220J9B200
2	C15, C16	Capacitor, ceramic X7R	AVX	CM21X7R474K16AT
1	C17	Capacitor, tantalum, chip	AVX	TPSD106K035R0125
3	C3, C6, C9	Capacitor, ceramic, X7R, 0603	AVX	06035C104KAT2A
3	CR1 to CR3	Diode, SMD LED	Chicago Mini Lamp	CMD67-21VGC/TR8
2	I2CSCL, PICSCL	Connector, PCB, test point, brown	Components Corporation	TP104-01-01
2	I2CSDA, PICSDA	Connector, PCB, test point, orange	Components Corporation	TP104-01-03
1	P2	Connector, PCB, USB, Type B, R/A, thru hole	AMP	4-1734376-8
1	P3	Connector, PCB, header, vertical, 5-position	AMP	AMP640456-5
1	P4	Connector, PCB, Berg, header, ST, male, 6P	Samtec	TSW-106-08-G-S
1	P6	Connector, PCB, Berg, header, ST, male, 3P	Samtec	TSW-103-08-G-S
3	P7 to P9	Connector, PCB, Berg, jumper, ST, male, 2P	Berg	69157-102
4	R3, R4, R9, R10	Resistor, film, SMD, 0603	Multicomp	MC0603WG00000T5E-TC
6	R5, R11 to R14, R16	Resistor, film, SMD, 0603	Phycomp (Yageo)	9C06031A2001FKHFT
1	R15	Resistor, precision, thick film chip, R0603	Panasonic	ERJ-3EKF1004V
1	R17	Resistor, film, SMD, 0603	Panasonic	ERA-3YEB331V
1	RESET	Switch, SPST, ST, push button	C&K	TP11SH9CBE
1	U2	IC, high performance USB microcontrollers	Microchip Technology	PIC18F4550-I/PT
1	VDD	Connector, PCB, test point, red	Components Corporation	TP-104-01-02
1	VSS	Connector, PCB, test point, black	Components Corporation	TP-104-01-00
1	Y1	IC, crystal oscillator	ECS	ECS-200-20-18

APPENDIX

Prior to this evaluation board revision, Analog Devices offered an early version of this evaluation board and the companion adaptor.

The early version evaluation kit was composed of the following:

- ADN29xx evaluation board
- Adaptor
- USB cable
- A document CD
- Customized cable

Figure 21 shows where changes were made in the new evaluation board design (marked in yellow), and how the early version of the evaluation board connected to the early version adaptor.

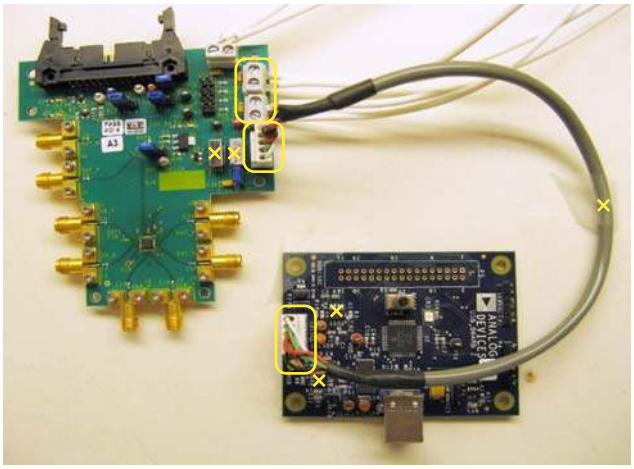

Figure 21. Early Version Evaluation Board and Adaptor

For more details on the early version evaluation board, customized cable, and companion adaptor, contact Analog Devices sales (www.analog.com/sales).