#### **Features**

- Fast Read Access Time 90 ns
- Dual Voltage Range Operation
  - Low Voltage Power Supply Range, 3.0V to 3.6V or Standard 5V  $\pm$  10% Supply Range
- Compatible With JEDEC Standard AT27C040
- Low Power 3.3-volt CMOS Operation
  - 20  $\mu$ A max. (less than 1  $\mu$ A typical) Standby for  $V_{CC}$  = 3.6V
  - 36 mW max. Active at 5 MHz for V<sub>CC</sub> = 3.6V
- JEDEC Standard Packages
  - 32-Lead PLCC
  - 32-Lead TSOP (8 x 20 mm)
  - 32-Lead VSOP (8 x 14 mm)
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid<sup>™</sup> Programming Algorithm 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
  - JEDEC Standard for LVTTL
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

#### **Description**

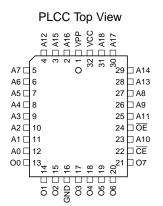
The AT27LV040A is a high performance, low power, low voltage, 4,194,304-bit one-time programmable read only memory (OTP EPROM) organized as 512K by 8 bits. It requires only one supply in the range of 3.0 to 3.6V in normal read mode operation, making it ideal for fast, portable systems using battery power.

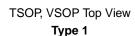
Atmel's innovative design techniques provide fast speeds that rival 5V parts while keeping the low power consumption of a 3V supply. At  $V_{CC}$  = 3.0V, any byte can be accessed in less than 90 ns. With a typical power dissipation of only 18 mW at 5 MHz and  $V_{CC}$  = 3.3V, the AT27LV040A consumes less than one half the power of a standard 5V EPROM. Standby mode supply current is typically less than 1  $\mu$ A at 3.3V.

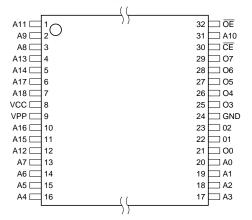
(continued)

# **Pin Configurations**

Pin Name	Function
A0 - A18	Addresses
O0 - O7	Outputs
CE	Chip Enable
ŌĒ	Output Enable









4-Megabit (512K x 8) Low Voltage OTP EPROM

AT27LV040A

Rev. 0557B-10/98





The AT27LV040A is available in industry standard JEDEC-approved one-time programmable (OTP) plastic PLCC, TSOP, and VSOP packages. All devices feature two-line control (CE, OE) to give designers the flexibility to prevent bus contention.

The AT27LV040A operating with  $V_{CC}$  at 3.0V produces TTL level outputs that are compatible with standard TTL logic devices operating at  $V_{CC}$  = 5.0V. The device is also capable of standard 5-volt operation making it ideally suited for dual supply range systems or card products that are pluggable in both 3-volt and 5-volt hosts.

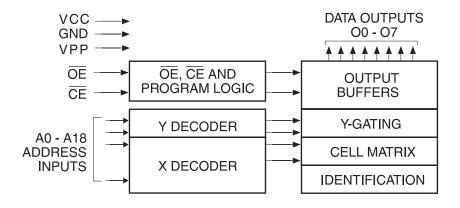
Atmel's AT27LV040A has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 μs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV040A pro-

grams exactly the same way as a standard 5V AT27C040 and uses the same programming equipment.

#### **System Considerations**

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1  $\mu\text{F}$  high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V $_{\text{CC}}$  and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7  $\mu\text{F}$  bulk electrolytic capacitor should be utilized, again connected between the V $_{\text{CC}}$  and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

#### **Block Diagram**



#### **Absolute Maximum Ratings\***

Temperature Under Bias40°C to +85°C
Storage Temperature65°C to +125°C
Voltage on Any Pin with Respect to Ground2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground2.0V to +14.0V <sup>(1)</sup>
V <sub>PP</sub> Supply Voltage with Respect to Ground2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under "Absolute

> Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect

device reliability

Note:

Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V<sub>CC</sub> + 0.75V dc which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

#### **Operating Modes**

Mode \ Pin	CE	ŌĒ	Ai	V <sub>PP</sub>	V <sub>cc</sub>	Outputs
Read <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	Ai	X <sup>(1)</sup>	V <sub>CC</sub> <sup>(2)</sup>	D <sub>OUT</sub>
Output Disable <sup>(2)</sup>	Х	V <sub>IH</sub>	X	Х	V <sub>CC</sub> <sup>(2)</sup>	High Z
Standby <sup>(2)</sup>	V <sub>IH</sub>	Х	Х	Х	V <sub>CC</sub> <sup>(2)</sup>	High Z
Rapid Program <sup>(3)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	Ai	V <sub>PP</sub>	V <sub>CC</sub> <sup>(3)</sup>	D <sub>IN</sub>
PGM Verify <sup>(3)</sup>	Х	V <sub>IL</sub>	Ai	V <sub>PP</sub>	V <sub>CC</sub> <sup>(3)</sup>	D <sub>OUT</sub>
PGM Inhibit <sup>(3)</sup>	V <sub>IH</sub>	V <sub>IH</sub>	Х	V <sub>PP</sub>	V <sub>CC</sub> <sup>(3)</sup>	High Z
Product Identification <sup>(3)(5)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	$A9 = V_{H}^{(4)}$ $A0 = V_{IH} \text{ or } V_{IL}$ $A1 - A18 = V_{IL}$	х	V <sub>CC</sub> <sup>(3)</sup>	Identification Code

Notes:

- 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
- 2. Read, output disable, and standby modes require,  $3.0V \le V_{CC} \le 3.6V$ , or  $4.5V \le V_{CC} \le 5.5V$ .
- 3. Refer to Programming Characteristics. Programming modes require  $V_{CC}$  = 6.5V.
- 4.  $V_H = 12.0 \pm 0.5 V$ .
- 5. Two identifier bytes may be selected. All Ai inputs are held low  $(V_{IL})$ , except A9 which is set to  $V_H$  and A0 which is toggled low  $(V_{IL})$  to select the Manufacturer's Identification byte and high  $(V_{IH})$  to select the Device Code byte.





# **DC and AC Operating Conditions for Read Operation**

		AT27LV040A-90	AT27LV040A-12	AT27LV040A-15
Operating Temperature	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
(Case)	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V <sub>CC</sub> Power Supply		3.0V to 3.6V	3.0V to 3.6V	3.0V to 3.6V
		5V ± 10%	5V ± 10%	5V ± 10%

# **DC and Operating Characteristics for Read Operation**

Symbol	Parameter	Condition	Min	Max	Units
V <sub>CC</sub> = 3.0V	to 3.6V				
I <sub>LI</sub>	Input Load Current	$V_{IN} = 0V \text{ to } V_{CC}$		±1	μΑ
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>		±5	μΑ
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	$V_{PP} = V_{CC}$		10	μΑ
1	V (1) Standby Current	$I_{SB1}$ (CMOS), $\overline{CE} = V_{CC \pm} 0.3V$		20	μΑ
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	$I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V		100	μΑ
I <sub>CC</sub>	V <sub>CC</sub> Active Current	$f = 5 \text{ MHz}, I_{OUT} = 0 \text{ mA}, \overline{CE} = V_{IL}$		10	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.0 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2.0 mA	2.4		V
V <sub>CC</sub> = 4.5V	to 5.5V				
I <sub>LI</sub>	Input Load Current	$V_{IN} = 0V \text{ to } V_{CC}$		±1	μΑ
$I_{LO}$	Output Leakage Current	$V_{OUT} = 0V$ to $V_{CC}$		±5	μΑ
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	$V_{PP} = V_{CC}$		10	μΑ
	V (1) Ctandley Compat	$I_{SB1}$ (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μΑ
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	$I_{SB2}$ (TTL), $\overline{CE}$ = 2.0 to $V_{CC}$ + 0.5V		1	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	$f = 5 \text{ MHz}, I_{OUT} = 0 \text{ mA}, \overline{CE} = V_{IL}$		30	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

Notes: 1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously with or after  $V_{PP}$ 

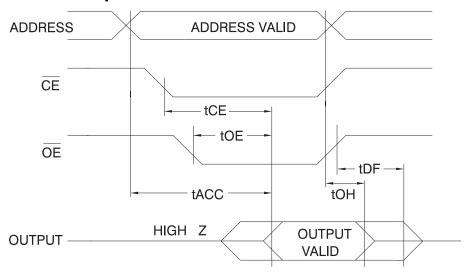
<sup>2.</sup>  $V_{PP}$  may be connected directly to  $V_{CC}$ , except during programming. The supply current would then be the sum of  $I_{CC}$  and  $I_{PP}$ 

#### **AC Characteristics for Read Operation**

 $V_{CC}$  = 3.0V to 3.6V and 4.5V to 5.5V

			AT27LV	AT27LV040A-90		AT27LV040A-12		AT27LV040A-15	
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Units
t <sub>ACC</sub> (3)	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		90		120		150	ns
t <sub>CE</sub> <sup>(2)</sup>	CE to Output Delay	OE = V <sub>IL</sub>		90		120		150	ns
t <sub>OE</sub> <sup>(2)(3)</sup>	OE to Output Delay	CE = V <sub>IL</sub>		50		50		60	ns
t <sub>DF</sub> <sup>(4)(5)</sup>	OE or CE High to Output Float, whichever occurred first			60		40		50	ns
t <sub>OH</sub>	Output Hold from Address, CE or OE, whichever occurred first		0		0		0		ns

# AC Waveforms for Read Operation<sup>(1)</sup>



- Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V. See Input Test Waveforms and Measurement Levels.
  - 2.  $\overline{\text{OE}}$  may be delayed up to  $t_{\text{CE}}$   $t_{\text{OE}}$  after the falling edge of  $\overline{\text{CE}}$  without impact on  $t_{\text{CE}}$ .
  - 3.  $\overline{\text{OE}}$  may be delayed up to  $t_{\text{ACC}}$   $t_{\text{OE}}$  after the address is valid without impact on  $t_{\text{ACC}}$ .
  - 4. This parameter is only sampled and is not 100% tested.
  - 5. Output float is defined as the point when data is no longer driven.

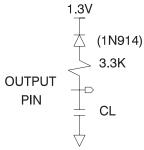




# **Input Test Waveforms and Measurement Level**

# AC DRIVING LEVELS 0.45V $\begin{array}{c} 2.4V \\ \hline \\ 0.8 \\ \hline \\ 1.8 \\ \hline \\ 0.8 \\ \hline 0.8 \\ \hline \\ 0.8 \\$

#### **Output Test Load**



Note: CL = 100 pF including jig capacitance.

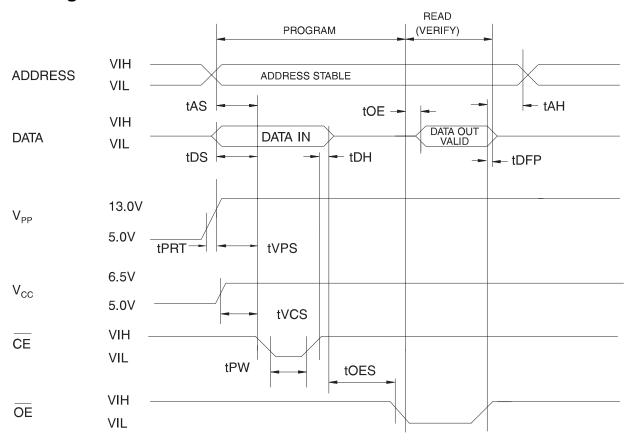
# **Pin Capacitance**

 $f = 1 \text{ MHz}, T = 25^{\circ}C^{(1)}$ 

Symbol	Тур	Max	Units	Conditions
C <sub>IN</sub>	4	8	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub>	8	12	pF	V <sub>OUT</sub> = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

# **Programming Waveforms**<sup>(1)</sup>



- Notes: 1. The Input Timing Reference is 0.8V for  $V_{\rm IL}$  and 2.0V for  $V_{\rm IH}$ .
  - $t_{\text{OE}}$  and  $t_{\text{DFP}}$  are characteristics of the device but must be accommodated by the programmer.
  - When programming the AT27LV040A a 0.1  $\mu$ F capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients.

# **DC Programming Characteristics**

 $T_A = 25 \pm 5^{\circ}C, \ V_{CC} = 6.5 \pm 0.25V, \ V_{PP} = 13.0 \pm 0.25V$ 

			Limits		
Symbol	Parameter	<b>Test Conditions</b>	Min	Max	Units
I <sub>LI</sub>	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		±10	μΑ
$V_{IL}$	Input Low Level		-0.6	0.8	V
$V_{IH}$	Input High Level		2.0	V <sub>CC</sub> + 0.5	V
$V_{OL}$	Output Low Voltage	I <sub>OL</sub> = 2.1 mA		0.4	V
$V_{OH}$	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Program and Verify)			40	mA
I <sub>PP2</sub>	V <sub>PP</sub> Supply Current	CE = V <sub>IL</sub>		20	mA
V <sub>ID</sub>	A9 Product Identification Voltage		11.5	12.5	V



## **AC Programming Characteristics**

 $T_A = 25 \pm 5^{\circ}C, \ V_{CC} = 6.5 \pm 0.25V, \ V_{PP} = 13.0 \pm 0.25V$ 

			Lir		
Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Units
t <sub>AS</sub>	Address Setup Time		2		μs
t <sub>OES</sub>	OE Setup Time	Input Disc and Fall Times	2		μs
t <sub>DS</sub>	Data Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns	2		μs
t <sub>AH</sub>	Address Hold Time		0		μs
t <sub>DH</sub>	Data Hold Time	Input Pulse Levels:	2		μs
t <sub>DFP</sub>	OE High to Output Float Delay <sup>(2)</sup>	.0.45V to 2.4V	0	130	ns
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	Input Timing Reference Level:	2		μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	0.8V to 2.0V	2		μs
t <sub>PW</sub>	CE Program Pulse Width <sup>(3)</sup>	Output Timing Reference Level:	95	105	μs
t <sub>OE</sub>	Data Valid from $\overline{OE^{(2)}}$	0.8V to 2.0V		150	ns
t <sub>PRT</sub>	V <sub>PP</sub> Pulse Rise Time During Programming		50		ns

Notes: 1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ 

# Atmel's 27LV040A Integrated Product Identification Code<sup>(1)</sup>

		Pins					Hex			
Codes	Α0	07	06	<b>O</b> 5	04	О3	02	01	00	Data
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Note: 1. The AT27LV040A has the same Product Identification Code as the AT27C040. Both are programming compatible.

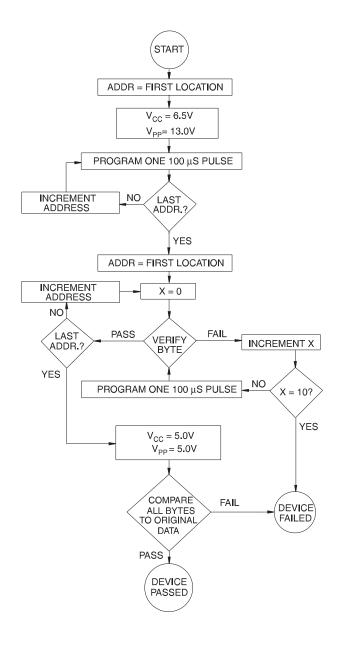
<sup>2.</sup> This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

<sup>3.</sup> Program Pulse width tolerance is 100  $\mu$ sec  $\pm$  5%.

#### **Rapid Programming Algorithm**

A 100  $\mu s$   $\overline{CE}$  pulse width is used to program. The address is set to the first location.  $V_{CC}$  is raised to 6.5V and  $V_{PP}$  is raised to 13.0V. Each address is first programmed with one 100  $\mu s$   $\overline{CE}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100  $\mu s$  pulses are applied with a verification after each

pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $V_{PP}$  is then lowered to 5.0V and  $V_{CC}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.







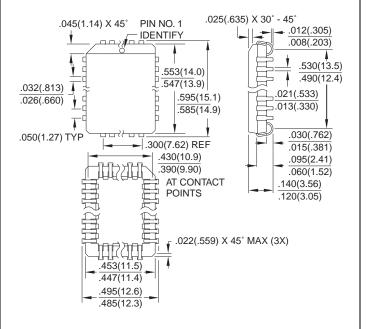
# **Ordering Information**

		(mA)					
t <sub>ACC</sub>	V <sub>CC</sub> = 3.6V		400		0.1.10.1.	<b>D</b>	O
(ns)	Active	Standby	Ordering Code	Package	Operation Range		
90	8	0.02	AT27LV040A-90JC	32J	Commercial		
			AT27LV040A-90TC	32T	(0°C to 70°C)		
			AT27LV040A-90VC	32V			
	8	0.02	AT27LV040A-90JI	32J	Industrial		
			AT27LV040A-90TI	32T	(-40°C to 85°C)		
			AT27LV040A-90VI	32V			
120	8	0.02	AT27LV040A-12JC	32J	Commercial		
			AT27LV040A-12TC	32T	(0°C to 70°C)		
			AT27LV040A-12VC	32V			
	8	0.02	AT27LV040A-12JI	32J	Industrial		
			AT27LV040A-12TI	32T	(-40°C to 85°C)		
			AT27LV040A-12VI	32V			
150	8	0.02	AT27LV040A-15JC	32J	Commercial		
			AT27LV040A-15TC	32T	(0°C to 70°C)		
			AT27LV040A-15VC	32V			
	8	0.02	AT27LV040A-15JI	32J	Industrial		
			AT27LV040A-15TI	32T	(-40°C to 85°C)		
			AT27LV040A-15VI	32V			

	Package Type			
32J	32-Lead, Plastic J-Leaded Chip Carrier (PLCC)			
32T	32-Lead, Plastic Thin Small Outline Package (TSOP) (8 x 20 mm)			
32V	32-Lead, Plastic Thin Small Outline Package (VSOP) (8 x 14 mm)			

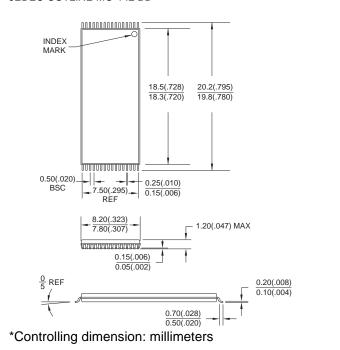
### **Packaging Information**

**32J**, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC) Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-016 AE



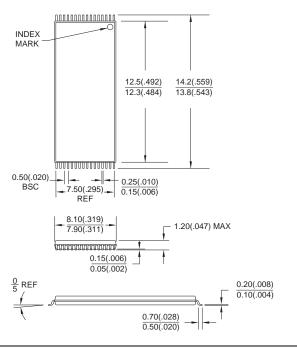
**32T**, 32-Lead, Plastic Thin Small Outline Package (TSOP)

Dimensions in Millimeters and (Inches)\*
JEDEC OUTLINE MO-142 BD



**32V**, 32-Lead, Plastic Thin Small Outline Package (VSOP)

Dimensions in Inches and (Millimeters)
JEDEC OUTLINE MO-142 BA







#### **Atmel Headquarters**

#### Corporate Headquarters

2325 Orchard Parkway San Jose, CA 95131 TEL (408) 441-0311 FAX (408) 487-2600

#### Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

#### Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East
Kowloon, Hong Kong
TEL (852) 27219778
FAX (852) 27221369

#### Japan

Atmel Japan K.K. Tonetsu Shinkawa Bldg., 9F 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan TEL (81) 3-3523-3551 FAX (81) 3-3523-7581

#### **Atmel Operations**

#### Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906 TEL (719) 576-3300 FAX (719) 540-1759

#### Atmel Rousset

Zone Industrielle 13106 Rousset Cedex, France TEL (33) 4 42 53 60 00 FAX (33) 4 42 53 60 01

> Fax-on-Demand North America: 1-(800) 292-8635 International:

1-(408) 441-0732

*e-mail* literature@atmel.com

Web Site http://www.atmel.com

*BBS* 1-(408) 436-4309

#### © Atmel Corporation 1998.

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's website. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

Marks bearing ® and/or ™ are registered trademarks and trademarks of Atmel Corporation.

Printed on recycled paper.

Terms and product names in this document may be trademarks of others.