# HD404202 Series/ HD404222 Series

## Description

These MCU's are CMOS 4-bit single-chip microcomputers with the same architecture as the HMCS400 Series. Each microcomputers incorporate ROM, RAM, I/O, and peripheral functions such as one or two timer/counters. Also, HD404222 Series has two-channel comparators, and a serial interface.

The HD404202 Series includes four chips: the HD404201 with 1-kword ROM and 5-V operation; HD40L4201 with 1-kword ROM and low-voltage operation; HD404202 with 2-kword ROM and 5-V operation; HD40L4202 with 2-kword ROM and low-voltage operation. The HD404222 Series includes three chips: HD404222 with 2-kword ROM and 5-V operation; HD40L4222 with 2-kword and low-voltage operation; HD4074224 with 4-kword PROM.

The HD4074224, incorporating PROM, is a ZTAT™ microcomputer which can dramatically shorten system development period and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

## Features

- The differences between HD404202 Series and HD404222 Series.

| | HD404202 Series | HD404222 Series |
|---|---|---|
| RAM (digits) | 64 | 128 |
| Timers | 8-bit × 1 | 8-bit × 2 |
| Serial interface | — | Clock-synchronous 8-bit × 1 |
| Comparators | — | 2 channels |

- HMCS400 CPU (software-compatible with the HMCS400 Series)
- 1024-word × 10-bit mask ROM (HD404201, HD40L4201)
- 2048-word × 10-bit mask ROM (HD404202, HD40L4202, HD404222, HD40L4222)
- 4096-word × 10-bit PROM (HD4074224)
- 64-digit × 4-bit RAM (HD404201, HD40L4201, HD404202, and HD40L4202)
- 128-digit × 4-bit RAM (HD404222, HD40L4222, and HD4074224)
- 22 I/O pins including 10 high-current pins
- Two timer/counters
  - — 8-bit free-running or watchdog timer (watchdog timer is selectable by mask option) (HD404222 Series)
  - — 8-bit auto-reloading timer/event counter
- Clock-synchronous 8-bit serial interface (HD404222 Series)
- Two-channel comparators (HD404222 Series)
  - — Two analog input pins
  - — Reference voltage pin
- One external interrupt
- Low-power dissipation modes
  - — Standby mode
  - — Stop mode
- Built-in oscillator
  - — Resistor or ceramic oscillator (an external clock is also possible)
- Minimum instruction cycle time
  - — 0.89 µs ($f_{OSC}$ = 4.5 MHz, $V_{CC}$ = 3.5 V–6.0 V)
  - — 3.55 µs ($f_{OSC}$ = 1.125 MHz, $V_{CC}$ = 2.5 V–6.0 V)
  - — 2.0 µs ($f_{OSC}$ = 2.0 MHz, $V_{CC}$ = 2.5 V–6.0 V) for HD40L4222
- Package
  - — 28 pin shrink-type plastic DIP (DP-28S)
  - — 28-pin SOP (FP-28DA)
  - — 30-pin SSOP (FP-30D)

## Type of Product

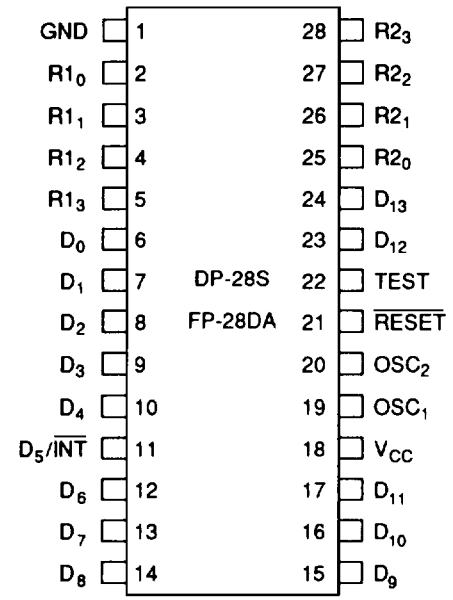
| Device | | ROM Size | Options | Package |
|---|---|---|---|---|
| Mask ROM | HD404201S<br>HD40L4201S | 1024 | Selected by mask option | DP-28S |
| | HD404201FP<br>HD40L4201FP | | | FP-28DA |
| | HD404201FT<br>HD40L4201FT | | | FP-30D |
| | HD404202S<br>HD40L4202S | 2048 | | DP-28S |
| | HD404202FP<br>HD40L4202FP | | | FP-28DA |
| | HD404202FT<br>HD40L4202FT | | | FP-30D |
| | HD404222S<br>HD40L4222S | | | DP-28S |
| | HD404222FP<br>HD40L4222FP | | | FP-28DA |
| | HD404222FT<br>HD40L4222FT | | | FP-30D |
| ZTAT™ | HD4074224S01 | 4096 | Timer A: Free-running timer<br>Oscillator: Resistor | DP-28S |
| | HD4074224S02 | | Timer A: Free-running timer<br>Oscillator: Ceramic oscillator | |
| | HD4074224S03 | | Timer A: Watchdog timer<br>Oscillator: Resistor | |
| | HD4074224S04 | | Timer A: Watchdog timer<br>Oscillator: Ceramic oscillator | |
| | HD4074224FP01 | | Timer A: Free-running timer<br>Oscillator: Resistor | FP-28DA |
| | HD4074224FP02 | | Timer A: Free-running timer<br>Oscillator: Ceramic oscillator | |
| | HD4074224FP03 | | Timer A: Watchdog timer<br>Oscillator: Resistor | |
| | HD4074224FP04 | | Timer A: Watchdog timer<br>Oscillator: Ceramic oscillator | |
| | HD4074224FT01 | | Timer A: Free-running timer<br>Oscillator: Resistor | FP-30D |
| | HD4074224FT02 | | Timer A: Free-running timer<br>Oscillator: Ceramic oscillator | |
| | HD4074224FT03 | | Timer A: Watchdog timer<br>Oscillator: Resistor | |
| | HD4074224FT04 | | Timer A: Watchdog timer<br>Oscillator: Ceramic oscillator | |

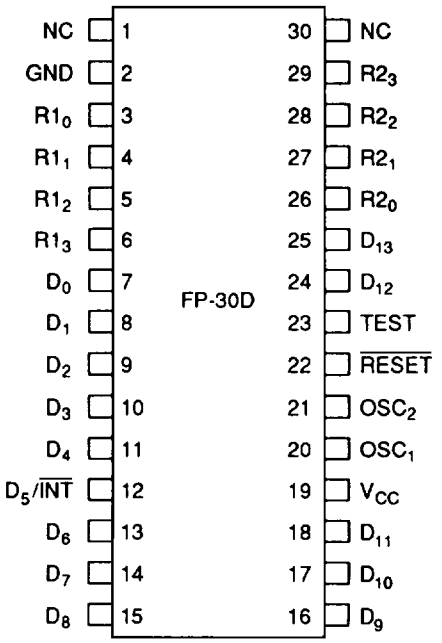
# Differences between Mask ROM and ZTAT™ Microcomputers

| Item | | Mask ROM | | | | | | ZTAT™ |
|---|---|---|---|---|---|---|---|---|
| | | HD404201 | HD40L4201 | HD404202 | HD40L4202 | HD404222 | HD40L4222 | HD4074224 |
| Power supply voltage ($V_{CC}$) | | 3.5 to 6.0 V | 2.5 to 6.0 V | 3.5 to 6.0 V | 2.5 to 6.0 V | 3.5 to 6.0 V | 2.5 to 6.0 V | 3.5 to 5.5 V, 2.7 to 3.5 V |
| Instruction cycle time ($t_{cyc}$) | | 0.89 to 4.0 µs | 3.55 to 10.0 µs | 0.89 to 4.0 µs | 3.55 to 10.0 µs | 0.89 to 4.0 µs | 2.0 to 10.0 µs | 0.89 to 4.0 µs, 2.0 to 10.0 µs |
| ROM | | 1024 × 10-bit | 1024 × 10-bit | 2048 × 10-bit | 2048 × 10-bit | 2048 × 10-bit | 2048 × 10-bit | 4096 × 10-bit |
| RAM | | 64 × 4-bit | 64 × 4-bit | 64 × 4-bit | 64 × 4-bit | 128 × 4-bit | 128 × 4-bit | 128 × 4-bit |
| Watchdog timer/ free running timer | | — | — | — | — | 1 | 1 | 1 |
| Serial interface | | — | — | — | — | 1 | 1 | 1 |
| Comparator | | — | — | — | — | 2 ch | 2 ch | 2 ch |
| I/O pin circuit (standard pins) | Without pull-up MOS (NMOS open drain) (option A) | Available | Available | Available | Available | Available | Available | — |
| | With pull-up MOS (option B) | Available | Available | Available | Available | Available | Available | Available |
| | CMOS (option C) | Available | Available | Available | Available | Available | Available | — |
| Clock generation | Ceramic | Available | Available | Available | Available | Available | Available | Available |
| | Resistor | Available with $t_{cyc}$ = 1.33 to 4.0 µs | — | Available with $t_{cyc}$ = 1.33 to 4.0 µs | — | Available with $t_{cyc}$ = 1.33 to 4.0 µs | — | Available only under $V_{CC}$ = 3.5 to 5.5 V with $t_{cyc}$ = 1.33 to 4.0 µs |
| | External | Available | Available | Available | Available | Available | Available | Available |
| Package | | DP-28S FP-28DA FP-30D | DP-28S FP-28DA FP-30D | DP-28S FP-28DA FP-30D | DP-28S FP-28DA FP-30D | DP-28S FP-28DA FP-30D | DP-28S FP-28DA FP-30D | DP-28S FP-28DA FP-30D |

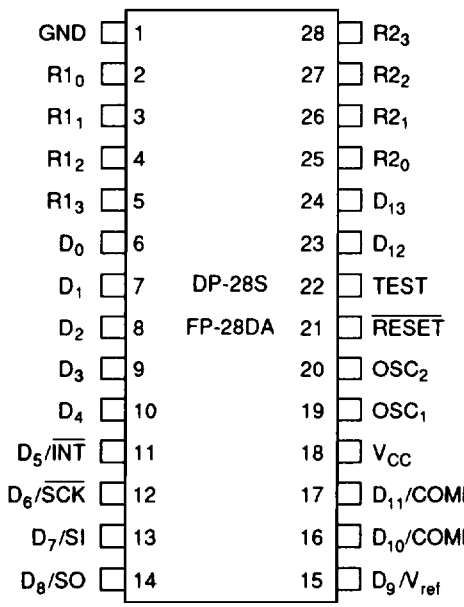
## Pin Arrangement

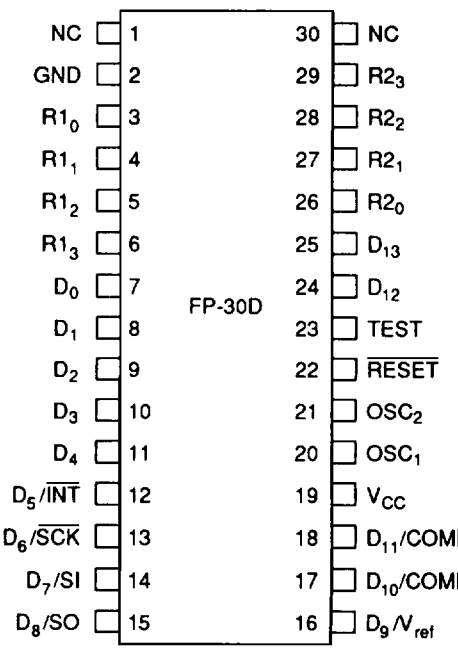
**HD404201, HD40L4201, HD404202, HD40L4202**



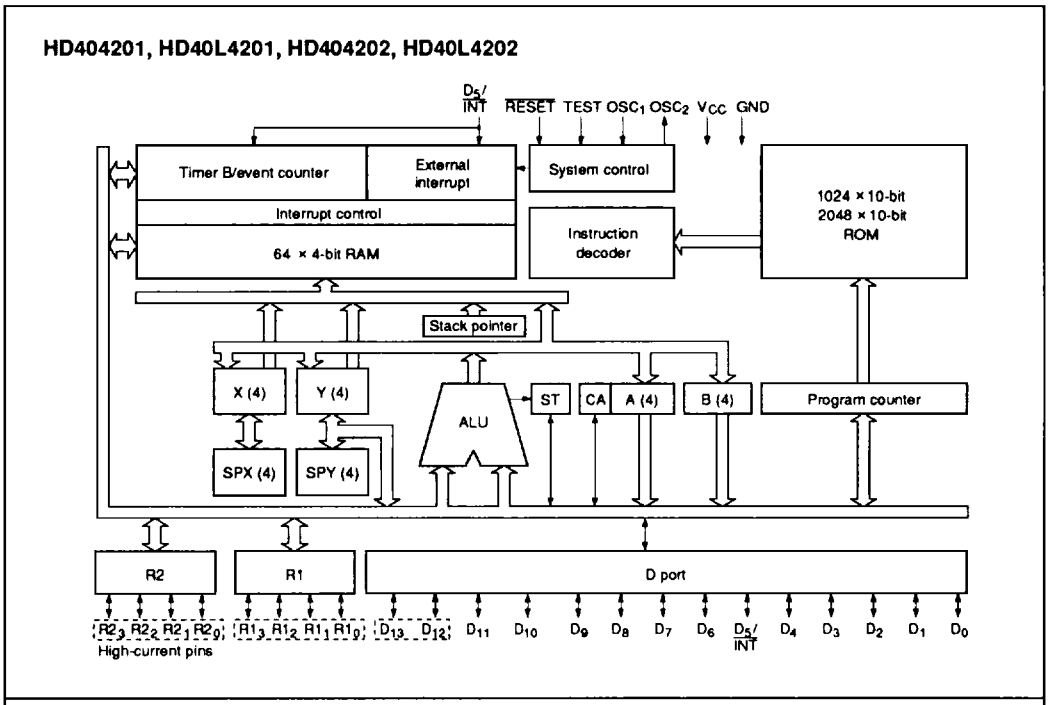



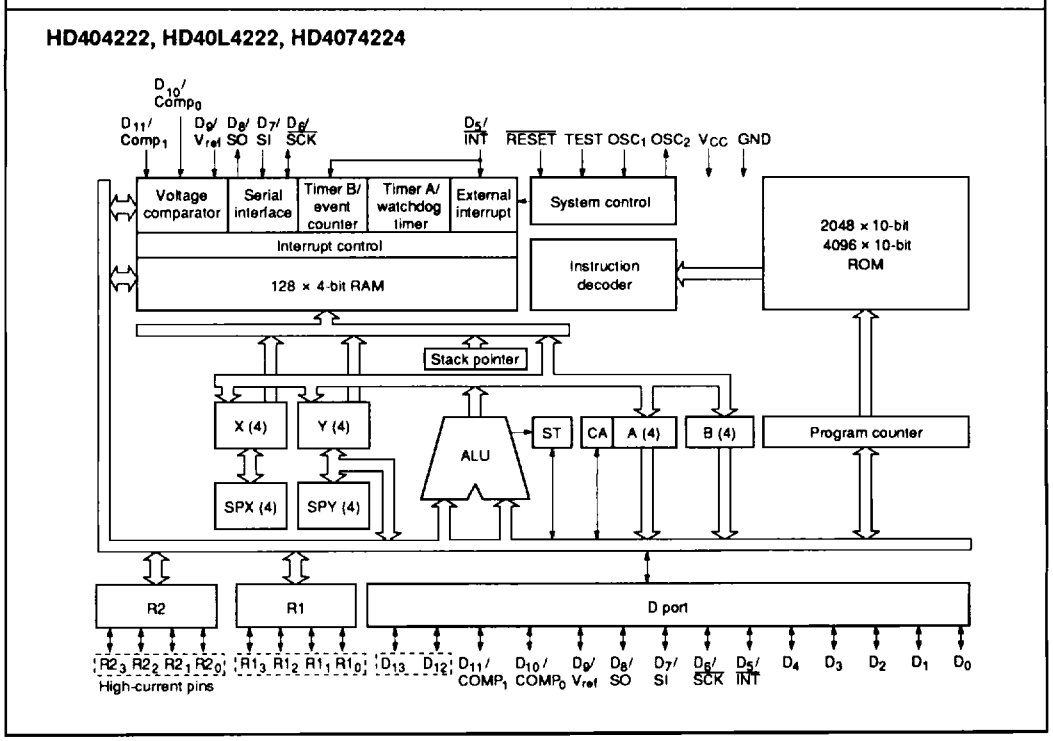

**HD404222, HD40L4222, HD4074224**



## Block Diagram



## Pin Description

| Item | Symbol | Pin Number DP-28S FP-28DA | Pin Number FP-30D | I/O | Function |
|---|---|---|---|---|---|
| Power supply | $V_{CC}$ | 18 | 19 | | Power supply pin |
| | GND | 1 | 2 | | Ground connection pin |
| Test | TEST | 22 | 23 | I | Pin used for test purposes only. Connect it to ground. |
| Reset | $\overline{RESET}$ | 21 | 22 | I | MCU reset pins |
| Oscillator | $OSC_1$, | 19 | 20 | I | Pins for the internal oscillator circuit. Connect them to a resistor or a ceramic oscillator, or connect $OSC_1$ to an external oscillator circuit. The internal oscillator is selected by mask option. |
| | $OSC_2$ | 20 | 21 | O | |
| Port | $D_0$–$D_{13}$ | 6–17, 23, 24 | 7–18, 24, 25 | I/O | Input/output ports addressable by individual bits. Pins $D_{12}$ and $D_{13}$ can output 15 mA maximum. |
| | $R1_0$–$R2_3$ | 2–5, 25–28 | 3–6, 26–29 | I/O | Input/output ports addressable in 4-bit units. These pins can output 15 mA maximum. |
| Interrupt | $\overline{INT}$ | 11 | 12 | I | Input pin for external interrupt. It is also used as an external event input for timer B. It is multiplexed with pin $D_5$. |
| Serial interface* | $\overline{SCK}$ | 12 | 13 | I/O | Serial interface clock input/output pin. It is multiplexed with pin$D_6$. |
| | SI | 13 | 14 | I | Serial interface receive data input pin. It is multiplexed with pin $D_7$. |
| | SO | 14 | 15 | O | Serial interface transmit data output pin. It is multiplexed with pin $D_8$. |
| Comparator* | $V_{ref}$ | 15 | 16 | I | Reference voltage pin to input the threshold voltage of the analog input pins |
| | $COMP_0$, $COMP_1$ | 16, 17 | 17, 18 | I | Analog input pins for the voltage comparator |

* Only applicable for the HD404222 Series.

## Memory Map

### ROM Memory Map

The areas in ROM are described below with its memory map shown in figure 1.

**Vector Address Area:** Locations $0000 through $0009 can be used for JMPL instructions to branch to the starting address of an initialization program for interrupt programs. After MCU reset or an interrupt is performed, the program is executed from a vector address.

**Zero-Page Subroutine Area:** Locations $0000 through $003F can be used for subroutines. The CAL instruction branches to subroutines within this area.

**Pattern Area ($0000 to $03FF: HD404201, HD40L4201; $0000 to $07FF: HD404202, HD40L4202, HD404222, HD40L4222; $0000 to $0FFF: HD4074224):** The P instruction allows reference to ROM data in this area as a pattern.

**Program Area ($0000 to $03FF: HD404201, HD40L4201; $0000 to $07FF: HD404202, HD40L4202, HD404222, HD40L4222; $0000 to $0FFF: HD4074224)**

### RAM Memory Map

In addition to data and stack areas, interrupt control bits and special function registers are also mapped in RAM memory. The RAM memory map shown in figure 2 is described below.

**Interrupt Control Bits Area ($0000 to $0002):** The interrupt control bits area (figure 3) is used for interrupt control. This area and CMR (location $03) register is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Note that if unusable bits are manipulated, the MCU may malfunction (HD404202 Series: bits 0, 1 of $001, and $002; HD404222 Series: bits 2, 3 of $002).

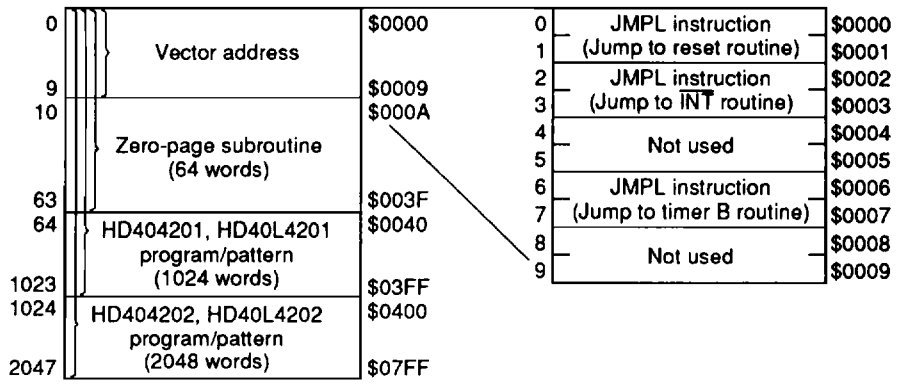
**Special Function Registers Area ($003 to $00C):** The special function registers are the mode or data registers for external interrupt, the serial interface, the timer/counters, comparator and are also used as data control registers for I/O ports. These registers are classified into three types: write-only, read-only, and read/write, as shown in figure 2. These registers cannot be accessed by RAM bit manipulation instructions (except for CMR register).

Note that if the unusable locations are set, the MCU may mulfunction (only applicable for HD404202 Series $003, $005 to $008 and $00C).

**Data Area ($020 to $03F: HD404202 Series; $020 to $07F: HD404222 Series):** The 16 digits of $020 through $02F are called memory registers (MR) and are also accessible by the LAMR and XMRA instructions (figure 4).

**Stack Area ($0E0 to $0FF):** Locations $0E0 through $0FF are reserved for LIFO stacks to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when a subroutine call (CAL or CALL instruction) or interrupt is performed. This area can be used as an 8-level nesting stack in which one level requires 4 digits. Figure 4 shows the stack area levels. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. When this area is not used as a stack, it becomes available as a data area.

**HD404201, HD40L4201, HD404202, HD40L4202**




**HD404222, HD40L4222, HD4074224**

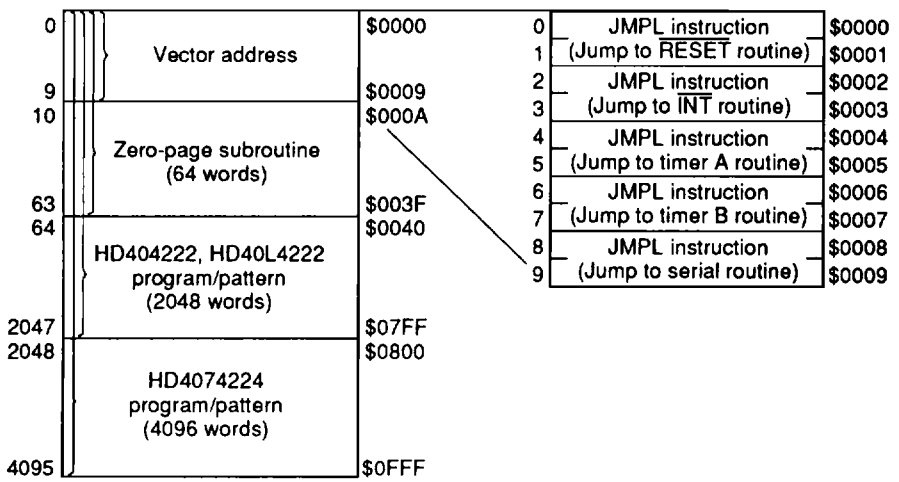



**Figure 1 ROM Memory Map**

**HD404201, HD40L4201, HD404202, HD40L4202**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | RAM mapped registers (32 digits) | $000 | 0 | Interrupt control bits | | $000 |
| | | | 2 | | | $002 |
| 31 | | $01F | 3 | Not used | | $003 |
| 32 | Memory registers (MR) (16 digits) | $020 | 4 | Port mode register (PMR) | W | $004 |
| 47 | | $02F | 5 | Not used | | $005 |
| 48 | Data (16 digits) | $030 | | | | |
| 63 | | $03F | | | | |
| 64 | Not used (160 digits) | $040 | 8 | | | $008 |
| | | | 9 | Timer mode register B (TMB) | W | $009 |
| | | | 10 | Timer B* (TCBL)/(TLRL) | R/W | $00A |
| | | | 11 | Timer B* (TCBU)/(TLRU) | R/W | $00B |
| | | | 12 | Not used | | $00C |
| 223 | | $0DF | | | | |
| 224 | Stack (32 digits) | $0E0 | | | | |
| 255 | | $0FF | 31 | | | $01F |

**HD404222, HD40L4222, HD4074224**

| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | RAM mapped registers (32 digits) | $000 | 0 | Interrupt control bits | | $000 |
| | | | 2 | | | $002 |
| 31 | | $01F | 3 | Comparator mode register (CMR) | R/W | $003 |
| 32 | Memory registers (MR) (16 digits) | $020 | 4 | Port mode register (PMR) | W | $004 |
| 47 | | $02F | 5 | Serial mode register (SMR) | W | $005 |
| 48 | Data (80 digits) | $030 | 6 | Serial data register lower (SRL) | R/W | $006 |
| | | | 7 | Serial data register upper (SRU) | R/W | $007 |
| | | | 8 | Timer mode register A (TMA) | W | $008 |
| 127 | | $07F | 9 | Timer mode register B (TMB) | W | $009 |
| 128 | Not used (96 digits) | $080 | 10 | Timer B* (TCBL)/(TLRL) | R/W | $00A |
| | | | 11 | Timer B* (TCBU)/(TLRU) | R/W | $00B |
| | | | 12 | Reference voltage select register (RSR) | R/W | $00C |
| 223 | | $0DF | | | | |
| 224 | Stack (32 digits) | $0E0 | | Not used | | |
| 255 | | $0FF | 31 | | | $01F |

Note: The status flag becomes invalid when CMR bits are tested by the TM or TMD instructions (only applicable for HD404222 Series).

R: Read only
W: Write only
R/W: Read/Write

| | | | | | | |
|---|---|---|---|---|---|---|
| 10 | Timer/event counter B lower (TCBL) | R | Timer load register B lower (TLRL) | W | $00A |
| 11 | Timer/event counter B upper (TCBU) | R | Timer load register B upper (TLRU) | W | $00B |

* Two registers are mapped on the same address.

**Figure 2 RAM Memory Map**

| | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---|---|---|---|---|---|
| 0 | IM of external $\overline{INT}$ (IMEX) | IF of external $\overline{INT}$ (IFEX) | Reset SP bit (RSP) | Interrupt enable flag (IE) | $000 |
| 1 | IM of timer B (IMTB) | IF of timer B (IFTB) | IM of timer A * (IMTA) | IF of timer A * (IFTA) | $001 |
| 2 | Not used | Not used | IM of serial * (IMS) | IF of serial * (IFS) | $002 |

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Each bit in the interrupt control bits area is set by the SEM/SEMD instruction, reset by the REM/REMD instruction, and tested by the TM/TMD instruction. It is not affected by other instructions. Furthermore, the interrupt request flag is not affected by the SEM/SEMD instruction.
The status flag becomes invalid when the unused bits and RSP bit are tested by the TM or TMD instruction.
* Only applicable for the HD404222 Series.

**Figure 3 Configuration of Interrupt Control Bits Area**

Memory registers

| | | |
|---|---|---|
| 32 | MR (0) | $020 |
| 33 | MR (1) | $021 |
| 34 | MR (2) | $022 |
| 35 | MR (3) | $023 |
| 36 | MR (4) | $024 |
| 37 | MR (5) | $025 |
| 38 | MR (6) | $026 |
| 39 | MR (7) | $027 |
| 40 | MR (8) | $028 |
| 41 | MR (9) | $029 |
| 42 | MR (10) | $02A |
| 43 | MR (11) | $02B |
| 44 | MR (12) | $02C |
| 45 | MR (13) | $02D |
| 46 | MR (14) | $02E |
| 47 | MR (15) | $02F |

Stack area

| | | |
|---|---|---|
| 224 | Level 8 | $0E0 |
| | Level 7 | |
| | Level 6 | |
| | Level 5 | |
| | Level 4 | |
| | Level 3 | |
| | Level 2 | |
| 255 | Level 1 | $0FF |

| | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---|---|---|---|---|---|
| 252 | ST | $\overline{PC_{13}}$ | $\overline{PC_{12}}$ | $\overline{PC_{11}}$ | $0FC |
| 253 | $\overline{PC_{10}}$ | $\overline{PC_9}$ | $\overline{PC_8}$ | $\overline{PC_7}$ | $0FD |
| 254 | CA | $\overline{PC_6}$ | $\overline{PC_5}$ | $\overline{PC_4}$ | $0FE |
| 255 | $\overline{PC_3}$ | $\overline{PC_2}$ | $\overline{PC_1}$ | $\overline{PC_0}$ | $0FF |

$\overline{PC_{11}}$ – $\overline{PC_0}$: Program counter
ST: Status flag
CA: Carry flag

Note: According to on-chip ROM capacity, following area are ignored.
HD404201, HD40L4201: $\overline{PC_{13}}$ – $\overline{PC_{10}}$
HD404202, HD40L4202, HD404222, HD40L4222: $\overline{PC_{13}}$ – $\overline{PC_{11}}$
HD4074224: $\overline{PC_{13}}$, $\overline{PC_{12}}$

**Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position**

## Functional Description

### Registers and Flags

The MCU has eight registers and two flags for CPU operations (figure 5).

**Accumulator (A), B Register (B):** The 4-bit accumulator and B register hold the results of the arithmetic logic unit (ALU), and transfer data to/from memory, I/O, and other registers.

**X Register (X), Y Register (Y):** The X and Y registers are 4-bit registers used for indirect addressing of RAM. The Y register is also used for D port addressing.

**SPX Register (SPX), SPY Register (SPY):** The 4-bit registers SPX and SPY are used to assist the X and Y registers, respectively.

**Carry Flag (CA):** The carry flag stores the overflow from the ALU generated by an arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions.

During an interrupt, the carry flag is pushed onto the stack and is pulled from the stack only by the RTNI instruction.

**Status Flag (ST):** The status flag holds the ALU overflow, ALU non-zero, and the results of a bit test instruction for arithmetic or compare instructions. The status flag is also used as a branch condition for the BR, BRL, CAL, and CALL instructions. The value of the status flag remains

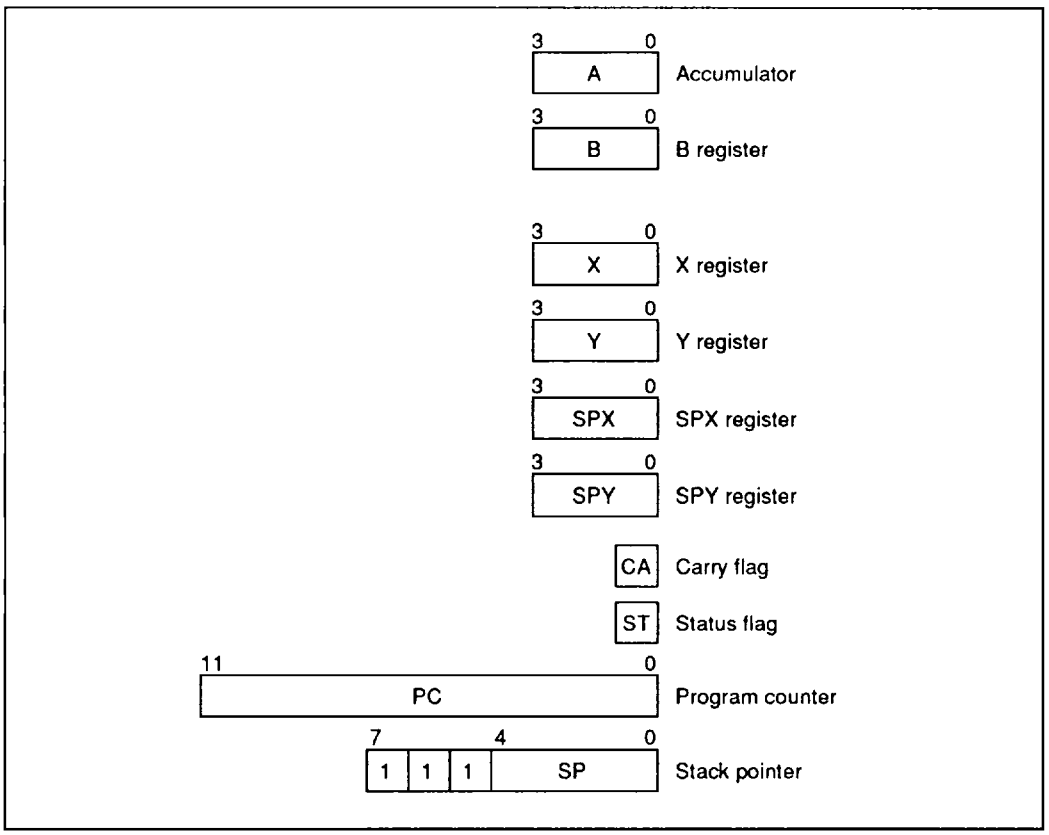



**Figure 5 Registers and Flags**

unchanged until the next arithmetic, compare, or bit test instruction is executed. The status flag becomes a 1 after the BR, BRL, CAL, or CALL instruction was either executed or not. During an interrupt, the status flag is pushed onto the stack and can be pulled from the stack only by the RTNI instruction.

**Program Counter (PC):** The program counter is a 12-bit binary counter which controls the sequence in which the instructions stored in ROM are executed.

**Stack Pointer (SP):** The stack pointer (SP) is used to point to the address of the next stack area (up to 8 levels).

The stack pointer is initialized to RAM address $FF. It is decremented by 4 when data is pushed onto the stack, and incremented by 4 when data is pulled from it. The stack can only be used up to 8 levels deep because the upper 3 bits of the stack pointer are fixed at 111.

**Table 1 Initial Values After MCU Reset**

| Item | | Initial Value by MCU Reset ($\overline{RESET}$ = 0) | Contents |
|---|---|---|---|
| Program counter (PC) | | $0000 | Execute program from the top of ROM address |
| Status flag (ST) | | 1 | Enable branching with conditional branch instructions |
| Stack pointer (SP) | | $0FF | Stack level is 0 |
| I/O pins, output registers | Without pull-up MOS | 1 | Enable input |
| | With pull-up MOS | 1 | Enable input |
| | CMOS | 1 | — |
| Interrupt flags and mask | Interrupt enable flag (IE) | 0 | Inhibit all interrupts |
| | Interrupt request flag (IF) | 0 | No interrupt request |
| | Interrupt mask (IM) | 1 | Mask interrupt request |
| Mode registers | Port mode register (PMR) | 000 | See Port Mode Register section |
| | Serial mode register (SMR)* | 0000 | See Serial Mode Register section |
| | Timer mode register A (TMA)* | 0000 | See Timer Mode Register A section |
| | Timer mode register B (TMB) | 0000 | See Timer Mode Register B section |
| | Comparator mode register (CMR)* | 00 | See Comparator Mode Register section |
| Comparator | Reference voltage select register (RSR)* | 0000 | See Reference Voltage Select Register section |
| Timer/counters, serial interface | Prescaler | $000 | — |
| | Timer counter A (TCA)* | $00 | — |
| | Timer counter B (TCB) | $00 | — |
| | Timer load register B (TLR) | $00 | — |
| | Octal counter* | 000 | — |

* Only applicable for the HD404222 Series.

The stack pointer is initialized to $FF by either MCU reset or RSP bit reset by the REM/REMD instruction.

**Reset**

The MCU is reset by pulling the $\overline{\text{RESET}}$ pin low. At power-on or when cancelling the stop mode, the reset period must satisfy $t_{RC}$ for the oscillator to stabilize. In other cases, at least two instruction cycles are required for the MCU to be reset.

Table 1 shows the components initialized by the MCU reset, and the status of each component.

Table 2 shows how registers recover from the stop mode.

Take note that the reset signal is not acknowledged immediately at power-on by the MCU but at the time the oscillator has stabilized, so during this period the statuses within the MCU and at the I/O pins are not defined.

**Table 2 Initial Values After MCU Reset**

| Item | | After MCU Reset to Recover from Stop Mode | After MCU Reset to Recover from Other Modes |
|---|---|---|---|
| Carry flag | (CA) | The contents of the items before MCU reset are not retained and must be initialized by software. | The contents of the items before MCU reset are not retained and must be initialized by software. |
| Accumulator | (A) | | |
| B register | (B) | | |
| X/SPX registers | (X/SPX) | | |
| Y/SPY registers | (Y/SPY) | | |
| Serial data register | (SR)* | | |
| RAM | | The contents of RAM before MCU reset (just before the STOP instruction) are retained. | The contents of RAM before MCU reset are not retained and must be initialized by software. |

* Only applicable for the HD404222 Series.

## Interrupts

Two interrupt sources are available on the MCU of HD404202 Series. They are an external request ($\overline{INT}$) and timer/counter (timer B). HD404222 Series has four interrupt sources: the two sources stated above, timer A and serial interface. For each source, an interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. An interrupt enable flag (IE) is also used to control interrupt operations.

**Interrupt Control Bits and Interrupt Operation:** The interrupt control bits are mapped on $000 through $002 of the RAM. These bits are accessible by RAM bit manipulation instructions. The interrupt request flag (IF) cannot be set by software. At MCU reset initialization, the IE and IF are cleared to 0, and IM is set to 1.

Figure 6 is a block diagram of the interrupt control circuit. Table 3 shows the interrupt priority and vector addresses, and table 4 shows the interrupt conditions corresponding to each interrupt source.

An interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 during this period, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. Also in the second cycle and third cycle, the carry flag, status flag, and program counter are pushed onto the stack. Included in the third cycle is the generation of the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.

**Table 3 Vector Addresses and Interrupt Priority**

**HD404202 Series**

| Reset/Interrupts | Priority | Vector Addresses |
|---|---|---|
| $\overline{RESET}$ | — | $000 |
| $\overline{INT}$ | 1 | $002 |
| Timer B | 2 | $006 |

**HD404222 Series**

| Reset/Interrupts | Priority | Vector Addresses |
|---|---|---|
| $\overline{RESET}$ | — | $000 |
| $\overline{INT}$ | 1 | $002 |
| Timer A | 2 | $004 |
| Timer B | 3 | $006 |
| Serial | 4 | $008 |

**Table 4 Interrupt Conditions**

**HD404202 Series**

| Interrupt Control Bits | $\overline{INT}$ | Timer B |
|---|---|---|
| IE | 1 | 1 |
| IFEX · $\overline{IMEX}$ | 1 | 0 |
| IFTB · $\overline{IMTB}$ | * | 1 |

* indicates don't care

**HD404222 Series**

| Interrupt Control Bits | $\overline{INT}$ | Timer A | Timer B | Serial |
|---|---|---|---|---|
| IE | 1 | 1 | 1 | 1 |
| IFEX · $\overline{IMEX}$ | 1 | 0 | 0 | 0 |
| IFTA · $\overline{IMTA}$ | * | 1 | 0 | 0 |
| IFTB · $\overline{IMTB}$ | * | * | 1 | 0 |
| IFS · $\overline{IMS}$ | * | * | * | 1 |

* indicates don't care

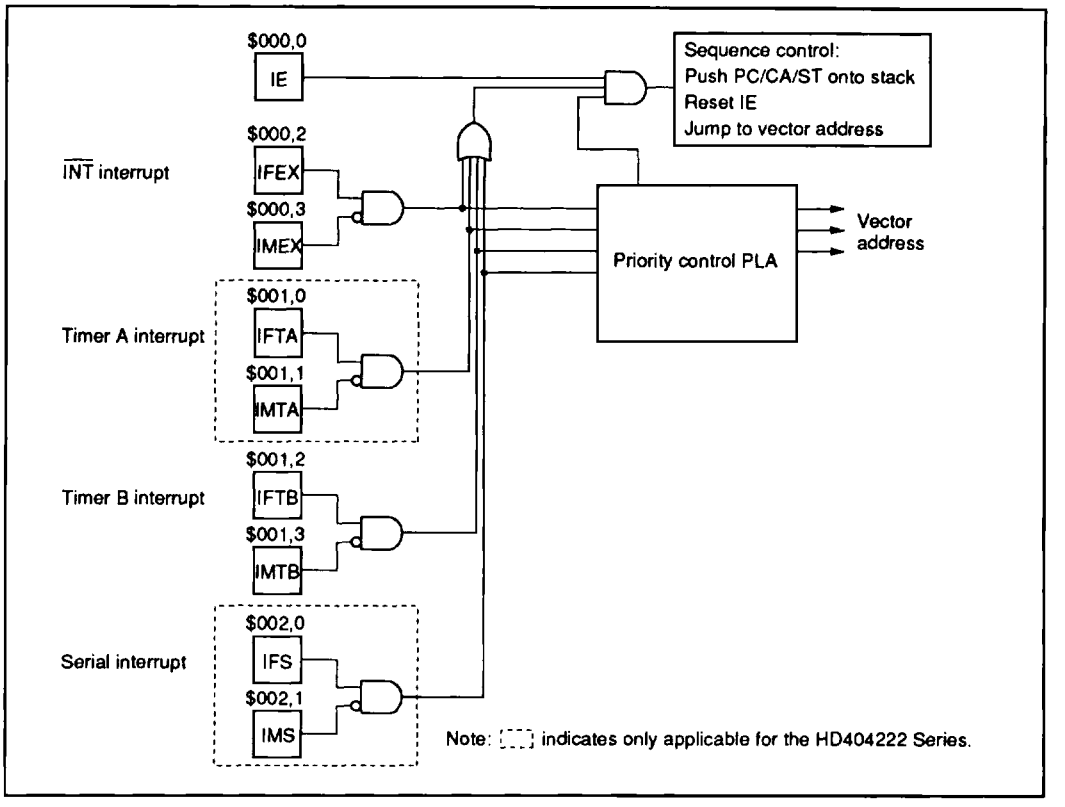



**Figure 6 Interrupt Control Circuit Block Diagram**

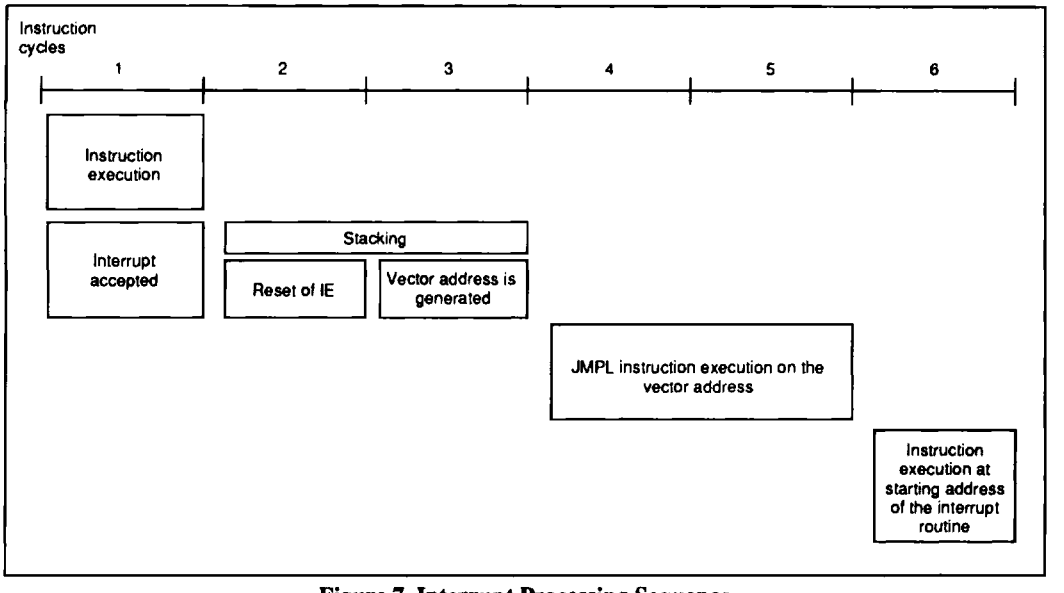



**Figure 7 Interrupt Processing Sequence**

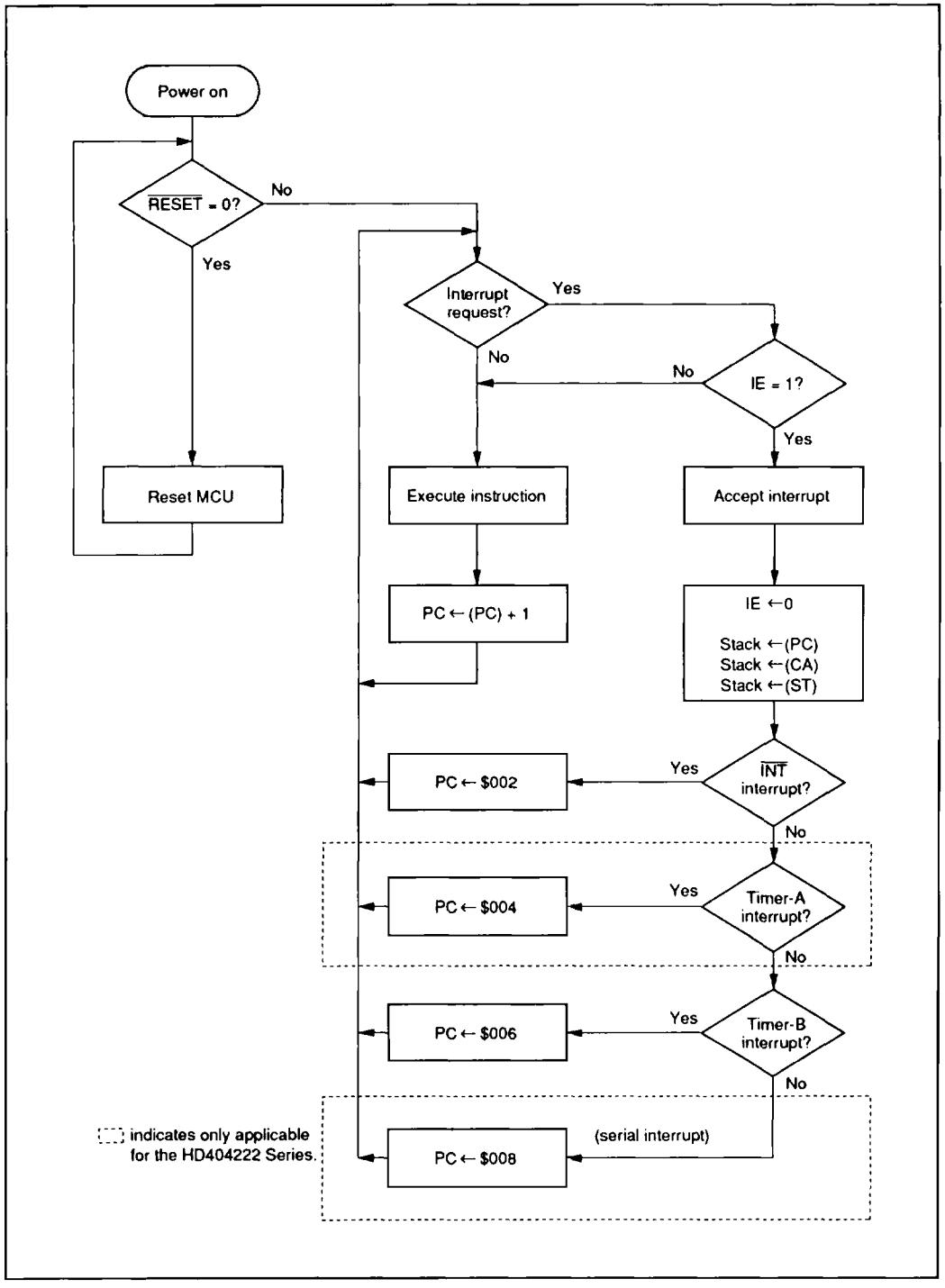



**Figure 8 Interrupt Processing Flowchart**

**Interrupt Enable Flag (IE: $000, Bit 0):** The interrupt enable flag (table 5) enables or disables interrupt requests. It is reset by an interrupt and set by the RTNI instruction.

**External Interrupt ($\overline{INT}$):** The external interrupt request input ($\overline{INT}$) can be selected by the port mode register (PMR: $004). Setting bit 2 of PMR causes the $D_5/\overline{INT}$ pin to be used as $\overline{INT}$.

The external interrupt request flag IFEX (table 6) is set at the falling edge of $\overline{INT}$ input.

The $\overline{INT}$ input can be used as a clock signal input to timer B, which counts up at each falling edge of the $\overline{INT}$ input. When using $\overline{INT}$ as the timer B external event input, the external interrupt mask IMEX (table 7) has to be set so that the $\overline{INT}$ interrupt request will not be accepted.

**External Interrupt Request Flag (IFEX: $000, Bit 2):** The external interrupt request flag is set the falling edge of the $\overline{INT}$ input.

**External Interrupt Mask (IMEX: $000, Bit 3):** The external interrupt mask (table 7) masks the external interrupt request.

**Timer A Interrupt Request Flag (IFTA: $001, Bit 0):** The timer A interrupt request flag (table 8) is set by the timer A overflow output. It can be only used by the HD404222 Series.

**Timer A Interrupt Mask (IMTA: $001, Bit 1):** The timer A interrupt mask (table 9) prevents an interrupt request from being generated by the timer A interrupt request flag. It can be only used by the HD404222 Series.

**Table 5 Interrupt Enable Flag**

| IE | Interrupt Enabled/Disabled |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

**Table 6 External Interrupt Request Flag**

| IFEX | Interrupt Request |
|---|---|
| 0 | No |
| 1 | Yes |

**Table 7 External Interrupt Mask**

| IMEX | Interrupt Request |
|---|---|
| 0 | Enabled |
| 1 | Disabled (masked) |

**Table 8 Timer A Interrupt Request Flag**

| IFTA | Interrupt Request |
|---|---|
| 0 | No |
| 1 | Yes |

**Table 9 Timer A Interrupt Mask**

| IMTA | Interrupt Request |
|---|---|
| 0 | Enabled |
| 1 | Disabled (masked) |

**Timer B Interrupt Request Flag (IFTB: $001, Bit 2):** The timer B interrupt request flag (table 10) is set by the overflow output of timer B.

**Timer B Interrupt Mask (IMTB: $001, Bit 3):** The timer B interrupt mask (table 11) prevents an interrupt request from being generated by the timer B interrupt request flag.

**Serial Interrupt Request Flag (IFS: $002, Bit 0):** The serial interrupt request flag (table 12) will be set when the octal counter counts eight transmit clock signals, or when data transfer is discontinued by resetting the octal counter. It can be only used by the HD404222 Series.

**Serial Interrupt Mask (IMS: $002, Bit 1):** The serial interrupt mask (table 13) masks the interrupt request. It can be only used by the HD404222 Series.

**Port Mode Register (PMR: $004):** The 3-bit write-only port mode register controls the $D_5/\overline{INT}$, $D_7$/SI, and $D_8$/SO pins as shown in table 14. The port mode register is initialized to $0 by MCU reset. Therefore these pins are initially used as ports. Note that if unusable bit 3 is set, the MCU may malfunction.

**Table 10 Timer B Interrupt Request Flag**

| IFTB | Interrupt Request |
|---|---|
| 0 | No |
| 1 | Yes |

**Table 11 Timer B Interrupt Mask**

| IMTB | Interrupt Request |
|---|---|
| 0 | Enabled |
| 1 | Disabled (masked) |

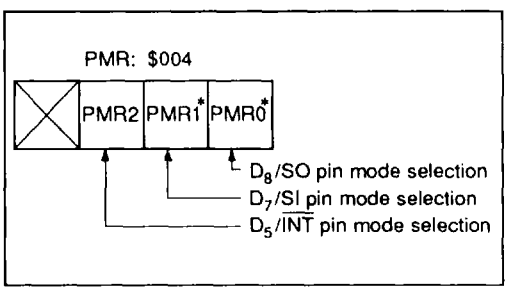
**Table 12 Serial Interrupt Request Flag**

| IFS | Interrupt Request |
|---|---|
| 0 | No |
| 1 | Yes |

**Table 13 Serial Interrupt Mask**

| IMS | Interrupt Request |
|---|---|
| 0 | Enabled |
| 1 | Disabled (masked) |

**Table 14 Port Mode Register**




| PMR2 | $D_5/\overline{INT}$ Pin |
|---|---|
| 0 | Used as $D_5$ port input/output pin |
| 1 | Used as $\overline{INT}$ input pin |

| PMR1* | $D_7$/SI Pin |
|---|---|
| 0 | Used as $D_7$ port input/output pin |
| 1 | Used as SI input pin |

| PMR0* | $D_8$/SO Pin |
|---|---|
| 0 | Used as $D_8$ port input/output pin |
| 1 | Used as SO output pin |

* PMR0 and PMR1 can be only used by the HD404222 Series.

## Operating Modes

The MCU has two low-power dissipation modes, standby mode and stop mode (table 15). Figure 9 shows a mode transition diagram of these modes.

**Standby Mode:** Executing the SBY instruction places the MCU into standby mode. In standby mode, the oscillator circuit, interrupts, timer/counters, and serial interface remain active. On the other hand, the CPU stops since the clock related to the instruction execution stops. Registers, RAM, and I/O pins retain the states they were in just before the MCU went into standby mode.

**Table 15 Low-Power Dissipation Mode Function**

| Low-Power Dissipation Mode | Instruction | Oscillator Circuit | Instruction Execution | Registers, Flags | Interrupt Function |
|---|---|---|---|---|---|
| Standby mode | SBY instruction | Active | Stop | Retained | Active |
| Stop mode | STOP instruction | Stop | Stop | Reset*1 | Stop |

**Table 15 Low-Power Dissipation Mode Function (cont)**

| Low-Power Dissipation Mode | RAM | Input/ Output Pins | Timer/ Counters, Serial Interface*3 | Comparator*3 | Cancellation Method |
|---|---|---|---|---|---|
| Standby mode | Retained | Retained*2 | Active | Stop | $\overline{\text{RESET}}$ input, interrupt request |
| Stop mode | Retained | High impedance | Stop | Stop | $\overline{\text{RESET}}$ input |

Notes: *1. The MCU recovers from stop mode by $\overline{\text{RESET}}$ input. Refer to table 1 for the contents of the flags and registers.
*2. If an I/O circuit is active, an I/O current may flow, depending on the state of the I/O pin in standby mode. This current is in addition to the current dissipation in standby mode.
*3. Serial interface and comparator can be only used by the HD404222 Series.

The Standby mode may be cancelled by enabling $\overline{\text{RESET}}$ or by asserting an interrupt request. In the former case, the MCU is reset. In the latter case, the MCU becomes active and executes the next instruction following the SBY instruction. After this instruction is completed and if the interrupt enable flag is 1 when an interrupt request asserted, the interrupt is executed, while if it is 0, the interrupt request is put on hold and normal instruction execution continues.

Figure 10 shows the flowchart of the standby mode.

**Stop Mode:** Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and all functions of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 11, the $\overline{\text{RESET}}$ input must be applied for at least $t_{RC}$ for the oscillation to stabilize. (Refer to the AC Characteristics table.) After stop mode is cancelled, the RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, X/SPX and Y/SPY registers, carry flag, and serial data register will not retain their contents. (The serial data resister can be only used by the HD404222 Series.)

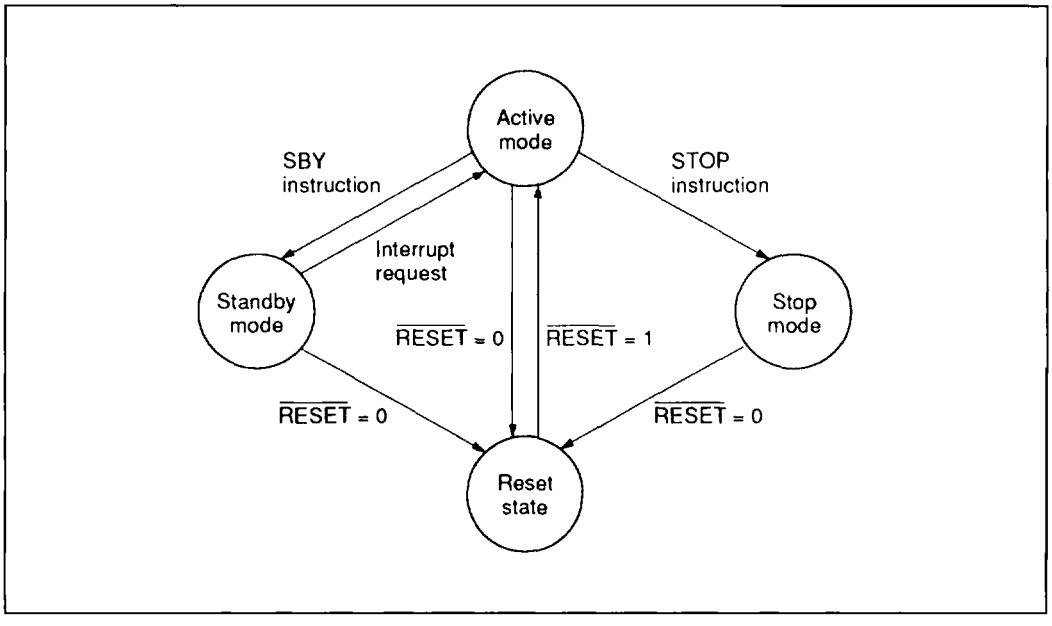



**Figure 9 MCU Operation Mode Transition**

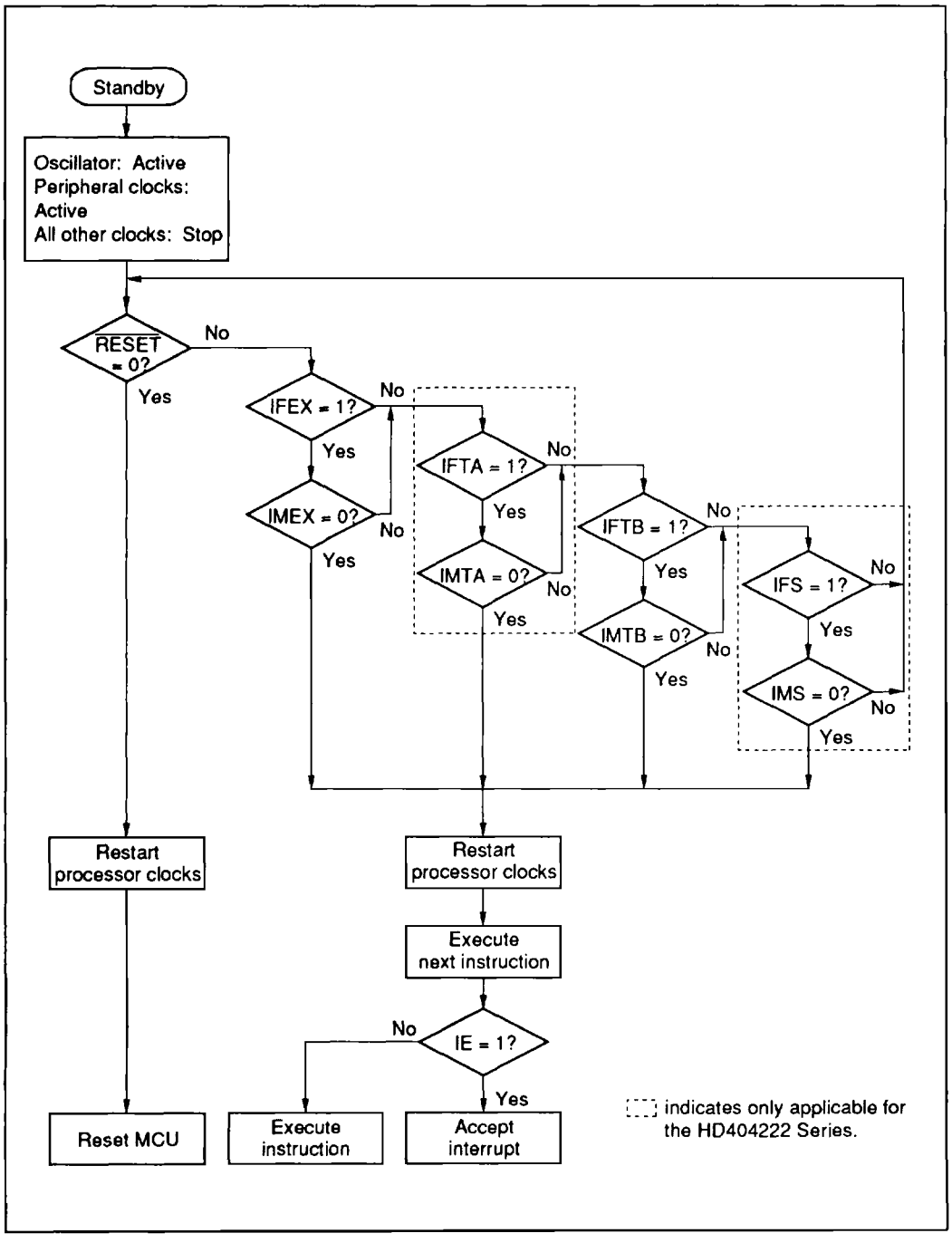



**Figure 10 MCU Operating Flowchart in Standby Mode**

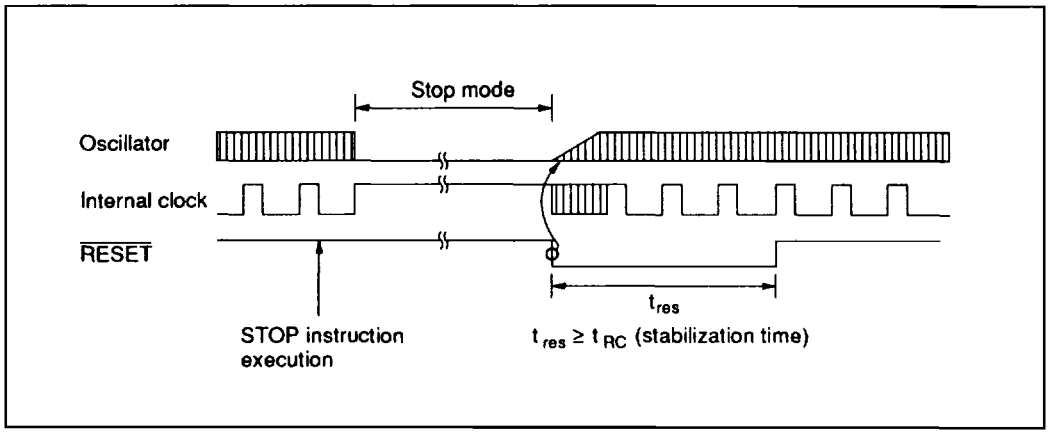



**Figure 11 Timing of Stop Mode Cancellation**

## Internal Oscillator Circuit

Figure 12 shows a block diagram of the internal oscillator circuit. Through mask options, either a ceramic oscillator or resistor can be selected as the oscillator type and connected to $OSC_1$ and $OSC_2$. See figure 13 for the layout of the ceramic oscillator. For other cases, an external clock operation is available.

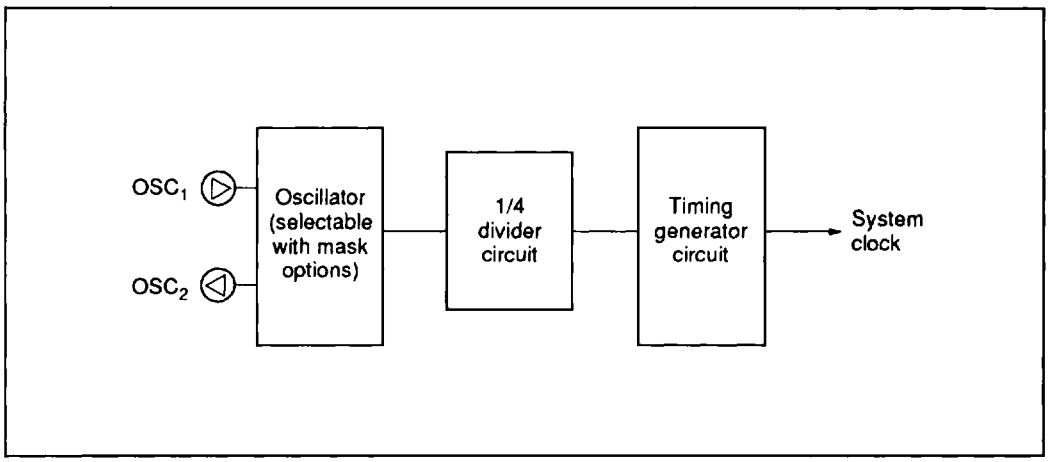



**Figure 12 Internal Oscillator Circuit**

**Table 16 Examples of Oscillator Circuits**

| | Circuit Configuration | Circuit Constants |
|---|---|---|
| External clock operation | Oscillator — $OSC_1$; Open — $OSC_2$ | |
| Ceramic oscillator | $C_1$, $R_f$, $C_2$, $R_f$; $OSC_1$, $OSC_2$ | Ceramic oscillator: CSA4.00MG (MURATA)<br>$C_1 = C_2$: 30 pF ±20%<br>$R_f$: 1 MΩ ±20%<br>Ceramic oscillator: CSB1000J (MURATA)<br>$C_1 = C_2$: 220 pF ±20%<br>$R_f$: 1 MΩ ±20% |
| Resistor | $R_f$; $OSC_1$, $OSC_2$ | $R_f$: 20 kΩ ±1% |

Notes: The circuit parameters listed above are dependent on the ceramic oscillator and the floating capacitance when designing the board. In employing the resonator, consult with the ceramic oscillator manufacturer to determine the circuit parameters.

The wiring between $OSC_1$, $OSC_2$, and the elements should be as short as possible without crossing over other wires. Refer to the layout of the ceramic oscillator in figure 13.

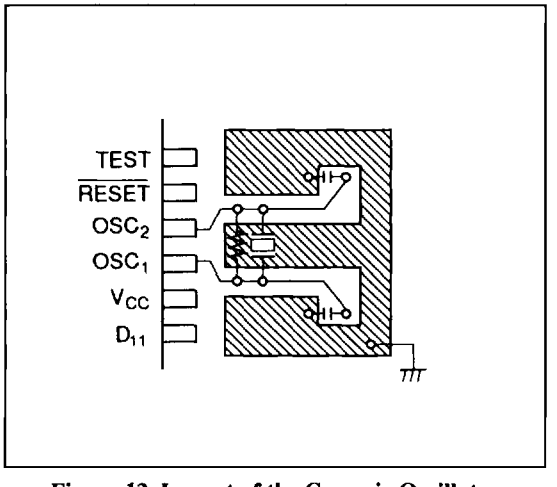



**Figure 13 Layout of the Ceramic Oscillator**

## Input/Output

The MCU has 22 standard I/O pins. As for the mask ROM version of HD404201, HD40L4201, HD404202, HD40L4202, HD404222 and HD40L4222, one of three circuit types can be selected by the mask option for each standard pin: with pull-up MOS or without pull-up MOS (NMOS open drain) or CMOS.

The I/O pins for the HD4074224 are fixed as with pull-up MOS.

When every input/output pin is used as an input pin, the mask option and output data must be selected as specified in table 17.

**Output Circuit Operation of with Pull-Up MOS Standard Pins:** In the standard pin option with pull-up MOS, the circuit shown in figure 14 is used to shorten the rise time of output.

When the MCU executes an output instruction, it generates a write pulse to the R port addressed by this instruction. This pulse will switch the PMOS (B) on (in figure 14) and shorten the rise time. The write pulse keeps PMOS on for two-eighths of the instruction cycle time. While the write pulse is 0, a high output level is maintained by the pull-up MOS (C).

When the $\overline{HLT}$ signal becomes 0 in stop mode, MOSs (A), (B), and (C) turn off. When the $\overline{HLT}$ signal is 1, the pins' states are maintained.

**D Port:** The D port has 14 discrete I/O pins, each of which can be addressed independently. The D port can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions.

For the HD404222 Series pins $D_5$ to $D_{11}$ are multiplexed with pins $\overline{INT}$, $\overline{SCK}$, SI, SO, $V_{ref}$, $COMP_0$, and $COMP_1$, respectively. Setting, resetting, or testing non-existing ports results in invalid data. As for the HD404202 Series only pin $D_5/\overline{INT}$ applies.

**R Ports:** The R ports are I/O pins that are accessed in 4-bit units. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. Writing into non-existing ports will not affect the MCU, however, the values read from the non-existing ports cannot be guaranteed.

**Unused I/O Pins:** If unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

- Select the option of without pull-up MOS for unused I/O pins and connect them to GND of the printed circuit board.
- For the HD404222 Series sets $D_5/\overline{INT}$, $D_6/\overline{SCK}$, $D_7$/SI, $D_8$/SO, $D_9/V_{ref}$, $D_{10}/COMP_0$, and $D_{11}/COMP_1$ as $D_5$ to $D_{11}$, respectively, by software. As for the HD404202 Series only pin $D_5/\overline{INT}$ applies.

**Table 17 Data Input from Common Input/Output Pins**

| I/O Pin Circuit Type | | Input Possible | Input Pin State |
|---|---|---|---|
| Standard pins | CMOS | No | — |
| | Without pull-up MOS (NMOS open drain) | Yes | 1 |
| | With pull-up MOS | Yes | 1 |

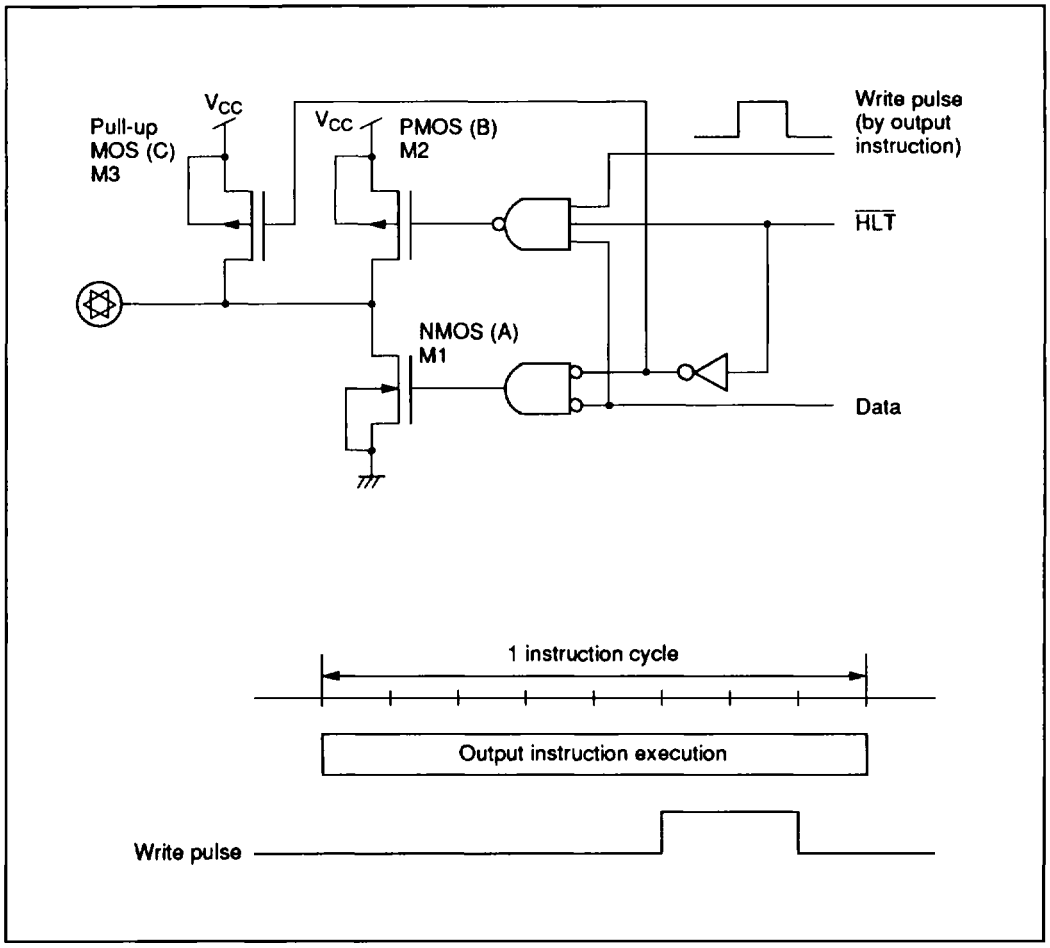
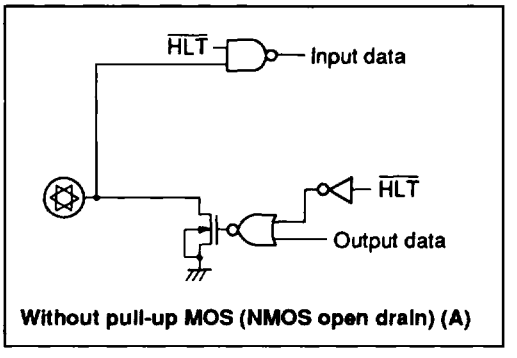



**Figure 14 Output Circuit Operation of Standard Pins with Pull-Up MOS Option**

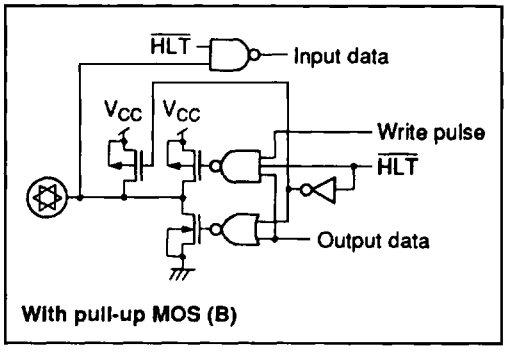
**Table 18 I/O Pin Circuit Types**

**Standard Pins**

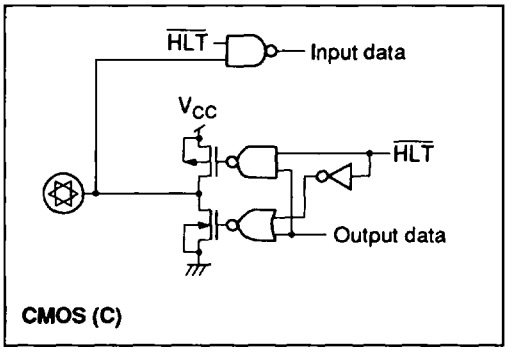
**I/O common pins ($D_0$–$D_{13}$, $R1_0$–$R1_3$, $R2_0$–$R2_3$)**




**Without pull-up MOS (NMOS open drain) (A)**

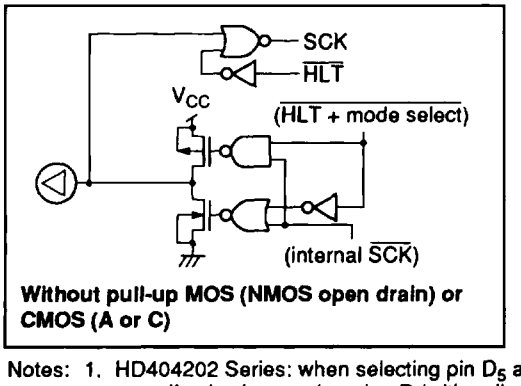



**With pull-up MOS (B)**

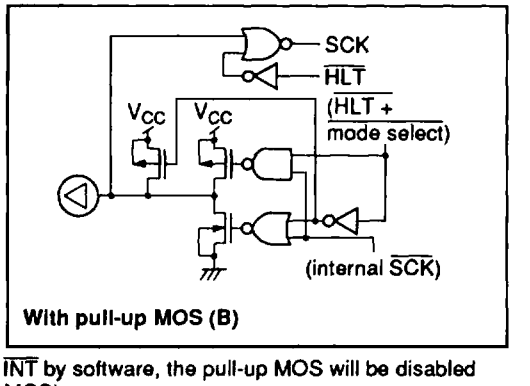



**CMOS (C)**

**I/O common pins ($\overline{SCK}$ (output mode))***




**Without pull-up MOS (NMOS open drain) or CMOS (A or C)**




**With pull-up MOS (B)**

Notes: 1. HD404202 Series: when selecting pin $D_5$ as $\overline{INT}$ by software, the pull-up MOS will be disabled even if selecting mask option B (with pull-up MOS).

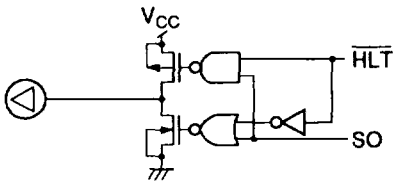
2. HD404222 and HD40L4222: when selecting pins $D_5$, $D_6$, and $D_7$ as $\overline{INT}$, $\overline{SCK}$, and SI input, respectively, by software, the pull-up MOS of each terminal will be disabled even if selecting mask option B (with pull-up MOS).
HD4074224: pins $D_5$, $D_6$, and $D_7$ are fixed as with pull-up MOS (B). But when selecting these pins as $\overline{INT}$, $\overline{SCK}$, and SI input, respectively, by software, the pull-up MOS of each terminal will be disabled

* Only applicable for the HD404222 Series.

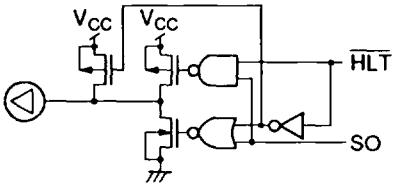
**Table 18 I/O Pin Circuit Types (cont)**

**Standard Pins**

**Output pins (SO)***

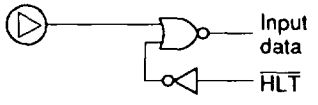



**Without pull-up MOS (NMOS open drain) or CMOS (A or C)**

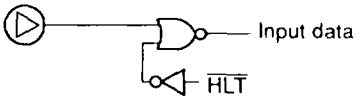



**With pull-up MOS (B)**

**Input pins (INT, SI*, SCK* (Input mode))**

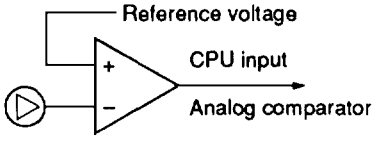



**Without pull-up MOS (NMOS open drain) or CMOS (A or C)**



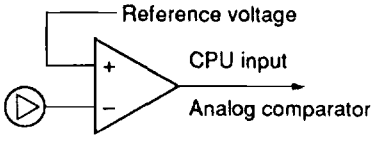

**With pull-up MOS (B)**

**Input pins ($COMP_0$*, $COMP_1$*)**




**Without pull-up MOS (NMOS open drain) or CMOS (A or C)**

**Input pins ($COMP_0$*, $COMP_1$*)**




**With pull-up MOS (B)**

Notes: 1. HD404202 Series: when selecting pin $D_5$ as $\overline{INT}$ by software, the pull-up MOS will be disabled even if selecting mask option B (with pull-up MOS).

2. HD404222 and HD40L4222: when selecting pins $D_5$, $D_6$, and $D_7$ as $\overline{INT}$, $\overline{SCK}$, and SI input, respectively, by software, the pull-up MOS of each terminal will be disabled even if selecting mask option B (with pull-up MOS).
HD4074224: pins $D_5$, $D_6$, and $D_7$ are fixed as with pull-up MOS (B). But when selecting these pins as $\overline{INT}$, $\overline{SCK}$, and SI input, respectively, by software, the pull-up MOS of each terminal will be disabled

* Only applicable for the HD404222 Series.

## Timers

The MCU of HD404202 Series contains a prescaler and a timer/counter (timer B), where as one prescaler and two timer/counters (timers A and B) are available on the MCU of HD404222 Series. Figure 15 shows the block diagram of timer/counters. The prescaler is an 11-bit counter, timer A is an 8-bit free-running/watchdog timer, and timer B is an 8-bit auto-reload timer/event counter.

**Prescaler:** The system clock signal is input to the prescaler. At MCU reset, the prescaler is initialized to $000 and starts dividing the system clock frequency.

The prescaler keeps counting up except at MCU reset and stop mode. The prescaler provides clock signals to timer A, timer B, and the serial interface (Timer A and the serial interface can be only used by the HD404222 Series). The prescaler divide ratio is selected by timer mode register A (TMA), timer mode register B (TMB), and serial mode register (SMR) (TMA and SMR can be only used by the HD404222 Series).

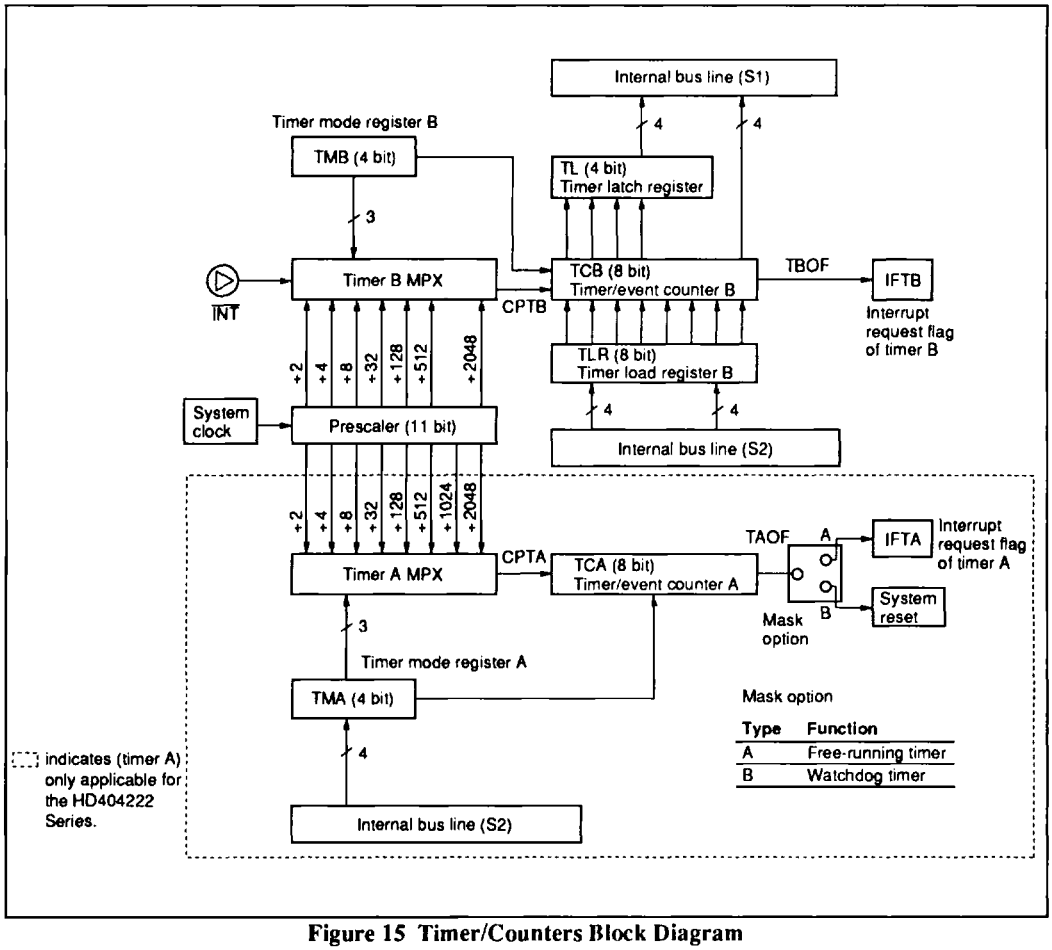



**Figure 15 Timer/Counters Block Diagram**

**Timer A Operation (Only Applicable for the HD404222 Series):** Timer A's function is selected via the mask option.

When timer A is used as a free-running timer, it counts up every input clock signal after timer A has been initialized to $00 by MCU reset. When the next clock signal is input after timer A counts up to $FF, timer A is set to $00 again, and generates an overflow output. This sets the timer A interrupt request flag (IFTA: $001, bit 0) to 1. Therefore, this timer can function as an interval timer periodically generating overflow output at every 256th clock signal. The clock signals input to timer A are selected by timer mode register A (TMA: $008).

Note that when timer A is used as a free-running timer, if setting bit 3 of timer mode resister A may cause the MCU to malfunction.

When timer A is used as a watchdog timer, the input clock is specified as 1/2048 output divided by the prescaler. The watchdog timer is initialized to $00 at MCU reset, then counts up every input clock signal. If a clock signal is applied after the timer becomes $FF, an overflow is generated and the MCU is reset.
After reset, the MCU re-executes the program from the beginning. The program must set bit 3 of timer mode register A to reset timer counter A.

**Timer B Operation:** Timer mode register B (TMB: $009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When the external event input is used as an input clock signal to timer B, select $D_5/\overline{INT}$ as $\overline{INT}$ and set the external interrupt mask (IMEX) to prevent an external interrupt request from occurring.

Timer B is initialized by software according to the data written in timer load register B. Timer B counts up at every input clock signal. When the next clock signal is input after timer B is set to $FF, timer B will generate an overflow output. Then, if the auto-reload function is selected, timer B is initialized to the value of timer load register B. If it is not selected, timer B goes back to $00. The timer B interrupt request flag (IFTB: $001, bit 2) will hold the overflow output.

**Timer Mode Register A (TMA: $008):** Four-bit write-only timer mode register A selects the timer function for timer A and the prescaler divide ratio of timer A's clock input as shown in table 19. Timer mode register A is initialized to $0 by MCU reset.

**Table 19 Timer Mode Register A**

| TMA2 | TMA1 | TMA0 | Prescaler Divide Ratio |
|---|---|---|---|
| 0 | 0 | 0 | ÷ 2048 |
| 0 | 0 | 1 | ÷ 1024 |
| 0 | 1 | 0 | ÷ 512 |
| 0 | 1 | 1 | ÷ 128 |
| 1 | 0 | 0 | ÷ 32 |
| 1 | 0 | 1 | ÷ 8 |
| 1 | 1 | 0 | ÷ 4 |
| 1 | 1 | 1 | ÷ 2 |

**Table 20 Timer Mode Register B**

| TMB3 | Auto-Reload Function |
|---|---|
| 0 | No |
| 1 | Yes |

| TMB2 | TMB1 | TMB0 | Prescaler Divide Ratio, Clock Input Source |
|---|---|---|---|
| 0 | 0 | 0 | ÷ 2048 |
| 0 | 0 | 1 | ÷ 512 |
| 0 | 1 | 0 | ÷ 128 |
| 0 | 1 | 1 | ÷ 32 |
| 1 | 0 | 0 | ÷ 8 |
| 1 | 0 | 1 | ÷ 4 |
| 1 | 1 | 0 | ÷ 2 |
| 1 | 1 | 1 | $\overline{INT}$ (external event input) |

**Timer Mode Register B (TMB: $009):** Four-bit write-only timer mode register B (TMB) selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal as shown in table 20. Timer mode register B is initialized to $0 by MCU reset.

The operation mode of timer B changes at the second instruction cycle after timer mode register B is written to. Timer B should be initialized by writing data into timer load register B after the contents of TMB are changed. The configuration and function of timer mode register B is shown in figure 16.

**Timer B Load Register (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B):** Timer B consists of an 8-bit write-only timer load register and an 8-bit read-only timer/event counter. Each has a low-order digit (TCBL: $00A, TLRL: $00A) and a high-order digit (TCBU: $00B, TLRU: $00B) (figure 2).

The timer/event counter can be initialized by writing data into timer load register B. In this case, write the low-order digit first, and then the high-order digit. The timer/event counter is initialized when the high-order digit is written. The timer load register is initialized to $00 by MCU reset.

The counter value of timer B can be obtained by reading timer counter. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched at the time when the high-order digit is read.

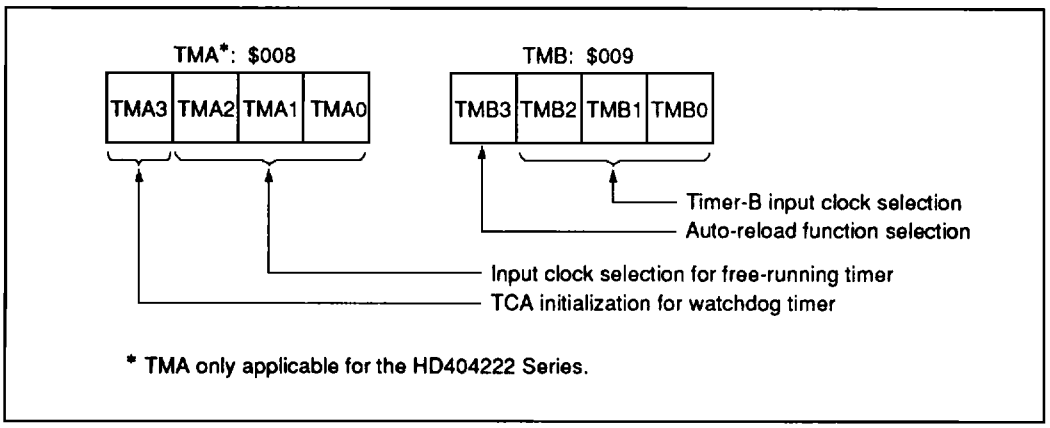



**Figure 16 Mode Registers Configuration and Function**

## Serial Interface

Only applicable for the HD404222 Series.

The serial interface is used to transmit/receive 8-bit data serially. It consists of the serial data register, serial mode register, octal counter, and multiplexer, as illustrated in figure 17. Pin $D_6/\overline{SCK}$ and the transmit clock signal are controlled by the serial mode register. The contents of the serial data register can be written into or read out by software. The data in the serial data register can be shifted synchronously with the transmit clock signal.

The STS instruction initiates serial interface operations and resets the octal counter to 000. The counter starts to count at the falling edge of the transmit clock ($\overline{SCK}$) signal and increments by one at the rising edge of the $\overline{SCK}$. When the octal counter is reset to 000 after eight transmit clock signals, or when a transmit/receive operation is discontinued by resetting the octal counter, the serial interrupt request flag will be set.

**Serial Mode Register (SMR: $005):** The 4-bit write-only serial mode register controls the $D_6/\overline{SCK}$, prescaler divide ratio, and transmit clock source as shown in table 21.

A write signal sent to the serial mode register controls the operating state of the serial interface.

The write signal to the serial mode register stops the serial data register and octal counter from using the transmit clock, and it also resets the octal counter to 000 simultaneously. Therefore, when the serial interface is in the transfer state, the write signal causes the serial mode register to cease the

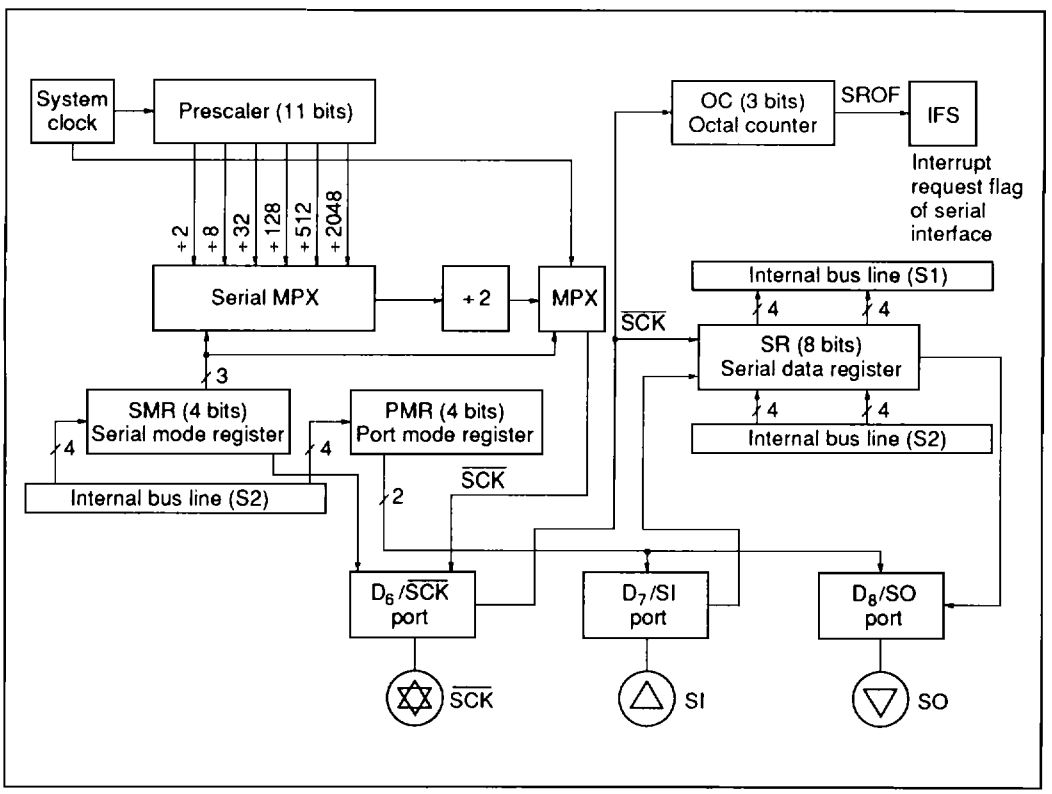



**Figure 17 Serial Interface Block Diagram**

data transfer and to set the serial interrupt request flag.

The contents of the serial mode register will be changed on the second instruction cycle after writing into the serial mode register. Therefore, it is necessary to execute the STS instruction after the data in the serial mode register has been changed completely. The serial mode register will be reset to $0 by MCU reset.

**Serial Data Register (SRL: $006, SRU: $007):** The 8-bit read/write serial data register consists of a low-order digit (SRL: $006) and a high-order digit (SRU: $007).

The data in the serial data register is output from the SO pin, from LSB to MSB, synchronously with the falling edge of the transmit clock signal. At the same time, external data will be input from the SI pin to the serial data register, to LSB first, synchronously with the rising edge of the transmit clock. Figure 18 shows the I/O timing chart for the transmit clock signal and the data.

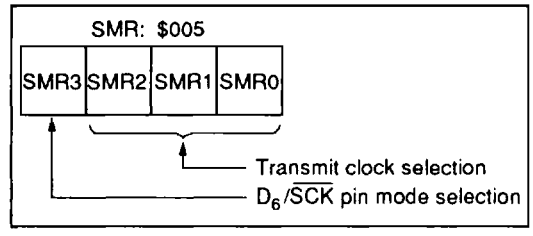
The read/write operations of the serial data register should be performed after the completion of data transmission/reception. Otherwise, the data may not be guaranteed.

**Selecting and Changing the Operation Mode:** Table 22 shows the serial interface operation modes which are determined by a combination of the values in the port mode register and in the serial mode register. Initialize the serial interface by the write signal to the serial mode register when the operation mode is changed.

**Operating State of the Serial Interface:** The serial interface has three operating states: the STS waiting state, transmit clock wait state, and transfer state, as shown in figure 19.

**Table 21 Serial Mode Register**

| SMR3 | $D_6/\overline{SCK}$ |
|---|---|
| 0 | Used as $D_6$ port input/output pin |
| 1 | Used as $\overline{SCK}$ input/output pin |




| | | | Transmit Clock | | | |
|---|---|---|---|---|---|---|
| SMR2 | SMR1 | SMR0 | $D_6/\overline{SCK}$ Port | Clock Source | Prescaler Divide Ratio | System Clock Divide Ratio |
| 0 | 0 | 0 | $\overline{SCK}$ output | Prescaler | + 2048 | + 4096 |
| 0 | 0 | 1 | $\overline{SCK}$ output | Prescaler | + 512 | + 1024 |
| 0 | 1 | 0 | $\overline{SCK}$ output | Prescaler | + 128 | + 256 |
| 0 | 1 | 1 | $\overline{SCK}$ output | Prescaler | + 32 | + 64 |
| 1 | 0 | 0 | $\overline{SCK}$ output | Prescaler | + 8 | + 16 |
| 1 | 0 | 1 | $\overline{SCK}$ output | Prescaler | + 2 | + 4 |
| 1 | 1 | 0 | $\overline{SCK}$ output | System clock | — | + 1 |
| 1 | 1 | 1 | $\overline{SCK}$ input | External clock | — | — |

**Table 22 Serial Interface Operation Mode**

| SMR3 | PMR1 | PMR0 | Serial Interface Operating Mode |
|---|---|---|---|
| 1 | 0 | 0 | Clock continuous output mode |
| 1 | 0 | 1 | Transmit mode |
| 1 | 1 | 0 | Receive mode |
| 1 | 1 | 1 | Transmit/receive mode |

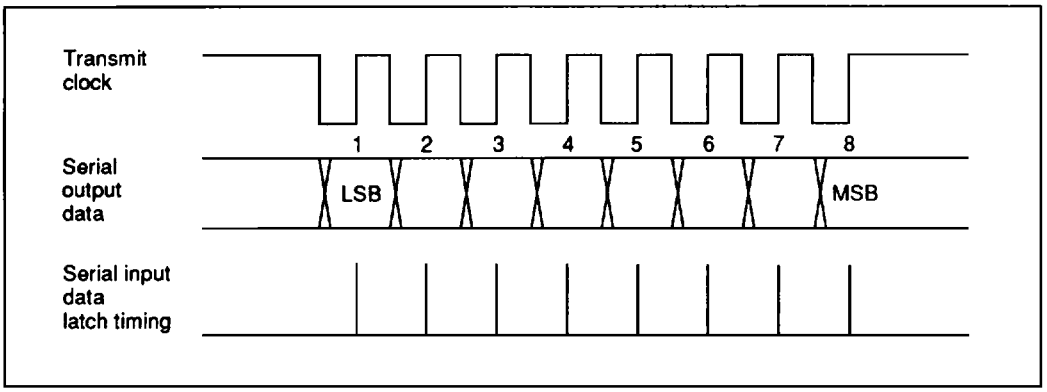



**Figure 18 Serial Interface I/O Timing**

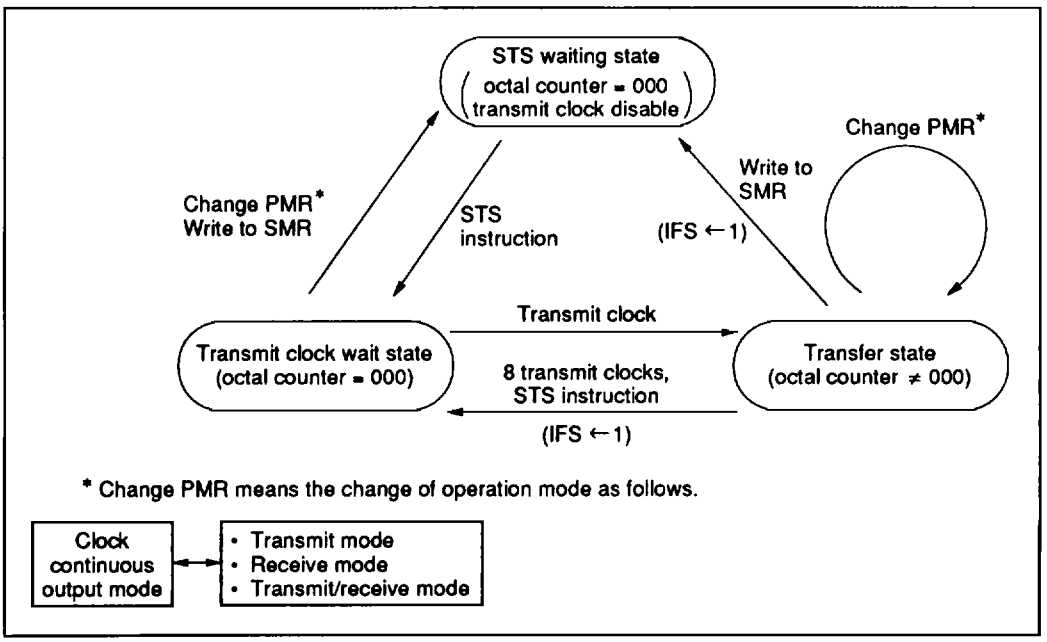



**Figure 19 Serial Interface Operation States**

The STS waiting state is the initialization of the serial interface. In this state, the serial interface does not operate even if the transmit clock is applied.

If the STS instruction is executed, the serial interface shifts to the transmit clock wait state. In this state the falling edge of the first transmit clock causes the serial interface to shift to the transfer state, in which the octal counter counts up and the serial data register shifts simultaneously. If clock continuous output mode is selected, however, the serial interface stays in the transmit clock wait state while the transmit clock outputs continuously.

The octal counter becomes 000 again after 8 transmit clocks or after the execution of the STS instruction, so that the serial interface is returned to the transmit clock wait state and the serial interrupt request flag is set simultaneously.
When the internal transmit clock is selected, the transmit clock output is triggered by the execution of the STS instruction, and stops after 8 clocks.

**Transmit Clock Error Detection:** The serial interface functions abnormally when the transmit clock is disturbed by external noise. In this case, transmit clock errors can be detected by the procedure shown in figure 20.

If more than 8 transmit clocks are applied in the transmit clock wait state, the state of the serial interface shifts in the following sequence: transfer state, transmit clock wait state, and transfer state again. The serial interrupt flag should be reset before entering into the STS state by writing data to SMR. This procedure causes the serial interface request flag to be set again.

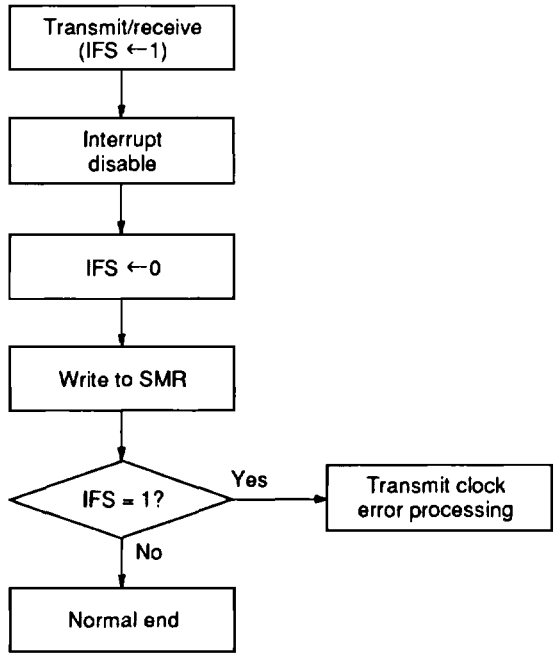



**Figure 20 Transmit Clock Error Detection**

## Comparator

Only applicable for the HD404222 Series.

The MCU has two-channel comparators that compare input data with the reference voltage.

Figure 21 shows the comparator block diagram. The comparator block consists of two analog comparators, the comparator mode register (CMR) which selects the comparator operation, the reference voltage select register (RSR) which selects the reference voltage, a ladder resistance which generates the internal reference voltage, and peripheral circuits.

For the $COMP_0$ input, either the external reference voltage or the internal reference voltage, which is generated by dividing $V_{CC}$ with the internal ladder resistance, can be selected as the reference voltage.

For the $COMP_1$ input, only the external reference voltage is used; the internal reference voltage cannot be selected.

The power consumption increases after the comparator operation is selected by CMR, because direct current is constantly supplied to assure the analog comparator characteristics. To reduce the power consumption during comparator use, the comparator operation should not be selected by software except when analog comparison is required. In this case, a maximum of two instruction cycles are required after the comparator operation is selected in order for the analog comparator to stabilize and operate correctly. Therefore, the comparison result should be read at least two instruction cycles after the comparator operation is selected.

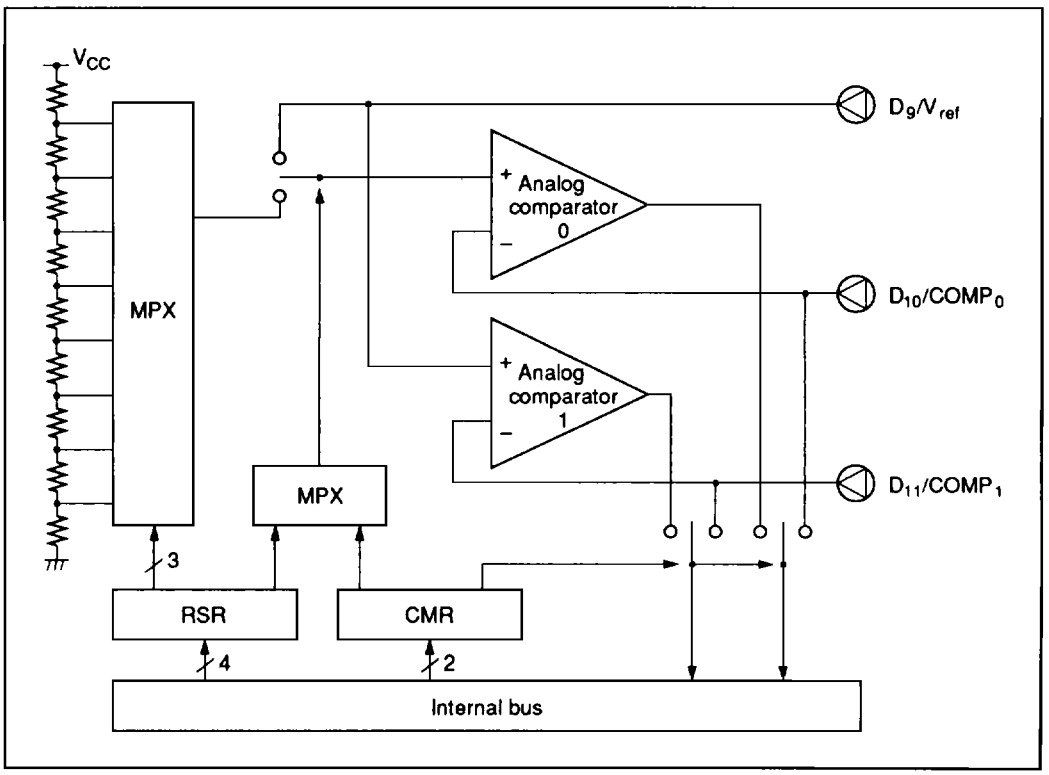



**Figure 21 Comparator Block Diagram**

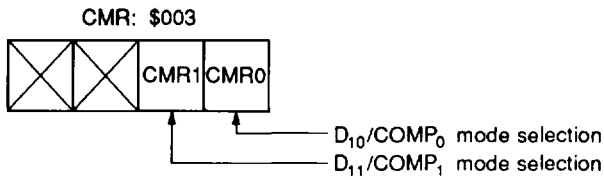
The comparison result is obtained by executing the TD or TDD instruction. When the analog input voltage is higher than the reference voltage, a 1 is read as input data from the comparator. The comparator automatically stops operating in standby and stop modes.

**Comparator Mode Register (CMR: $003):** This 2-bit register selects the $D_{10}$/$COMP_0$ and $D_{11}$/$COMP_1$ functions.

CMR is only affected by the bit manipulation instructions (set by the SEM or SEMD instruction and reset by the REM or REMD instruction). It is initialized to $0 by MCU reset. Therefore, it becomes input/output mode after MCU reset.

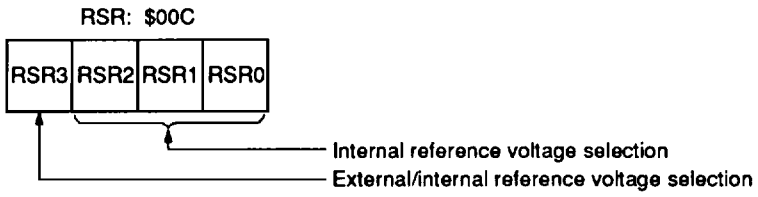
**Reference Voltage Select Register (RSR: $00C):** This 4-bit read/write register selects the $COMP_0$ reference voltage for the analog comparator from the eight-level internal voltage or the external voltage. It is initialized to $0 by MCU reset.

**Notes for Use:** When using the analog comparator, carefully program the data output instruction and data input into the port next to $COMP_0$ and $COMP_1$ to assure precise and stabilized comparator operation.




| CMR | | Mode Selection | |
|---|---|---|---|
| Bit 1 | Bit 0 | $D_{10}$/$COMP_0$ | $D_{11}$/$COMP_1$ |
| 0 | 0 | $D_{10}$ | $D_{11}$ |
| 0 | 1 | $COMP_0$ | $D_{11}$ |
| 1 | 0 | $D_{10}$ | $COMP_1$ |
| 1 | 1 | $COMP_0$ | $COMP_1$ |

**Figure 22 Comparator Mode Register**




| RSR | | | | |
|---|---|---|---|---|
| **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** | **Reference Voltage** |
| 0 | 0 | 0 | 0 | 1/11 $V_{CC}$ |
| 0 | 0 | 0 | 1 | 2/11 $V_{CC}$ |
| 0 | 0 | 1 | 0 | 3/11 $V_{CC}$ |
| 0 | 0 | 1 | 1 | 4/11 $V_{CC}$ |
| 0 | 1 | 0 | 0 | 5/11 $V_{CC}$ |
| 0 | 1 | 0 | 1 | 6/11 $V_{CC}$ |
| 0 | 1 | 1 | 0 | 7/11 $V_{CC}$ |
| 0 | 1 | 1 | 1 | 8/11 $V_{CC}$ |
| 1 | — | — | — | External $V_{ref}$ ($D_9/V_{ref}$) |

— indicates 0 or 1

**Figure 23 Reference Voltage Select Register**

### Pins for PROM Mode

**$V_{PP}$ (Program Voltage):** $V_{PP}$ is the input program voltage (12.5 V ±0.3 V) for programming the PROM.

**$\overline{CE}$ (Chip Enable):** $\overline{CE}$ input enables programming and verification of the internal PROM.

**$\overline{OE}$ (Output Enable):** $\overline{OE}$ is the data output control signal for verification.

**$A_0$–$A_{12}$ (Address Bus):** $A_0$–$A_{12}$ are address input pins for the internal PROM.

**$O_0$–$O_4$ (PROM Data Bus):** $O_0$–$O_4$ are the data bus pins for the internal PROM.

### PROM Mode Pin Description

| Pin No. | | MCU Mode | | PROM Mode | |
|---|---|---|---|---|---|
| DP-28S, FP-28DA | FP-30D | Symbol | I/O | Symbol | I/O |
| 1 | 2 | GND | | GND | |
| 2 | 3 | $R1_0$ | I/O | $A_5$ | I |
| 3 | 4 | $R1_1$ | I/O | $A_6$ | I |
| 4 | 5 | $R1_2$ | I/O | $A_7$ | I |
| 5 | 6 | $R1_3$ | I/O | $A_8$ | I |
| 6 | 7 | $D_0$ | I/O | $A_1$ | I |
| 7 | 8 | $D_1$ | I/O | $A_2$ | I |
| 8 | 9 | $D_2$ | I/O | $A_3$ | I |
| 9 | 10 | $D_3$ | I/O | $A_4$ | I |
| 10 | 11 | $D_4$ | I/O | $A_0$ | I |
| 11 | 12 | $D_5/\overline{INT}$ | I/O | $O_0$ | I/O |
| 12 | 13 | $D_6/\overline{SCK}$ | I/O | $O_1$ | I/O |
| 13 | 14 | $D_7$/SI | I/O | $O_2$ | I/O |
| 14 | 15 | $D_8$/SO | I/O | $O_3$ | I/O |
| 15 | 16 | $D_9/V_{ref}$ | I/O | $O_4$ | I/O |
| 16 | 17 | $D_{10}/COMP_0$ | I/O | $\overline{CE}$ | I |
| 17 | 18 | $D_{11}/COMP_1$ | I/O | $\overline{OE}$ | I |
| 18 | 19 | $V_{CC}$ | | $V_{CC}$ | |
| 19 | 20 | $OSC_1$ | I | $V_{CC}$ | |
| 20 | 21 | $OSC_2$ | O | | |
| 21 | 22 | $\overline{RESET}$ | I | GND | |
| 22 | 23 | TEST | I | $V_{PP}$ | |
| 23 | 24 | $D_{12}$ | I/O | $V_{CC}$ | |
| 24 | 25 | $D_{13}$ | I/O | GND | |
| 25 | 26 | $R2_0$ | I/O | $A_9$ | I |
| 26 | 27 | $R2_1$ | I/O | $A_{10}$ | I |
| 27 | 28 | $R2_2$ | I/O | $A_{11}$ | I |
| 28 | 29 | $R2_3$ | I/O | $A_{12}$ | I |

### Programmable ROM Operation

The HD4074224's on-chip PROM is programmed in PROM mode.

In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 28-to-28-pin socket adapter as shown in figure 24. Table 23 lists the recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputer incorporates a conversion circuit to enable the use of a general purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, lower 5 bits and upper 5 bits. For example, if 4 kwords of on-chip PROM are programmed by a general purpose PROM programmer, 8 kbytes of addresses ($0000–$1FFF) should be specified.

### Programming and Verification

The HD4074224 can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 24 shows how programming and verification modes are selected.

### Precautions

1. Addresses $0000 to $1FFF should be specified if the PROM is programmed by a PROM programmer. Note that the plastic package type devices cannot be erased and reprogrammed.

2. Be careful that the wrong PROM programmer or socket adapter may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed onto the socket adapter, and that the socket adapter is firmly fixed in the programmer.

3. The PROM should be programmed with $V_{PP}$ = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the HD4074224, the LSI may be permanently damaged. 12.5 V is Intel's 27256 $V_{PP}$.

**Table 23 PROM Programmer and Socket Adapter**

**PROM Programmer**

| Maker | Type Name |
|---|---|
| DATA I/O | 29B<br>UNISITE |
| AVAL Corp. | PKW-1100<br>PKW-3100 |

**Socket Adapter**

| Package | Type Name | Maker |
|---|---|---|
| DP-28S | HS422ESS01H | Hitachi |
| FP-28DA | HS422ESP01H | Hitachi |
| FP-30D | HS4224ESF01H | Hitachi |

**Table 24 PROM Mode Selection**

| | Pin | | | |
|---|---|---|---|---|
| **Mode** | $\overline{CE}$ | $\overline{OE}$ | $V_{PP}$ | $O_0$–$O_4$ |
| Programming | Low | High | $V_{PP}$ | Data input |
| Verification | High | Low | $V_{PP}$ | Data output |
| Programming inhibited | High | High | $V_{PP}$ | High impedance |

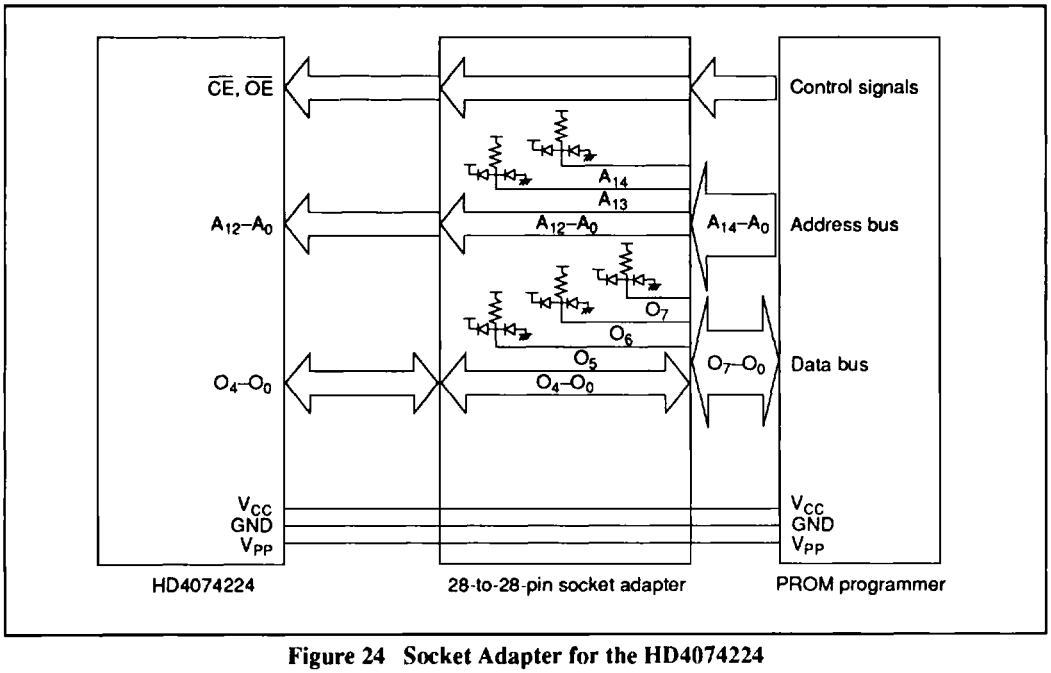



**Figure 24 Socket Adapter for the HD4074224**

## Addressing Modes

### RAM Addressing Modes

As shown in figure 25, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

**Register Indirect Addressing:** The contents (8 bits) of the X and Y registers are used as the RAM address.

**Direct Addressing:** A direct addressing instruction consists of two words, the first word contains the opcode, the second word (10 bits) is used as the RAM address.

**Memory Register Addressing:** The memory registers (16 digits from $020 to $02F) are accessed by executing the LAMR and XMRA instructions.

### ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 26.

**Direct Addressing Mode:** The program can branch to any address in ROM memory by executing the JMPL, BRL, or CALL instruction. These instructions replace the 12 program counter bits ($PC_{11}$ to $PC_0$) with 12-bit immediate data.

**Current Page Addressing Mode:** The MCU has 8 pages of ROM with 256 words per page. The program can branch to an address on the current page by executing the BR instruction. This instruction replaces the lower eight bits of the program counter ($PC_7$ to $PC_0$) with 8-bit immediate data.

When the BR instruction falls on a page boundary (256n + 255), executing the BR instruction transfers the PC contents to the next page (figure 27) according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400 series cross macroassembler has an automatic paging facility for ROM pages.

**Zero-Page Addressing Mode:** By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at $0000–$003F. When the CAL instruction is executed, 6-bits of immediate data are placed in the low-order six bits of the program counter ($PC_5$ to $PC_0$) and 0s are placed in the high-order six bits ($PC_{11}$ to $PC_6$).

**Table Data Addressing Mode:** By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

**P Instruction:** ROM data addressed by table data addressing can be referenced by the P instruction (figure 28). When bit 8 of the ROM data is 1 ($RO_8$ = 1), 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1 ($RO_9$ = 1), 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1 ($RO_8$ = 1, $RO_9$ = 1), ROM data are written into the accumulator, B register, and R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

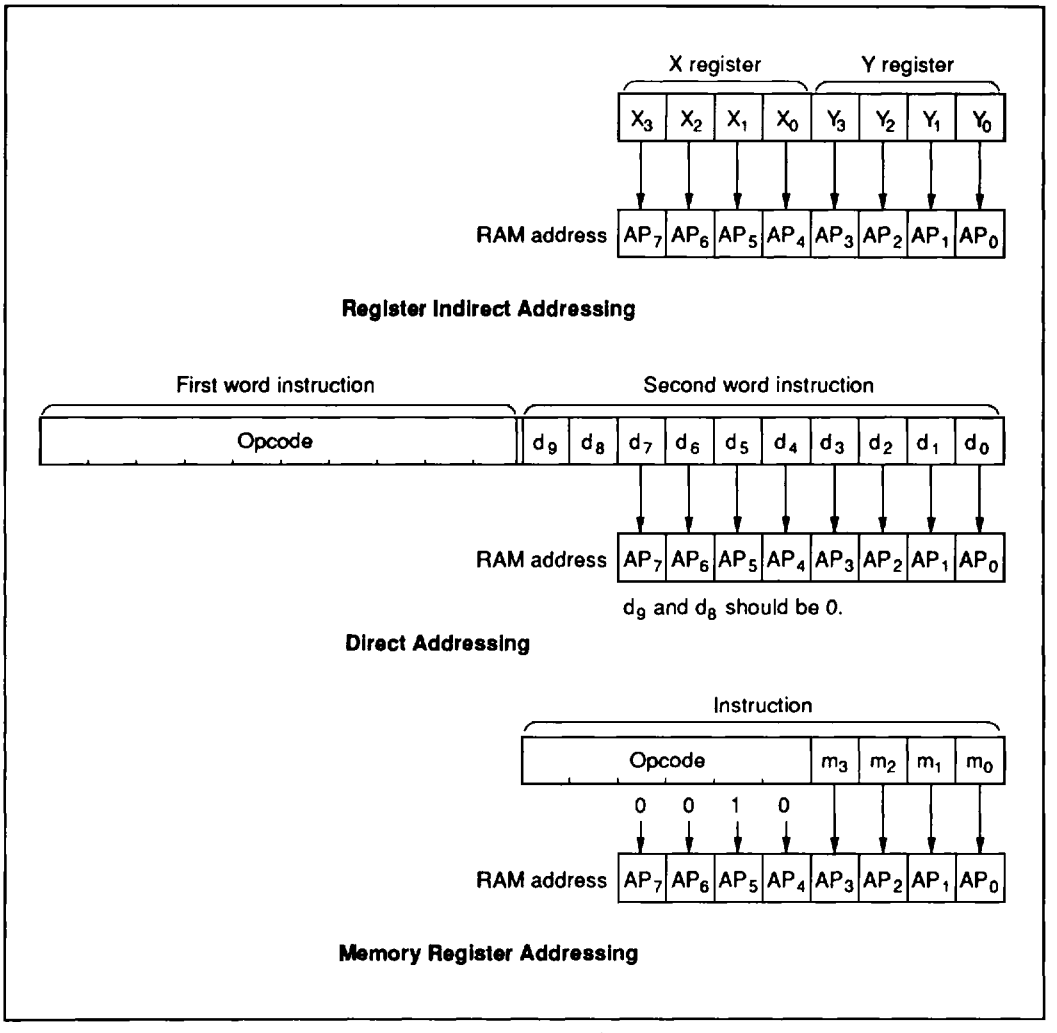



**Figure 25 RAM Addressing Modes**

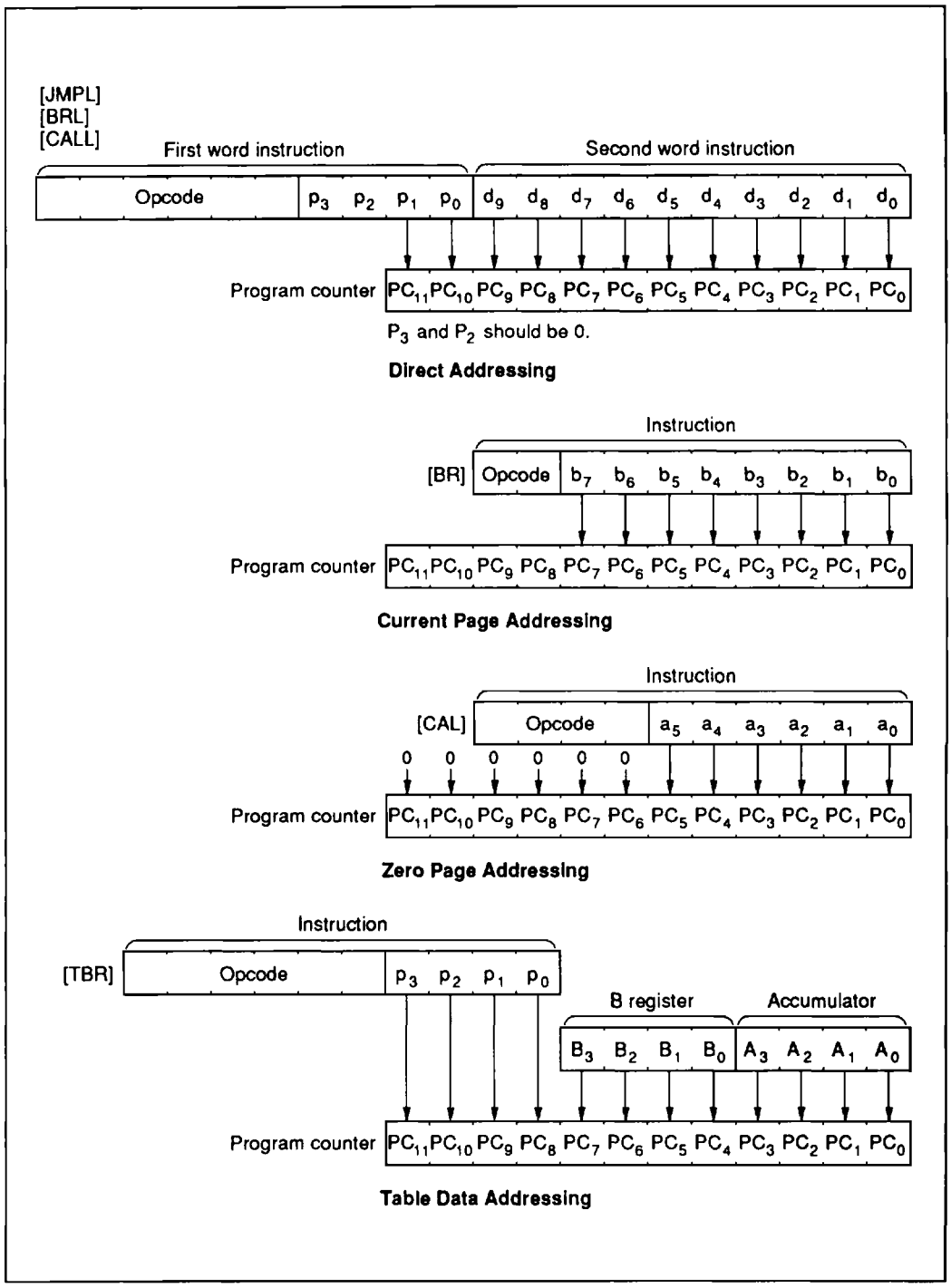



**Figure 26 ROM Addressing Modes**

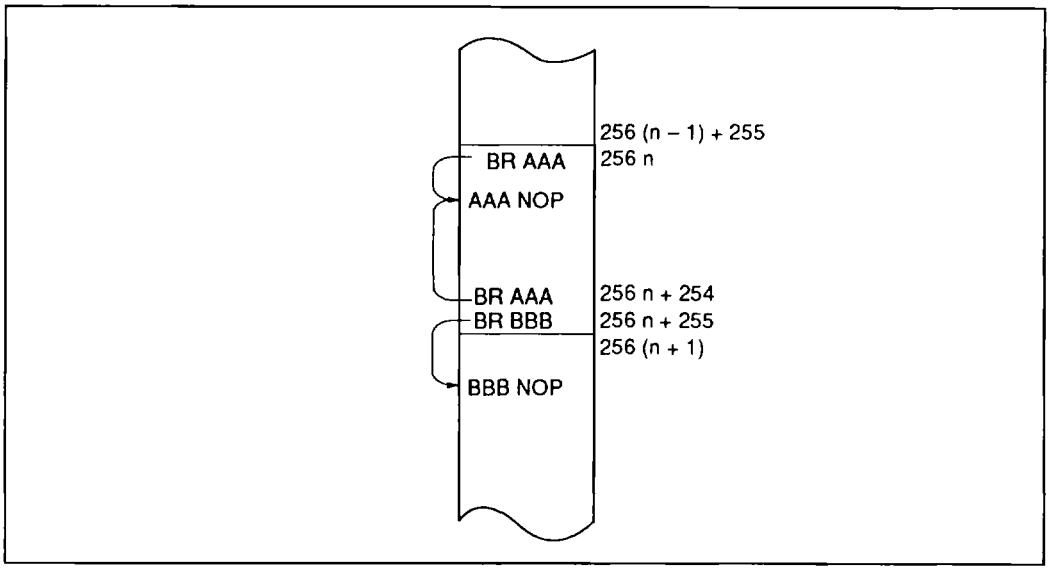



**Figure 27 BR Instruction Branch Destination on a Page Boundary**

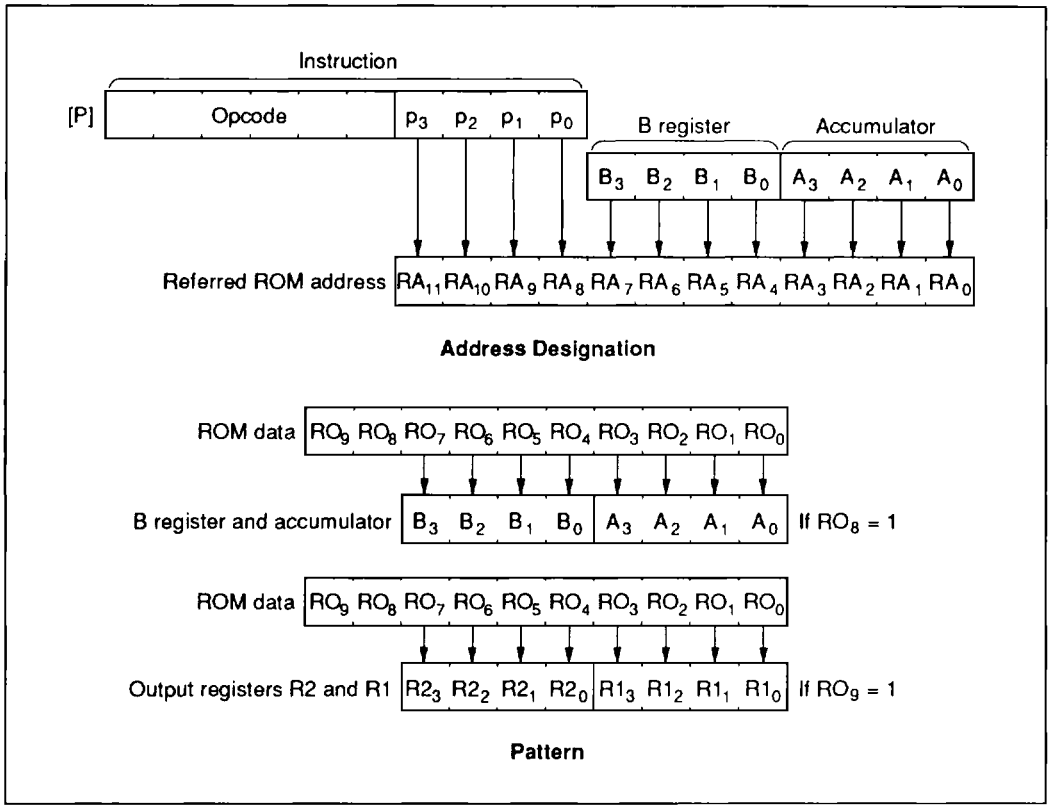



**Figure 28 P Instruction**

## Absolute Maximum Ratings

| Item | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | –0.3 to +7.0 | V | |
| Programming voltage | $V_{PP}$ | –0.3 to +14 | V | 1 |
| Pin voltage | $V_T$ | –0.3 to $V_{CC}$ + 0.3 | V | |
| Total permissible input current | $\Sigma I_o$ | 100 | mA | 2 |
| Total permissible output current | $-\Sigma I_o$ | 30 | mA | 3 |
| Maximum input current | $I_o$ | 30 | mA | 4, 6 |
| | | 4 | mA | 5, 6 |
| Maximum output current | $-I_o$ | 4 | mA | 7 |
| Operating temperature | $T_{opr}$ | –20 to +75 | °C | |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C | |

Notes: 1. Applies to HD4074224.
2. The total permissible input current is the total of input currents simultaneously flowing in from all I/O pins to GND.
3. The total permissible output current is the total of output currents simultaneously flowing out from $V_{CC}$ to all I/O pins.
4. Applies to $D_{12}$, $D_{13}$, $R1_0$ to $R1_3$, and $R2_0$ to $R2_3$.
5. Applies to $D_0$ to $D_{11}$.
6. The maximum input current is the maximum current flowing from any I/O pins to GND.
7. The maximum output current is the maximum current flowing from $V_{CC}$ to any I/O pins.

Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

All voltages are with respect to GND.

## HD404201, HD404202, HD404222 Electrical Characteristics

**DC Characteristics** ($V_{CC}$ = 3.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C)

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$* | $0.9V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| | | SI* | $0.9V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| | | $OSC_1$ | $V_{CC}$ – 0.5 | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$* | –0.3 | — | $0.2V_{CC}$ | V | | |
| | | SI* | –0.3 | — | $0.2V_{CC}$ | V | | |
| | | $OSC_1$ | –0.3 | — | 0.5 | V | | |
| Output high voltage* | $V_{OH}$ | $\overline{SCK}$, SO | $V_{CC}$ – 1.0 | — | — | V | $-I_{OH}$ = 1.0 mA | |
| Output low voltage* | $V_{OL}$ | $\overline{SCK}$, SO | — | — | 0.4 | V | $I_{OL}$ = 0.5 mA | |
| Input/output leakage current | $\lvert I_{IL} \rvert$ | $\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$*, SI*, SO*, $OSC_1$ | — | — | 1 | μA | $V_{in}$ = 0 V to $V_{CC}$ | 1 |
| Current dissipation in active mode | $I_{CC}$ | $V_{CC}$ | — | — | 3.5 | mA | $V_{CC}$ = 5 V, $f_{OSC}$ = 4 MHz | 2, 5 |
| | $I_{CMP}$* | $V_{CC}$ | — | — | 5.5 | mA | $V_{CC}$ = 5 V, $f_{OSC}$ = 4 MHz Comparator active | 3, 5 |
| Current dissipation in standby mode | $I_{SBY}$ | $V_{CC}$ | — | — | 1.7 | mA | $V_{CC}$ = 5 V, $f_{OSC}$ = 4 MHz | 4, 5 |
| Current dissipation in stop mode | $I_{STOP}$ | $V_{CC}$ | — | — | 10 | μA | $V_{in(\overline{RESET})}$ = $V_{CC}$ – 0.3 V to $V_{CC}$, $V_{in(TEST)}$ = 0 V to 0.3 V | |
| Stop mode retaining voltage | $V_{STOP}$ | $V_{CC}$ | 2 | — | — | V | | |

Notes on next page.
* Applies to HD404222.

**DC Characteristics** ($V_{CC}$ = 3.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C) (cont)

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage* | $V_{IHA}$ | $COMP_0$, $COMP_1$ | $VC_{ref}$ + 0.1 | — | — | V | | |
| Input low voltage* | $V_{ILA}$ | $COMP_0$, $COMP_1$ | 0 | — | $VC_{ref}$ – 0.1 | V | | |
| Comparator input reference voltage scope* | $VC_{ref}$ | $V_{ref}$ | 0 | — | $V_{CC}$ – 1.2 | V | | |
| Deviation of internal reference voltage* | $V_{OFS}$ | — | –0.1 | — | 0.1 | V | $V_{CC}$ = 4.5 V to 6.0 V | 6 |

Notes: 1. Excluding output buffer current and pull-up MOS current.

2. $I_{CC}$ is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$ at GND, TEST at GND
   $D_0$ to $D_{13}$, R1, R2 at $V_{CC}$

3. $I_{CMP}$ is the source current when no I/O current is flowing while the MCU comparator is in operation.
   Test conditions: MCU: Comparator active
   Pins: $\overline{RESET}$ at $V_{CC}$, TEST at GND
   $D_0$ to $D_8$, $D_{12}$, $D_{13}$, R1, R2 at $V_{CC}$
   $D_9$ to $D_{11}$ at GND

4. $I_{SBY}$ is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions: MCU: I/O same as at reset
   Standby mode
   Pins: $\overline{RESET}$ at $V_{CC}$
   TEST at GND
   $D_0$ to $D_{13}$, R1, R2 at $V_{CC}$

5. Power dissipation is in proportion to $f_{OSC}$ while the MCU is operating or is in standby mode. The value of the dissipation current when $f_{OSC}$ = x MHz is given by the following equation:
   Maximum value ($f_{OSC}$ = x MHz) = x/4 × maximum value ($f_{OSC}$ = 4 MHz)

6. The reference voltage is the expected internal $VC_{ref}$ voltage selected by the reference voltage select register (RSR).
   Example: when RSR = $1 reference voltage is 2/11 × $V_{CC}$.

* Applies to HD404222.

**Input/Output Characteristics** ($V_{CC}$ = 3.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C )

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $D_0$–$D_{13}$, R1, R2 | $0.7V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $D_0$–$D_{13}$, R1, R2 | –0.3 | — | $0.3V_{CC}$ | V | | |
| Output high voltage | $V_{OH}$ | $D_0$–$D_{13}$, R1, R2 | $V_{CC}$ – 1.0 | — | — | V | $-I_{OH}$ = 1.0 mA | 1 |
| Output low voltage | $V_{OL}$ | $D_0$–$D_{13}$, R1, R2 | — | — | 0.4 | V | $I_{OL}$ = 0.5 mA | |
| | | $D_{12}$, $D_{13}$, R1, R2 | — | — | 2 | V | $I_{OL}$ = 15 mA, $V_{CC}$ = 4.5 V to 6.0 V | |
| Input/output leakage current | $\|I_{IL}\|$ | $D_0$–$D_{13}$, R1, R2 | — | — | 1 | μA | $V_{in}$ = 0 V to $V_{CC}$ | 2 |
| Pull-up MOS current | $-I_{PU}$ | $D_0$–$D_{13}$, R1, R2 | 40 | 80 | 160 | μA | $V_{CC}$ = 5 V, $V_{in}$ = 0 V | 3 |

Notes: 1. For I/O pins selected as CMOS output by mask option.
2. Excluding output buffer current and pull-up MOS current.
3. Applies to I/O pins selected as with pull-up MOS by mask option.

**AC Characteristics** ($V_{CC}$ = 3.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C)

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{OSC}$ | $OSC_1$, $OSC_2$ | 1 | 4 | 4.5 | MHz | Ceramic oscillator | |
| | | | 1 | — | 3 | MHz | Resistor oscillator $R_f$ = 20 kΩ ±1% | |
| Instruction cycle time | $t_{cyc}$ | — | 0.89 | 1 | 4 | µs | Ceramic oscillator divided by 4 | |
| | | | 1.33 | — | 4 | µs | Resistor oscillator divided by 4 | |
| Oscillator stabilization time | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 20 | ms | Ceramic oscillator | 1 |
| | | | — | — | 0.5 | ms | Resistor oscillator | |
| Capacitance between pins | $C_{RF}$ | $OSC_1$, $OSC_2$ | — | — | 1 | pF | | |
| External clock high and low widths | $t_{CPH}$, $t_{CPL}$ | $OSC_1$ | 92 | — | — | ns | | 2 |
| External clock rise time | $t_{CPr}$ | $OSC_1$ | — | — | 20 | ns | | 2 |
| External clock fall time | $t_{CPf}$ | $OSC_1$ | — | — | 20 | ns | | 2 |
| $\overline{INT}$ high width | $t_{IH}$ | $\overline{INT}$ | 2 | — | — | $t_{cyc}$ | | 3 |
| $\overline{INT}$ low width | $t_{IL}$ | $\overline{INT}$ | 2 | — | — | $t_{cyc}$ | | 3 |
| $\overline{RESET}$ low width | $t_{RSTL}$ | $\overline{RESET}$ | 2 | — | — | $t_{cyc}$ | | 4 |
| $\overline{RESET}$ rise time | $t_{RSTr}$ | $\overline{RESET}$ | — | — | 20 | ms | | 4 |
| Input capacitance | $C_{in}$ | All pins | — | — | 15 | pF | f = 1 MHz, $V_{in}$ = 0 V, $T_a$ = 25°C | |
| Comparator stabilization time* | $t_{CSTB}$ | $COMP_0$ | — | — | 2 | $t_{cyc}$ | | |

Notes: 1. The oscillator stabilization time is the period from when $V_{CC}$ reaches its minimum allowable voltage (3.5 V) at power-on until when the oscillator stabilizes, or after $\overline{RESET}$ goes low. At power-on or stop mode recovery, $\overline{RESET}$ must be kept low for at least $t_{RC}$. Since $t_{RC}$ depends on the ceramic oscillator's circuit constant and stray capacitance, consult with the ceramic oscillator manufacturer when designing the reset circuit.

2. Refer to figure 29.
3. Refer to figure 30.
4. Refer to figure 31.

* Applies to HD404222.

**Serial Interface Timing Characteristics (HD404222: $V_{CC}$ = 3.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C )**

**During Transmit Clock Output**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | Load shown in figure 33 | 1 |
| Transmit clock high and low widths | $t_{SCKH}$, $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | Load shown in figure 33 | 1 |
| Transmit clock rise and fall times | $t_{SCKr}$, $t_{SCKf}$ | $\overline{SCK}$ | — | — | 100 | ns | Load shown in figure 33 | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 250 | ns | Load shown in figure 33 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 300 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 150 | — | — | ns | | 1 |

**During Transmit Clock Input**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | | 1 |
| Transmit clock high and low widths | $t_{SCKH}$, $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | | 1 |
| Transmit clock rise and fall times | $t_{SCKr}$, $t_{SCKf}$ | $\overline{SCK}$ | — | — | 100 | ns | | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 250 | ns | Load shown in figure 33 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 300 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 150 | — | — | ns | | 1 |

Note: 1. Refer to figure 32.

## HD40L4201, HD40L4202, HD40L4222 Electrical Characteristics

**DC Characteristics** ($V_{CC}$ = 2.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C)

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$* | $0.9V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| | | SI* | $0.9V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| | | $OSC_1$ | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$* | –0.3 | — | $0.2V_{CC}$ | V | | |
| | | SI* | –0.3 | — | $0.2V_{CC}$ | V | | |
| | | $OSC_1$ | –0.3 | — | 0.3 | V | | |
| Output high voltage* | $V_{OH}$ | $\overline{SCK}$, SO | $V_{CC}$ – 0.5 | — | — | V | $-I_{OH}$ = 0.5 mA | |
| Output low voltage* | $V_{OL}$ | $\overline{SCK}$, SO | — | — | 0.4 | V | $I_{OL}$ = 0.5 mA | |
| Input/output leakage current | $\|I_{IL}\|$ | $\overline{RESET}$, $\overline{INT}$, $\overline{SCK}$*, SI*, SO*, $OSC_1$ | — | — | 1 | µA | $V_{in}$ = 0 V to $V_{CC}$ | 1 |
| Current dissipation in active mode | $I_{CC}$ | $V_{CC}$ | — | — | 1 | mA | $V_{CC}$ = 3 V, $f_{OSC}$ = 1 MHz | 2, 5 |
| | $I_{CMP}$* | $V_{CC}$ | — | — | 1.6 | mA | $V_{CC}$ = 3 V, $f_{OSC}$ = 1 MHz Comparator active | 3, 5 |
| Current dissipation in standby mode | $I_{SBY}$ | $V_{CC}$ | — | — | 0.5 | mA | $V_{CC}$ = 3 V, $f_{OSC}$ = 1 MHz | 4, 5 |
| Current dissipation in stop mode | $I_{STOP}$ | $V_{CC}$ | — | — | 10 | µA | $V_{in(\overline{RESET})}$ = $V_{CC}$ – 0.3 V to $V_{CC}$, $V_{in(TEST)}$ = 0 V to 0.3 V | |
| Stop mode retaining voltage | $V_{STOP}$ | $V_{CC}$ | 2 | — | — | V | | |

Notes on next page.

**DC Characteristics ($V_{CC}$ = 2.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C) (cont)**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage* | $V_{IHA}$ | $COMP_0$, $COMP_1$ | $VC_{ref}$ + 0.1 | — | — | V | | |
| Input low voltage* | $V_{ILA}$ | $COMP_0$, $COMP_1$ | 0 | — | $VC_{ref}$ – 0.1 | V | | |
| Comparator input reference voltage scope* | $VC_{ref}$ | $V_{ref}$ | 0 | — | $V_{CC}$ – 1.2 | V | | |
| Deviation of internal reference voltage* | $V_{OFS}$ | — | –0.1 | — | 0.1 | V | $V_{CC}$ = 4.5 V to 6.0 V | 6 |

Notes: 1. Excluding output buffer current and pull-up MOS current.

2. $I_{CC}$ is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$ at GND, TEST at GND
   $D_0$ to $D_{13}$, R1, R2 at $V_{CC}$

3. $I_{CMP}$ is the source current when no I/O current is flowing while the MCU comparator is in operation.
   Test conditions: MCU: Comparator active
   Pins: $\overline{RESET}$ at $V_{CC}$, TEST at GND
   $D_0$ to $D_8$, $D_{12}$, $D_{13}$, R1, R2 at $V_{CC}$
   $D_9$ to $D_{11}$ at GND

4. $I_{SBY}$ is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions: MCU: I/O same as at reset
   Standby mode
   Pins: $\overline{RESET}$ at $V_{CC}$
   TEST at GND
   $D_0$ to $D_{13}$, R1, R2 at $V_{CC}$

5. Power dissipation is in proportion to $f_{OSC}$ while the MCU is operating or is in standby mode. The value of the dissipation current when $f_{OSC}$ = x MHz is given by the following equation:
   Maximum value ($f_{OSC}$ = x MHz) = x/4 × maximum value ($f_{OSC}$ = 1 MHz)

6. The reference voltage is the expected internal $VC_{ref}$ voltage selected by the reference voltage select register (RSR).
   Example: when RSR = $1 reference voltage is 2/11 × $V_{CC}$.

* Applies to HD40L4222.

**Input/Output Characteristics** ($V_{CC}$ = 2.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C )

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $D_0$–$D_{13}$, R1, R2 | $0.7V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $D_0$–$D_{13}$, R1, R2 | –0.3 | — | $0.3V_{CC}$ | V | | |
| Output high voltage | $V_{OH}$ | $D_0$–$D_{13}$, R1, R2 | $V_{CC}$ – 0.5 | — | — | V | $-I_{OH}$ = 0.5 mA | 1 |
| Output low voltage | $V_{OL}$ | $D_0$–$D_{13}$, R1, R2 | — | — | 0.4 | V | $I_{OL}$ = 0.4 mA | |
| | | $D_{12}$, $D_{13}$, R1, R2 | — | — | 2 | V | $I_{OL}$ = 15 mA, $V_{CC}$ = 4.5 V to 6.0 V | |
| Input/output leakage current | $\|I_{IL}\|$ | $D_0$–$D_{13}$, R1, R2 | — | — | 1 | µA | $V_{in}$ = 0 V to $V_{CC}$ | 2 |
| Pull-up MOS current | $-I_{PU}$ | $D_0$–$D_{13}$, R1, R2 | 10 | 25 | 60 | µA | $V_{CC}$ = 3 V, $V_{in}$ = 0 V | 3 |

Notes: 1. For I/O pins selected as CMOS output by mask option.
2. Excluding output buffer current and pull-up MOS current.
3. Applies to I/O pins selected as with pull-up MOS by mask option.

**AC Characteristics** ($V_{CC}$ = 2.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C)

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{OSC}$ | $OSC_1$, $OSC_2$ | 0.4 | 1 | 1.125 | MHz | Ceramic oscillator | |
| Instruction cycle time | $t_{cyc}$ | — | 3.55 | 4 | 10 | µs | Ceramic oscillator divided by 4 | |
| Oscillator stabilization time | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 20 | ms | Ceramic oscillator | 1 |
| External clock high and low widths | $t_{CPH}$, $t_{CPL}$ | $OSC_1$ | 425 | — | — | ns | | 2 |
| External clock rise time | $t_{CPr}$ | $OSC_1$ | — | — | 20 | ns | | 2 |
| External clock fall time | $t_{CPf}$ | $OSC_1$ | — | — | 20 | ns | | 2 |
| $\overline{INT}$ high width | $t_{IH}$ | $\overline{INT}$ | 2 | — | — | $t_{cyc}$ | | 3 |
| $\overline{INT}$ low width | $t_{IL}$ | $\overline{INT}$ | 2 | — | — | $t_{cyc}$ | | 3 |
| $\overline{RESET}$ low width | $t_{RSTL}$ | $\overline{RESET}$ | 2 | — | — | $t_{cyc}$ | | 4 |
| $\overline{RESET}$ rise time | $t_{RSTr}$ | $\overline{RESET}$ | — | — | 20 | ms | | 4 |
| Input capacitance | $C_{in}$ | All pins | — | — | 15 | pF | f = 1 MHz, $V_{in}$ = 0 V, $T_a$ = 25°C | |
| Comparator stabilization time* | $t_{CSTB}$ | $COMP_0$ | — | — | 2 | $t_{cyc}$ | | |

Notes: 1. The oscillator stabilization time is the period from when $V_{CC}$ reaches its minimum allowable voltage (2.5 V) at power-on until when the oscillator stabilizes, or after $\overline{RESET}$ goes low. At power-on or stop mode recovery, $\overline{RESET}$ must be kept low for at least $t_{RC}$. Since $t_{RC}$ depends on the ceramic oscillator's circuit constant and stray capacitance, consult with the ceramic oscillator manufacturer when designing the reset circuit.

2. Refer to figure 29.
3. Refer to figure 30.
4. Refer to figure 31.

* Applies to HD40L4222.

## Serial Interface Timing Characteristics ($V_{CC}$ = 2.5 V to 6.0 V, GND = 0 V, $T_a$ = –20°C to +75°C )

### During Transmit Clock Output

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | Load shown in figure 33 | 1 |
| Transmit clock high and low widths | $t_{SCKH}$, $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | Load shown in figure 33 | 1 |
| Transmit clock rise and fall times | $t_{SCKr}$, $t_{SCKf}$ | $\overline{SCK}$ | — | — | 300 | ns | Load shown in figure 33 | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 600 | ns | Load shown in figure 33 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 1000 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 500 | — | — | ns | | 1 |

### During Transmit Clock Input

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | | 1 |
| Transmit clock high and low widths | $t_{SCKH}$, $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | | 1 |
| Transmit clock rise and fall times | $t_{SCKr}$, $t_{SCKf}$ | $\overline{SCK}$ | — | — | 300 | ns | | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 600 | ns | Load shown in figure 33 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 1000 | — | — | ns | | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 500 | — | — | ns | | 1 |

Note: 1. Refer to figure 32.

## HD4074224 Electrical Characteristics

**DC Characteristics ($V_{CC}$ = 2.7 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C)**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $\overline{RESET}$, SCK, $\overline{INT}$ | $0.9V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| | | SI | $0.7V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| | | $OSC_1$ | $V_{CC}$ – 0.3 | — | $V_{CC}$ + 0.3 | V | 2.7 V ≤ $V_{CC}$ < 3.5 V | |
| | | | $V_{CC}$ – 0.5 | — | $V_{CC}$ + 0.3 | V | 3.5 V ≤ $V_{CC}$ ≤ 5.5 V | |
| Input low voltage | $V_{IL}$ | $\overline{RESET}$, SCK, $\overline{INT}$ | –0.3 | — | $0.2V_{CC}$ | V | | |
| | | SI | –0.3 | — | $0.3V_{CC}$ | V | | |
| | | $OSC_1$ | –0.3 | — | 0.3 | V | 2.7 V ≤ $V_{CC}$ < 3.5 V | |
| | | | –0.3 | — | 0.5 | V | 3.5 V ≤ $V_{CC}$ ≤ 5.5 V | |
| Output high voltage | $V_{OH}$ | SCK, SO | $V_{CC}$ – 0.5 | — | — | V | 2.7 V ≤ $V_{CC}$ < 3.5 V – $I_{OH}$ = 0.5 mA | |
| | | | $V_{CC}$ – 1.0 | — | — | V | 3.5 V ≤ $V_{CC}$ ≤ 5.5 V – $I_{OH}$ = 1.0 mA | |
| Output low voltage | $V_{OL}$ | SCK, SO | — | — | 0.4 | V | $I_{OL}$ = 0.5 mA | |
| Input/output leakage current | $\|I_{IL}\|$ | $\overline{RESET}$, SCK, $\overline{INT}$, SI, SO, $OSC_1$ | — | — | 1 | μA | $V_{in}$ = 0 V to $V_{CC}$ | 1 |
| Current dissipation in active mode | $I_{CC}$ | $V_{CC}$ | — | — | 4.2 | mA | $V_{CC}$ = 5 V, $f_{OSC}$ = 4 MHz | 2, 5 |
| | | | — | — | 1 | mA | $V_{CC}$ = 3 V, $f_{OSC}$ = 1 MHz | 2, 5 |
| | $I_{CMP}$ | $V_{CC}$ | — | — | 6.5 | mA | $V_{CC}$ = 5 V, $f_{OSC}$ = 4 MHz, comparator active | 3, 5 |
| | | | — | — | 1.6 | mA | $V_{CC}$ = 3 V, $f_{OSC}$ = 1 MHz comparator active | 3, 5 |
| Current dissipation in standby mode | $I_{SBY}$ | $V_{CC}$ | — | — | 2 | mA | $V_{CC}$ = 5 V, $f_{OSC}$ = 4 MHz | 4, 5 |
| | | | — | — | 0.5 | mA | $V_{CC}$ = 3 V, $f_{OSC}$ = 1 MHz | 4, 5 |
| Current dissipation in stop mode | $I_{STOP}$ | $V_{CC}$ | — | — | 10 | μA | $V_{in(\overline{RESET})}$ = $V_{CC}$ – 0.3 V to $V_{CC}$ $V_{in(TEST)}$ = 0 V to 0.3 V | |
| Stop mode retaining voltage | $V_{STOP}$ | $V_{CC}$ | 2 | — | — | V | | |

Notes on next page.

**DC Characteristics ($V_{CC}$ = 2.7 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C) (cont)**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IHA}$ | $COMP_0$, $COMP_1$ | $VC_{ref}$ + 0.1 | — | — | V | | |
| Input low voltage | $V_{ILA}$ | $COMP_0$, $COMP_1$ | 0 | — | $VC_{ref}$ – 0.1 | V | | |
| Comparator input reference voltage scope | $VC_{ref}$ | $V_{ref}$ | 0 | — | $V_{CC}$ – 1.2 | V | | |
| Deviation of internal reference voltage | $V_{OFS}$ | — | –0.1 | — | 0.1 | V | $V_{CC}$ = 4.5 V to 5.5 V | 6 |

Notes:
1. Excluding output buffer current and pull-up MOS current.
2. $I_{CC}$ is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$ at GND, TEST at GND
   $D_0$ to $D_{13}$, R1, R2 at $V_{CC}$
3. $I_{CMP}$ is the source current when no I/O current is flowing while the MCU comparator is in operation.
   Test conditions: MCU: Comparator active
   Pins: $\overline{RESET}$ at $V_{CC}$, TEST at GND
   $D_0$ to $D_8$, $D_{12}$, $D_{13}$, R1, R2 at $V_{CC}$
   $D_9$ to $D_{11}$ at GND
4. $I_{SBY}$ is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions: MCU: I/O same as at reset
   Standby mode
   Pins: $\overline{RESET}$ at $V_{CC}$, TEST at GND
   $D_0$ to $D_{13}$, R1, R2 at $V_{CC}$
5. Power dissipation is in proportion to $f_{OSC}$ while the MCU is operating or is in standby mode. The value of the dissipation current when $f_{OSC}$ = x MHz is given by the following equation:
   Maximum value ($f_{OSC}$ = x MHz) = x/4 × maximum value ($f_{OSC}$ = 4 MHz)
6. The reference voltage is the expected internal $VC_{ref}$ voltage selected by the reference voltage select register (RSR).
   Example: When RSR = $1, the reference voltage is 2/11 × $V_{CC}$.

**Input/Output Characteristics ($V_{CC}$ = 2.7 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C)**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | $D_0$–$D_{13}$, R1, R2 | $0.7V_{CC}$ | — | $V_{CC}$ + 0.3 | V | | |
| Input low voltage | $V_{IL}$ | $D_0$–$D_{13}$, R1, R2 | –0.3 | — | $0.3V_{CC}$ | V | | |
| Output low voltage | $V_{OL}$ | $D_0$–$D_{13}$, R1, R2 | — | — | 0.4 | V | $I_{OL}$ = 0.5 mA | |
| | | $D_{12}$, $D_{13}$, R1, R2 | — | — | 2 | V | $I_{OL}$ = 15 mA, $V_{CC}$ = 4.5 V to 5.5 V | |
| Input/output leakage current | $\|I_{IL}\|$ | $D_0$–$D_{13}$, R1, R2 | — | — | 1 | μA | $V_{in}$ = 0 V to $V_{CC}$ | 1 |
| Pull-up MOS current | $-I_{PU}$ | $D_0$–$D_{13}$, R1, R2 | 40 | 80 | 160 | μA | $V_{CC}$ = 5 V, $V_{in}$ = 0 V | |
| | | | 10 | 25 | 60 | μA | $V_{CC}$ = 3 V, $V_{in}$ = 0 V | |

Note: 1. Excluding output buffer current and pull-up MOS current.

**AC Characteristics ($V_{CC}$ = 2.7 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C)**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Oscillation frequency (ceramic oscillator) | $f_{OSC}$ | $OSC_1$, $OSC_2$ | 1 | 4 | 4.5 | MHz | $V_{CC}$ = 3.5 V to 5.5 V | |
| | | | 0.4 | 1 | 1.125 | MHz | $V_{CC}$ = 2.7 V to 3.5 V | |
| Instruction cycle time (ceramic oscillator) | $t_{cyc}$ | — | 0.89 | 1 | 4 | µs | $V_{CC}$ = 3.5 V to 5.5 V divided by 4 | |
| | | | 3.55 | 4 | 10 | µs | $V_{CC}$ = 2.7 V to 3.5 V divided by 4 | |
| Oscillator stabilization time (ceramic oscillator) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 20 | ms | | 1 |
| Oscillation frequency (resistor oscillator) | $f_{OSC}$ | $OSC_1$, $OSC_2$ | 1 | — | 3 | MHz | $V_{CC}$ = 3.5 V to 5.5 V $R_f$ = 20 kΩ ± 1% | |
| Instruction cycle time (resistor oscillator) | $t_{cyc}$ | — | 1.33 | — | 4 | µs | $V_{CC}$ = 3.5 V to 5.5 V divided by 4 | |
| Oscillator stabilization time (resistor oscillator) | $t_{RC}$ | $OSC_1$, $OSC_2$ | — | — | 0.5 | ms | $V_{CC}$ = 3.5 V to 5.5 V | |
| Capacitance between pins | $C_{RF}$ | $OSC_1$, $OSC_2$ | — | — | 1 | pF | $V_{CC}$ = 3.5 V to 5.5 V | |
| External clock high and low widths | $t_{CPH}$, $t_{CPL}$ | $OSC_1$ | 92 | — | — | ns | $V_{CC}$ = 3.5 V to 5.5 V | 2 |
| | | | 425 | — | — | ns | $V_{CC}$ = 2.7 V to 3.5 V | 2 |
| External clock rise time | $t_{CPr}$ | $OSC_1$ | — | — | 20 | ns | | 2 |
| External clock fall time | $t_{CPf}$ | $OSC_1$ | — | — | 20 | ns | | 2 |
| $\overline{INT}$ high width | $t_{IH}$ | $\overline{INT}$ | 2 | — | — | $t_{cyc}$ | | 3 |
| $\overline{INT}$ low width | $t_{IL}$ | $\overline{INT}$ | 2 | — | — | $t_{cyc}$ | | 3 |
| $\overline{RESET}$ low width | $t_{RSTL}$ | $\overline{RESET}$ | 2 | — | — | $t_{cyc}$ | | 4 |
| $\overline{RESET}$ rise time | $t_{RSTr}$ | $\overline{RESET}$ | — | — | 20 | ms | | 4 |
| Input capacitance | $C_{in}$ | TEST | — | — | 180 | pF | f = 1 MHz, $V_{in}$ = 0 V, $T_a$ = 25°C | |
| | | Others | — | — | 15 | pF | | |
| Comparator stabilization time | $t_{CSTB}$ | $COMP_0$ | — | — | 2 | $t_{cyc}$ | | |

Notes: 1. The oscillator stabilization time is the period from when $V_{CC}$ reaches its minimum allowable voltage (3.5 V) at power-on to when the oscillator stabilizes, or after $\overline{RESET}$ goes low. At power-on or stop mode release, $\overline{RESET}$ must be kept low for at least $t_{RC}$. Since $t_{RC}$ depends on the ceramic oscillator's circuit constant and stray capacitance, consult with the ceramic oscillator manufacturer when designing the reset circuit.
2. Refer to figure 29.
3. Refer to figure 30.
4. Refer to figure 31.

**Serial Interface Timing Characteristics ($V_{CC}$ = 2.7 V to 5.5 V, GND = 0 V, $T_a$ = –20°C to +75°C)**

**During Transmit Clock Output**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | Load shown in figure 33 | 1 |
| Transmit clock high and low widths | $t_{SCKH}$, $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | Load shown in figure 33 | 1 |
| Transmit clock rise and fall times | $t_{SCKr}$, $t_{SCKf}$ | $\overline{SCK}$ | — | — | 100 | ns | $V_{CC}$ = 3.5 V to 5.5 V, load shown in figure 33 | 1 |
| | | | — | — | 300 | ns | $V_{CC}$ = 2.7 V to 3.5 V, load shown in figure 33 | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 250 | ns | $V_{CC}$ = 3.5 V to 5.5 V, load shown in figure 33 | 1 |
| | | | — | — | 600 | ns | $V_{CC}$ = 2.7 V to 3.5 V, load shown in figure 33 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 300 | — | — | ns | $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | 1000 | — | — | ns | $V_{CC}$ = 2.7 V to 3.5 V | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 150 | — | — | ns | $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | 500 | — | — | ns | $V_{CC}$ = 2.7 V to 3.5 V | 1 |

**During Transmit Clock Input**

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Note |
|---|---|---|---|---|---|---|---|---|
| Transmit clock cycle time | $t_{Scyc}$ | $\overline{SCK}$ | 1 | — | — | $t_{cyc}$ | | 1 |
| Transmit clock high and low widths | $t_{SCKH}$, $t_{SCKL}$ | $\overline{SCK}$ | 0.4 | — | — | $t_{Scyc}$ | | 1 |
| Transmit clock rise and fall times | $t_{SCKr}$, $t_{SCKf}$ | $\overline{SCK}$ | — | — | 100 | ns | $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | — | — | 300 | ns | $V_{CC}$ = 2.7 V to 3.5 V | 1 |
| Serial output data delay time | $t_{DSO}$ | SO | — | — | 250 | ns | $V_{CC}$ = 3.5 V to 5.5 V, load shown in figure 33 | 1 |
| | | | — | — | 600 | ns | $V_{CC}$ = 2.7 V to 3.5 V, load shown in figure 33 | 1 |
| Serial input data setup time | $t_{SSI}$ | SI | 300 | — | — | ns | $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | 1000 | — | — | ns | $V_{CC}$ = 2.7 V to 3.5 V | 1 |
| Serial input data hold time | $t_{HSI}$ | SI | 150 | — | — | ns | $V_{CC}$ = 3.5 V to 5.5 V | 1 |
| | | | 500 | — | — | ns | $V_{CC}$ = 2.7 V to 3.5 V | 1 |

Note: 1. Refer to figure 32.

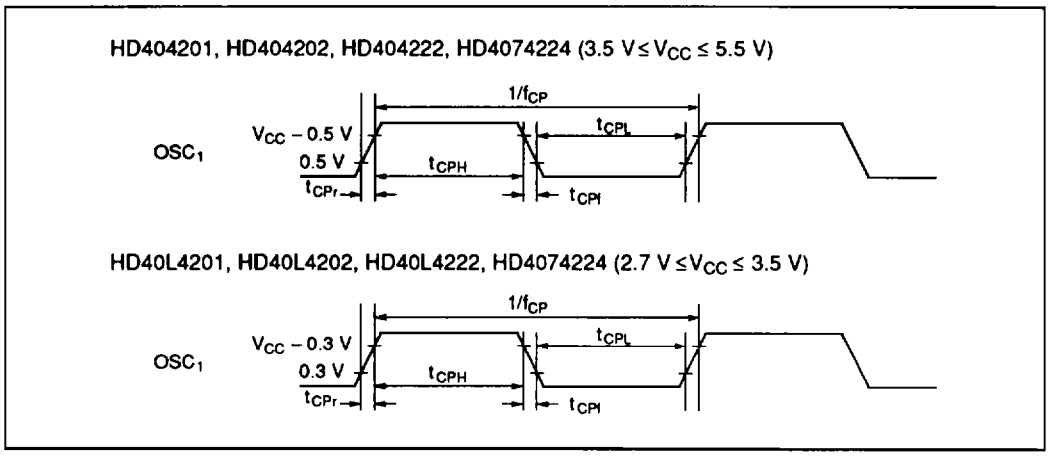



**Figure 29 External Clock Timing**

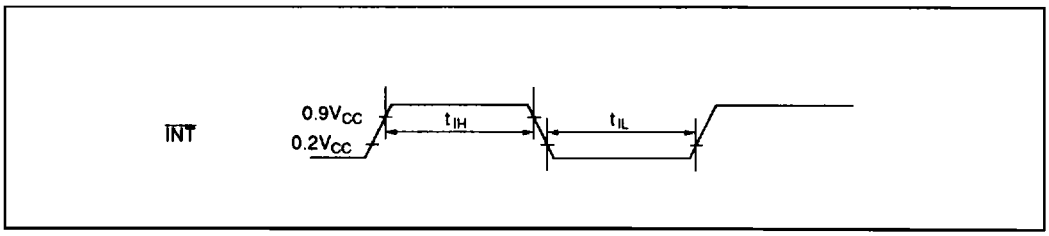



**Figure 30 Interrupt Timing**

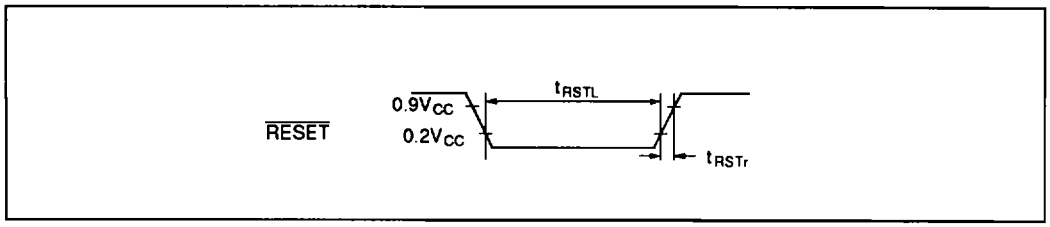
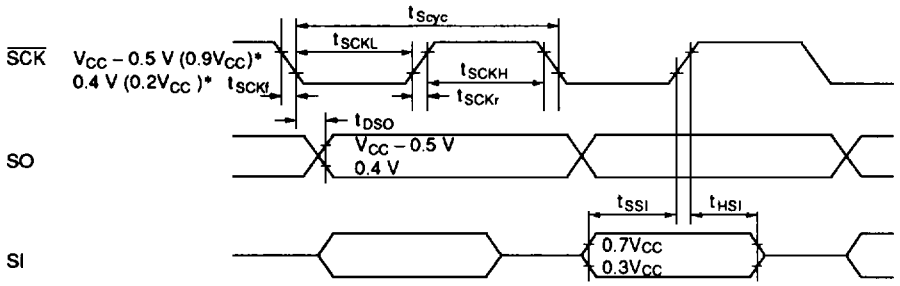
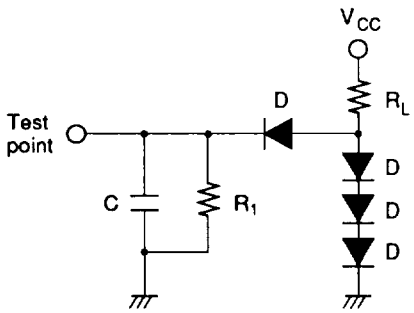



**Figure 31 $\overline{\text{RESET}}$ Timing**




Note: * $V_{CC}$ – 0.5 V and 0.4 V are the threshold voltages for transmit clock output.
0.9$V_{CC}$ and 0.2$V_{CC}$ are the threshold voltages for transmit clock input.

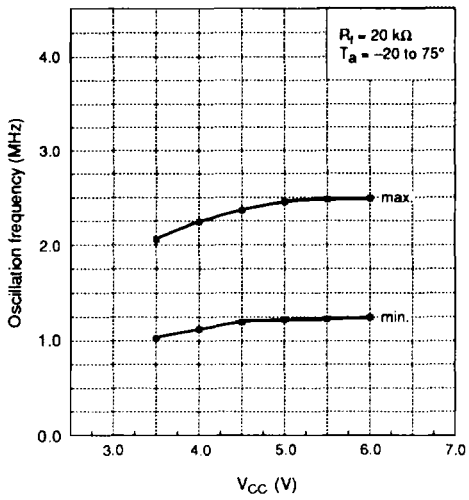
**Figure 32 Serial Interface Timing**



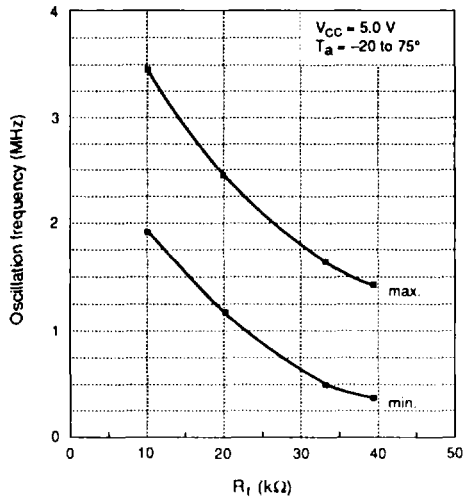

D: 1S2074Ⓗ
$R_L$: 2.6 kΩ
$R_1$: 12 kΩ
C: 30 pF

**Figure 33 Timing Load Circuit**

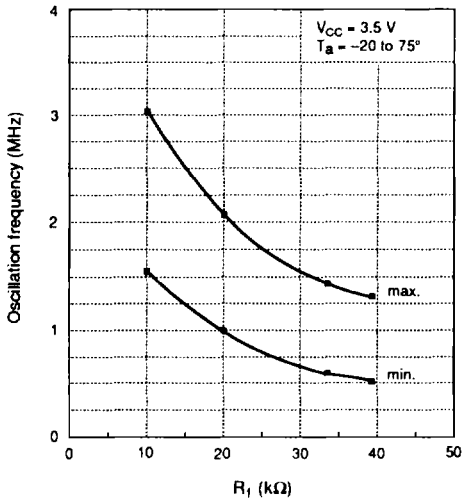
## Electrical Characteristics (Reference data)



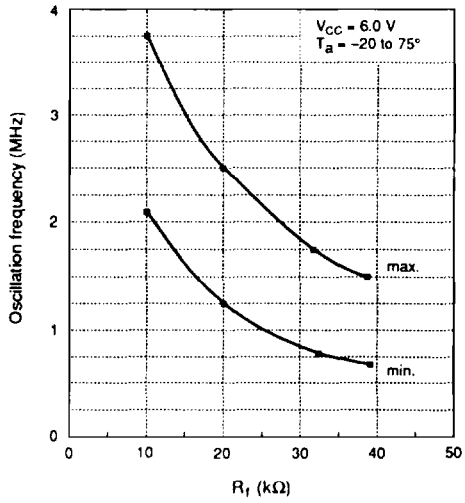

Resistor oscillator characteristics (1)
Oscillator frequency v.s. $V_{CC}$ ($R_f$ = 20 kΩ)




Resistor oscillator characteristics (2)
Oscillator frequency v.s. $R_f$ ($V_{CC}$ = 5.0 V)




Resistor oscillator characteristics (3)
Oscillator frequency v.s. $R_f$ ($V_{CC}$ = 3.5 V)



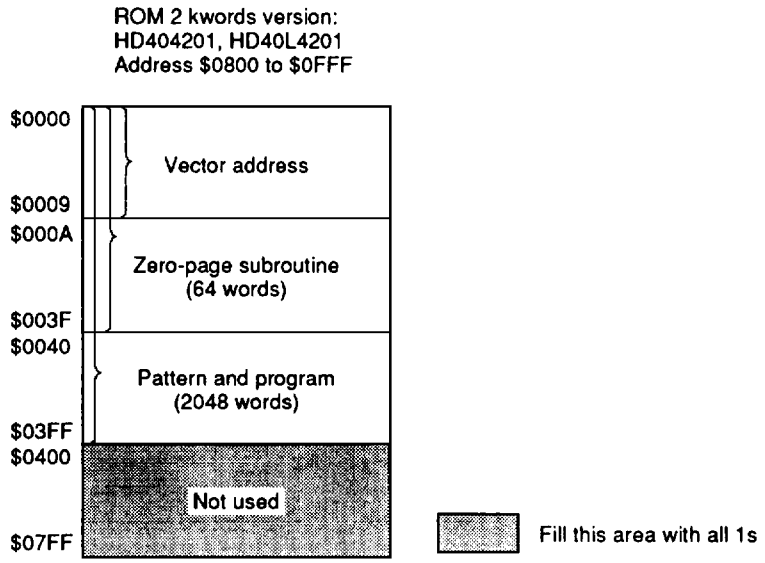

Resistor oscillator characteristics (4)
Oscillator frequency v.s. $R_f$ ($V_{CC}$ = 6.0 V)

## Notes On ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as 2-kword versions (HD404202, HD40L4202). A 2-kword data size is required to change ROM data to mask manufacturing data since the program used is for a 2-kword version.

This limitation apply to the case of using EPROM and the case of using data base.



# HD404201/HD40L4201/HD404202/HD40L4202 Option List

Please check off the appropriate applications and enter the necessary information.

| | |
|---|---|
| Order date | |
| Customer name | |
| Department | |
| Name | |
| ROM code name | |
| LSI type name | |

## 1. ROM Size

| | |
|---|---|
| ☐ 5-V operation: HD404201 | 1-kword |
| ☐ Low-voltage operation: HD40L4201 | |
| ☐ 5-V operation: HD404202 | 2-kword |
| ☐ Low-voltage operation: HD40L4202 | |

## 2. I/O Options

A: Without pull-up MOS (open-drain NMOS); B: With pull-up MOS; C: CMOS (cannot be used as input)

| Pin name | I/O | I/O option | | |
|---|---|---|---|---|
| | | A | B | C |
| D0 | I/O | | | |
| D1 | I/O | | | |
| D2 | I/O | | | |
| D3 | I/O | | | |
| D4 | I/O | | | |
| D5 | I/O | | | |
| D6 | I/O | | | |
| D7 | I/O | | | |
| D8 | I/O | | | |
| D9 | I/O | | | |
| D10 | I/O | | | |

| Pin name | | I/O | I/O option | | |
|---|---|---|---|---|---|
| | | | A | B | C |
| D11 | | I/O | | | |
| D12 | | I/O | | | |
| D13 | | I/O | | | |
| R1 | R10 | I/O | | | |
| | R11 | I/O | | | |
| | R12 | I/O | | | |
| | R13 | I/O | | | |
| R2 | R20 | I/O | | | |
| | R21 | I/O | | | |
| | R22 | I/O | | | |
| | R23 | I/O | | | |

## 3. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

| |
|---|
| ☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...). |
| ☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS. |

## 4. System Oscillator (OSC1 and OSC2)

| HD404201/HD404202 | | | HD40L4201/HD40L4202 | | |
|---|---|---|---|---|---|
| ☐ External clock | f = | MHz | ☐ External clock | f = | MHz |
| ☐ Resistor | f = | MHz | | | |
| ☐ Ceramic oscillator | f = | MHz | ☐ Ceramic oscillator | f = | MHz |

## 5. Stop Mode

| |
|---|
| ☐ Used |
| ☐ Not used |

## 6. Package

| |
|---|
| ☐ DP-28S |
| ☐ FP-28DA |
| ☐ FP-30D |

# HD404222/HD40L4222 Option List

Please check off the appropriate applications and enter the necessary information.

| | |
|---|---|
| Order date | |
| Customer name | |
| Department | |
| Name | |
| ROM code name | |
| LSI type name | |

## 1. ROM Size

| |
|---|
| ☐ 5-V operation: HD404222 |
| ☐ Low-voltage operation: HD40L4222 |

## 2. I/O Options

A: Without pull-up MOS (open-drain NMOS); B: With pull-up MOS; C: CMOS (cannot be used as input)

| Pin name | I/O | I/O option | | |
|---|---|---|---|---|
| | | A | B | C |
| D0 | I/O | | | |
| D1 | I/O | | | |
| D2 | I/O | | | |
| D3 | I/O | | | |
| D4 | I/O | | | |
| D5 | I/O | | | |
| D6 | I/O | | | |
| D7 | I/O | | | |
| D8 | I/O | | | |
| D9 | I/O | | | |
| D10 | I/O | | | |

| Pin name | | I/O | I/O option | | |
|---|---|---|---|---|---|
| | | | A | B | C |
| D11 | | I/O | | | |
| D12 | | I/O | | | |
| D13 | | I/O | | | |
| R1 | R10 | I/O | | | |
| | R11 | I/O | | | |
| | R12 | I/O | | | |
| | R13 | I/O | | | |
| R2 | R20 | I/O | | | |
| | R21 | I/O | | | |
| | R22 | I/O | | | |
| | R23 | I/O | | | |

## 3. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

| |
|---|
| ☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...). |
| ☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS. |

## 4. System Oscillator (OSC1 and OSC2)

| HD404222 | | | HD40L4222 | | |
|---|---|---|---|---|---|
| ☐ External clock | f = | MHz | ☐ External clock | f = | MHz |
| ☐ Resistor | f = | MHz | | | |
| ☐ Ceramic oscillator | f = | MHz | ☐ Ceramic oscillator | f = | MHz |

## 5. Timer A

| |
|---|
| ☐ Free-running timer operation |
| ☐ Watchdog timer operation |

## 6. Stop Mode

| |
|---|
| ☐ Used |
| ☐ Not used |

## 7. Package

| |
|---|
| ☐ DP-28S |
| ☐ FP-28DA |
| ☐ FP-30D |