

***TLV320AIC12KEVM,  
TLV320AIC14KEVM***

*User's Guide*

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

## EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. **THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.**

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

**EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.**

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265

## **EVM WARNINGS AND RESTRICTIONS**

It is important to operate this EVM with a maximum input supply voltage not exceeding 4 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

### **Mailing Address:**

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265

# Read This First

---

---

---

---

### ***About This Manual***

This users guide describes the operation and use of the TLV320AIC12K codec family. A complete circuit description, schematic diagram, and bill of materials are also included.

### ***How to Use This Manual***

This document contains the following chapters:

- Chapter 1—EVM Overview
- Chapter 2—Digital Interface
- Chapter 3—Analog Interface
- Chapter 4—EVM Operation
- Chapter 5—TLV320AIC12KEVM/14KEVM Bill of Materials
- Appendix A—TLV320AIC12KEVM/14KEVM Schematic

### ***FCC Warning***

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

**Related Documentation From Texas Instruments**

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through our website at [www.ti.com](http://www.ti.com).

**Data Sheets:**

TLV320AIC12K  
TLV320AIC14K

**Literature Number:**

SLWS115  
SLWS115

# Contents

---

---

---

<b>1</b>	<b>EVM Overview</b> .....	<b>1-1</b>
<b>2</b>	<b>Digital Interface</b> .....	<b>2-1</b>
2.1	Codec-to-Platform .....	2-2
2.2	Jumper Options .....	2-4
2.2.1	Stand-Alone Slave .....	2-4
2.2.2	Single Master Only .....	2-5
2.2.3	Master/Slave Cascade .....	2-5
<b>3</b>	<b>Analog Interface</b> .....	<b>3-1</b>
<b>4</b>	<b>EVM Operation</b> .....	<b>4-1</b>
<b>5</b>	<b>TLV320AIC12KEVM/14KEVM Bill of Materials</b> .....	<b>5-1</b>
<b>6</b>	<b>TLV320AIC12KEVM/14KEVM Schematic</b> .....	<b>A-1</b>

# Figures

---

---

---

1-1	EVM .....	1-1
4-1	EVM Captured Signals .....	4-2

# Tables

---

---

---

2-1	Pinout for 40-Pin Connector .....	2-2
2-2	Jumper Options .....	2-4
2-3	Stand-Alone Slave Jumper Settings .....	2-5
2-4	Single Master Only Jumper Settings .....	2-5
2-5	Master/Slave Cascade Jumper Settings .....	2-5
3-1	Analog Interface Connectors .....	3-1



# EVM Overview

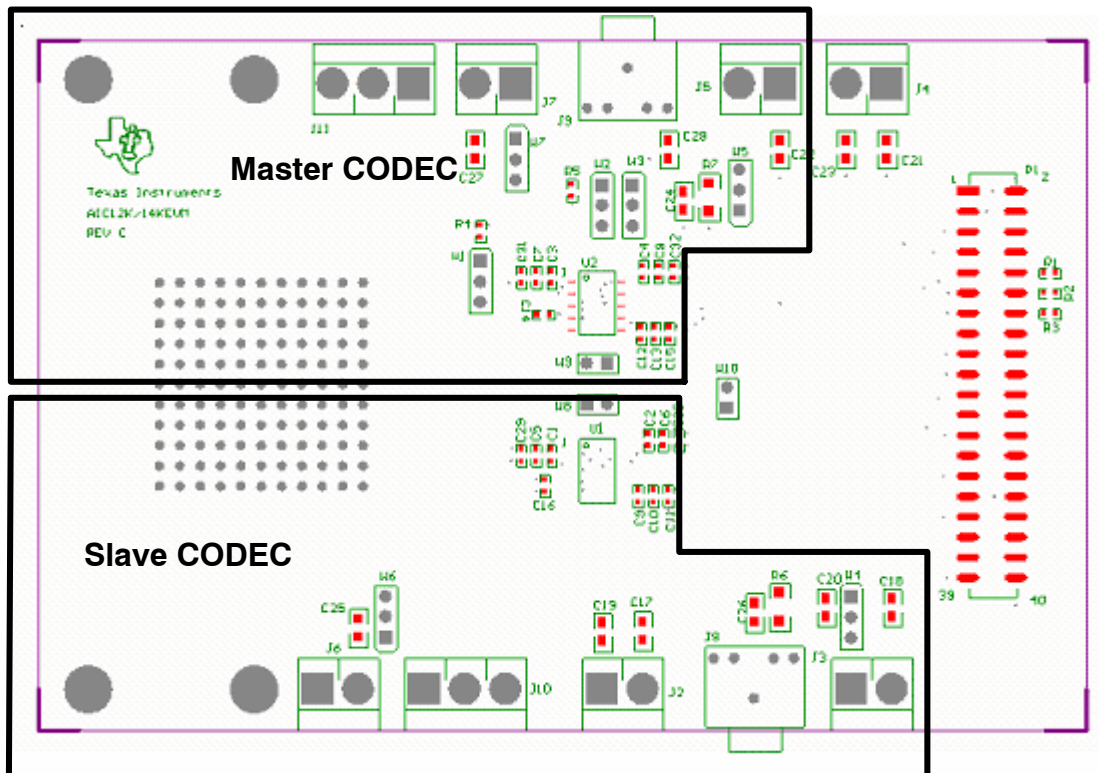
This user's guide supports the following devices:

- TLV320AIC12K
- TLV320AIC14K

This guide refers to the TLV320AIC12K only, since the remaining device feature set is a subset of the TLV320AIC12K. Any important differences are noted.

Figure 1-1. EVM

The EVM is split into two complementary halves as shown in Figure 1-1.





# Digital Interface

---

---

---

---

The digital signals required to operate this codec originate from the 40-pin connector—J1. There are two methods to drive the digital interface:

- Create a custom interface between the codec EVM and the host system.
- Alternatively, if a TI DSK (DSP starter kit) is the host system, a development platform is available from TI. This platform provides the additional functions that the codec requires in a convenient form factor.

<b>Topic</b>	<b>Page</b>
<b>2.1 Codec-to-Platform</b> .....	<b>2-2</b>
<b>2.2 Jumper Options</b> .....	<b>2-4</b>

## 2.1 Codec-to-Platform

The TLV320AIC12K, and 14K mate with the development platform via a 40-pin Samtec connector. The mating connector (Samtec part number, TSM-120-01-T-DV-P) is used on the development platform to provide the electrical connections necessary. Consult Samtec at [www.samtec.com](http://www.samtec.com) or 1-800-SAMTEC-9 for more information.

The pinout for the 40-pin connector is listed in Table 2-1.

Table 2-1. Pinout for 40-Pin Connector

Pin Number	Signal	Description
J1.1	MCLK	Master clock
J1.2	DGND	Digital ground
J1.3	SCLK	Serial data clock
J1.4	DGND	Digital ground
J1.5	DIN	Data in
J1.6	DGND	Digital ground
J1.7	DOUT	Data out
J1.8	Reserved	Reserved for future use
J1.9	FS	Frame sync
J1.10	Reserved	Reserved for future use
J1.11	CLKX	Transmit clock
J1.12	Reserved	Reserved for future use
J1.13	FSX	Frame sync transmit
J1.14	Reserved	Reserved for future use
J1.15	DX	Data transmit
J1.16	DR	Data receive
J1.17	RESET	Global reset for all devices
J1.18	FSR	Frame sync receive
J1.19	PWDN	Global powerdown for all devices
J1.20	CLKR	Receive clock
J1.21	CNTLb	GPIO pin
J1.22	CNTLa	GPIO pin
J1.23	STATb	Status pin
J1.24	STATa	Status pin
J1.25	3.3V_D	Digital 3.3 V
J1.26	Reserved	Reserved for future use
J1.27	3.3V_D	Digital 3.3 V
J1.28	DGND	Digital ground
J1.29	1.8V_D	Digital 1.8 V
J1.30	DGND	Digital ground
J1.31	1.8V_D	Digital 1.8 V
J1.32	DGND	Digital ground

Table 2–1. Pinout for 40-Pin Connector (Continued)

Pin Number	Signal	Description
J1.33	3.3V_A_DRV	Output driver supply 3.3 V
J1.34	AGND	Analog ground
J1.35	3.3V_A_DRV	Output driver supply 3.3 V
J1.36	AGND	Analog ground
J1.37	3.3V_A	Analog 3.3 V
J1.38	AGND	Analog ground
J1.39	3.3V_A	Analog 3.3 V
J1.40	AGND	Analog ground

The development platform supports a number of functions that the codecs require. These are:

- MCLK generation
- Manual reset generation
- Power options

Refer to the *DSP – Codec Development Platform User's Guide* (SLAU090) for details regarding the development platform.

Further descriptions regarding the operation of this EVM assumes that the development platform is being used for all additional signals and power.

## 2.2 Jumper Options

There are various jumpers on the board that can be configured in various ways, depending upon the user's requirements. Their functions are briefly presented in Table 2–2:

Table 2–2. Jumper Options

Jumper	Function
W1	Selects whether U2 is either a master or a slave codec
W2	Used along with W2 for correct polarity for FSD
W3	Manages FSD from the master. Either connecting FSD to next co- dec or providing relevant polarity.
W4	Source for INM1b
W5	Source for INM1a
W6	Coupling for OUP1b. Either directly or via capacitor.
W7	Coupling for OUP1a. Either directly or via capacitor.
W8	Connects analog and digital ground together
W9	Gives user the option of disconnecting the 3.3-V driver ground from the regular analog ground
W10	Use for odd number codec channels. Isolate the data from the co- dec not participating in the chain.
P1.9–P1.10	Last FSD in the chain must be high
P1.11–P1.12	SCL must be high
P1.13–P1.14	SDA must be high

Since the EVM contains two codecs, there a variety of options available to the user:

- Stand-alone slave codec
- Single master codec
- Master/slave cascade

Each of these options are discussed in the following sections.

### 2.2.1 Stand-Alone Slave

This configuration applies to EVM1 only. When a single codec is to be used in slave mode, U2 is always the slave codec. Follow the jumper settings detailed in Table 2–3 for this condition.

Table 2–3. Stand-Alone Slave Jumper Settings

Jumper	1–2	2–3
W1	Not inserted	Inserted
W2	Inserted	Not inserted
W3	Inserted	Not inserted
W4	Not inserted	Inserted
P1.9–P1.10	N/A	N/A
P1.11–P1.12	Inserted	Inserted
P1.13–P1.14	Inserted	Inserted

### 2.2.2 Single Master Only

This configuration applies to EVM1 only. When a single codec is to be used in master mode, U2 is always the master codec. Follow the jumper settings detailed in Table 2–4 for this condition.

Table 2–4. Single Master Only Jumper Settings

Jumper	1–2	2–3
W2	Inserted	Not inserted
W3	Inserted	Not inserted
W4	Inserted	Not inserted
P1.9–P1.10	N/A	N/A
P1.11–P1.12	Inserted	Inserted
P1.13–P1.14	Inserted	Inserted

### 2.2.3 Master/Slave Cascade

This configuration applies to EVM1 only and is the factory-set shipping condition. When both codecs are used, both U1 and U2 are active. In this condition U2 is always the master codec, and U1 is always the slave codec. Follow the jumper settings detailed in Table 2–5.

Table 2–5. Master/Slave Cascade Jumper Settings

Jumper	1–2	2–3
W1	Inserted	Not inserted
W2	N/A	N/A
W3	Not inserted	Inserted
W4	Inserted	Inserted
P1.9–P1.10	Inserted	Inserted
P1.11–P1.12	Inserted	Inserted
P1.13–P1.14	Inserted	Inserted

# Analog Interface

Table 3–1 indicates the applicable connectors for each codec in the family. In order to enable a wide range of sources and loads to be connected to the codecs, screw terminals have been used wherever possible.

*Table 3–1. Analog Interface Connectors*

	TLV320AIC12K		TLV320AIC14K	
	Master	Slave	Master	Slave
<b>Input Sources</b>				
Microphone input	J9	J8	J9	J8
INP1	J5	J3	J5	J3
INP2	J4	J2	J4	J2
<b>Output Loads</b>				
OUTP1/OUTM1 600-Ω line output	J7	J6	J7	J6
OUTP2/OUTP3 16-Ω driver output	J11	J10	NA	





# EVM Operation

---

---

---

---

The EVM is shipped from the factory in master/slave cascade mode. To check if the EVM is working properly, simply install the EVM onto the development platform, and apply power to the DSK. The EVM should begin working immediately.

In the default mode, the codecs recognize that there are two channels connected in the master/slave configuration, consequently the resultant SCLK and FS signals transmitted by the master codec adjust automatically based on the available MCLK.

It is now possible to calculate what should be observed after power up by calculating what FS and SCLK should be observed:

FS

- In this example, MCLK is generated by the development platform and is equal to 100 MHz.
- $FS = MCLK / 16 \times m \times n \times p$
- Default values for m, n, and p are 16, 6, and 8 respectively
- $FS = 100 \times 10^6 / 16 \times 16 \times 6 \times 8$
- $FS = 8138 \text{ Hz}$

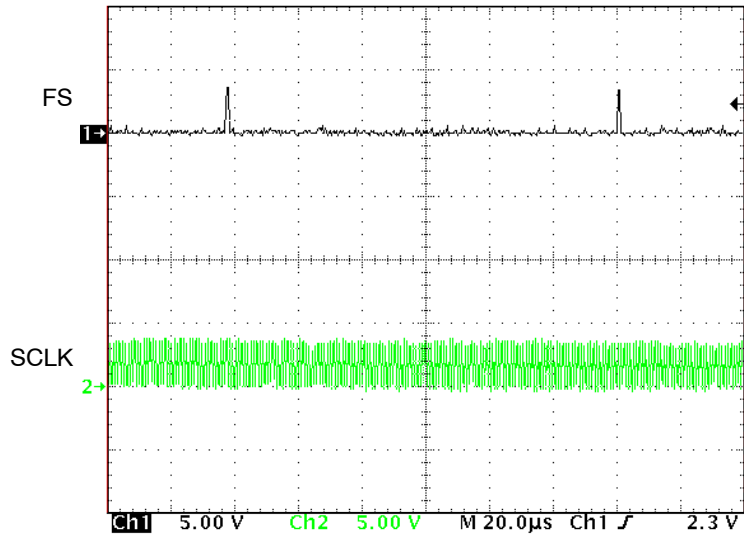
SCLK

- $SCLK = 16 \times FS \times (\text{number of devices}) \times \text{mode}$
- $SCLK = 16 \times 8138 \times 2 \times 1$
- $SCLK = 260 \text{ kHz}$

FS can be observed either directly at the FS pin of U1 or U2 (pin 4) or on the development platform at TP9. SCLK can be observed easily at P1 pin 3 of the EVM or on the development platform at TP8.

The captured signals are shown in Figure 4-1.

Figure 4-1. EVM Captured Signals



# TLV320AIC12K/14K Bill of Materials

The following table contains a complete bill of materials for the TLV320AIC12K/14K family of EVMs. The schematic diagram is also provided for reference. Contact the Product Information Center or e-mail [dataconvapps@list.ti.com](mailto:dataconvapps@list.ti.com) for questions regarding this EVM.

Used	Value	Ref Des	Description	Vendor	Part number
4	0.01 $\mu$ F	C29 C30 C31 C32	Capacitor 10000-pF 50-V ceramic Y5V 0603	Panasonic	ECJ-1VF1H103Z
12	0.1 $\mu$ F	C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16	Capacitor 0.1- $\mu$ F 25-V ceramic Y5V 0603	Panasonic	ECJ-1VF1E104Z
16	0.1 $\mu$ F	C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28	Capacitor 0.1- $\mu$ F 50-V ceramic X7R 0805	Panasonic	ECJ-2YB1H104K
4	1 $\mu$ F	C1 C2 C3 C4	Capacitor 1- $\mu$ F 10-V ceramic Y5V 0603	Panasonic	ECJ-1VF1A105Z
5	10 k $\Omega$	R1 R2 R3 R4 R5	Resistor 10-k $\Omega$ 1/16-W 5% 0603 SMD	Panasonic	ERJ-3GEYJ103V
2	10 k $\Omega$	R6 R7	Resistor 10.0-k $\Omega$ 1/8-W 1% 1206 SMD	Panasonic	ERJ-8ENF1002V
2		U1 U2 *	IC CODEC 1CH 16-bit 3.3-V 30 TSSOP	Texas Instruments	TLV320AIC12KIDBT
	* Alternate		IC CODEC 1CH 16-bit 3.3-V 30 TSSOP	Texas Instruments	TLV320AIC14KIDBT
1			TLV320AIC12 PWB	Texas Instruments	6435621
1		J1	40-Pin SMT socket	Samtec	SSW-120-22-F-D-VS-K
1		P1	40-Pin SMT plug	Samtec	TSM-120-01-T-DV-P
6		J2 J3 J4 J5 J6 J7	2 Terminal screw connector	Lumberg	KRMZ2
2		J10 J11	3 Terminal screw connector	Lumberg	KRMZ3
2		J8 J9	161-3504	Mouser	161-3504
3		W8 W9 W10	2 Position jumper	Samtec	TSW-102-07-L-S
7		W1 W2 W3 W4 W5 W6 W7	3-Position jumper	Samtec	TSW-103-07-L-S
2		See Assy Dwg	1.000/4-40 Nylon hex thread SP	Keystone Electronics	1902E

---

Used	Value	Ref Des	Description	Vendor	Part number
2		See Assy Dwg	0.500/4-40 Nylon hex thread SP	Keystone Electronics	1902C
2		See Assy Dwg	4-40 X 1/4 Machine screw PH SS	Building Fasteners	PMSSS 440 0025 PH

# **TLV320AIC12K/14K EVM Schematic**

---

---

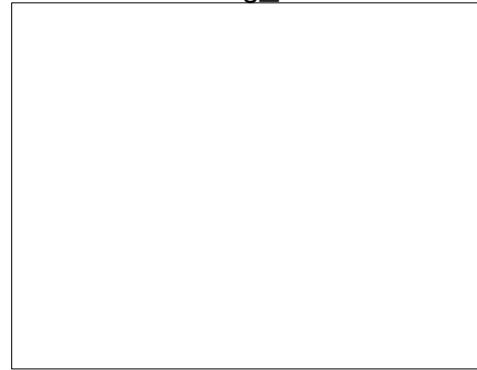
---

---

The TLV320AIC12K/14K EVM schematics are provided on the following pages.

Revision History		
REV	ECN Number	Approved

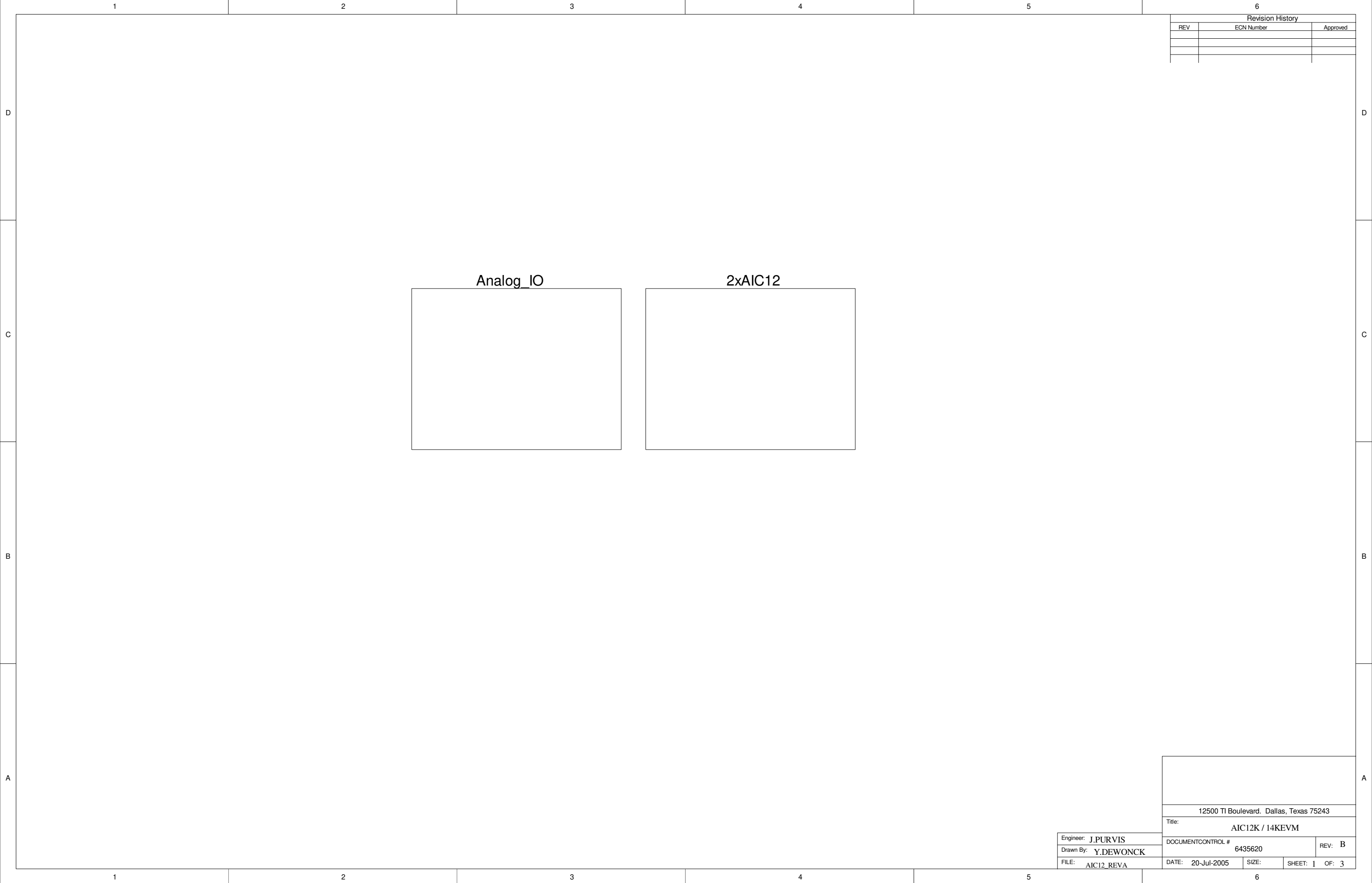
Analog\_IO



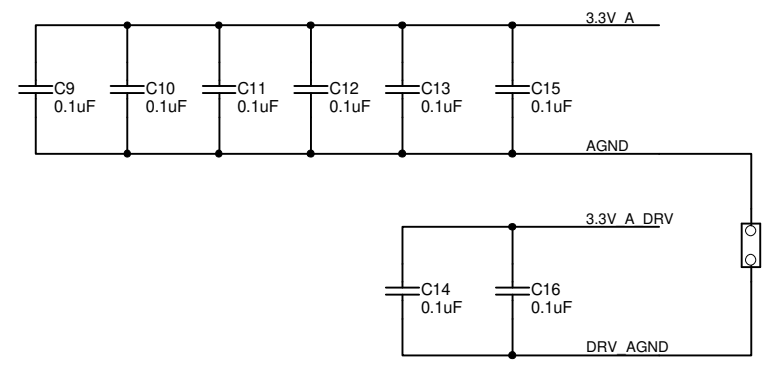
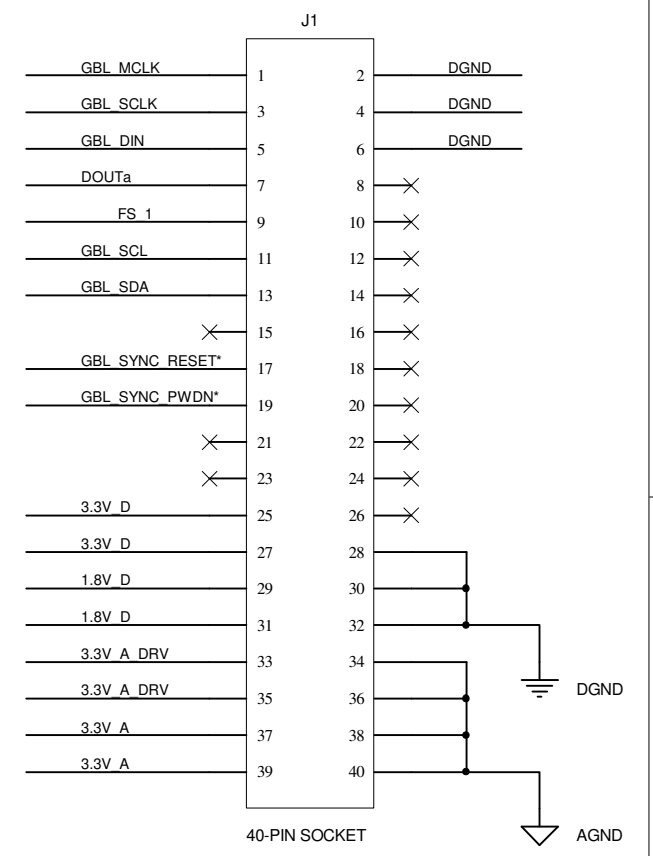
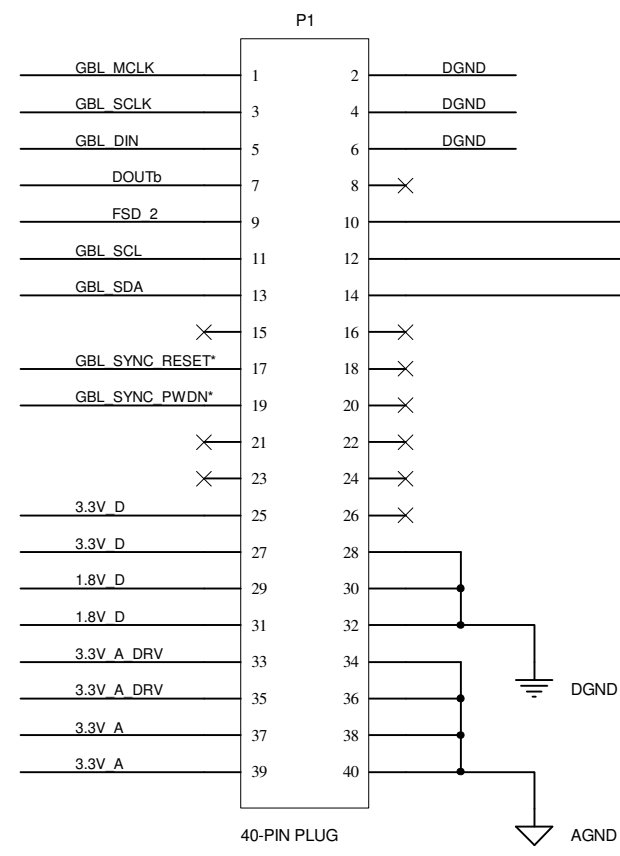
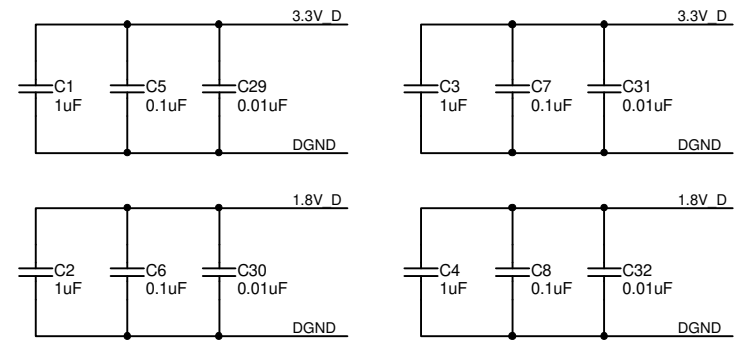
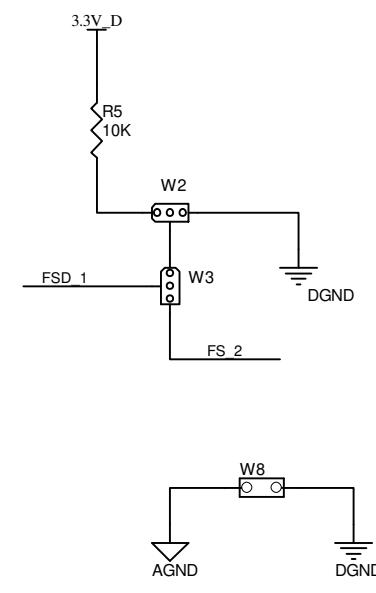
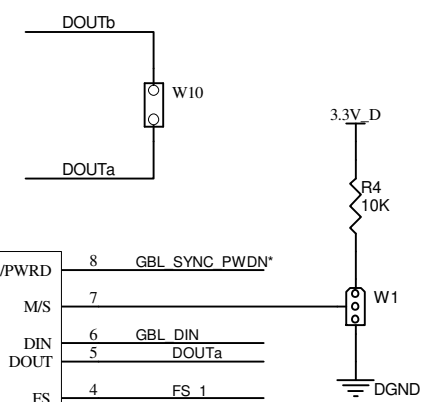
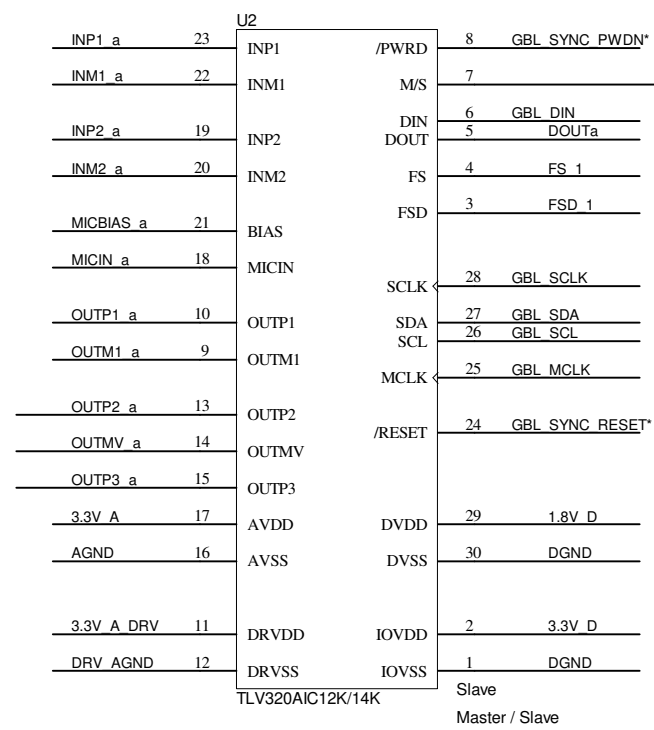
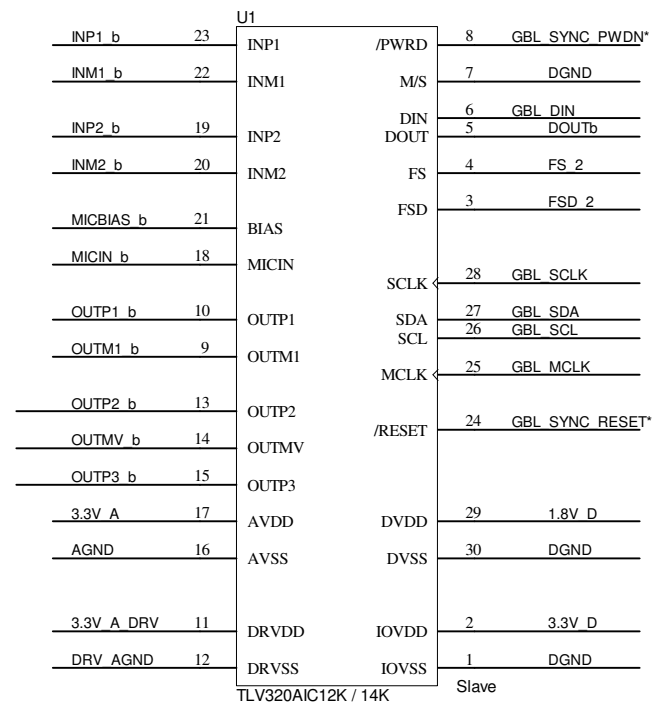
2xAIC12



12500 TI Boulevard. Dallas, Texas 75243	
Title: AIC12K / 14KEVM	
Engineer: J.PURVIS	DOCUMENTCONTROL # 6435620
Drawn By: Y.DEWONCK	REV: B
FILE: AIC12_REVA	DATE: 20-Jul-2005
SIZE:	SHEET: 1 OF: 3



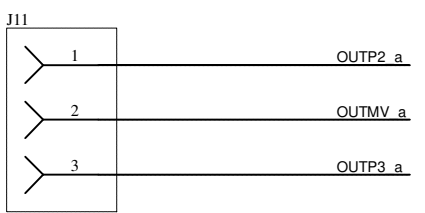
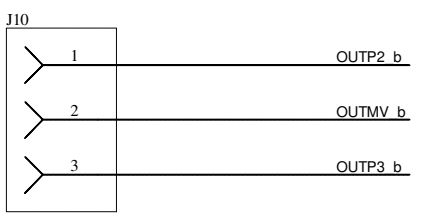
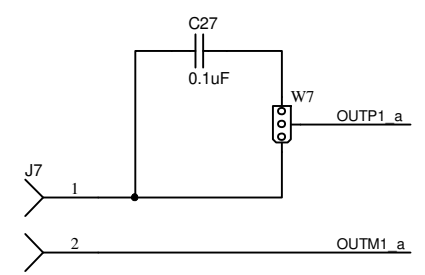
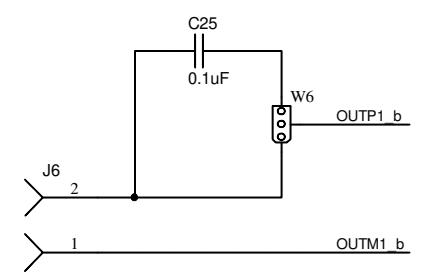
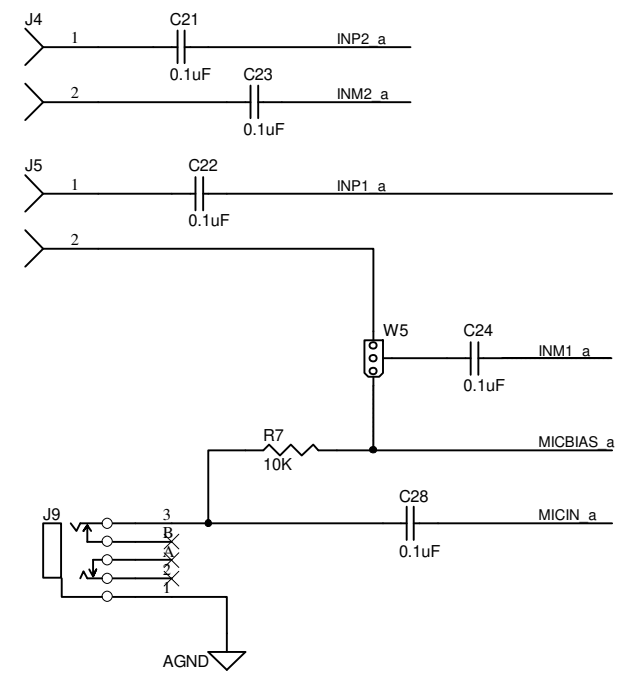
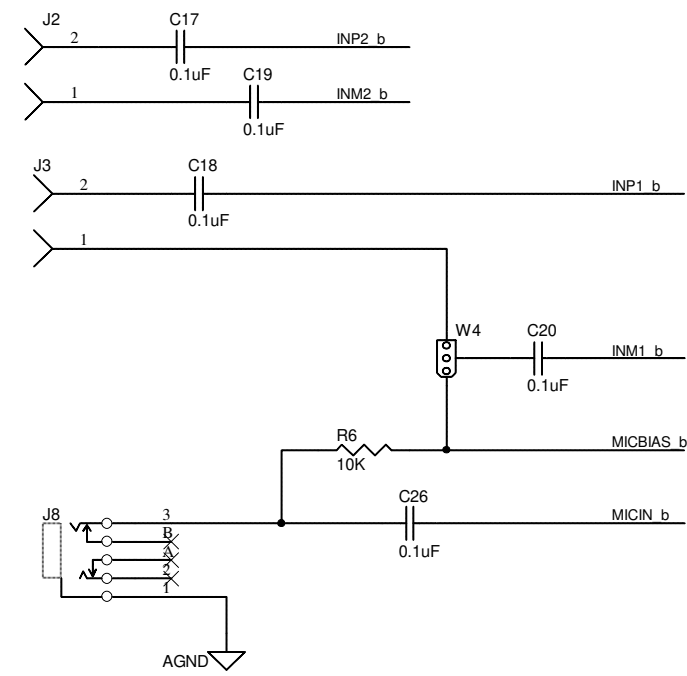
Revision History		
REV	ECN Number	Approved



12500 TI Boulevard, Dallas, Texas 75243		
Title: AIC12K/14KEVM		
Engineer: J.PURVIS	DOCUMENTCONTROL # 6435620	REV: B
Drawn By: Y.DEWONCK	DATE: 20 Jul-2005	SIZE: 6 OF: 3
FILE: 2xAIC12	SHEET: 2	OF: 3



Revision History		
REV	ECN Number	Approved



12500 TI Boulevard, Dallas, Texas 75243		
Title: AIC12K / 14KEVM		
Engineer: J.PURVIS	DOCUMENTCONTROL # 6435620	REV: B
Drawn By: Y.DEWONCK	DATE: 20-Jul-2005	SIZE: 6 SHEET: 3 OF: 3
FILE: Analog_IO		