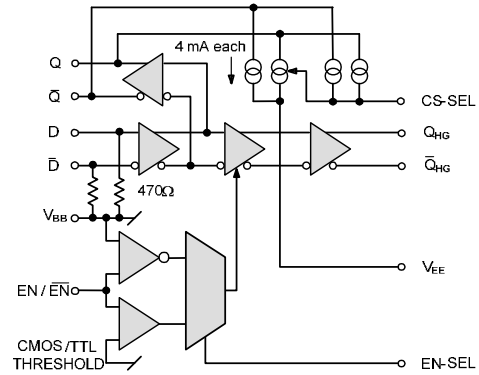


**FEATURES**

- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS or PECL)
- 3V to 5.5V Power Supply
- Similar Operation as CTS100LVEL16VT Except with LVDS Outputs

**BLOCK DIAGRAM**



**DESCRIPTION**

The CTSLV399 is a specialized oscillator gain stage with an LVDS output buffer including an enable. The selectable enable input allows continuous oscillator operation by only controlling the Q<sub>HG</sub> / Q<sub>HG</sub> outputs.

The CTSLV399 provides adjustable internal pull-down current sources for the Q/Q outputs. Internal input biasing further reduces the number of needed external components

**ENGINEERING NOTES**

The CTSLV399 is a specialized oscillator gain stage with LVDS output buffer including an enable. The enable input (EN) allows continuous oscillator operation by only controlling the Q<sub>HG</sub> / Q<sub>HG</sub> outputs. The CTSLV399 also provides a V<sub>BB</sub> and 470Ω internal bias resistors from D to V<sub>BB</sub> and D-bar to V<sub>BB</sub>. The V<sub>BB</sub> pin can support 1.5 mA sink/source current. Bypassing V<sub>BB</sub> to ground with a 0.01 μF capacitor is recommended.

**Functionality MLP8 Package (CTSLV399NG)**

The MLP8, NG options of the CTSLV399, provide a PECL/ECL level enable input (EN-bar). When the EN-bar input is LOW, the Q and Q<sub>HG</sub> / Q<sub>HG</sub> outputs pass data from the inputs. When EN-bar is HIGH, the Q output continues to pass data while the Q<sub>HG</sub> output is forced high and the Q<sub>HG</sub> output is forced low.

Only the Q-bar output operates with a current source (4 mA) to V<sub>EE</sub>. This is accomplished by internal bonding of CS-SEL. An external resistor may also be used to increase pull-down current to a maximum of 25mA (includes 4mA on-chip current source).

The CTSLV399NB and CTSLV399ND versions operate with a single ended data input (D). The D-bar input is internally bonded directly to the V<sub>BB</sub> pin bypassing the 470Ω bias resistor.

**Functionality MLP8 Package (CTSLV399N) & MSOP8 Package (CTSLV399T)**

The MSOP8 (T) and MLP8 (N) versions of the CTSLV399 provide a CMOS/TTL level enable input (EN). When the EN input is HIGH, the Q and Q<sub>HG</sub> / Q<sub>HG</sub> outputs pass data from the inputs. When EN is LOW, the Q output continues to pass data while the Q<sub>HG</sub> output is forced high and the Q<sub>HG</sub> output is forced low.

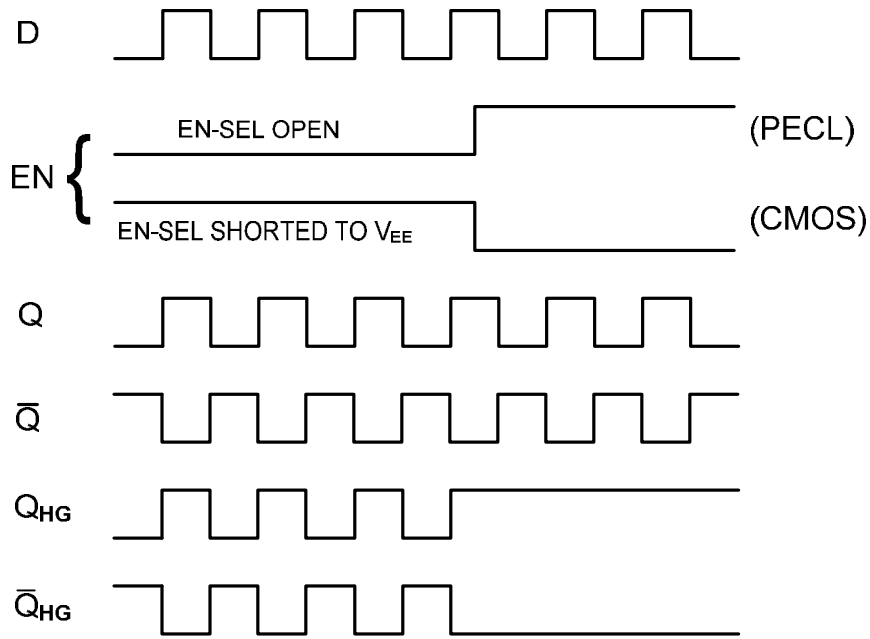
Only the Q-bar output operates with a current source (4 mA) to V<sub>EE</sub>. This is accomplished by internal bonding of CS-SEL. An external resistor may also be used to increase pull-down current to a maximum of 25mA (includes 4mA on-chip current source).

The MSOP8 (T) and MLP8 (N) CTSLV399 operates with a single ended data input (D). The D-bar input is internally bonded directly to the V<sub>RR</sub> pin bypassing the 470Ω bias resistor.

**Enable Truth Table**

EN-SEL	EN/ $\overline{\text{EN}}$	Q/ $\overline{\text{Q}}$	Q <sub>HG</sub>	$\overline{\text{Q}}_{\text{HG}}$
NC	PECL Low, V <sub>EE</sub> or NC	Data	Data	Data
	PECL High or V <sub>CC</sub>	Data	High	Low
V <sub>EE</sub> <sup>1</sup>	CMOS/TTL Low, V <sub>EE</sub> or NC	Data	High	Low
	CMOS/TTL High or V <sub>CC</sub> <sup>2</sup>	Data	Data	Data

- 1 EN-SEL connections must be less than 1Ω.
- 2 An external ≤ 20kΩ pull-up resistor between EN and V<sub>CC</sub> ensures a High when the EN pin is not driven.

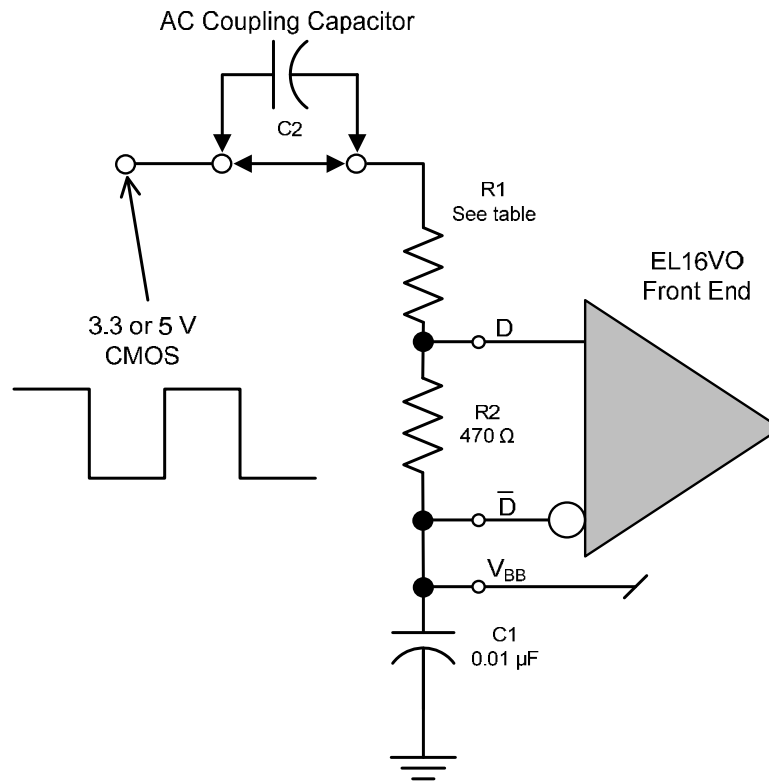


**Timing Diagram**

**Current Source Truth Table**

CS-SEL	Q	$\overline{\text{Q}}$
NC	4mA typ	4mA typ
V <sub>EE</sub> <sup>1</sup>	8mA typ	8mA typ
V <sub>CC</sub> <sup>1</sup>	0	4mA typ

<sup>1</sup> Connection must be less than 1Ω.



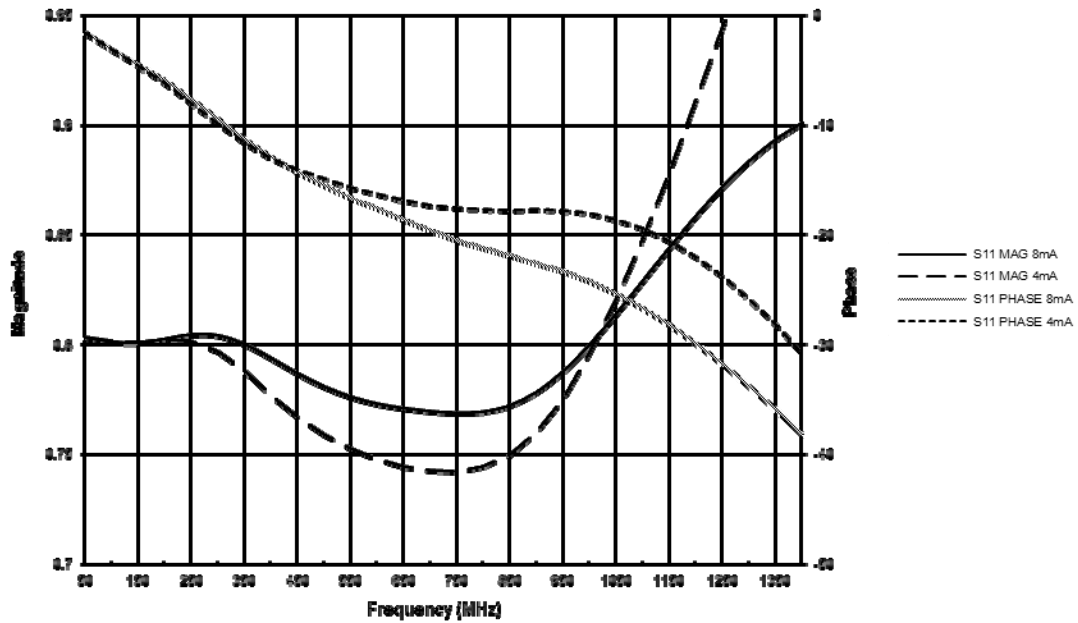
**Application Circuit for CMOS inputs**

**Recommended Component Values for CMOS Single Ended Inputs**

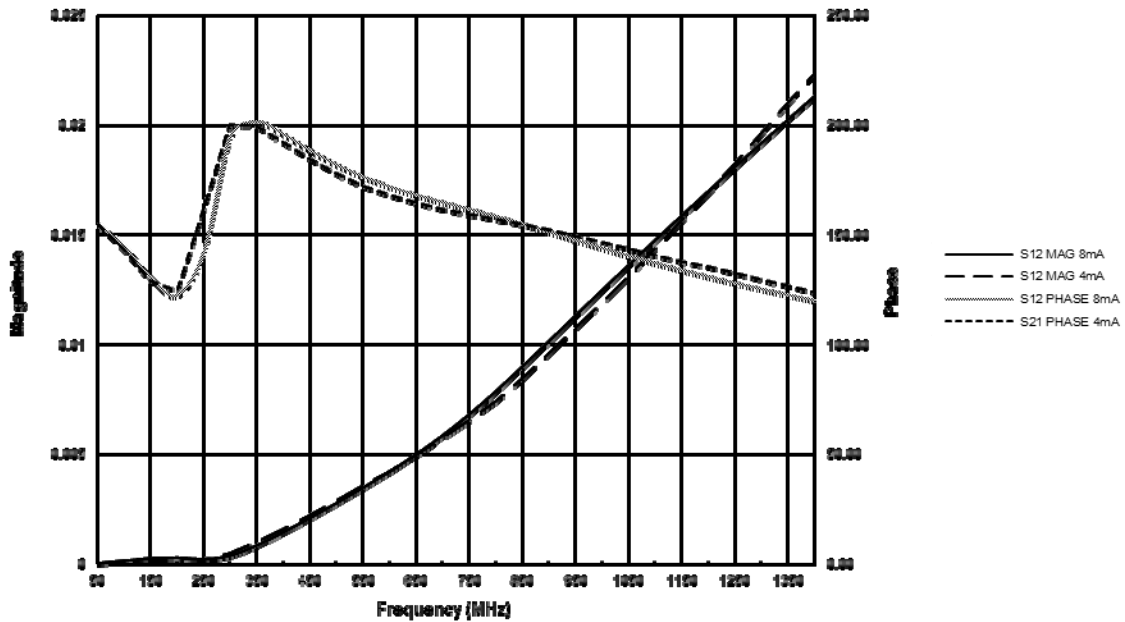
Input Type	R1 <sup>1</sup> Value	
	AC Coupled (C2 in circuit)	DC Coupled (C2 shorted)
3.3 V CMOS	1.1 kΩ	2.0 kΩ
5.0 V CMOS	1.6 kΩ	3.3 kΩ

R1 should be chosen so that the input swing on the D input with respect to  $\bar{D}$  is in the range of  $\pm 80$  to  $\pm 1000$  mV, per the AC Characteristics table and the D input is  $< \pm 750$  mV with respect to  $V_{BB}$ .

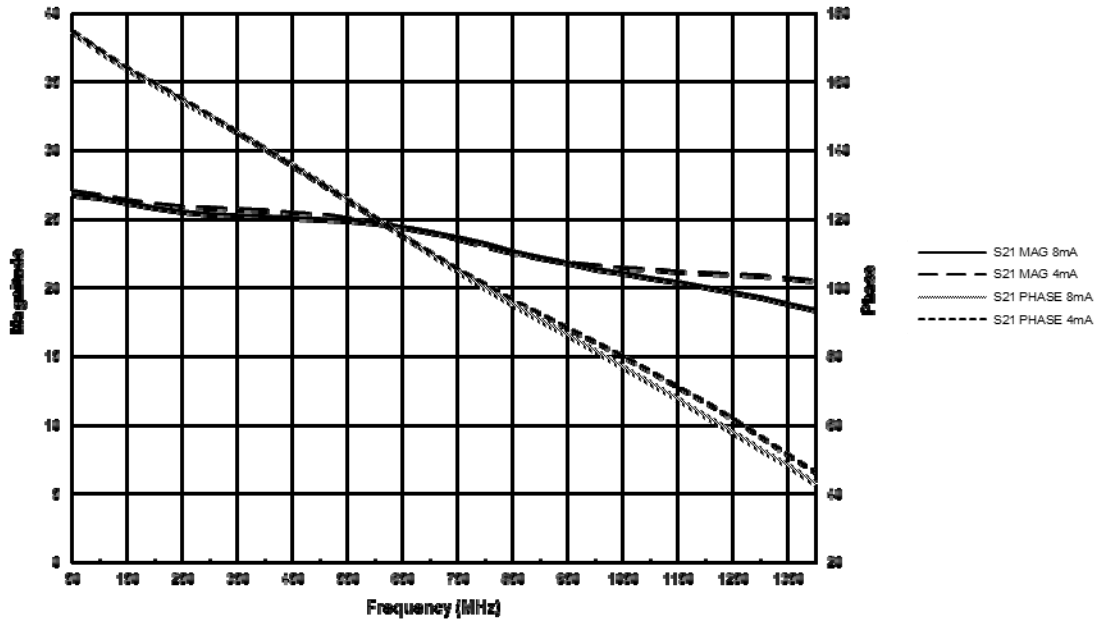
Not recommended for new designs



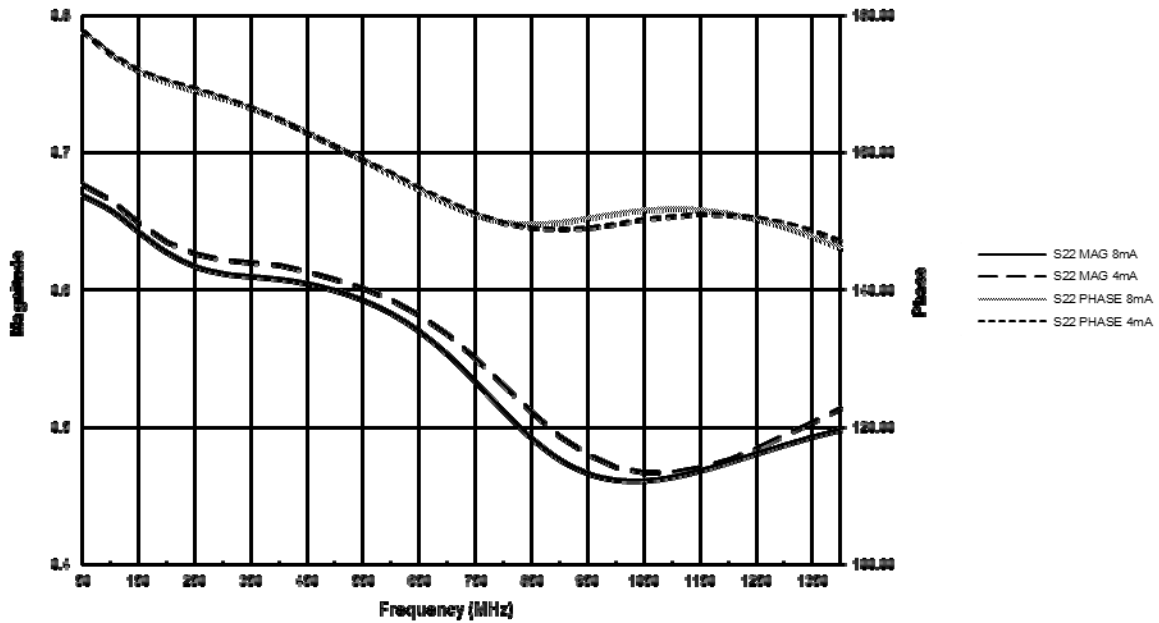
S11, 50Ω AC load



S12, 50Ω AC load



S21, 50Ω AC load



S22, 50Ω AC load

## Electrical Specifications

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
$V_{CC}$	PECL Power Supply	$V_{EE} = 0V$	0 to + 6.0	V
$V_I$	PECL Input Voltage	$V_{EE} = 0V$	0 to + 6.0	V
$V_{D/I}$	D/ $\bar{D}$ Input Voltage	Referenced to $V_{BB}$	$\pm 0.75$	V
$I_{OUT}$	Output Current	Continuous Q/ $\bar{Q}$	25	mA
		Surge Q/ $\bar{Q}$	50	
		Continuous $Q_{HG}/\bar{Q}_{HG}$	5	
		Surge $Q_{HG}/\bar{Q}_{HG}$	10	
$T_A$	Operating Temperature Range	-	-40 to +85	$^{\circ}C$
$T_{STG}$	Storage Temperature Range	-	-65 to +150	$^{\circ}C$
$ESD_{HBM}$	Human Body Model Electro Static Discharge	-	2500	V
$ESD_{MM}$	Machine Model Electro Static Discharge	-	200	V
$ESD_{CDM}$	Charged Device Model Electro Static Discharge	-	2000	V

### 100K LVPECL DC Characteristics ( $V_{EE} = GND, V_{CC} = +3.3V$ )

Symbol	Characteristic	-40 $^{\circ}C$		0 $^{\circ}C$		25 $^{\circ}C$		85 $^{\circ}C$		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage <sup>1,2</sup>	2255	2465	2275	2465	2275	2465	2275	2465	mV
$V_{OL}$	Output LOW Voltage <sup>1,2</sup>	1375	1745	1400	1680	1400	1680	1400	1680	mV
$V_{IH}$	Input HIGH Voltage D,EN (EN-SEL open) <sup>1</sup>	2135	2560	2135	2560	2135	2560	2135	2560	mV
	Input HIGH Voltage EN (EN-SEL tied to $V_{EE}$ ) <sup>1</sup>	2000	$V_{CC}$	2000	$V_{CC}$	2000	$V_{CC}$	2000	$V_{CC}$	mV
$V_{IL}$	Input LOW Voltage D,EN (EN-SEL open) <sup>1</sup>	1400	1825	1400	1825	1400	1825	1400	1825	mV
	Input LOW Voltage EN (EN-SEL tied to $V_{EE}$ ) <sup>1</sup>	GND	800	GND	800	GND	800	GND	800	mV
$V_{BB}$	Reference Voltage <sup>1</sup>	1910	2050	1910	2050	1910	2050	1910	2050	mV
$I_{IH}$	Input HIGH Current EN <sup>3</sup>		150		150		150		150	$\mu A$
$I_{IL}$	Input LOW Current EN <sup>3</sup>	0.5		0.5		0.5		0.5		$\mu A$
$I_{EE}$	Power Supply Current <sup>2</sup>		48		48		48		48	mA

<sup>1</sup> Voltage levels vary 1:1 with  $V_{CC}$ .

<sup>2</sup> Specified with CS-SEL open.

<sup>3</sup> Specified with EN-SEL open.

**100K PECL DC Characteristics (V<sub>EE</sub> = GND, V<sub>CC</sub> = +5.0V)**

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage <sup>1,2</sup>	3955	4165	3975	4165	3975	4165	3975	4165	mV
V <sub>OL</sub>	Output LOW Voltage <sup>1,2</sup>	3075	3445	3100	3380	3100	3380	3100	3380	mV
V <sub>IH</sub>	Input HIGH Voltage D,EN (EN-SEL open) <sup>1</sup>	3835	4260	3835	4260	3835	4260	3835	4260	mV
	Input HIGH Voltage EN (EN-SEL tied to V <sub>EE</sub> ) <sup>1</sup>	2000	V <sub>CC</sub>	2000	V <sub>CC</sub>	2000	V <sub>CC</sub>	2000	V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage D,EN (EN-SEL open) <sup>1</sup>	3100	3525	3100	3525	3100	3525	3100	3525	mV
	Input LOW Voltage EN (EN-SEL tied to V <sub>EE</sub> ) <sup>1</sup>	GND	800	GND	800	GND	800	GND	800	mV
V <sub>BB</sub>	Reference Voltage <sup>1</sup>	3610	3750	3610	3750	3610	3750	3610	3750	mV
I <sub>IH</sub>	Input HIGH Current EN <sup>3</sup>		150		150		150		150	μA
I <sub>IL</sub>	Input LOW Current EN <sup>3</sup>	0.5		0.5		0.5		0.5		μA
I <sub>EE</sub>	Power Supply Current <sup>2</sup>		48		48		48		52	mA

- 1 Voltage levels vary 1:1 with V<sub>CC</sub>.
- 2 Specified with CS-SEL open.
- 3 Specified with EN-SEL open.

**LVDS DC Characteristics for Q<sub>HG</sub>/ $\bar{Q}$ <sub>HG</sub> Outputs<sup>1</sup> (V<sub>EE</sub> = GND, V<sub>CC</sub> = +3.0V to +5.5V)**

Symbol	Characteristic	-40 C		0 C		25 C		85 C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage		1600		1600		1600		1600	mV
V <sub>OL</sub>	Output LOW Voltage	900		900		900		900		mV
V <sub>OC</sub>	Output Common Mode Voltage <sup>2</sup>	1125	1375	1125	1375	1125	1375	1125	1375	mV
V <sub>OC</sub>	Change in Common Mode Voltage <sup>3</sup>	-50	50	-50	50	-50	50	-50	50	mV
V <sub>OUT</sub>	Single-Ended Output Swing	250	450	250	450	250	450	250	450	mV
V <sub>DIFF_OUT</sub>	Differential Output Swing	500	900	500	900	500	900	500	900	mV

- 1 Specified with 100Ω resistor connecting Q<sub>HG</sub> and  $\bar{Q}$ <sub>HG</sub> together.
- 2 Common mode voltage is the center voltage between Q<sub>HG</sub> and  $\bar{Q}$ <sub>HG</sub> during a steady state.
- 3 Change in common mode voltage is the difference between common mode voltages at opposite binary states.

**AC Characteristics ( $V_{EE} = -3.0V$  to  $-5.5V$ ;  $V_{CC}=GND$  or  $V_{EE}=GND$ ;  $V_{CC} = +3.0V$  to  $+5.5V$ )**

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{PLH}/t_{PHL}$	Propagation Delay													
	D to $Q/\bar{Q}$ <sup>1</sup>			400			400			400			430	ps
	D to $Q_{HG}/\bar{Q}_{HG}$ <sup>2</sup>			550			550			550			630	ps
$t_{SKEW}$	Duty Cycle Skew <sup>3</sup>		5	20		5	20		5	20		5	20	ps
$V_{PP}$ (AC)	Input Swing <sup>4</sup>	80		1000	80		1000	80		1000	80		1000	mV
$t_r/t_f$	Output Rise/Fall <sup>1</sup> (20% - 80%) - Q	100		260	100		260	100		260	100		260	
	Output Rise/Fall <sup>1</sup> (20% - 80%) - $Q_{HG}$	180		280	180		280	180		280	180		280	ps

<sup>1</sup> Specified with CS-SEL connected to  $V_{EE}$  and  $Q/\bar{Q}$  with AC coupled 50Ω loads.

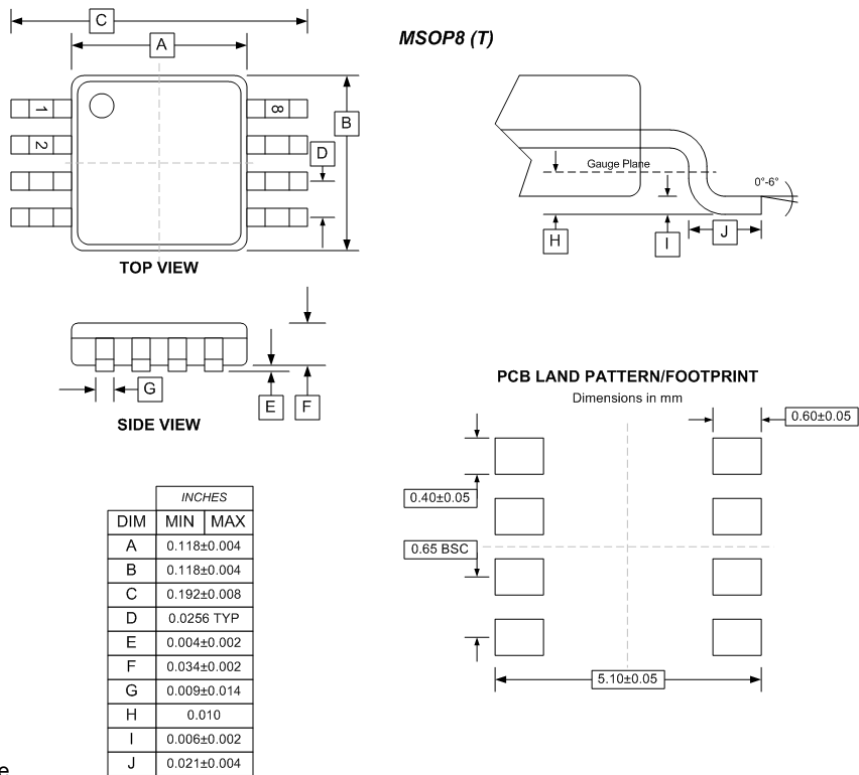
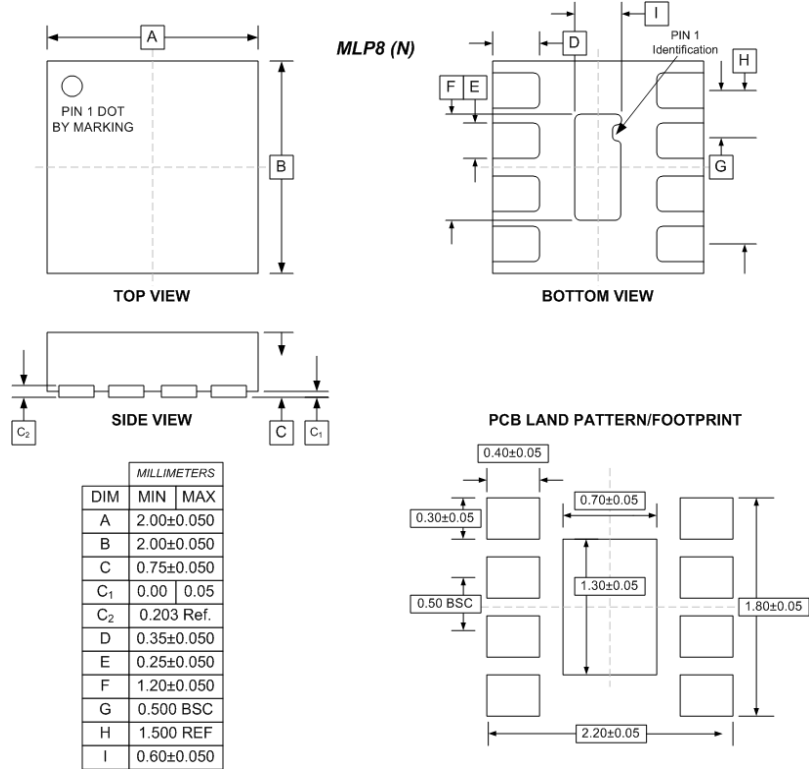
<sup>2</sup> Specified with 100Ω resistor connecting  $Q_{HG}$  and  $\bar{Q}_{HG}$  together.

<sup>3</sup> Duty cycle skew is the difference between a  $t_{PLH}$  and  $t_{PHL}$  propagation delay through a device.

<sup>4</sup> The peak-to-peak differential input swing is the range for which AC parameters guaranteed.  $V_D$  and  $V$  must remain within the range of  $\pm 750$  mV with respect to  $V_{BB}$ .



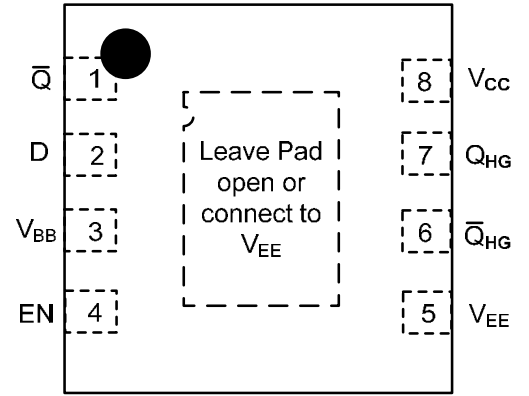
PACKAGE DIMENSIONS



**Pin Description and Configuration**

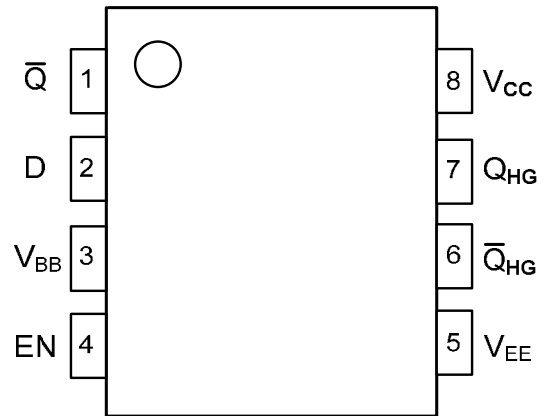
**Pin Assignments for CTSLV399NG**

Pin	Name	Type	Function
1	$\bar{Q}$	Output	Inverting PECL Output
2	D	Input	Data Input
3	$V_{BB}$	Output	Reference Voltage
4	EN	Input	Output Enable
5	$V_{EE}$	Power	Negative Supply
6	$\bar{Q}_{HG}$	Output	Inverting LVDS Output
7	$Q_{HG}$	Output	LVDS Output
8	$V_{CC}$	Power	Positive Supply



**Pin Assignments for CTSLV399TG**

Pin	Name	Type	Function
1	$\bar{Q}$	Output	Inverting PECL Output
2	D	Input	Data Input
3	$V_{BB}$	Output	Reference Voltage
4	EN	Input	Output Enable
5	$V_{EE}$	Power	Negative Supply
6	$\bar{Q}_{HG}$	Output	Inverting LVDS Output
7	$Q_{HG}$	Output	LVDS Output
8	$V_{CC}$	Power	Positive Supply



**PART ORDERING INFORMATION**

Part Number	Package	Marking
CTSLV399NG	MLP8	V1G / YWW
CTSLV399TG	MSOP8	HV99G / YYWW