User's Guide
SLDU019B–December 2015–Revised March 2016

PGA450Q1EVM-S User's Guide and TIDA-00151 UART Demo Instructional

The Texas Instruments PGA450-Q1 small form-factor evaluation module (EVM) allows users to evaluate the operation and performance of the PGA450-Q1 fully integrated system-on-chip analog front-end for ultrasonic sensing. The small form-factor layout of this EVM is equivalent to that of an end-product form factor, allowing users to easily integrate this PGA450-Q1-based sensor module into a real system without the need for additional prototypes.

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1 Introduction

The PGA450Q1EVM-S is a fully assembled PCB design for real-world evaluation of the PGA450-Q1 ultrasonic-sensor signal-conditioner device, an ultrasonic transducer, and step-up transformer. This EVM can be integrated with systems for general object detection and distance measurement through air, in applications such as automotive park-assist, level sensing in tanks, collision avoidance for autonomous robotics, and unmanned aerial vehicle landing assist. This small form-factor EVM is intended to act as an ultrasonic module alternative to the full-scale PGA450Q1EVM. TI recommends that the user first begins evaluation with the PGA450Q1EVM before transitioning to evaluation with the PGA450Q1EVM-S.

2 Setup and Operation

This section describes how to setup and configure the PGA450Q1EVM-S for basic operation. A detailed description of connectors, jumpers, and test points are provided in addition to the typical operation setup of the EVM. An example of operation is also included.

Figure 1 shows the PGA450Q1EVM-S pinout for the available input and output connectors.

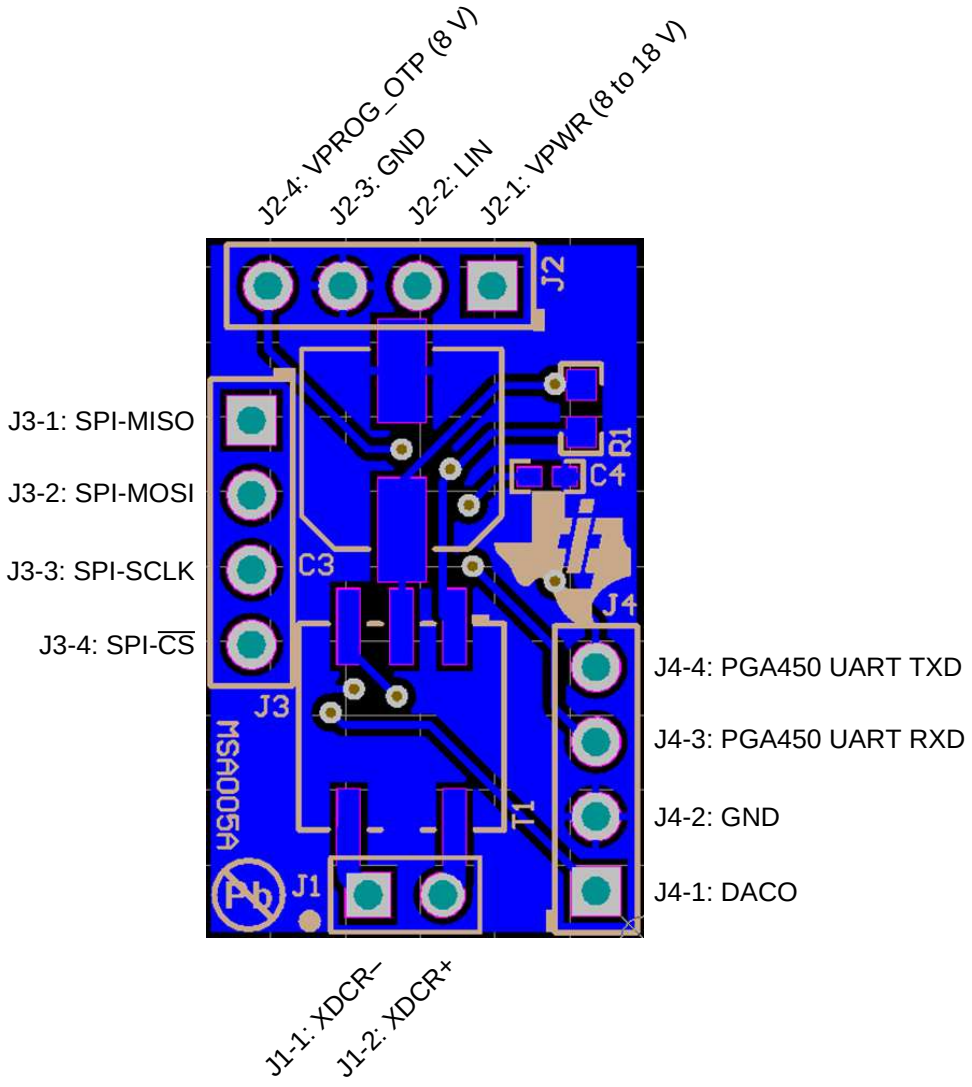


Figure 1. PGA460Q1EVM-S Pinout

2.1 Input and Output Connectors

The PGA450Q1EVM-S has two power connectors, three communication interfaces, and two outputs. Table 1 lists the connectors in addition to a function description which includes the electrical specifications.

Table 1. Terminal Descriptors

Terminal	Designator	Direction	Description
MAIN	J2-1	Input	Single-system power supply to the VPWR pin of the PGA450-Q1 device. This supply is rated at 7 to 18 V DC for powering the entire board.
LIN	J2-2	Input/Output	The PGA450-Q1 device implements the LIN 2.1 compliant physical layer. This physical layer can be used to communicate data between the PGA450-Q1 device and the master MCU.
GND	J2-3, J4-2	—	Ground terminal to complete the circuit.
VPROG	J2-4	Input	VPROG_OTP power supply input of 8 V for programming OTP memory of the PGA450-Q1 device.
SPI	J3	Input/Output	SPI is the communication that is required for use with the PGA450Q1EVM GUI and TI GER USB interface for programming the PGA450-Q1 device(1). The internal 8051W must be placed in reset to communicate using SPI.
UART	J4-3, J4-4	Input/Output	The TxD and RxD pins on the PGA450-Q1 device are connected to the 8051W UART. These two pins can be used either for software debugging or for implementing application-specific protocols.
DACO	J4-1	Output	Observe the echo signal as an amplified analog signal or from a DAC output which converts a digitally filtered echo signal. In the Evaluation tab of the GUI, the quick-access buttons, *Amplifier Output* (unfiltered) and *Datapath Output* (filtered), are available. The signal is viewable on the DACO pin. Only one mode can be selected at a time.
XDCR Connector	J1	Input/Output	The transducer (XDCR) connector is used to drive and listen for ultrasonic signals with an external transducer sensor element.

(1) The TI GER (Texas Instruments general equipment resource) USB interface board is included with the purchase of the PGA450Q1EVM, and cannot be purchased separately. Purchase the PGA450Q1EVM or develop a custom USB interface tool to program or evaluate the PGA450-Q1 device on the PGA450Q1EVM-S platform.

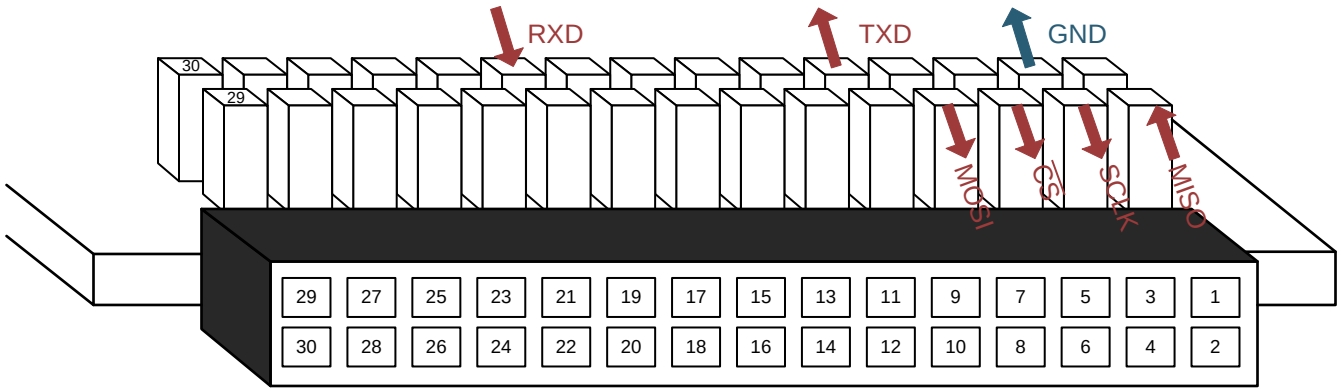
2.2 Basic Operation

The PGA450-Q1 device can operate from either OTP or DEVRAM memory, and from the LIN, UART, or SPI communication interfaces. Because of the various methods of operation, the configuration of OTP memory and UART communication for initial evaluation, development, and debug is used as the basic operation example throughout this document. To burst and capture an ultrasonic profile, the user must connect a 5-V logic-level compatible UART-to-USB interface device, and send the corresponding commands discussed in Section 2.3. The details of this section are limited to the minimum requirements because this user's guide assumes that the user has fully evaluated the PGA450Q1EVM, which provides more extensive and elaborate details.

2.2.1 Programming the PGA450-Q1 DEVRAM or OTP Memory

The PGA450Q1EVM-S memory is preprogrammed to operate from OTP memory, meaning that the PGA450-Q1 device is permanently programmed with a set of predefined commands as described in Section 2.3. If the user prefers to customize or modify the firmware for different commands, the PGA450-Q1 device must be replaced with a pristine PGA450-Q1 device, and follow the instructions provided in this section. Go to Section 2.3 if the device will not be replaced. Use the steps that follow to program the device for DEVRAM or OTP memory.

Step 1. Connect a 12-V system supply voltage to the EVM at J2-1 (MAIN) and connect the SPI pins of the EVM at J3 to the SPI pins on the TI GER board.



TI-GER Header and Ribbon Cable

Figure 2. TI GER Board SPI and UART Connections

Table 2. TI GER to PGA450Q1EVM-S Connections

Connection	TI-GER Pin	EVM Pin
SPI-MISO	1	J3-1 (SDO)
SPI-SCLK	3	J3-3 (SCLK)
SPI-$\overline{CS}$	5	J3-4 (CS)
SPI-MOSI	7	J3-2 (SDI)
UART-TXD	10	J4-3 (RXD)
UART-RXD	20	J4-4 (TXD)
GND	4	J2-4 (GND)

Step 2. Connect the TI GER board to the PC.

Step 3. Open the PGA450Q1EVM GUI.

Step 4. Click the *OFF (Micro Reset)* button on the ESFR tab.

Step 5. Click the *READ ALL* button to read all registers on the ESFR tab. Use register B4 (TEMP_SENS) as an indicator to ensure the device is operating and communicating properly through SPI. Proper communication can be verified if the data of the register reads a value other than 0x00 or 0xFF.

Step 6. Under the OTP tab, click *Check OTP Status* button. If the PGA450-Q1 device has not been previously been OTP programmed, the status displays *OTP Empty*.

Step 7. Connect the 8-V supply to the VPROG_OTP pin on the sensor to program the OTP memory, to program the DEVRAM memory for the first time, or if the OTP status displays *OTP Empty*.

Step 8. If programming DEVRAM memory, go to the DEVRAM tab. For a pristine IC that has never been programmed (OTP status displays *OTP Empty*), check the *Program OTP Memory Also* box for the GUI. This option programs both the OTP and DEVRAM memory. The OTP memory will be programmed with a long-jump statement to redirect the firmware to load into and be run from the DEVRAM memory. If programming OTP memory for production release or a permanently coded PGA450-Q1 device, go to the OTP tab, click *Load .HEX File into GUI*, and locate the appropriate OTP-based .HEX file.

Step 9. Programming and verification of the device occurs automatically.

Step 10. When the device is verified, disconnect the VPROG_OTP supply voltage (if applicable). Do not disconnect system supply voltage if DEVRAM has been programmed, because the DEVRAM memory will clear when the PGA450-Q1 device is power cycled.

2.2.2 Programming the PGA450-Q1 EEPROM

The PGA450Q1EVM-S is preloaded with the EEPROM values listed in Table 2. These instructions are provided in the event that the user prefers to modify the EEPROM using the PGA450Q1EVM GUI, rather than the corresponding UART command. Use the steps that follow to program the device for EEPROM memory.

Step 1. Assuming the MCU status is still set to *MICRO IS IN RESET*, go to the EEPROM tab, and enter the register values for addresses 0x00 through 0x1F as listed in Table 3.

The values at 0x00 to 0x1F are the threshold values used in software. TI recommends that the user begins with the example values provided, and then adjusts these values later as necessary.

The value at address 0x1F is the sensor address.

Step 2. Click the *WRITE SELECTED* button. To ensure the threshold values are written correctly, click the *READ ALL* button.

Step 3. Click the *PROGRAM EEPROM* button to store the threshold values.

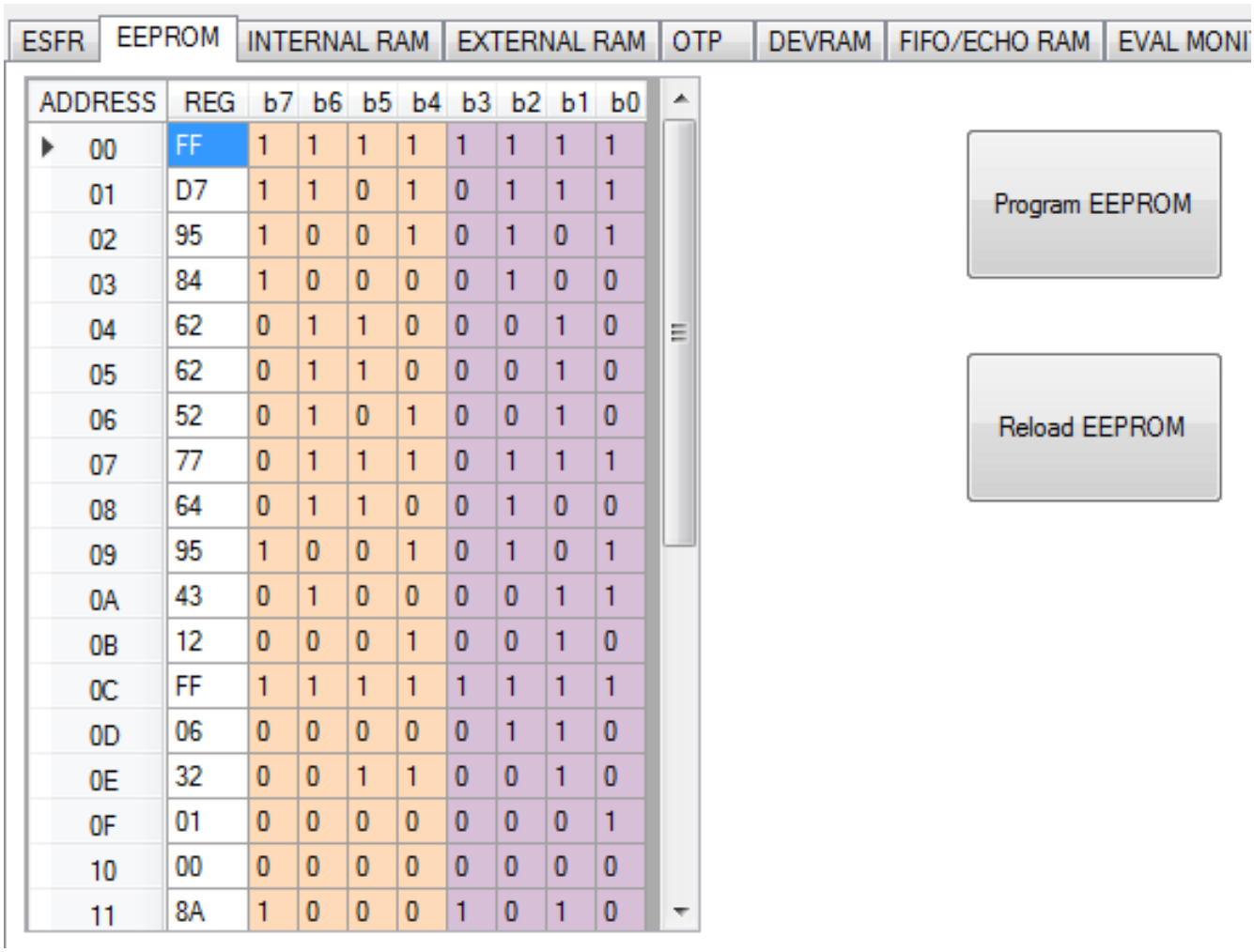
Step 4. Click the *Reload* button. To ensure the threshold values have been written correctly and retained, click the *READ ALL* button. The EEPROM table should appear as shown in Figure 3.

Table 3. EEPROM Register Map Values

Register Address	Register Value	Description
0x00	0xFF	Threshold level 0
0x01	0xD7	Threshold level 1
0x02	0x95	Threshold level 2
0x03	0x84	Threshold level 3
0x04	0x62	Threshold level 4
0x05	0x62	Threshold level 5
0x06	0x52	Threshold level 6
0x07	0x78	Where in FIFO to apply threshold level 7 defined at EEPROM address 0x08 from to the end of the FIFO. Long mode (most significant hex) multiplied by 40 [interval 40 to 600]. Short mode (least significant hex) multiplied by 8 [interval 8 to 120].
0x08	0x64	Threshold level 7, the fixed level of threshold to end of FIFO. Long mode and short mode multiplied by 5 and 1 respectively.
0x09	0x95	Threshold ignore count from beginning of FIFO for long (most significant hex) and short (least significant hex) modes respectively.
0x0A	0x43	1-6 change interval of the threshold level across FIFO for long mode (most significant hex) multiplied by 8 [interval 8 to 120]. Short mode (least significant hex) multiplied by 2 [interval 2 to 15].
0x0B	0x12	PULSE_CNTA
0x0C	0xFF	BLANKING_TIMER
0x0D	0x06	FIFO_CTRL
0x0E	0x32	DOWNSAMPLE
0x0F	0x01	CONTROL_1
0x10	0x00	BURST_MODE
0x11	0x8A	BURST_ONA_LSB
0x12	0x8A	BURST_OFFA_LSB
0x13	0x05	DEADTIME
0x14	0x09	SAT_DEGLITCH
0x15	0x03	BPF_B1_MSB
0x16	0x2D	BPF_B1_LSB
0x17	0xEC	BPF_A2_MSB

Table 3. EEPROM Register Map Values (continued)

Register Address	Register Value	Description
0x18	0x3D	BPF_A2_LSB
0x19	0xF9	BPF_A3_MSB
0x1A	0xA5	BPF_A3_LSB
0x1B	0x35	LPF_B1_MSB
0x1C	0xDD	LPF_B1_LSB
0x1D	0x14	LPF_A2_MSB
0x1E	0x46	LPF_A2_LSB
0x1F	0x01	Sensor address



(1) The *Program EEPROM* button programs the EEPROM cache into the EEPROM memory. The values displayed in the GUI are transferred to the cache before being programmed.

(2) The *Reload EEPROM* button copies the EEPROM memory into the EEPROM cache. The values in the GUI are then updated.

Figure 3. EEPROM Registers Programmed Correctly

2.2.3 Testing the UART Connection With the TI GER Board

Use the steps that follow to test the UART connection with the TI GER board.

Step 1. If the user has not disconnected the system power, ensure that the MCU is activated again by clicking the *ON (MicroActive)* on the ESFR tab.

Step 2. In the top-right of the PGA450Q1EVM GUI, click the *Direct TI GER Control* button. This button does not contain text; it is just an image (see the red circle in Figure 4).

Figure 4. Direct TI GER Control Button

Step 3. Under the GPIO tab, clicking the *IO-8 = IN* and *IO-9 = IN* buttons to ensure that IO-8 and IO-9 are set as *IN HIGH* (see Figure 5).

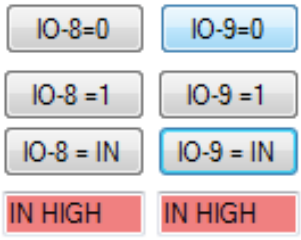


Figure 5. GPIO Tab

Step 4. Connect the UART pins of the sensor to the UART pins of the TI GER board (see Figure 3)
- Pin 10 (TxD) on the TI GER board goes to RXD on the Sensor.
- Pin 20 (RxD) on the TI GER board goes to TXD on the Sensor.

Step 5. On the UART tab, under the *UART CONTROL SETTING* section, select SETUP #9.

Step 6. In the *BAUD RATE* box in the lower right corner of the GUI, enter 19200.

Step 7. On the UART TEST tab, Select SETUP #9

Step 8. Click the *OPEN UART MODULE* button.

Step 9. Click the *CHANGE BAUD RATE* button, which should display 19200 and 1-bit = 52.1 μs.

Step 10. Click the *CHECK FOR ERRORS* to ensure there no errors occurred. If an error occurred, one of the boxes will be red, at which point the user must click the *CLOSE MODULE IMMEDIATELY* and *CLOSE UART MODULE* buttons. Then repeat the setup, beginning at Step 8 in Section 2.2.3.

Step 11. Write the values shown in Figure 6 in the TX box. Each byte must be typed on a separate row.

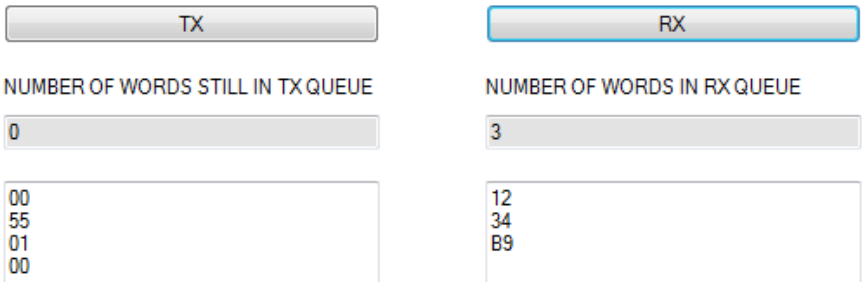


Figure 6. User Submitted Data Packet in TX Box and Valid RX Response

The description of the TX data packet is as follows:

- 00: is the break field
- 55: is the synchronization field
- 01: 0 is the command and 1 is the sensor address. Ensure that the sensor address matches what was programmed in the EEPROM address 0x07 from the previous steps.
- 00: is the checksum field; however, this data is discarded, so the user may enter any value here.

Step 12. Click the RX button to display the response of the sensor.

The description of the RX data packet is as follows:

- 12: is dummy byte 1 and has no special meaning.
- 34: is dummy byte 2 and has no special meaning.
- B9: is the checksum from byte 1 and byte 2.

The function that calculates the checksum is described as follows:

Table 4 provides a checksum calculation of four bytes shown. If the frame has four data bytes of the protected identifier and three data bytes, the calculation is the same. The data = 0x4A, 0x55, 0x93, 0xE5.

Table 4. Example of Checksum Calculation

Action	Hex	Carry	D7	D6	D5	D4	D3	D2	D1	D0
0x4A	0x4A		0	1	0	0	1	0	1	0
+0x55 = Add Carry	0x9F 0x9F	0	1 1	0 0	0 0	1 1	1 1	1 1	1 1	1 1
+0x93 = Add Carry	0x132 0x33	1	0 0	0 0	1 1	1 1	0 0	0 0	1 1	0 1
+0xE5 = Add Carry	0x118 0x19	1	0 0	0 0	0 0	1 1	1 1	0 0	0 0	0 1
Invert	0xE6		1	1	1	0	0	1	1	0
0x19 + 0.xE6 =	0xFF		1	1	1	1	1	1	1	1

The resulting sum is 0x19. Inversion yields the final result of: checksum = 0xE6. The receiving node can check the consistency of the received frame by using the same addition mechanism. When the received checksum (0xE6) is added to the intermediate result (0x19) the sum is 0xFF.

The previously described TX command is called *command0 – Sensor Check Command*. If the sensor is address 0x01 and the user attempts to communicate with a sensor using a different address, sensor 0x01 gives no response. In the following TX example shown in Figure 7, no response was received as displayed in the RX box because, in this example, command0 was sent to sensor address 0x02.

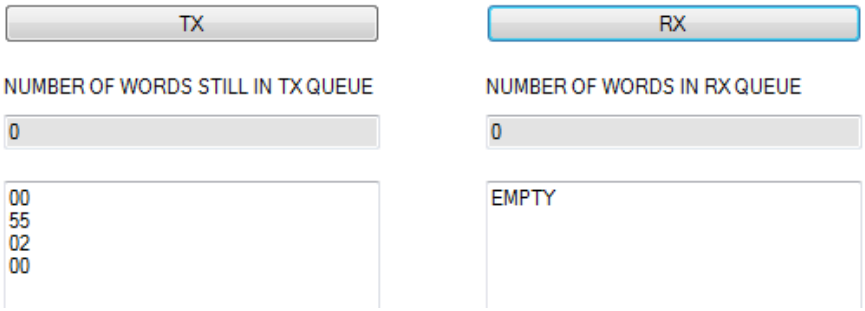


Figure 7. No Response in the RX Box

2.3 UART Command Listing

The following is a list of predefined commands made available on the default DEVRAM and OTP firmware provided for the PGA450Q1EVM-S.

Command 0— Test UART communication. If communication is working correctly, the PGA450-Q1 will return a value of 0x12 0x23.

Example hex entry: 0x00, 0x55, 0x01, 0x00
where:

- [0] 0x00: break field
- [1] 0x55: synchronization field
- [2] 0x01: 0 = command 0. 1 = sensor address set in EEPROM address 0x31
- [3] 0x00: ignored but required checksum

Command 1— Trigger a short or long distance burst and capture with hard-coded drive and receive settings. Also reads first instance of threshold crossing for closest object detected.

Example hex entry: 0x00, 0x55, 0x11, 0x02, 0x00
where:

- [0] 0x00: break field
- [1] 0x55: synchronization field
- [2] 0x11: 1 = command 1. 1 = sensor address set in EEPROM address 0x31
- [3] 0x02: 00 = listen. 01 = short. 02 = long.
- [4] 0x00: ignored but required checksum

Command 2— Read first instance of threshold crossing for closest object detected.

Example hex entry: 0x00, 0x55, 0x21, 0x00
where:

- [0] 0x00: break field
- [1] 0x55: synchronization field
- [2] 0x21: 2 = command 2. 1 = sensor address set in EEPROM address 0x31
- [3] 0x00: ignored but required checksum

Command 3— Update an EEPROM value.

Example hex entry: 0x00, 0x55, 0x31, 0x00, 0xFF, 0x00
where:

- [0] 0x00: break field
- [1] 0x55: synchronization field
- [2] 0x31: 3 = command 3. 1 = sensor address set in EEPROM address 0x31
- [3] 0x00: 00 = EEPROM address
- [4] 0xFF: FF = EEPROM data
- [5] 0x00: ignored but required checksum

Command 4— Read all 768 bytes of FIFO data.

Example hex entry: 0x00, 0x55, 0x41, 0x00
where:

- [0] 0x00: break field
- [1] 0x55: synchronization field
- [2] 0x41: 4 = command 4. 1 = sensor address set in EEPROM address 0x31
- [3] 0x00: ignored but required checksum

Command 5—Burst and capture ultrasonic profile based on EEPROM configuration of drive and receive settings.

Example hex entry: 0x00, 0x55, 0x51, 0x02, 0x00
where:

- [0] 0x00: break field
- [1] 0x55: synchronization field
- [2] 0x51: 5 = command 5. 1 = sensor address set in EEPROM address 0x31
- [3] 0x02: 0 = listen. 1 = short. 2 = long
- [4] 0x00: ignored but required checksum

Command 6—Threshold values report for selected mode of operation (short or long).

Example hex entry: 0x00, 0x55, 0x61, 0x02, 0x00
where:

- [0] 0x00: break field
- [1] 0x55: synchronization field
- [2] 0x61: 6 = command 6. 1 = sensor address set in EEPROM address 0x31
- [3] 0x02: 1 = short. 2 = long
- [4] 0x00: ignored but required checksum

Command 7—Not used in example firmware. Reserved for custom user defined function.

Example hex entry: 0x00, 0x55, 0x71, 0x00
where:

- [0] 0x00: break field
- [1] 0x55: synchronization field
- [2] 0x71: 7 = command 7. 1 = sensor address set in EEPROM address 0x31
- [3] 0x00: ignored but required checksum

3 Software

To modify the source-code made available through the PGA450Q1EVM-S firmware installer, download the Keil C51 Development Tool for all 8051 devices, which includes the uVision IDE required to open and edit the PGA450-Q1 project file. Keil products use a license management system. Without a current license, the product runs as an evaluation or *lite* edition which has a few limitations.

3.1 IDE Output File Configuration

Build the PGA450.uvproj to generate the custom .HEX file used to program the DEVRAM or OTP memory of the internal 8051 core.

3.1.1 Setup for DEVRAM Output File

Use the steps that follow to setup the output file of the DEVRAM memory.

Step 1. Change the code range to the DEVRAM memory space:

1. Right click on *Target 1* in the project window, and select *Options for Target*.
2. Go to the BL51 Locate tab, and modify the Code Range to go from 0x2000–0x3FFF.

Step 2. Copy the following text to the Code box:

```
?pr?external1_ISR?PGA450_isrs (0X2100),
?pr?timer0_ISR?PGA450_isrs (0X2400),
?pr?timer1_ISR?PGA450_isrs (0X2800),
?pr?serial_ISR?PGA450_isrs (0X2C00),
?pr?linPID_ISR?PGA450_isrs (0X3000),
?pr?linSciRxData_ISR?PGA450_isrs (0X3400),
?pr?linSciTxData_ISR?PGA450_isrs (0X3800),
?pr?external0_ISR?PGA450_isrs (0X3900),
?pr?linSync_ISR?PGA450_isrs (0X3D00)
```

Step 3. Comment out the OTP section in STARTUP.A51, and remove the comments from the DEVRAM section.

3.1.2 Setup for OTP Output File

Use the steps that follow to setup the output file of the OTP memory.

1. Change the code range to the OTP memory space:
   1. Right click on *Target 1* in the project window, and select *Options for Target*.
   2. Go to the BL51 Locate tab, and modify the Code Range to go from 0x0000–0x1FFF.
2. Delete everything in the Code box.
3. Comment out the DEVRAM section in STARTUP.A51, and remove the comments from the OTP section.

3.2 Interface Descriptions

The PGA450-Q1 device is compatible with three communication interface options including: SPI, LIN, and UART. All of these communication interfaces, related circuitry, or access points are integrated or present on the PGA450Q1EVM-S.

3.2.1 UART Interface

The TxD and RxD pins on the PGA450-Q1 device are connected to the 8051W UART. These two pins can be used either for software debugging or for implementing application-specific protocols. For a detailed example of how to use UART with the PGA450-Q1 device, refer to Section 2.3.

3.2.2 LIN Interface

The PGA450Q1EVM GUI can communicate with the PGA450-Q1 device using LIN. The UART of the TI GER USB communication board is the LIN master, and the PGA450-Q1 device is the LIN slave. The GUI can be used to configure the LIN frames that are transmitted to the PGA450-Q1 device. An external LIN transceiver is required to translate the UART of the TI GER board into the LIN compliant format. For a detailed example of how to use LIN with the PGA450-Q1 device, refer to *LIN Demonstration using PGA450Q1EVM Firmware Rev 2.1* (SLDA035).

3.2.3 Serial-Peripheral Interface

The PGA450-Q1 device can also be put into a RESET state where the microcontroller is not active. During this state, SPI is the only digital interface that can be used. The low-side drivers can still be triggered to begin an ultrasonic burst and the analog front-end and digital data path can still store the returned echo signal in the FIFO RAM. However, any processing of the FIFO RAM by the internal microprocessor to determine the location of an object does not occur. The FIFO RAM data can be read over SPI, allowing an external microprocessor to process the data.

To provide a quick evaluation of the performance of the PGA450-Q1 device using the PGA450Q1EVM-S and GUI without having to develop sophisticated 8051 μP software, the GUI provides an intuitive interface tab, the Evaluation Tab, that collects all required information regarding the transducer drive and receive. For the transducer drive, it includes: transducer frequency; transducer drive voltage, VREG; transformer configuration; and number of drive pulses. For the transducer signal receive, it includes signal-processing parameters: LNA gain setting; BPF and LPF coefficient; clock selection; FIFO mode; and FIFO downsample size.

4 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the schematic, bill of materials (BOM), and layout.

4.1 Schematic

Figure 8 sows the schematic of the PGA450Q1EVM-S.

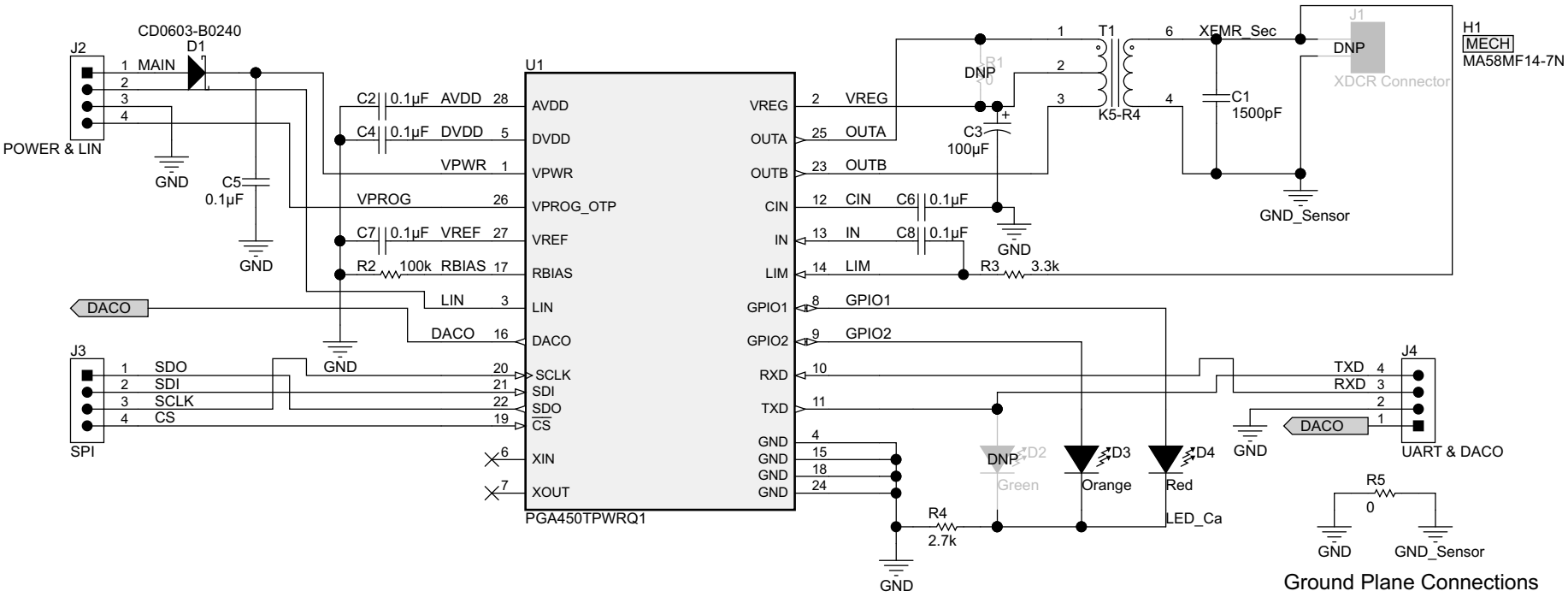


Figure 8. PGA450Q1EVM-S Schematic

4.2 Bill of Materials

Table 5 lists the bill of materials (BOM).

Table 5. BOM

Designator	Quantity	Value	Description	Package Reference	Part Number
C1	1	1500 pF	Capacitor, ceramic, 1500 pF, 100 V, ± 5%, C0G/NP0, 0805	0805	GRM2165C2A152JA01D
C2, C4, C5, C6, C7, C8	6	0.1 µF	Capacitor, ceramic, 0.1 µF, 50 V, ± 10%, X7R, 0402	0402	C1005X7R1H104K050BB
C3	1	100 µF	Capacitor, aluminum, 100 µF, 35 V, ± 20%, SMD	F80	EMVA350ADA101MF80G
D1	1	45 V	Diode, Schottky, 45 V, 0.2 A, 0603 Diode	0603 Diode	CD0603-B0240
D2	1	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190GKT
D3	1	Orange	LED, Orange, SMD	LED_0603	LTST-C191KFKT
D4	1	Red	LED, Red, SMD	LED_0603	LTST-C191KRKT
H1	1		Ultrasonic transducer	MA58MF14-7N	MuRata
J1	1		Header, 100 mil, 2 × 1, Tin, TH	Header, 2 pin, 100 mil, Tin	PEC02SAAN
J2, J3, J4	3		Header, 100 mil, 4 × 1, Tin, TH	Header, 4 × 1, 100 mil, TH	PEC04SAAN
R1, R5	2	0 Ω	Resistor, 0 Ω, 5%, 0.1 W, 0603	0603	MCR03EZPJ000
R2	1	100 kΩ	Resistor, 100 kΩ, 5%, 0.1 W, 0603	0603	CRCW0603100KJNEA
R3	1	3.3 kΩ	Resistor, 3.3 kΩ, 5%, 0.25 W, 1206	1206	CRCW12063K30JNEA
R4	1	2.7 kΩ	Resistor, 2.7 kΩ, 5%, 0.1 W, 0603	0603	RC0603JR-072K7L
T1	1		Transformer, TH	7x7mm	K5-R4
U1	1		ULTRASONIC-SENSOR SIGNAL CONDITIONER, PW0028A	PW0028A	PGA450TPWRQ1

4.3 Board Layout and Component Placement

Figure 9 and Figure 10 show the top and bottom views component placement. Figure 11 and Figure 12 show the top and bottom views of the board layout.

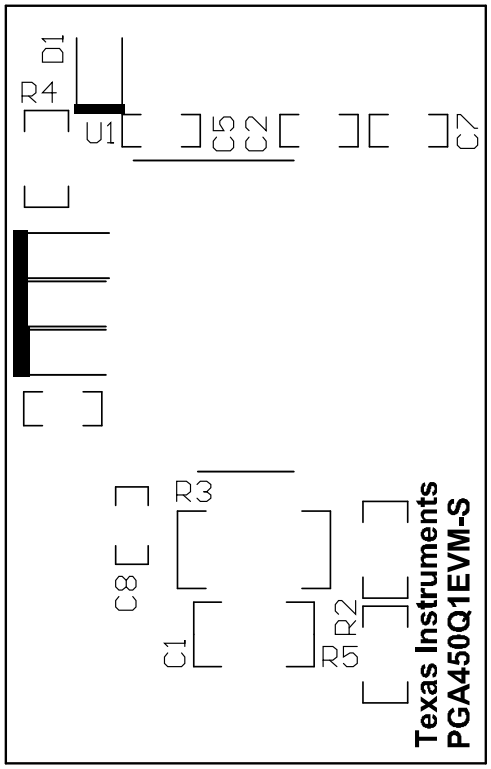


Figure 9. Component Placement – Top Overview

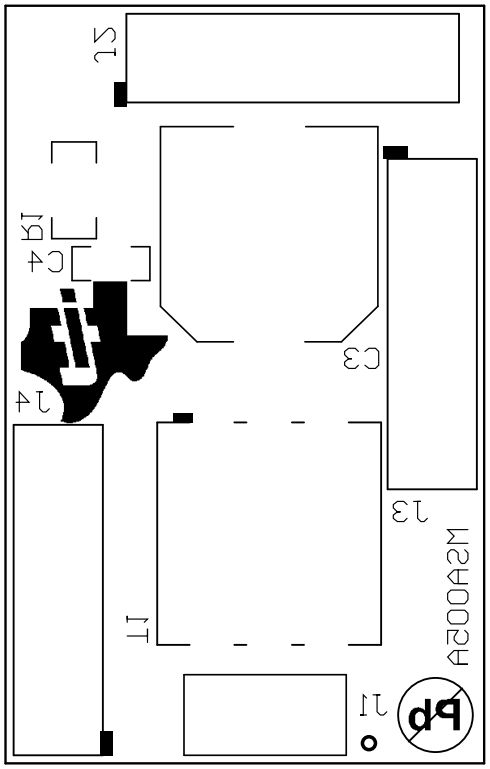


Figure 10. Component Placement – Bottom Overview

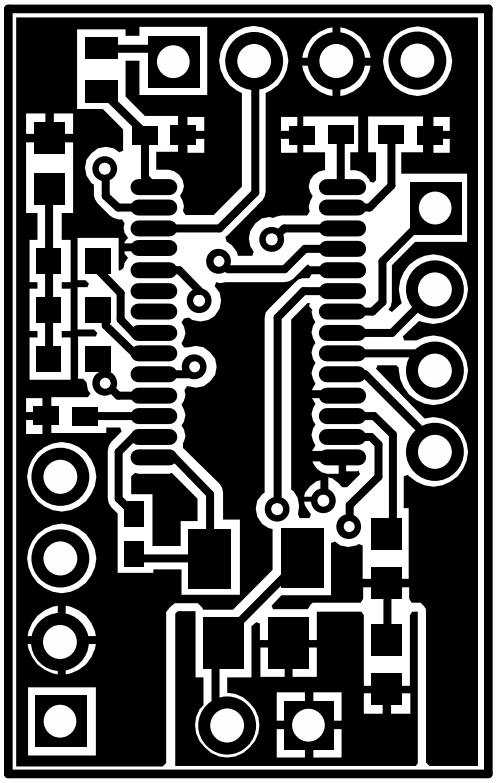


Figure 11. Layout – Top

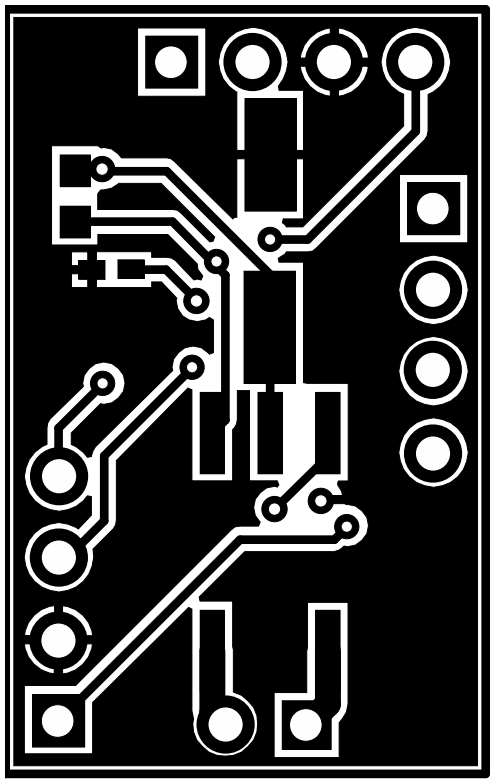


Figure 12. Layout – Bottom

5 References

For additional reference, see the following documents from TI:

- *PGA450-Q1 Ultrasonic-Sensor Signal Conditioner* (SLDS185)
- *PGA450Q1EVM User's Guide* (SLDU007)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (March 2016) to B Revision **Page**

- Added *TIDA-00151 UART Demo Instructional* to the document title 1
- Added the 0x00 value for Command 1 in the *UART Command Listing* section 9
- Changed the *PGA450Q1EVM-S Schematic* image 12
- Added H1 to the *Bill of Materials* 13

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