Ordering number : ENN*7980

Preliminary

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC75857E
LC75857W

CMOS IC

— 1/3, 1/4 Duty LCD Display Drivers with Key Input Function

Overview

The LC75857E and LC75857W are 1/3 duty and 1/4 duty LCD display drivers that can directly drive up to 164 segments and can control up to four general-purpose output ports. These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

Features

- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- 1/3 duty and 1/4 duty drive schemes can be controlled from serial data.
- 1/2 bias and 1/3 bias drive schemes can be controlled from serial data.
- Capable of driving up to 126 segments using 1/3 duty and up to 164 segments using 1/4 duty.
- Sleep mode and all segments off functions that are controlled from serial data.
- Switching between key scan output and segment output can be controlled from the serial data.
- The key scan operation enabled/disabled state can be controlled from the serial data.
- Switching between segment output port and general-purpose output port can be controlled from serial data.
- The common and segment output waveform frame frequency can be controlled from the serial data.
- Switching between RC oscillator mode and external clock mode can be controlled from the serial data.
- Serial data I/O supports CCB format communication with the system controller.
- Direct display of display data without the use of a decoder provides high generality.
- Independent V_{LCD} for the LCD driver block.
  (When the logic block supply voltage V_{DD} is in the range 3.6 to 6.0 V, V_{LCD} can be set to a voltage in the range $0.75 \times V_{DD}$ to 6.0 V, and when V_{DD} is in the range 2.7 to 3.6 V, V_{LCD} can be set to a voltage in the range 2.7 to 6.0 V.)
- Provision of an on-chip voltage-detection type reset circuit prevents incorrect displays.

SANYO Semiconductor Co., Ltd.
http://semicon.sanyo.com/en/network

Specifications

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	–0.3 to +7.0	V
	V_{LCD} max	V_{LCD}	–0.3 to +7.0	
Input voltage	$V_{IN}1$	CE, CL, DI	–0.3 to +7.0	V
	$V_{IN}2$	OSC,TEST	–0.3 to V_{DD} +0.3	
	$V_{IN}3$	$V_{LCD}1$, $V_{LCD}2$, KI1 to KI5	–0.3 to V_{LCD} +0.3	
Output voltage	$V_{OUT}1$	DO	–0.3 to +7.0	V
	$V_{OUT}2$	OSC	–0.3 to V_{DD} +0.3	
	$V_{OUT}3$	S1 to S42, COM1 to COM4, KS1 to KS6, P1 to P4	–0.3 to V_{LCD} +0.3	
Output current	$I_{OUT}1$	S1 to S42	300	µA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	KS1 to KS6	1	
	$I_{OUT}4$	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 85°C	200	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		6.0	V
	V_{LCD}	V_{LCD}: V_{DD} = 3.6 V to 6.0 V	0.75 V_{DD}		6.0	
		V_{LCD}: V_{DD} = 2.7 V to 3.6 V	2.7		6.0	
Input voltage	$V_{LCD}1$	$V_{LCD}1$		2/3 V_{LCD}	V_{LCD}	V
	$V_{LCD}2$	$V_{LCD}2$		1/3 V_{LCD}	V_{LCD}	
Input high level voltage	$V_{IH}1$	CE, CL, DI	0.8 V_{DD}		6.0	V
	$V_{IH}2$	KI1 to KI5	0.6 V_{LCD}		V_{LCD}	
	$V_{IH}3$	OSC: External clock mode	0.7 V_{DD}		V_{DD}	
Input low level voltage	$V_{IL}1$	CE, CL, DI	0		0.2 V_{DD}	V
	$V_{IL}2$	KI1 to KI5	0		0.2 V_{LCD}	
	$V_{IL}3$	OSC: External clock mode	0		0.3 V_{DD}	
Recommended RC oscillator external resistor	R_{OSC}	OSC: RC oscillator mode		39		kΩ
Recommended RC oscillator external capacitor	C_{OSC}	OSC: RC oscillator mode		1000		pF
Guaranteed RC oscillator operating range	f_{OSC}	OSC: RC oscillator mode	19	38	76	kHz
External clock frequency	f_{CK}	OSC: External clock mode :Figure 4	19	38	76	kHz
External clock duty	D_{CK}	OSC: External clock mode :Figure 4	30	50	70	%
Data setup time	t_{ds}	CL, DI :Figures 2,3	160			ns
Data hold time	t_{dh}	CL, DI :Figures 2,3	160			ns
CE wait time	t_{cp}	CE, CL :Figures 2,3	160			ns
CE setup time	t_{cs}	CE, CL :Figures 2,3	160			ns
CE hold time	t_{ch}	CE, CL :Figures 2,3	160			ns
High level clock pulse width	$t\phi_H$	CL :Figures 2,3	160			ns
Low level clock pulse width	$t\phi_L$	CL :Figures 2,3	160			ns
Rise time	t_r	CE, CL, DI :Figures 2,3		160		ns
Fall time	t_f	CE, CL, DI :Figures 2,3		160		ns
DO output delay time	t_{dc}	DO R_{PU}=4.7 kΩ, C_L=10pF *1 :Figures 2,3			1.5	µs
DO rise time	t_{dr}	DO R_{PU}=4.7 kΩ, C_L=10pF *1 :Figures 2,3			1.5	µs

Note: *1. Since DO is an open-drain output, these values depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_{H1}	CE, CL, DI		0.1 V_{DD}		V
	V_{H2}	KI1 to KI5		0.1 V_{LCD}		
Power-down detection voltage	V_{DET}		2.0	2.2	2.4	V
Input high level current	$I_{IH}1$	CE, CL, DI: V_I = 6.0 V			5.0	µA
	$I_{IH}2$	OSC: V_I = V_{DD} External clock mode			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI: V_I = 0 V	–5.0			µA
	$I_{IL}2$	OSC: V_I = 0 V External clock mode	–5.0			
Input floating voltage	V_{IF}	KI1 to KI5			0.05 V_{LCD}	V
Pull-down resistance	R_{PD}	KI1 to KI5: V_{LCD} = 5.0 V	50	100	250	kΩ
		KI1 to KI5: V_{LCD} = 3.0 V	100	200	500	
Output off leakage current	I_{OFFH}	DO: VO = 6.0 V			6.0	µA
Output high level voltage	$V_{OH}1$	KS1 to KS6: I_O = –500 µA V_{LCD} = 3.6 to 6.0 V	V_{LCD} – 1.0	V_{LCD} – 0.5	V_{LCD} – 0.2	V
		KS1 to KS6: I_O = –250 µA V_{LCD} = 2.7 to 3.6 V	V_{LCD} – 0.8	V_{LCD} – 0.4	V_{LCD} – 0.1	
	$V_{OH}2$	P1 to P4: I_O = –1 mA	V_{LCD} – 0.9			
	$V_{OH}3$	S1 to S42: I_O = –20 µA	V_{LCD} – 0.9			
	$V_{OH}4$	COM1 to COM4: I_O = –100 µA	V_{LCD} – 0.9			
Output low level voltage	$V_{OL}1$	KS1 to KS6: I_O = 25 µA V_{LCD} = 3.6 to 6.0 V	0.2	0.5	1.5	V
		KS1 to KS6: I_O = 12.5 µA V_{LCD} = 2.7 to 3.6 V	0.1	0.4	1.2	
	$V_{OL}2$	P1 to P4: I_O = 1 mA			0.9	
	$V_{OL}3$	S1 to S42: I_O = 20 µA			0.9	
	$V_{OL}4$	COM1 to COM4: I_O = 100 µA			0.9	
	$V_{OL}5$	DO: I_O = 1 mA		0.1	0.5	
Output middle level voltage *2	$V_{MID}1$	COM1 to COM4: 1/2 bias, I_O = ±100 µA	1/2 V_{LCD} – 0.9		1/2 V_{LCD} + 0.9	V
	$V_{MID}2$	S1 to S42: 1/3 bias,I_O = ±20 µA	2/3 V_{LCD} – 0.9		2/3 V_{LCD} + 0.9	
	$V_{MID}3$	S1 to S42: 1/3 bias, I_O = ±20 µA	1/3 V_{LCD} – 0.9		1/3 V_{LCD} + 0.9	
	$V_{MID}4$	COM1 to COM4: 1/3 bias,I_O = ±100 µA	2/3 V_{LCD} – 0.9		2/3 V_{LCD} + 0.9	
	$V_{MID}5$	COM1 to COM4: 1/3 bias,I_O = ±100 µA	1/3 V_{LCD} – 0.9		1/3 V_{LCD} + 0.9	
Oscillator frequency	fosc	OSC: R_{OSC} = 39 kΩ, C_{OSC} = 1000 pF	30.4	38	45.6	kHz
Current drain	$I_{DD}1$	V_{DD} :Sleep mode			100	µA
	$I_{DD}2$	V_{DD}: V_{DD} = 6.0 V, output open,fosc = 38 kHz		300	600	
	$I_{LCD}1$	V_{LCD} : Sleep mode			5	
	$I_{LCD}2$	V_{LCD}: V_{LCD} = 6.0 V, output open, 1/2 bias, fosc = 38 kHz		100	200	
	$I_{LCD}3$	V_{LCD}: V_{LCD} = 6.0 V, output open, 1/3 bias, fosc = 38 kHz		60	120	

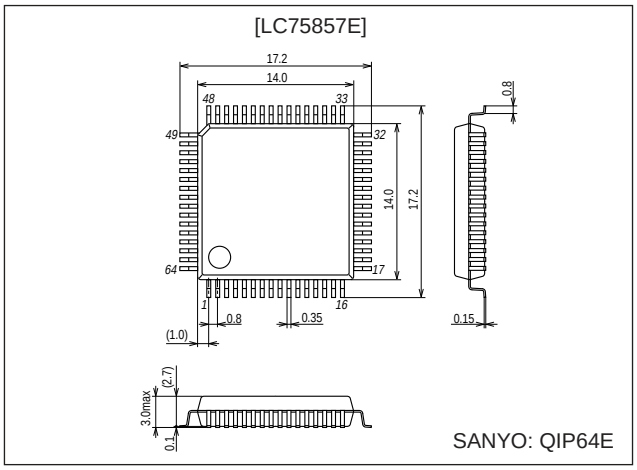
Nete: *2. Excluding the bias voltage generation divider resistor built into $V_{LCD}1$ and $V_{LCD}2$. (See Figure 1.)

Package Dimensions

unit: mm

3159A-QIP64E

[LC75857E]

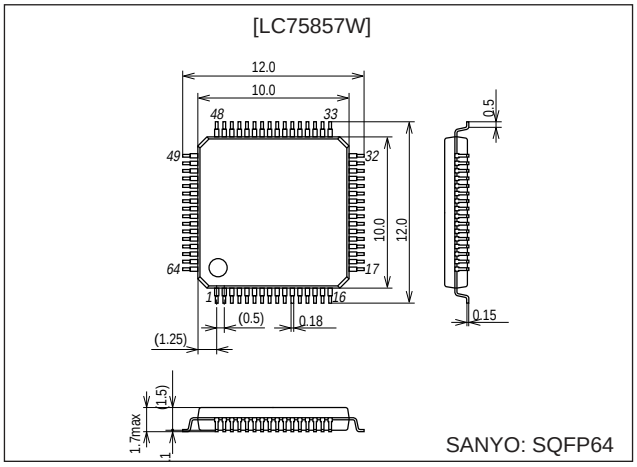


SANYO: QIP64E

unit: mm

3190A-SQFP64

[LC75857W]



SANYO: SQFP64

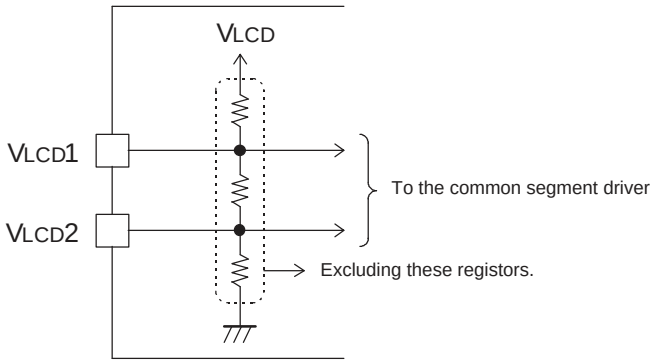


Figure 1

1. Serial data I/O timing when CL is stopped at the low level

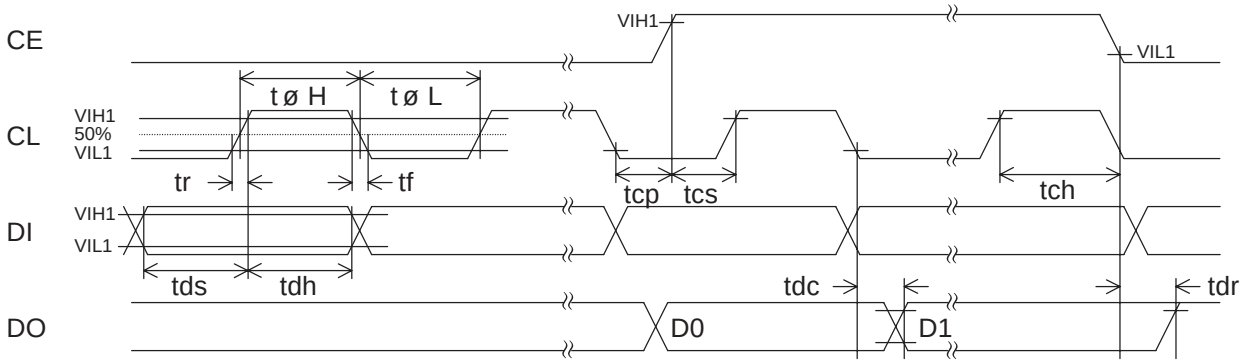


Figure 2

2. Serial data I/O timing when CL is stopped at the high level

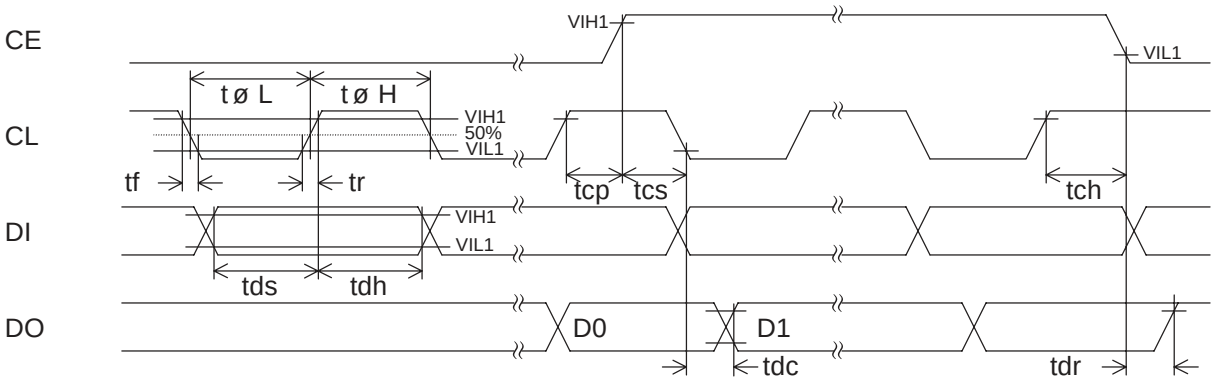
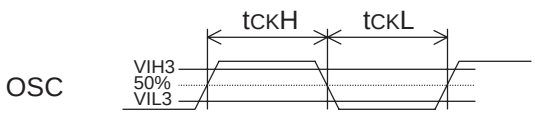


Figure 3

3. OSC pin clock timing in external clock mode

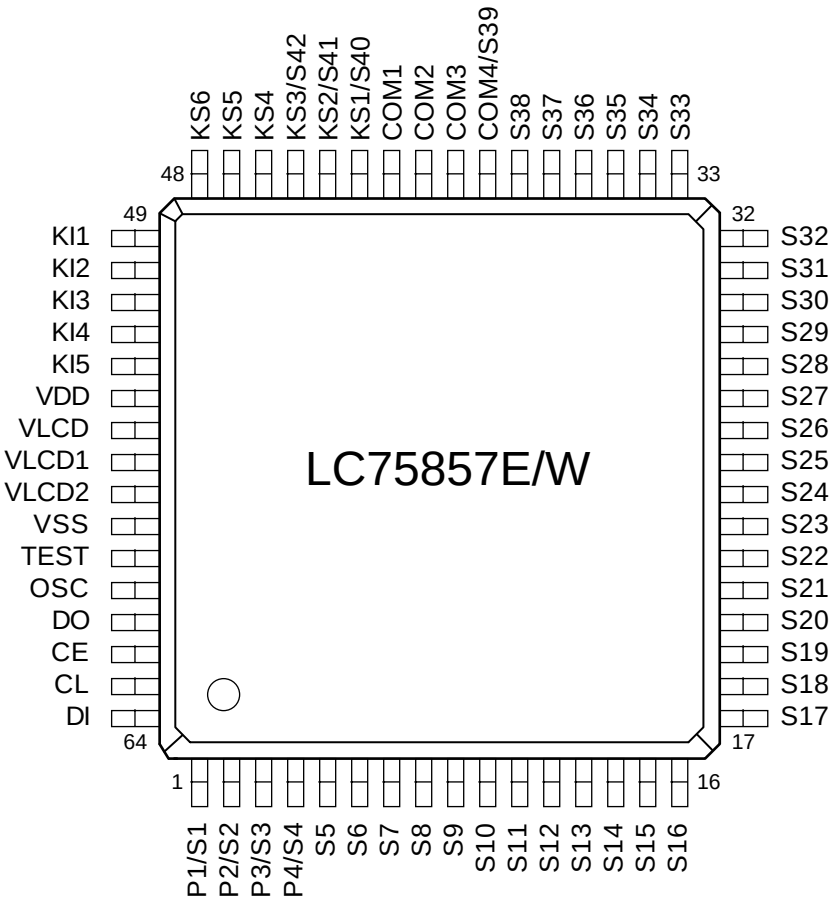


$$f_{CK} = \frac{1}{t_{CKH} + t_{CKL}} \text{ [kHz]}$$

$$D_{CK} = \frac{t_{CKH}}{t_{CKH} + t_{CKL}} \times 100[\%]$$

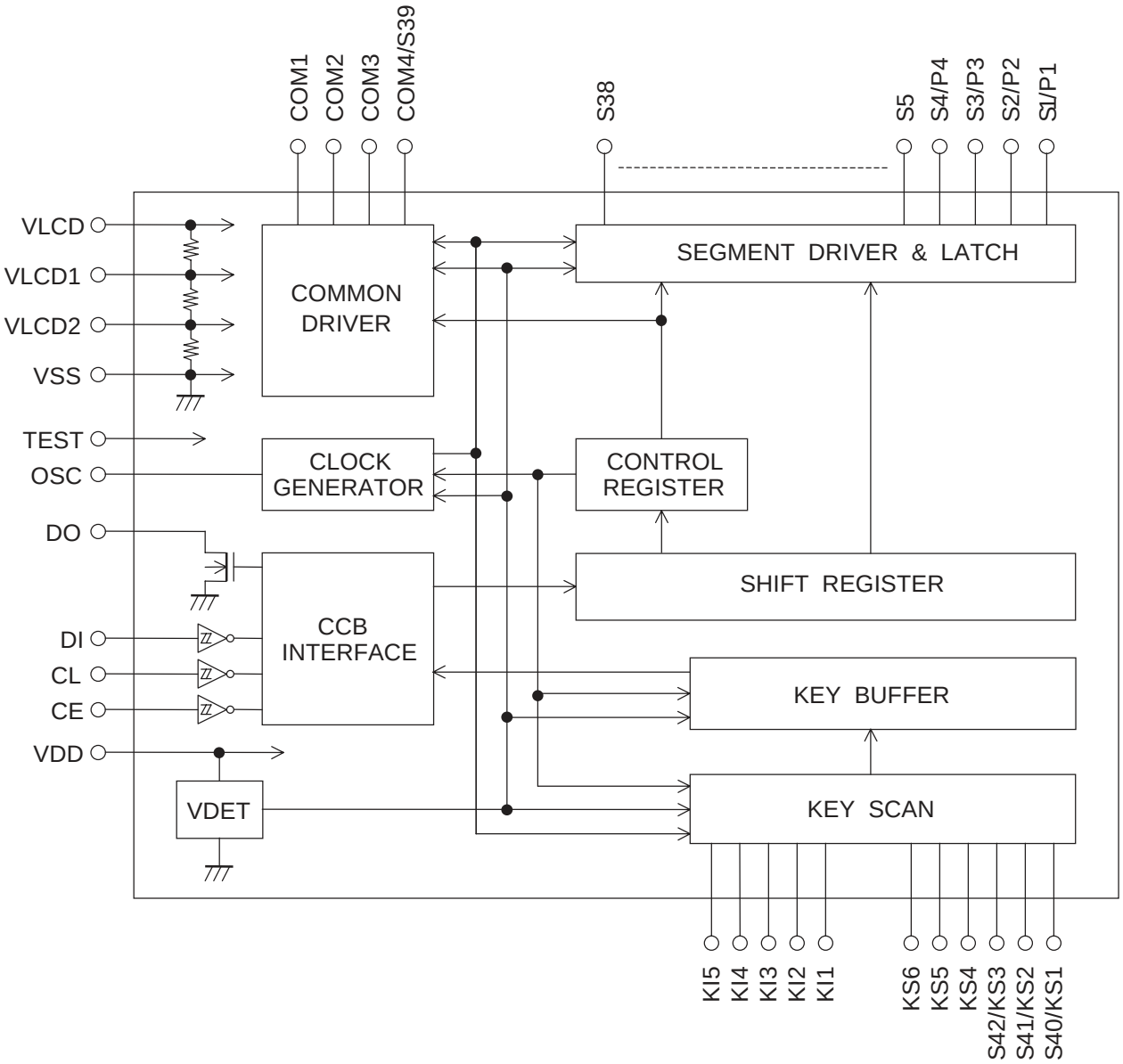
Figure 4

Pin Assignments



Top view

Block Diagram



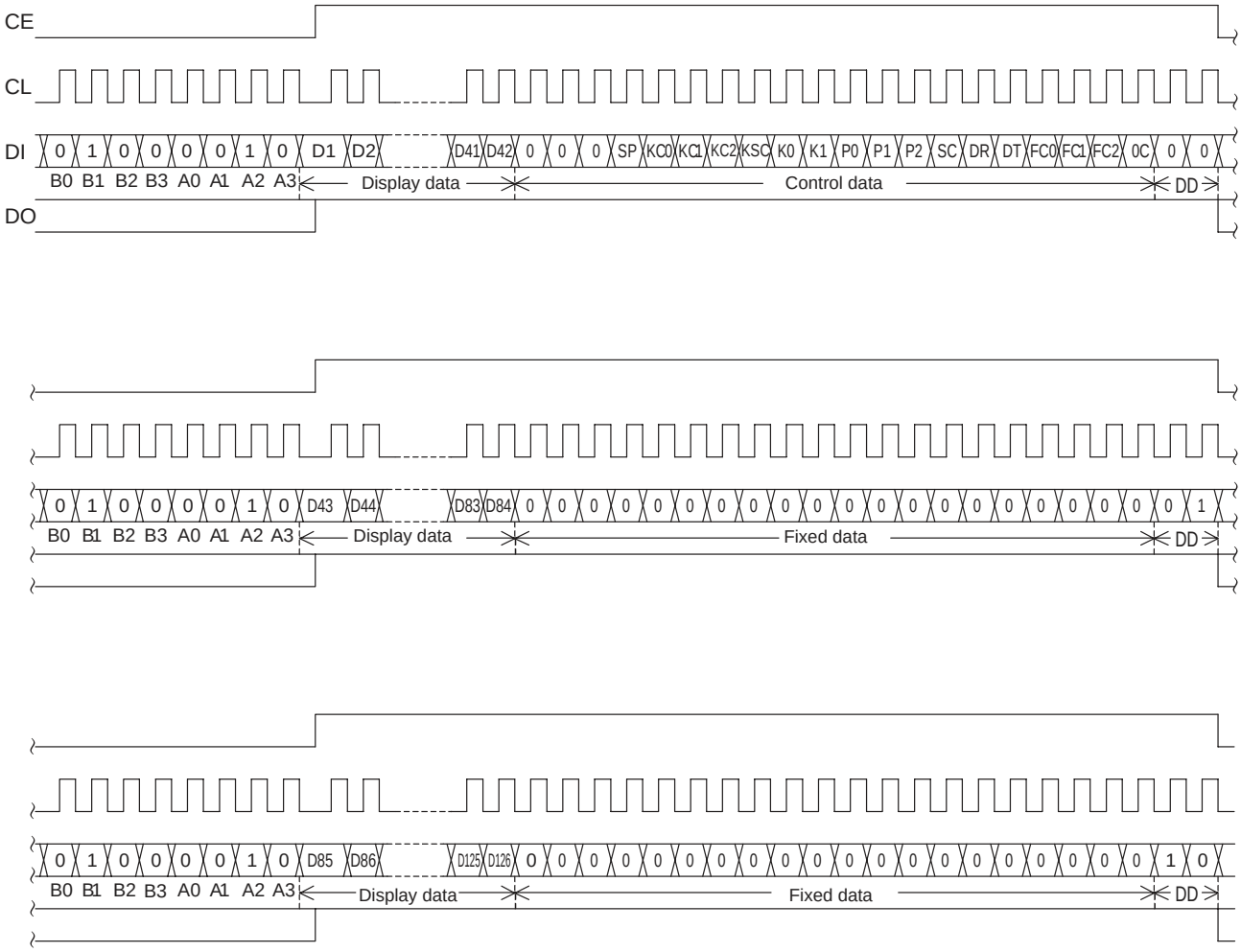
Pin Functions

Pin	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S4/P4 S5 to S38	1 to 4 5 to 38	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	—	O	OPEN
COM1 to COM3 COM4/S39	42 to 40 39	Common driver outputs The frame frequency is fo [Hz] The COM4/S39 pin can be used as a segment output in 1/3 duty.	—	O	OPEN
KS1/S40 KS2/S41 KS3/S42 KS4 to KS6	43 44 45 46 to 48	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S40 to KS3/S42 pins can be used as segment outputs when so specified by the control data.	—	O	OPEN
KI1 to KI5	49 to 53	Key scan inputs These pins have built-in pull-down resistors.	H	I	GND
OSC	60	The OSC pin can be used to form an oscillator circuit with an external resistor and an external capacitor. If external clock mode is selected with the control data, this pin is used to input an external clock signal.	—	I/O	V_{DD}
CE CL DI DO	62 63 64 61	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE :Chip enable CL :Synchronization clock DI :Transfer data DO :Output data	H ↑ — —	I I I O	GND OPEN
TEST	59	This pin must be connected to ground.	—	I	—
$V_{LCD}1$	56	Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to $V_{LCD}2$ when a 1/2 bias drive scheme is used.	—	I	OPEN
$V_{LCD}2$	57	Used for applying the LCD drive 1/3 bias voltage externally. Must be connected to $V_{LCD}1$ when a 1/2 bias drive scheme is used.	—	I	OPEN
V_{DD}	54	Logic block power supply connection. Provide a voltage of between 2.7 and 6.0V.	—	—	—
V_{LCD}	55	LCD driver block power supply connection. A voltage in the range 0.75 × VDD to 6.0 V must be provided when VDD is in the range 3.6 to 6.0 V, and a voltage in the range 2.7 V to 6.0 V must be provided when VDD is in the range 2.7 to 3.6 V.	—	—	—
V_{SS}	58	Power supply connection. Connect to ground.	—	—	—

Serial Data Input

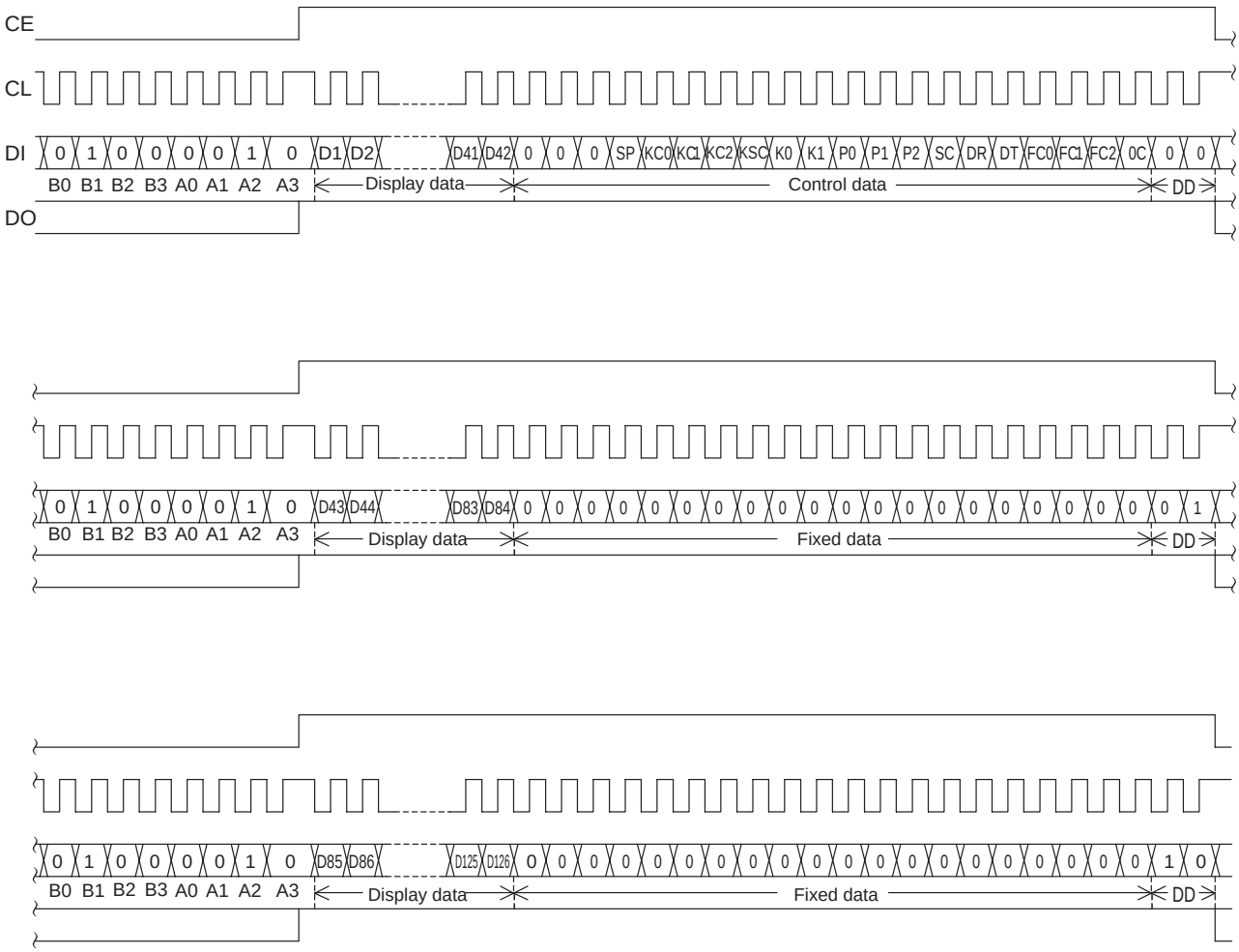
1. 1/3 duty

(1) When CL is stopped at the low level



Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

(2) When CL is stopped at the high level

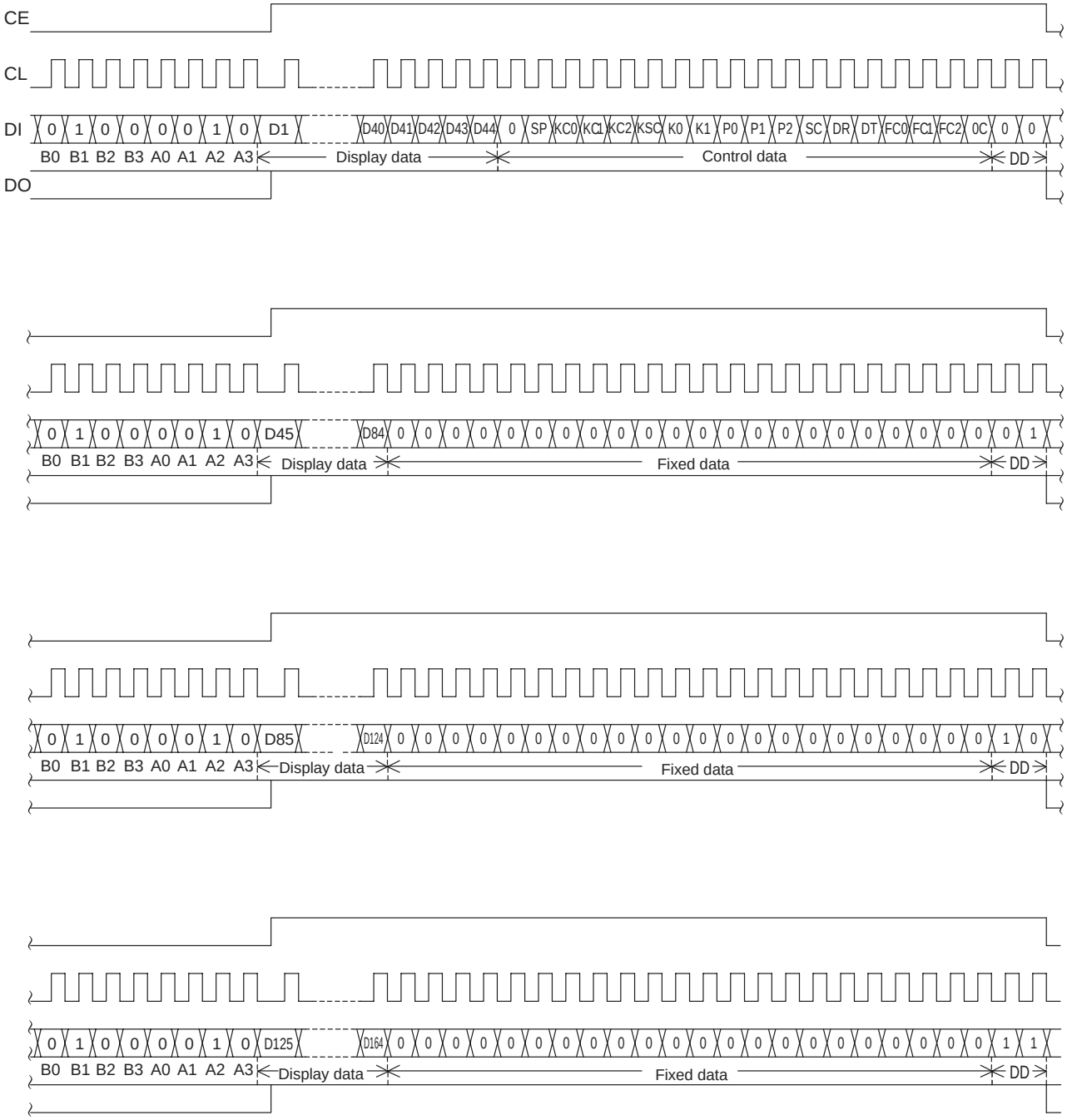


Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

CCB address····· 42H
D1 to D126 ····· Display data
SP ····· Normal mode/sleep mode control data
KC0 to KC2 ····· Key scan output state setting data
KSC····· Key scan operation enabled/disabled state setting data
K0, K1 ····· Key scan output/segment output selection data
P0 to P2 ····· Segment output port/general-purpose output port selection data
SC ····· Segment on/off control data
DR····· 1/2 bias or 1/3 bias drive selection data
DT ····· 1/3 duty or 1/4 duty drive selection data
FC0 to FC2 ····· Common and segment output waveform frame frequency setting data
OC····· RC oscillator mode/external clock mode switching selection data

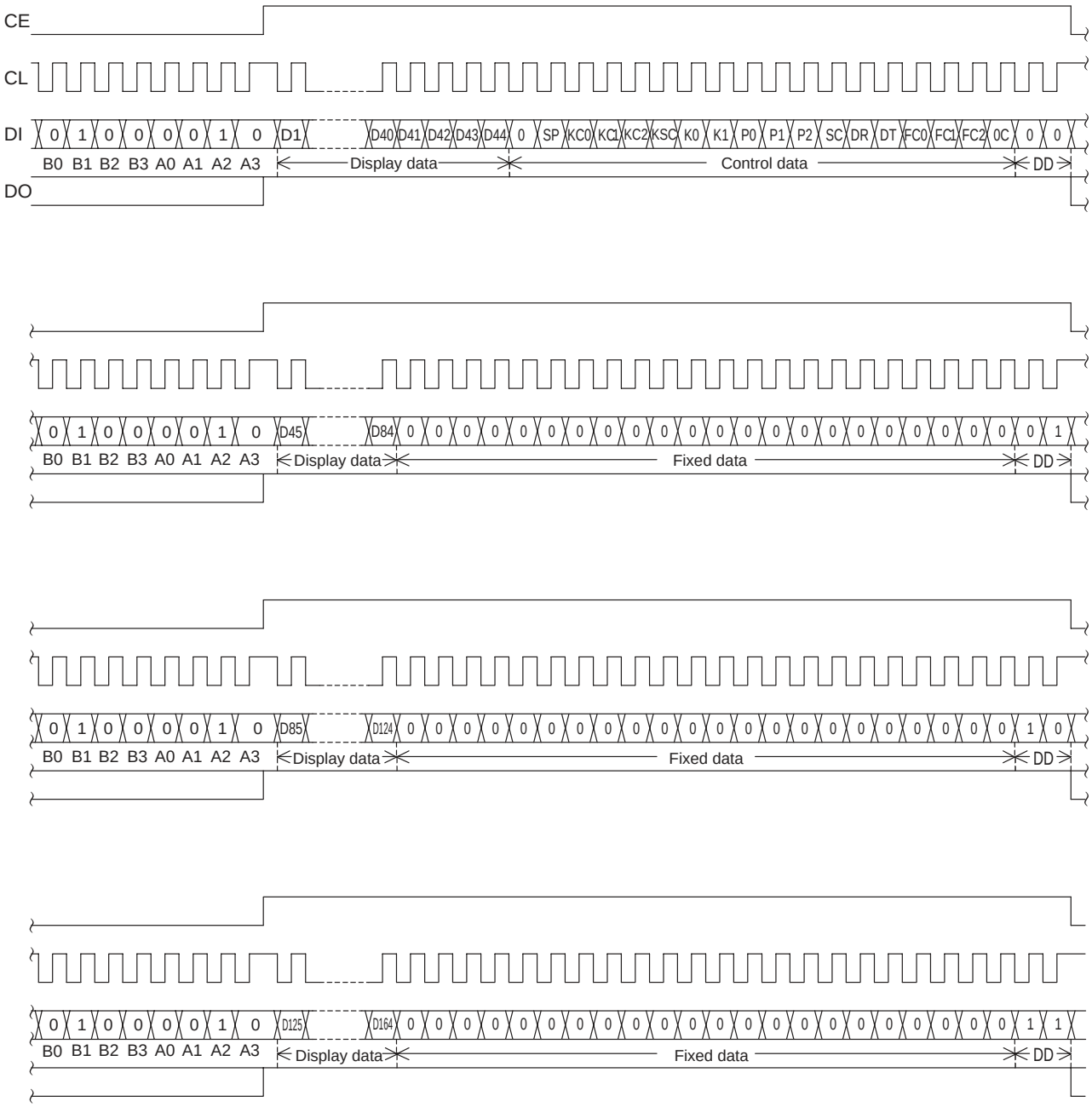
2. 1/4duty

(1) When CL is stopped at the low level



Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

(2) When CL is stopped at the high level



Note: B0 to B3, A0 to A3 ····· CCB address
DD····· Direction data

CCB address····· 42H
D1 to D164 ····· Display data
SP ····· Normal mode/sleep mode control data
KC0 to KC2 ····· Key scan output state setting data
KSC····· Key scan operation enabled/disabled state setting data
K0, K1 ····· Key scan output/segment output selection data
P0 to P2 ····· Segment output port/general-purpose output port selection data
SC ····· Segment on/off control data
DR····· 1/2 bias or 1/3 bias drive selection data
DT ····· 1/3 duty or 1/4 duty drive selection data
FC0 to FC2 ····· Common and segment output waveform frame frequency setting data
OC····· RC oscillator mode/external clock mode switching selection data

Control Data Functions

1. SP : Normal mode/sleep mode control data
   This control data bit switches the IC between normal mode and sleep mode.

SP	Mode	OSC pin state		Common and segment pin output states	Key scan operating state	General-purpose output port states
		RC oscillator mode	External clock mode			
0	Normal	Oscillator operating	External clock signal accepted	LCD drive waveforms are output	The state can be set	The state can be set
1	sleep	Oscillator stopped (The oscillator operates during key scan operations.)	Acceptance of the external clock signal is disabled. (The external clock signal is accepted during key scan operations)	L (VSS)		

Note: See the descriptions of the KC- to KC2, KSC, K0, K1, and P0 to P2 bits in the control data for details on setting the key scan operating state and setting the general-purpose output port state.

2. KC0 to KC2 : Key scan output state setting data
   These control data bits set the states of the key scan output pins KS1 to KS6.

Control data			Output pin states during key scan standby					
KC0	KC1	KC2	KS1	KS2	KS3	KS4	KS5	KS6
0	0	0	H	H	H	H	H	H
0	0	1	L	H	H	H	H	H
0	1	0	L	L	H	H	H	H
0	1	1	L	L	L	H	H	H
1	0	0	L	L	L	L	H	H
1	0	1	L	L	L	L	L	H
1	1	0	L	L	L	L	L	L

Note: This assumes that the KS1/S40 to KS3/S42 output pins are selected for key scan output.
Also note that key scan output signals are not output from output pins that are set to the low level.

3. KSC : Key scan operation enabled/disabled state setting data
   This control data bit enables or disables key scan operation.

KSC	Key scan operating state
0	Key scan operation enabled (A key scan operation is performed if any key on the lines corresponding to KS1 to KS6 pin which is set high is pressed .)
1	Key scan operation disabled (No key scan operation is performed, even if any of the keys in the key matrix are pressed. If this state is set up, the key data is forcibly reset to 0 and the key data read request is also cleared. (DO is set high.))

4. K0, K1 : Key scan output /segment output selection data
   These control data bits switch the functions of the KS1/S40 to KS3/S42 output pins between key scan output and segment output.

Control data		Output pin state			Maximum number of input keys
K0	K1	KS1/S40	KS2/S41	KS3/S42	
0	0	KS1	KS2	KS3	30
0	1	S40	KS2	KS3	25
1	0	S40	S41	KS3	20
1	1	S40	S41	S42	15

Note: KSn(n = 1 to 3) : Key scan output
Sn (n = 40 to 42): Segment output

5. P0 to P2 : Segment output port/general-purpose output port selection data
   These control data bits switch the functions of the S1/P1 to S4/P4 output pins between the segment output port and the general-purpose output port.

Control data			Output pin state			
P0	P1	P2	S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4

Note: Sn(n=1 to 4): Segment output port
Pn(n=1 to 4): General-purpose output port

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports.

Output pin	Corresponding display data	
	1/3 duty	1/4 duty
S1/P1	D1	D1
S2/P2	D4	D5
S3/P3	D7	D9
S4/P4	D10	D13

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port, the S4/P4 output pin will output a high level (V_{LCD}) when the display data D13 is 1, and will output a low level (Vss) when D13 is 0.

6. SC : Segment on/off control data
   This control data bit controls the on/off state of the segments.

SC	Display state
0	on
1	off

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

7. DR : 1/2 bias or 1/3 bias drive selection data
   This control data bit switches between LCD 1/2 bias or 1/3 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

8. DT : 1/3 duty or 1/4 duty drive selection data
   This control data bit switches between LCD 1/3 duty or 1/4 duty drive.

DT	Duty drive scheme	Output pin state (COM4/S39)
0	1/4 duty drive	COM4
1	1/3 duty drive	S39

Note: COM4: Common output
S39 : Segment output

9. FC0 to FC2 : Common and segment output waveform frame frequency setting data
   These control data bits set the common and segment output waveform frequency.

Control data			Frame frequency, fo (Hz)
FC0	FC1	FC2	
0	0	0	$f_{OSC}/768$, $f_{CK}/768$
0	0	1	$f_{OSC}/576$, $f_{CK}/576$
0	1	0	$f_{OSC}/384$, $f_{CK}/384$
0	1	1	$f_{OSC}/288$, $f_{CK}/288$
1	0	0	$f_{OSC}/192$, $f_{CK}/192$

10. OC : RC oscillator mode/external clock mode switching selection data
    This control data bit selects the OSC pin function (RC oscillator mode or external clock mode).

OC	OSC pin function
0	RC oscillator mode
1	External clock mode

Note: If RC oscillator mode is selected, connect an external resistor Rosc and an external capacitor Cosc to the OSC pin.

Display Data and Output Pin Correspondence

1. 1/3 duty

Output pin	COM1	COM2	COM3	Output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3	S22	D64	D65	D66
S2/P2	D4	D5	D6	S23	D67	D68	D69
S3/P3	D7	D8	D9	S24	D70	D71	D72
S4/P4	D10	D11	D12	S25	D73	D74	D75
S5	D13	D14	D15	S26	D76	D77	D78
S6	D16	D17	D18	S27	D79	D80	D81
S7	D19	D20	D21	S28	D82	D83	D84
S8	D22	D23	D24	S29	D85	D86	D87
S9	D25	D26	D27	S30	D88	D89	D90
S10	D28	D29	D30	S31	D91	D92	D93
S11	D31	D32	D33	S32	D94	D95	D96
S12	D34	D35	D36	S33	D97	D98	D99
S13	D37	D38	D39	S34	D100	D101	D102
S14	D40	D41	D42	S35	D103	D104	D105
S15	D43	D44	D45	S36	D106	D107	D108
S16	D46	D47	D48	S37	D109	D110	D111
S17	D49	D50	D51	S38	D112	D113	D114
S18	D52	D53	D54	COM4/S39	D115	D116	D117
S19	D55	D56	D57	KS1/S40	D118	D119	D120
S20	D58	D59	D60	KS2/S41	D121	D122	D123
S21	D61	D62	D63	KS3/S42	D124	D125	D126

Note: This is for the case where the output pins S1/P1 to S4/P4, COM4/S74, KS1/S40 to KS3/S42 are selected for use as segment outputs.

For example, the table below lists the segment output states for the S11 output pin.

Display data			Output pin state (S11)
D31	D32	D33	
0	0	0	The LCD segments for COM1, COM2 and COM3 are off.
0	0	1	The LCD segment for COM3 is on.
0	1	0	The LCD segment for COM2 is on.
0	1	1	The LCD segments for COM2 and COM3 are on.
1	0	0	The LCD segment for COM1 is on.
1	0	1	The LCD segments for COM1 and COM3 are on.
1	1	0	The LCD segments for COM1 and COM2 are on.
1	1	1	The LCD segments for COM1, COM2 and COM3 are on.

2. 1/4 duty

Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5	D17	D18	D19	D20
S6	D21	D22	D23	D24
S7	D25	D26	D27	D28
S8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84

Output pin	COM1	COM2	COM3	COM4
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
KS1/S40	D153	D154	D155	D156
KS2/S41	D157	D158	D159	D160
KS3/S42	D161	D162	D163	D164

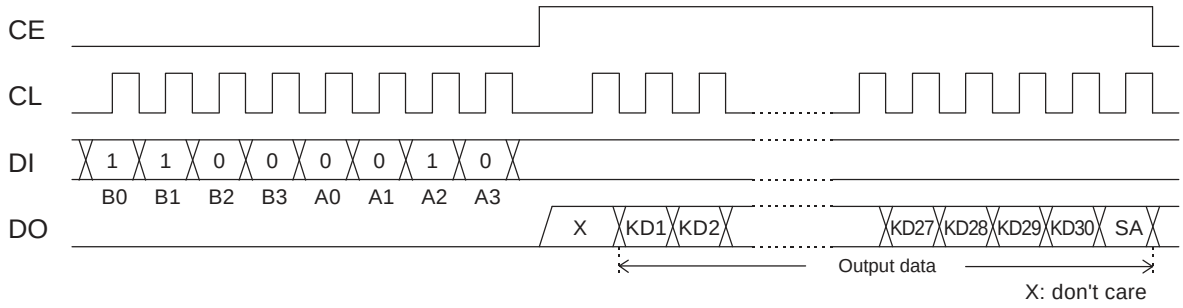
Note: This is for the case where the output pins S1/P1 to S4/P4, KS1/S40 to KS3/S42 are selected for use as segment outputs.

For example, the table below lists the segment output states for the S11 output pin.

Display data				Output pin state (S11)
D41	D42	D43	D44	
0	0	0	0	The LCD segments for COM1,COM2,COM3 and COM4 are off.
0	0	0	1	The LCD segment for COM4 is on.
0	0	1	0	The LCD segment for COM3 is on.
0	0	1	1	The LCD segments for COM3 and COM4 are on.
0	1	0	0	The LCD segment for COM2 is on.
0	1	0	1	The LCD segments for COM2 and COM4 are on.
0	1	1	0	The LCD segments for COM2 and COM3 are on.
0	1	1	1	The LCD segments for COM2,COM3 and COM4 are on.
1	0	0	0	The LCD segment for COM1 is on.
1	0	0	1	The LCD segments for COM1 and COM4 are on.
1	0	1	0	The LCD segments for COM1 and COM3 are on.
1	0	1	1	The LCD segments for COM1,COM3 and COM4 are on.
1	1	0	0	The LCD segments for COM1 and COM2 are on.
1	1	0	1	The LCD segments for COM1,COM2 and COM4 are on.
1	1	1	0	The LCD segments for COM1,COM2 and COM3 are on.
1	1	1	1	The LCD segments for COM1,COM2,COM3 and COM4 are on.

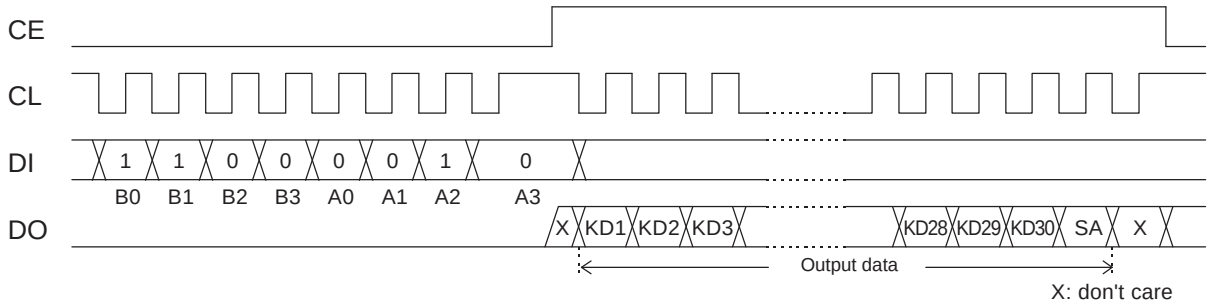
Serial Data Output

1. When CL is stopped at the low level



Note: B0 to B3, A0 to A3·····CCB address

2. When CL is stopped at the high level



Note: B0 to B3, A0 to A3·····CCB address

CCB address ····· 43H
KD1 to KD30····· Key data
SA····· Sleep acknowledge data

Note: If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data(SA) will be invalid.

Output Data

1. KD1 to KD30 : Key data
   When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

	KI1	KI2	KI3	KI4	KI5
KS1/S40	KD1	KD2	KD3	KD4	KD5
KS2/S41	KD6	KD7	KD8	KD9	KD10
KS3/S42	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

   When the KS1/S40 and KS2/S41 output pins are selected to be segment outputs by control data bits K0 and K1 and a key matrix of up to 20 keys is formed using the KS3/S42,KS4 to KS6 output pins and the KI1 to KI5 input pins, the KD1 to KD10 key data bits will be set to 0.

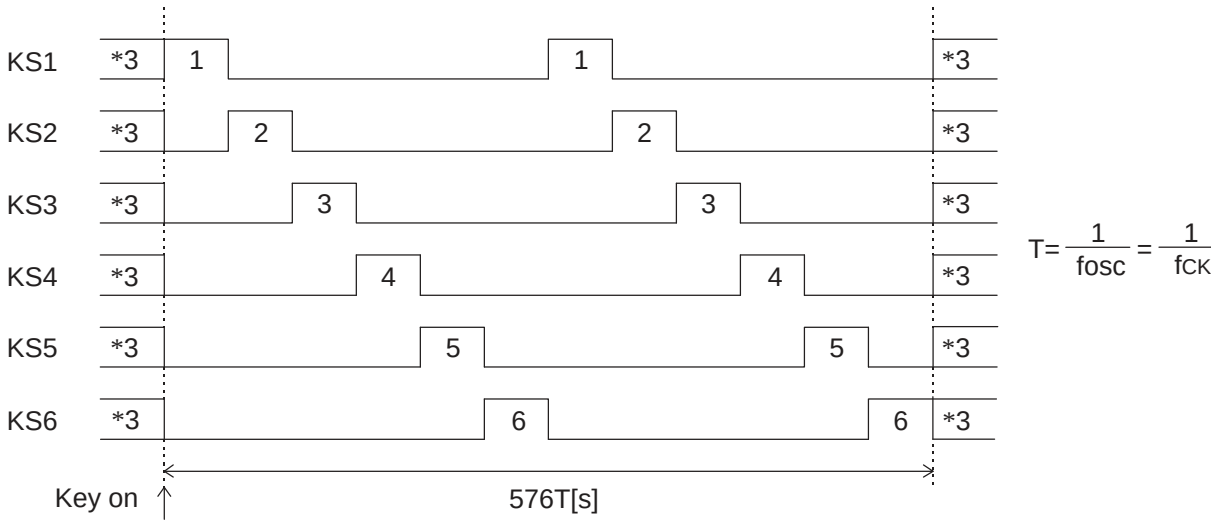
2. SA : Sleep acknowledge data
   This output data bit is set to the state when the key was pressed. Also, while DO will be low in this case, if serial data is input and the mode is set (to normal or sleep mode) during this period, that mode will be set. SA will be 1 in sleep mode and 0 in normal mode.

Sleep Mode Functions

Sleep mode is set up by setting SP in the control data to 1. When sleep mode is set up, both the segment and the common outputs will go to the low level. In RC oscillator mode (OC = 0), the oscillator on the OSC pin will stop (although it will operate during key scan operations), and in external clock mode (OC = 1), the external clock signal reception on the OSC pin will stop (although the clock signal will be received during key scan operations). Thus this mode reduces power consumption. However, the S1/P1 to S4/P4 output pins can be used as general-purpose output ports under control of the P0 to P2 bits in the control data even in sleep mode. Sleep mode is cancelled by setting SP in the control data to 0.

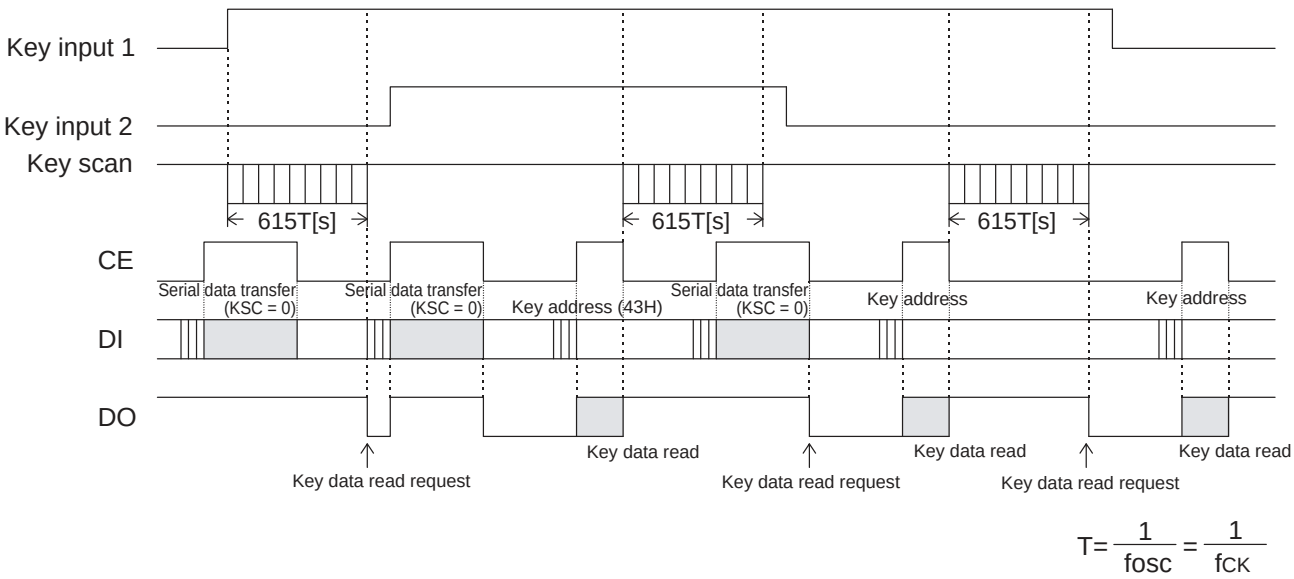
Key Scan Operation Functions

1. Key scan timing
   The key scan period is 288T(s). To reliably determine the on/off state of the keys, the LC75857E/W scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) 615T(s) after starting a key scan. If the key data dose not agree and a key was pressed at that point, it scans the keys again. Thus the LC75857E/W cannot detect a key press shorter than 615T(s).



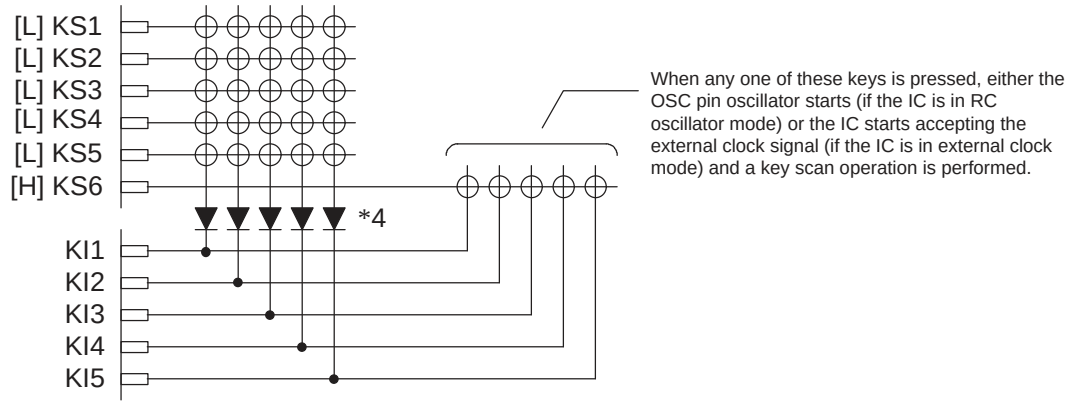
Note: *3. These are set to the high or low level by the KC0 to KC2 bits in the control data. Key scan output signals are not output from pins that are set to the low level.

2. Normal mode, when key scan operations are enabled
   - The KS1 to KS6 pins are set to the high or low level by the KC0 to KC2 bits in the control data. (See the description of the control data.)
   - When any key on the lines corresponding to KS1 to KS6 pin which is set high is pressed, a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
   - If a key is pressed for longer than 615 T (s) (Where T= $\frac{1}{fosc} = \frac{1}{fCK}$) the LC75857E/W outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
   - After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75857E/W performes another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 to 10 kΩ).

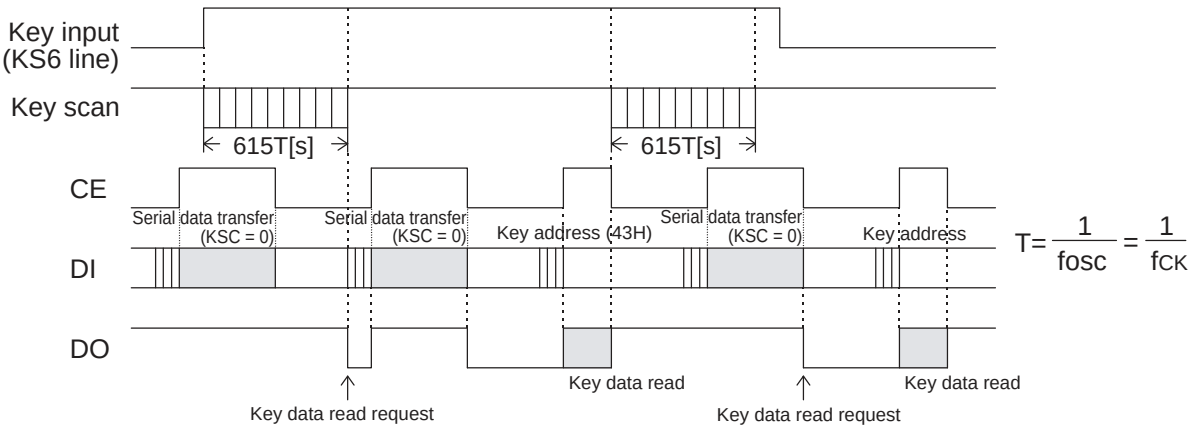


3. Sleep mode, when key scan operations are enabled
   - The KS1 to KS6 pins are set to the high or low level by the KC0 to KC2 bits in the control data. (See the description of the control data.)
   - When any key on the lines corresponding to KS1 to KS6 pin which is set high is pressed, either the OSC pin oscillator starts (if the IC is in RC oscillator mode) or the IC starts accepting the external clock signal (if the IC is in external clock mode), a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recoghized by determinig whether multiple key data bits are set.
   - If a key is pressed for longer than 615T(s)(Where $T=\frac{1}{fosc}=\frac{1}{f_{CK}}$) the LC75857E/W outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
   - After the controller reads the key data, the key data read request is cleared (DO is set high) and the LC75857E/W performs another key scan. However, this dose not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10 kΩ).
   - Sleep mode key scan example

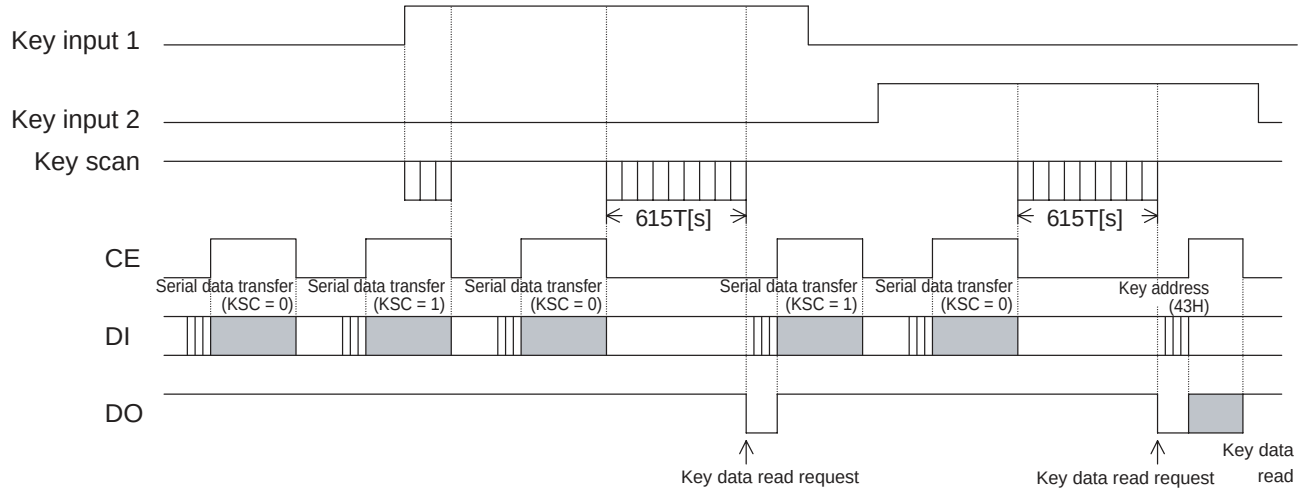
Example: KC0 = 1, KC1 = 0, KC2 = 1, (sleep with only KS6 high)



Note: *4. These diodes are required to reliable recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



4. Normal/sleep mode, when key scan operations are disabled
   - The KS1 to KS6 pins are set to the high or low level by the KC0 to KC2 bits in the control data.
   - No key scan operation is performed, whichever key is pressed.
   - If the key scan disabled state (KSC = 1 in the control data) is set during a key scan, the key scan is stopped.
   - If the key scan disabled state (KSC = 1 in the control data) is set when a key data read request (a low level on DO) is output to the controller, all the key data is set to 0 and the key data read request is cleared (DO is set high). Note that DO, being an open-drain output, requires a pull-up resister (between 1 to 10 kΩ).
   - The key scan disabled state is cleared by setting KSC in the control data to 0.

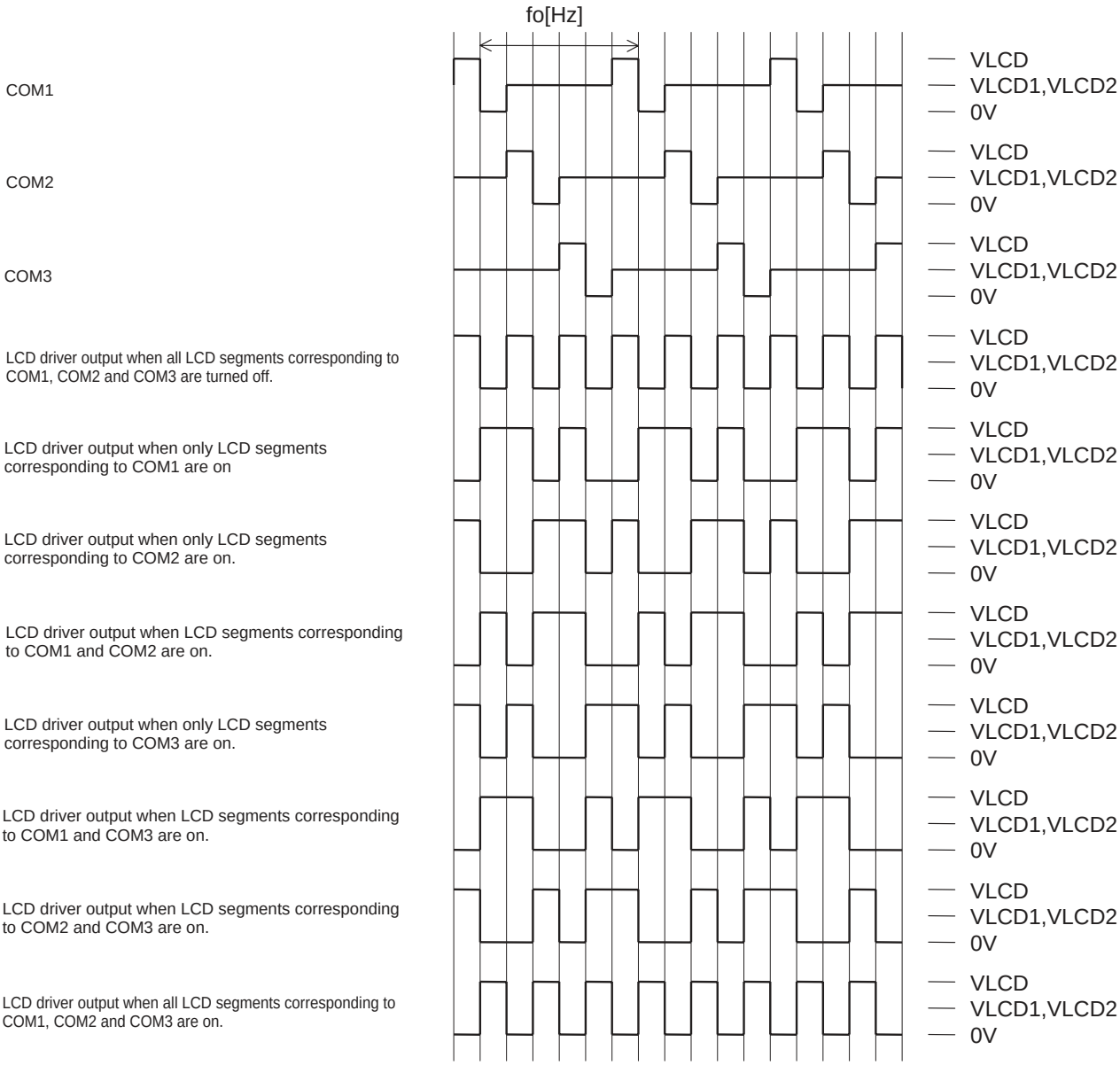


$$T = \frac{1}{fosc} = \frac{1}{fCK}$$

Multiple Key Presses

Although the LC75857E/W is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bits and ignore such data.

1/3 Duty, 1/2 Bias Drive Technique



1/3 Duty, 1/2 Bias Waveforms

Note: When FC0 = 0, FC1 = 0, and FC2 = 0 in the control data $f_0 = \frac{f_{osc}}{768} = \frac{f_{CK}}{768}$

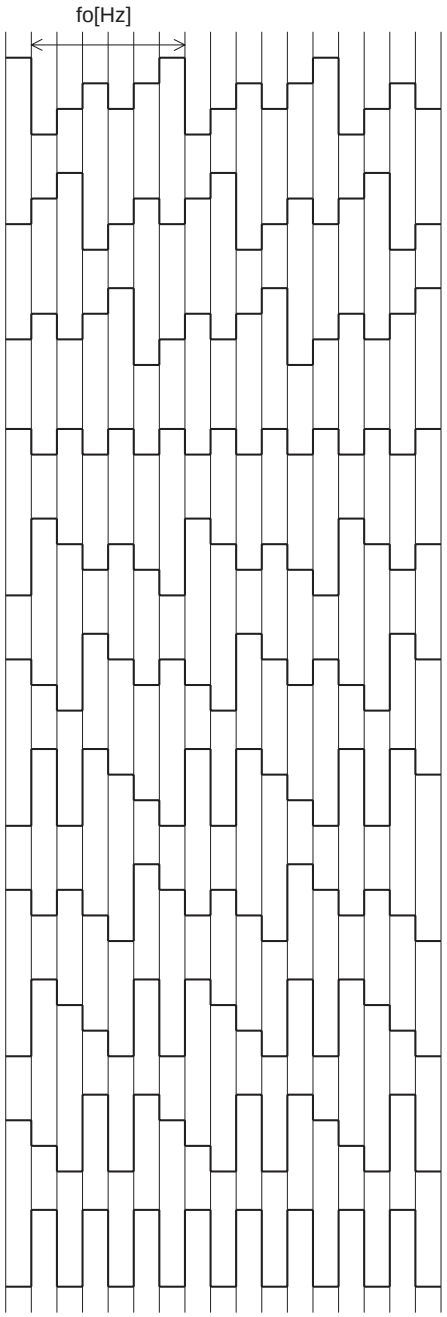
When FC0 = 0, FC1 = 0, and FC2 = 1 in the control data $f_0 = \frac{f_{osc}}{576} = \frac{f_{CK}}{576}$

When FC0 = 0, FC1 = 1, and FC2 = 0 in the control data $f_0 = \frac{f_{osc}}{384} = \frac{f_{CK}}{384}$

When FC0 = 0, FC1 = 1, and FC2 = 1 in the control data $f_0 = \frac{f_{osc}}{288} = \frac{f_{CK}}{288}$

When FC0 = 1, FC1 = 0, and FC2 = 0 in the control data $f_0 = \frac{f_{osc}}{192} = \frac{f_{CK}}{192}$

1/3 Duty, 1/3 Bias Drive Technique



COM1

COM2

COM3

LCD driver output when all LCD segments corresponding to COM1, COM2 and COM3 are turned off.

LCD driver output when only LCD segments corresponding to COM1 are on.

LCD driver output when only LCD segments corresponding to COM2 are on.

LCD driver output when LCD segments corresponding to COM1 and COM2 are on.

LCD driver output when only LCD segments corresponding to COM3 are on.

LCD driver output when LCD segments corresponding to COM1 and COM3 are on.

LCD driver output when LCD segments corresponding to COM2 and COM3 are on.

LCD driver output when all LCD segments corresponding to COM1, COM2 and COM3 are on.

1/3 Duty, 1/3 Bias Waveforms

Note: When FC0 = 0, FC1 = 0, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{768} = \frac{f_{CK}}{768}$

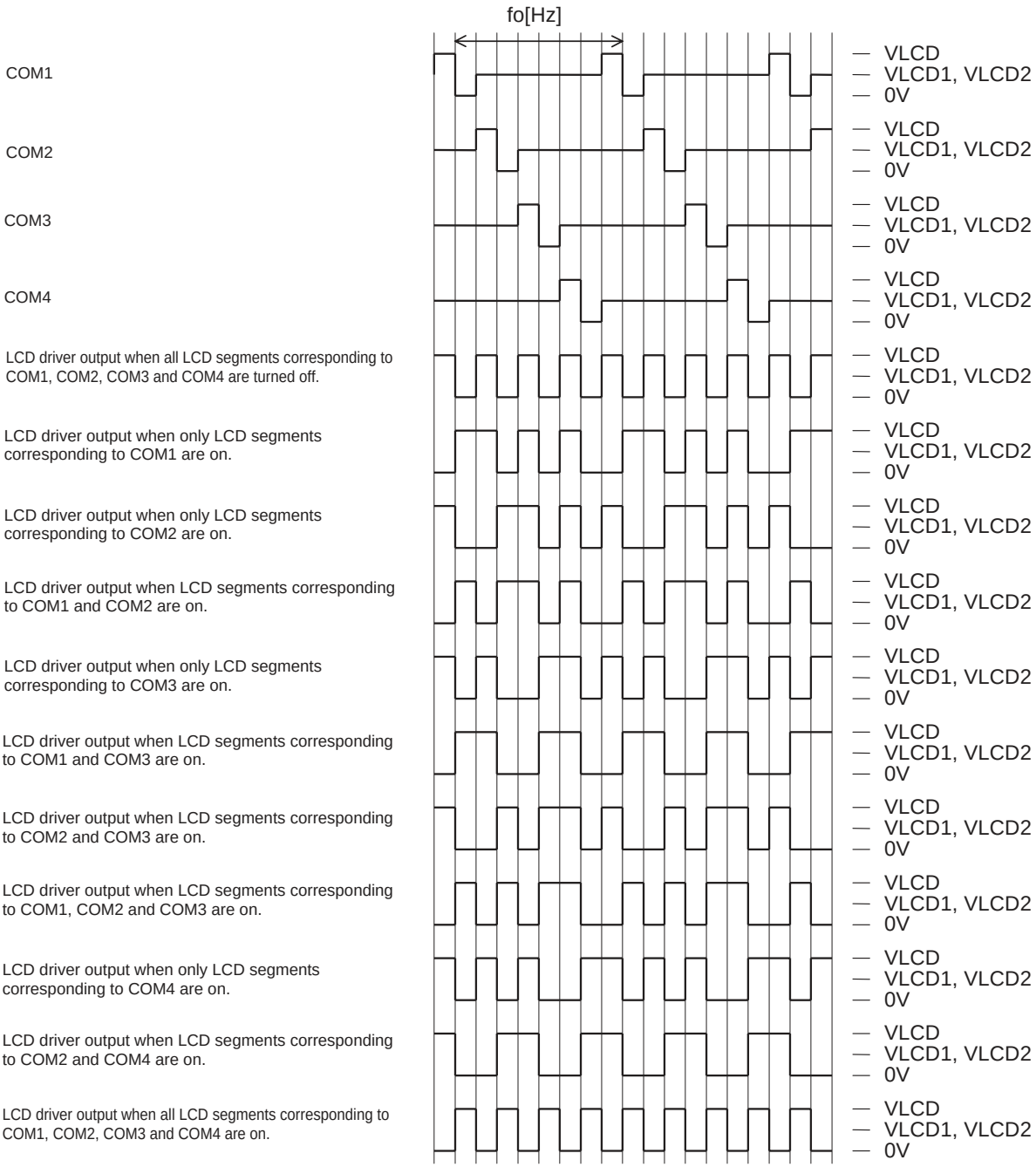
When FC0 = 0, FC1 = 0, and FC2 = 1 in the control data $f_0 = \frac{f_{OSC}}{576} = \frac{f_{CK}}{576}$

When FC0 = 0, FC1 = 1, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{384} = \frac{f_{CK}}{384}$

When FC0 = 0, FC1 = 1, and FC2 = 1 in the control data $f_0 = \frac{f_{OSC}}{288} = \frac{f_{CK}}{288}$

When FC0 = 1, FC1 = 0, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{192} = \frac{f_{CK}}{192}$

1/4 Duty, 1/2 Bias Drive Technique



1/4 Duty, 1/2 Bias Waveforms

Note: When FC0 = 0, FC1 = 0, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{768} = \frac{f_{CK}}{768}$

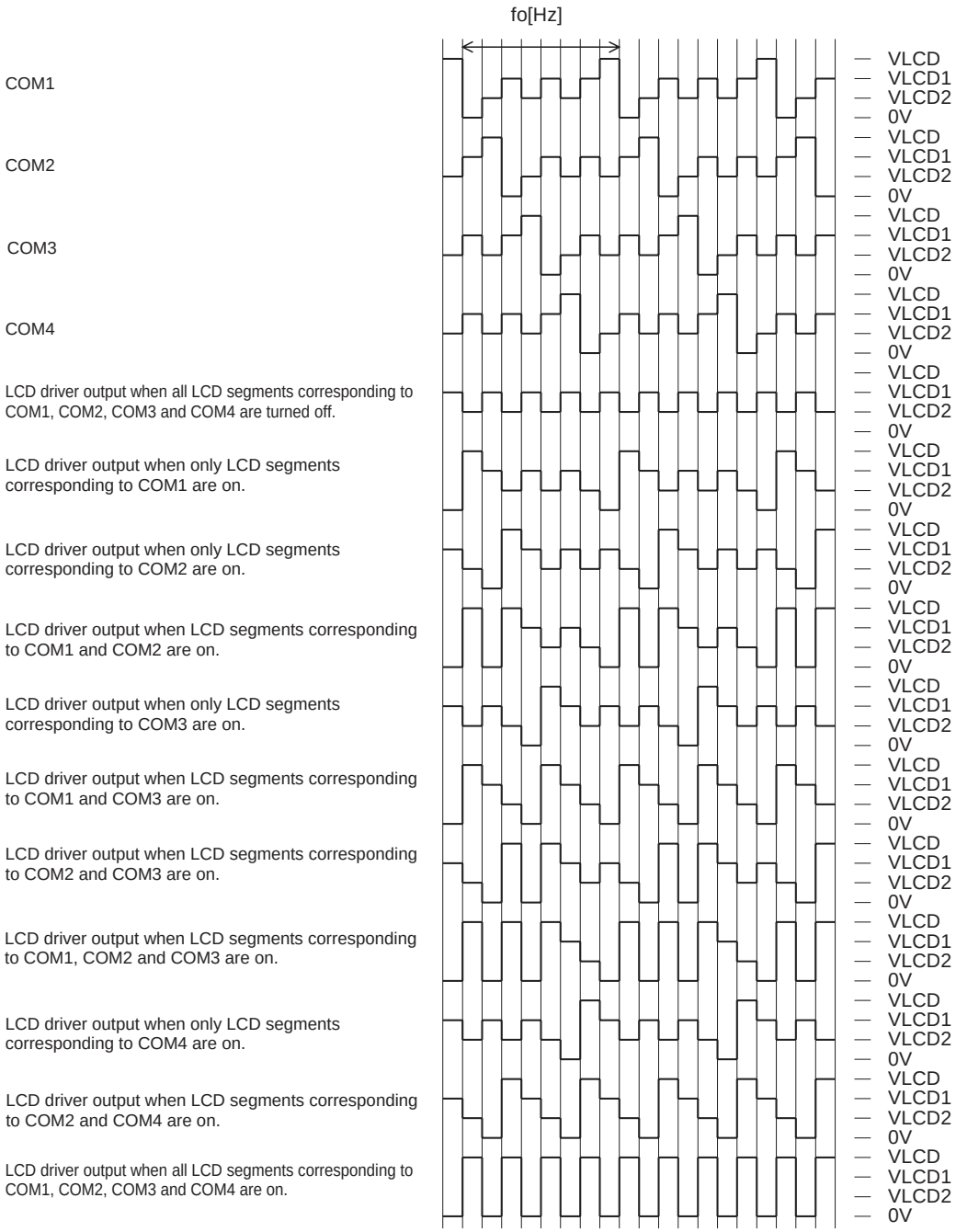
When FC0 = 0, FC1 = 0, and FC2 = 1 in the control data $f_0 = \frac{f_{OSC}}{576} = \frac{f_{CK}}{576}$

When FC0 = 0, FC1 = 1, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{384} = \frac{f_{CK}}{384}$

When FC0 = 0, FC1 = 1, and FC2 = 1 in the control data $f_0 = \frac{f_{OSC}}{288} = \frac{f_{CK}}{288}$

When FC0 = 1, FC1 = 0, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{192} = \frac{f_{CK}}{192}$

1/4 Duty, 1/3 Bias Drive Technique



1/4 Duty, 1/3 Bias Waveforms

Note: When FC0 = 0, FC1 = 0, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{768} = \frac{f_{CK}}{768}$

When FC0 = 0, FC1 = 0, and FC2 = 1 in the control data $f_0 = \frac{f_{OSC}}{576} = \frac{f_{CK}}{576}$

When FC0 = 0, FC1 = 1, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{384} = \frac{f_{CK}}{384}$

When FC0 = 0, FC1 = 1, and FC2 = 1 in the control data $f_0 = \frac{f_{OSC}}{288} = \frac{f_{CK}}{288}$

When FC0 = 1, FC1 = 0, and FC2 = 0 in the control data $f_0 = \frac{f_{OSC}}{192} = \frac{f_{CK}}{192}$

Voltage Detection Type Reset Circuit (VDET)

This circuit generates an output signal and resets the system when logic block power is first applied and when the voltage drops, i.e., when the logic block power supply voltage is less than or equal to the power down detection voltage VDET, which is 2.2V, typical. To assure that this function operates reliably, a capacitor must be added to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when the logic block power is first applied and the logic block power supply voltage V_{DD} fall time when the voltage drops are both at least 1 ms. (See Figure 5 and Figure 6.)

Power Supply Sequence

The following sequences must be observed when power is turned on and off. (See Figure 5 and Figure 6.)

- Power on :Logic block power supply(V_{DD}) on → LCD driver block power supply(V_{LCD}) on
- Power off:LCD driver block power supply(V_{LCD}) off → Logic block power supply(V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

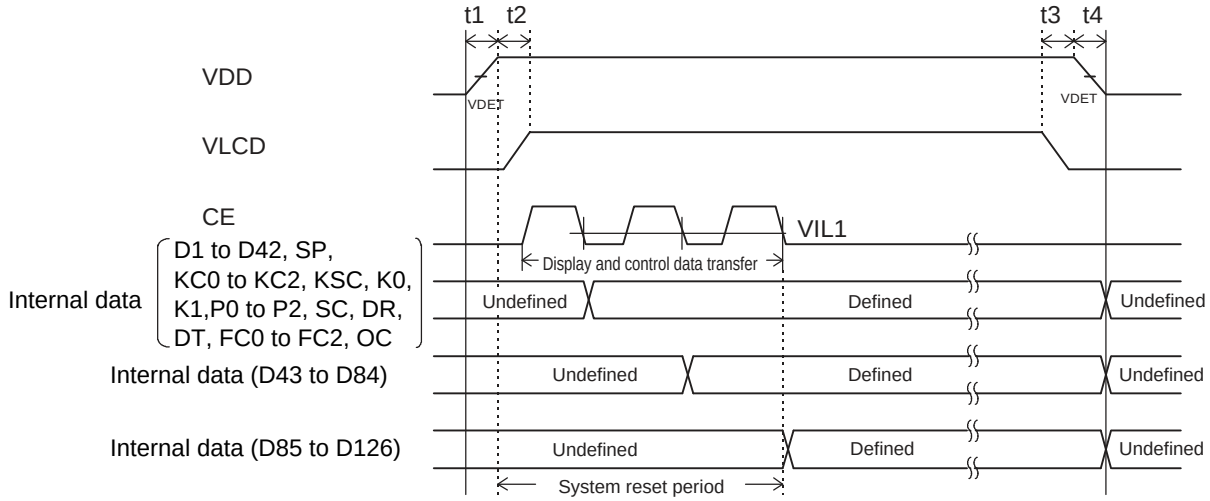
System Reset

The LC75857E/W supports the reset methods described below. When a system reset is applied, display is turned off, key scanning is stopped, and all the key data is reset to low. When the reset is cleared, display is turned on and key scanning become possible.

1. Reset methods

   If at least 1 ms is assured as the logic block supply voltage V_{DD} rise time when logic block power is applied, a system reset will be applied by the VDET output signal when the logic block supply voltage is brought up. If at least 1 ms is assured as the logic block supply voltage V_{DD} fall time when logic block power drops, a system reset will be applied in the same manner by the VDET output signal when the supply voltage is lowered. Note that the reset is cleared at the point when all the serial data (1/3 duty: the display data D1 to D126 and the control data, 1/4 duty: the display data D1 to D164 and the control data) has been transferred, i.e., on the fall of the CE signal on the transfer of the last direction data, after all the direction data has been transferred. (See Figure 5 and Figure 6.)

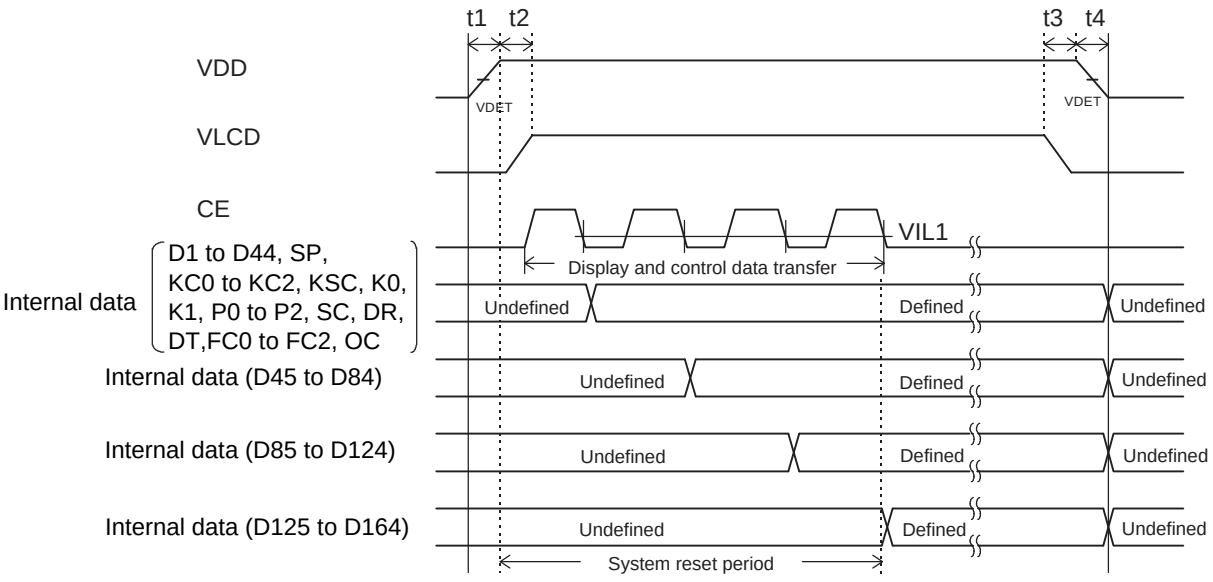
• 1/3 duty



Note: t1 ≥ 1 [ms] (Logic block power supply voltage V_{DD} rise time)
t2 ≥ 0
t3 ≥ 0
t4 ≥ 1 [ms] (Logic block power supply voltage V_{DD} fall time)

Figure 5

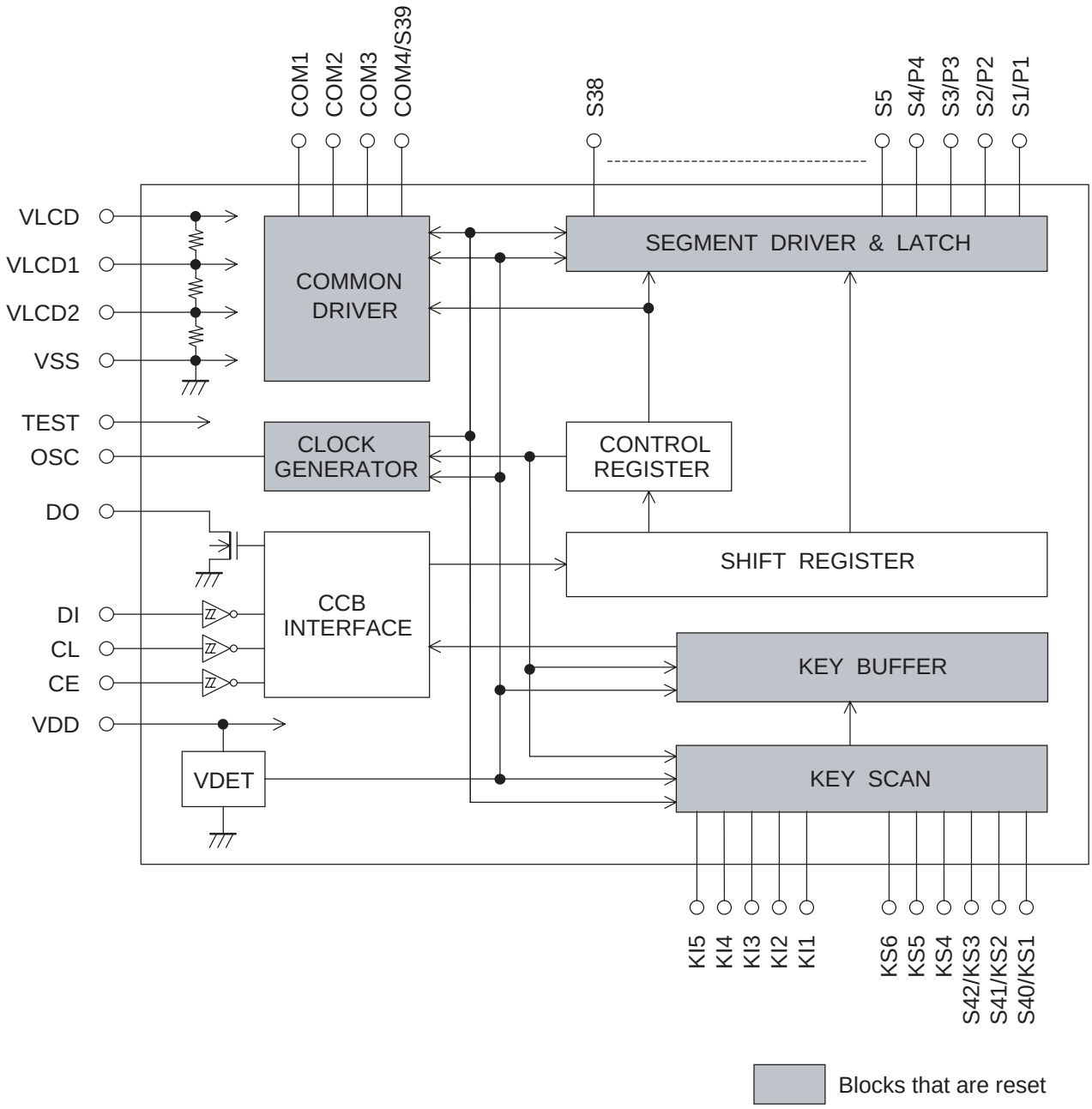
• 1/4 duty



Note: t1 ≥ 1 [ms] (Logic block power supply voltage V_{DD} rise time)
t2 ≥ 0
t3 ≥ 0
t4 ≥ 1 [ms] (Logic block power supply voltage V_{DD} fall time)

Figure 6

2. LC75857E/W internal block states during the reset period
   - CLOCK GENERATOR
     A reset is applied and either the OSC pin oscillator is stopped or external clock input is stopped.
   - COMMON DRIVER, SEGMENT DRIVER & LATCH
     Reset is applied and the display is turned off. However, display data can be input to the latch circuit in this state.
   - KEY SCAN
     Reset is applied, the circuit is set to the initial state, and at the same time the key scan operation is disabled.
   - KEY BUFFER
     Reset is applied and all the key data is set to low.
   - CCB INTERFACE, CONTROL REGISTER, SHIFT REGISTER
     Since serial data transfer is possible, these circuits are not reset.



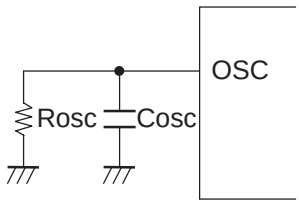
3. Pin states during the reset period

pin	State during reset
S1/P1 to S4/P4	L *5
S5 to S38	L
COM1 to COM3	L
COM4/S39	L *6
KS1/S40 to KS3/S42	L *5
KS4 to KS6	L *7
OSC	Z *8
DO	H *9

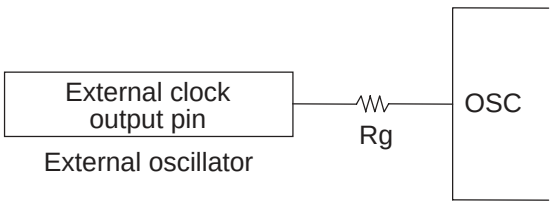
Notes: *5. These output pins are forcibly set to the segment output function and held low.
*6. When power is first applied, this output pin is forcibly set to the common output function and held low. However, when the DT control data bit is transferred, either the common output or the segment output function is selected.
*7. This output pin is forcibly held fixed at the low level.
*8. This I/O pin is forcibly set to the high-impedance state.
*9. Since this output pin is an open-drain output, a pull-up resistor of between 1 and 10 kΩ is required. This pin remains high during the reset period even if a key data read operation is performed.

Notes on the OSC Pin Peripheral Circuit

1. RC oscillator mode (control data bit OC = 0)
When RC oscillator mode is selected, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground.



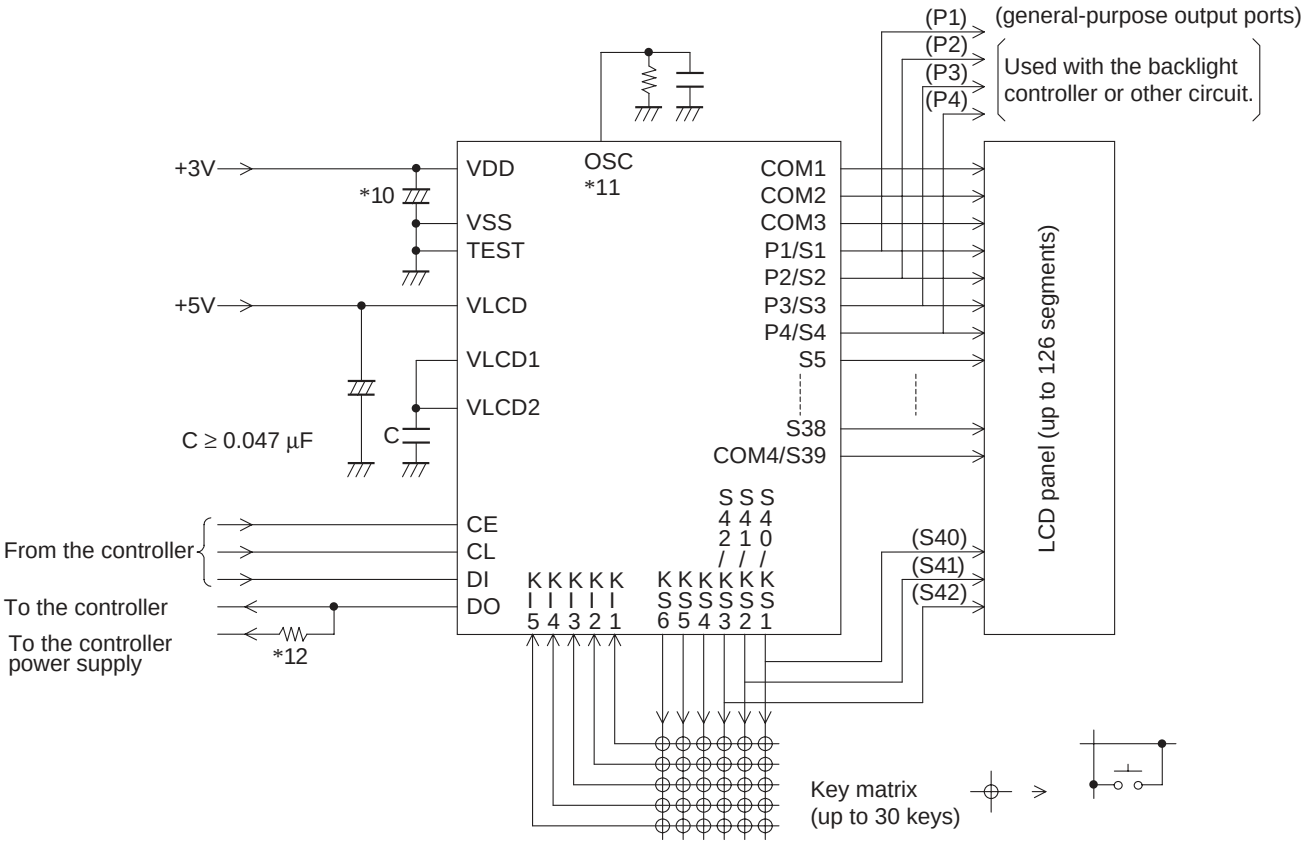
2. External clock mode (control data bit OC = 1)
When external clock mode is selected, the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). The value of this resistor is determined by the allowable current for the external clock output pin. Verify that the external clock waveform is not deformed significantly.



Note: The external clock output pin allowable current must be greater than VDD/Rg.

Sample Application Circuit 1

1/3 duty, 1/2 bias (for use with normal panels)



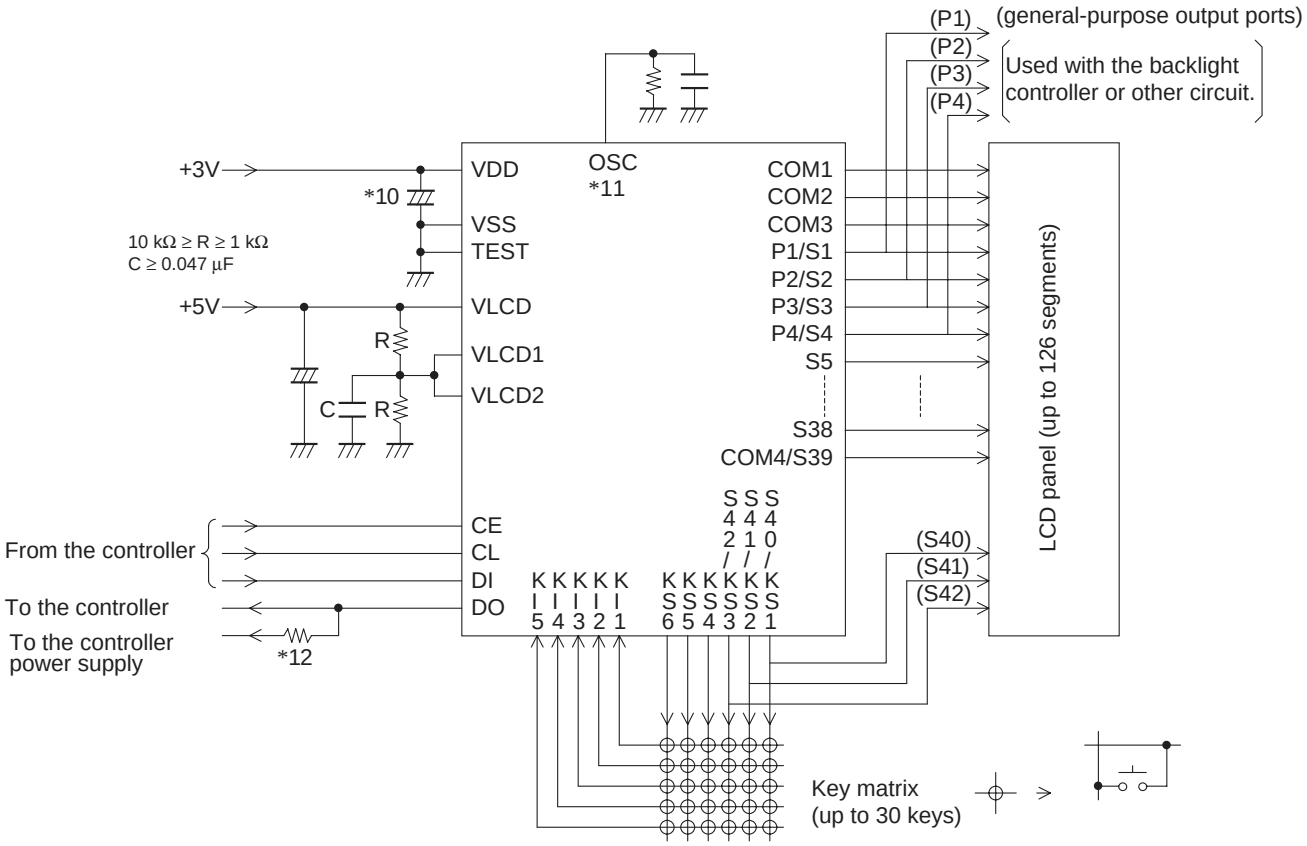
Notes: *10. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75857E/W is reset by the VDET.

*11. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*12. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 2

1/3 duty, 1/2 bias (for use with large panels)



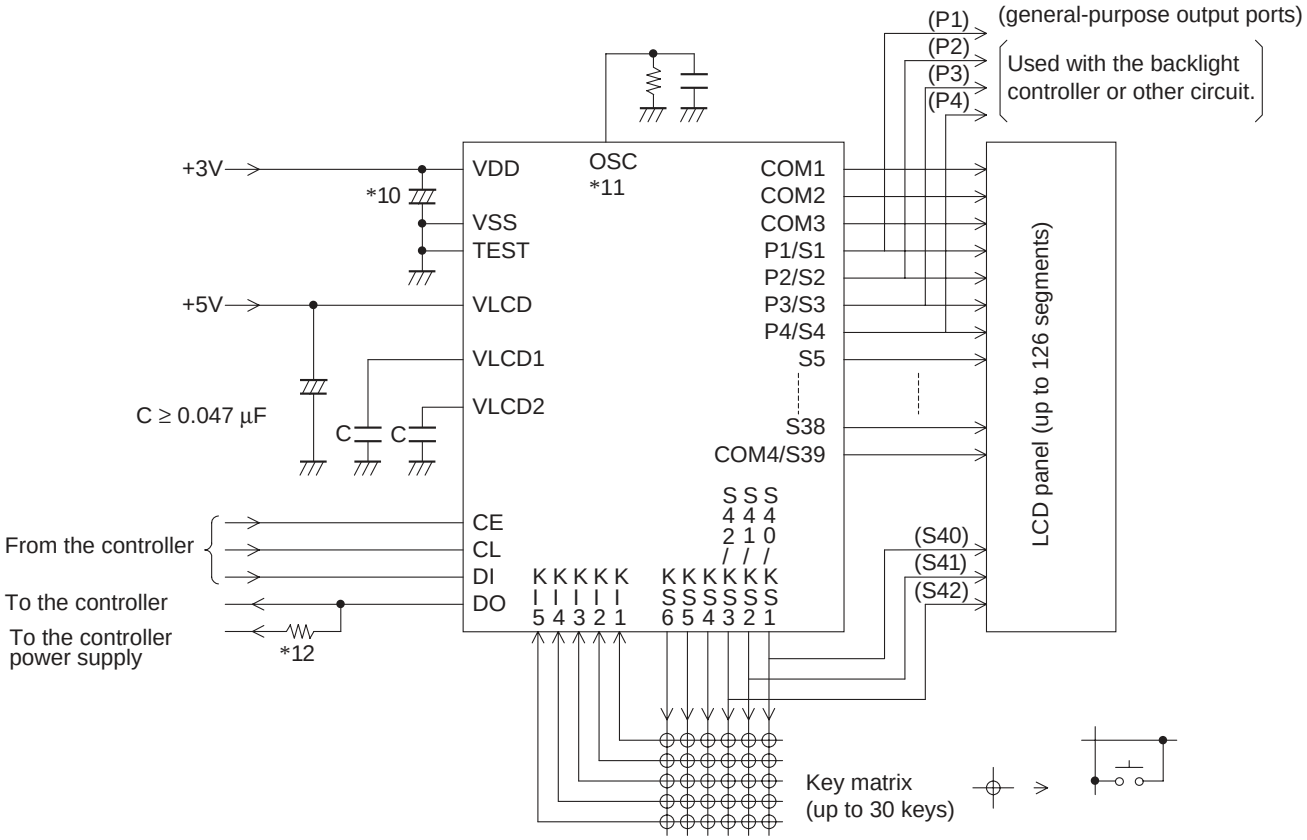
Notes: *10. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75857E/W is reset by the VDET.

*11. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*12. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 3

1/3 duty, 1/3 bias (for use with normal panels)



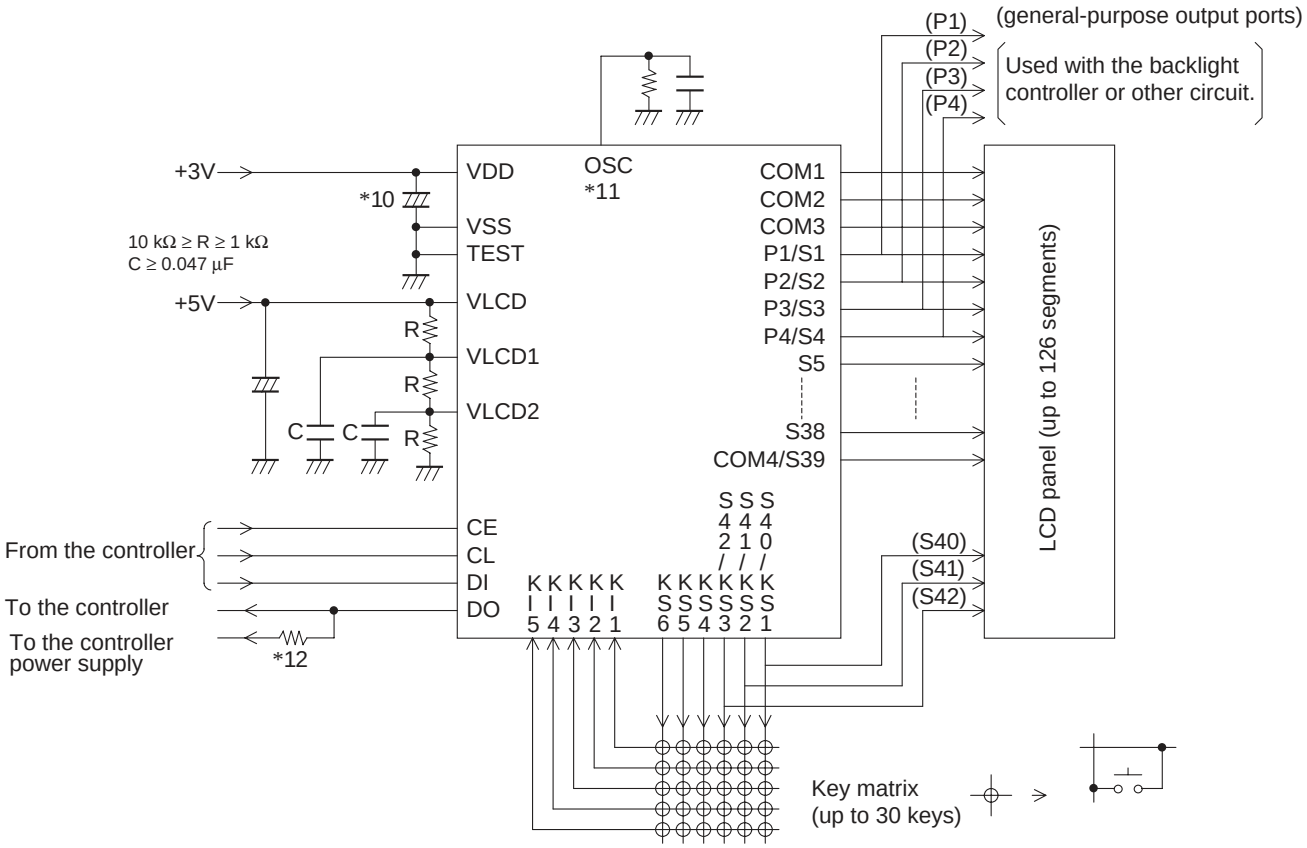
Notes: *10. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75857E/W is reset by the VDET.

*11. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*12. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 4

1/3 duty, 1/3 bias (for use with large panels)



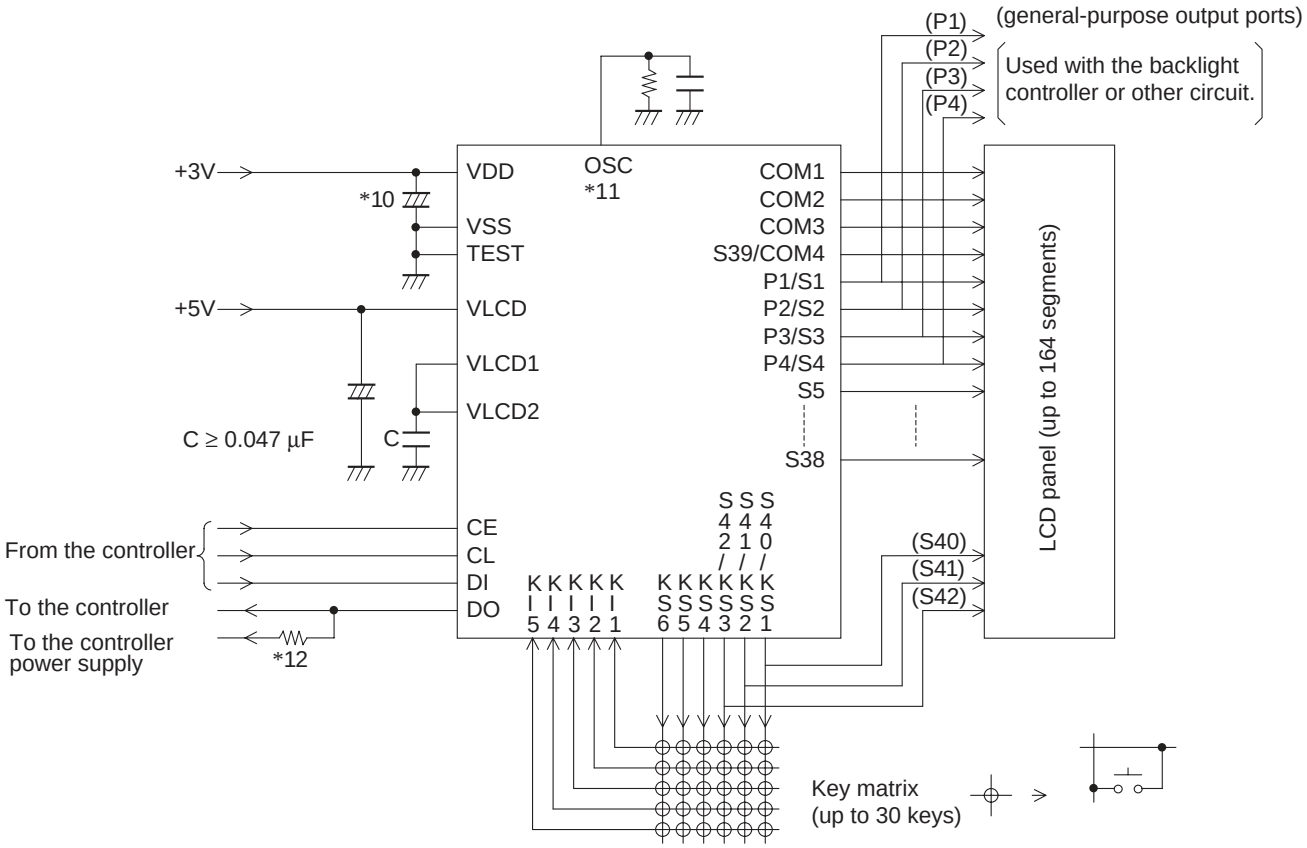
Notes: *10. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75857E/W is reset by the VDET.

*11. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*12. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 5

1/4 duty, 1/2 bias (for use with normal panels)



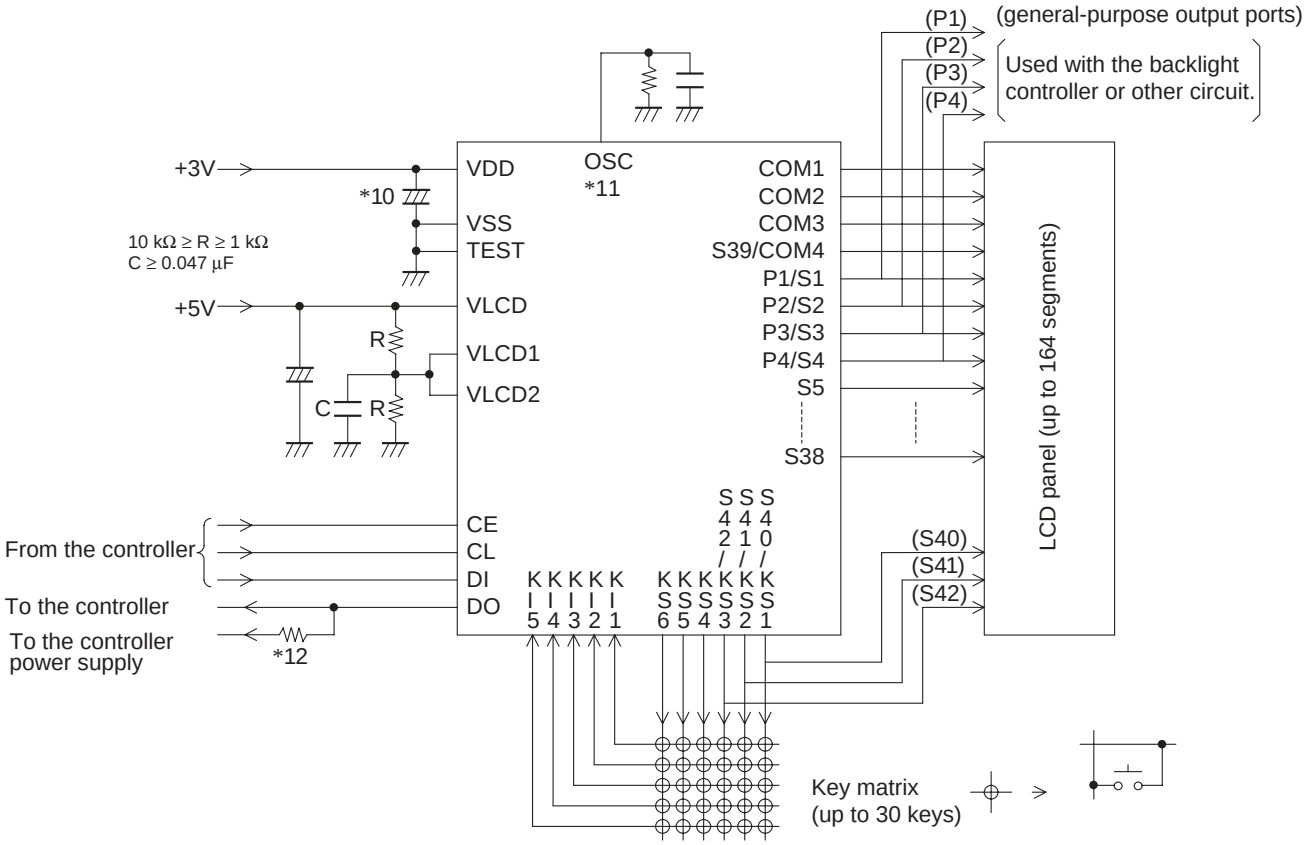
Notes: *10. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75857E/W is reset by the VDET.

*11. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*12. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 6

1/4 duty, 1/2 bias (for use with large panels)



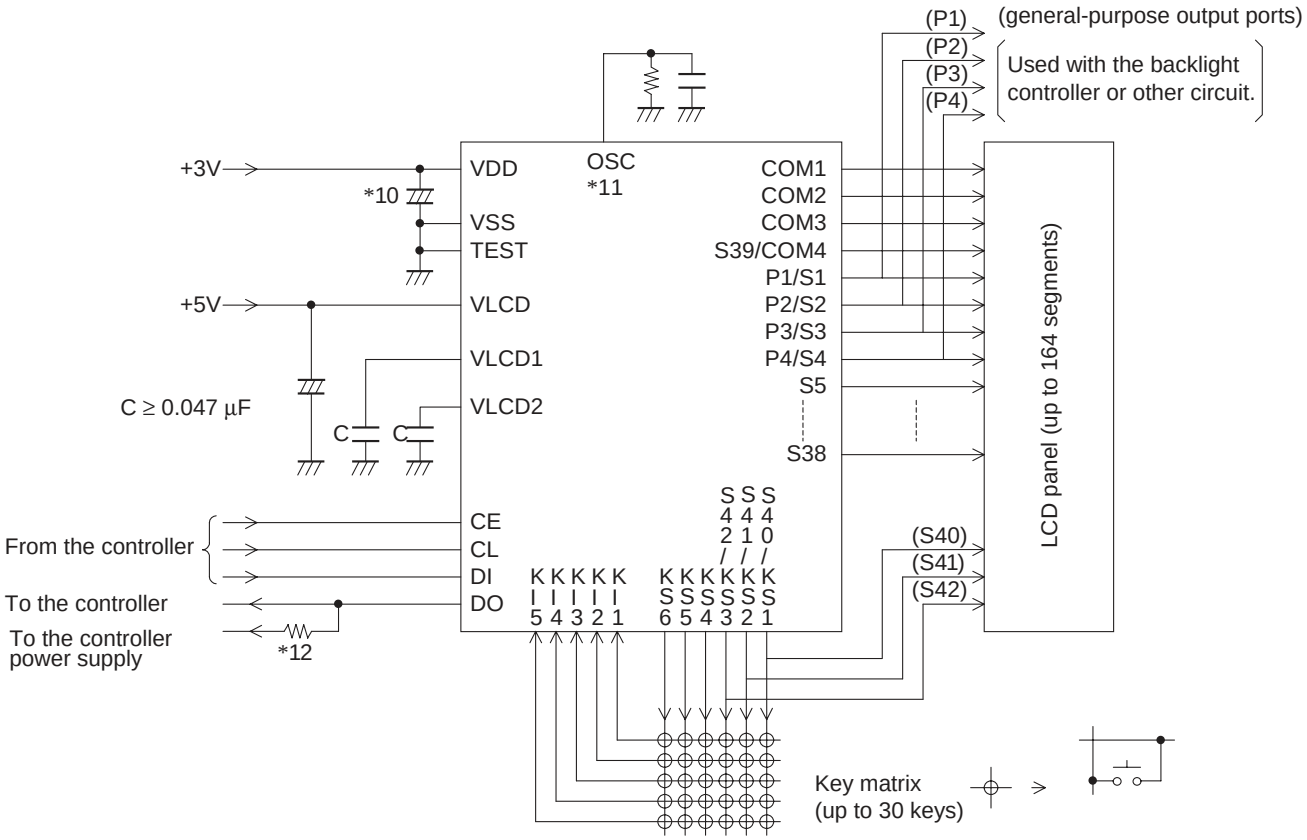
Notes: *10. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75857E/W is reset by the VDET.

*11. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*12. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 7

1/4 duty, 1/3 bias (for use with normal panels)



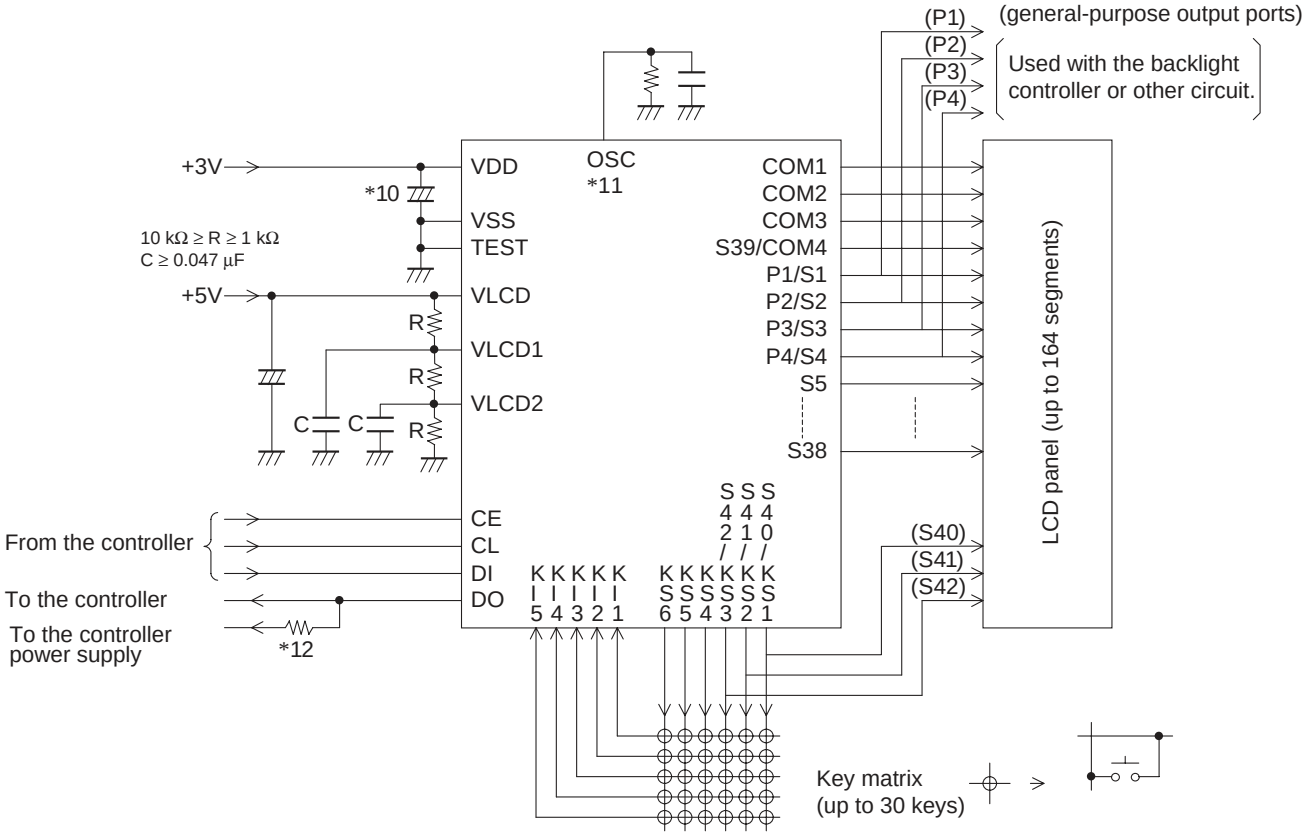
Notes: *10. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75857E/W is reset by the VDET.

*11. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*12. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

Sample Application Circuit 8

1/4 duty, 1/3 bias (for use with large panels)



Notes: *10. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1 ms, as the LC75857E/W is reset by the VDET.

*11. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47 kΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

*12. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10 kΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

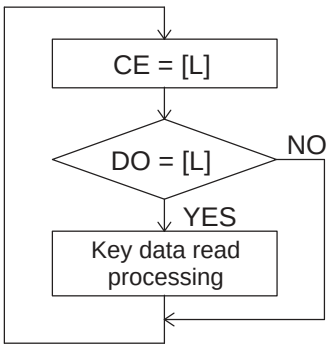
Notes on transferring display data from the controller

When using the LC75857E/W in 1/3 duty, applications transfer the display data (D1 to D126) in three operations, and in 1/4 duty, they transfer the display data (D1 to D164) in four operations. In either case, applications should transfer all of the display data within 30 ms to maintain the quality of the displayed image.

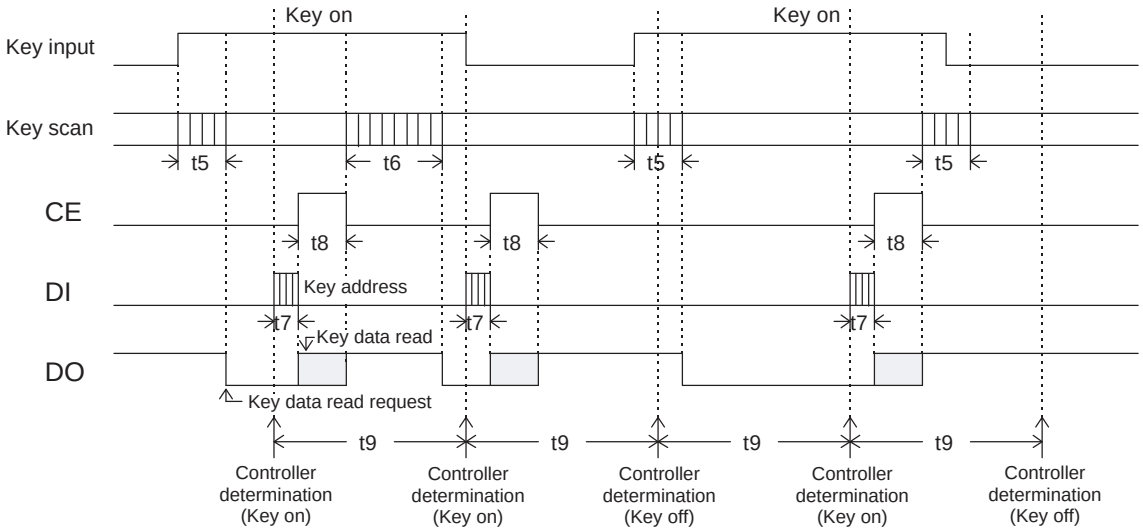
Notes on the controller key data read techniques

1. Timer based key data acquisition

(1) Flowchart



(2) Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (615T(s))
t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230T(s))
t7: Key address (43H) transfer time
t8: Key data read time

$$T = \frac{1}{fosc} = \frac{1}{fCK}$$

(3) Explanation

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t9 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

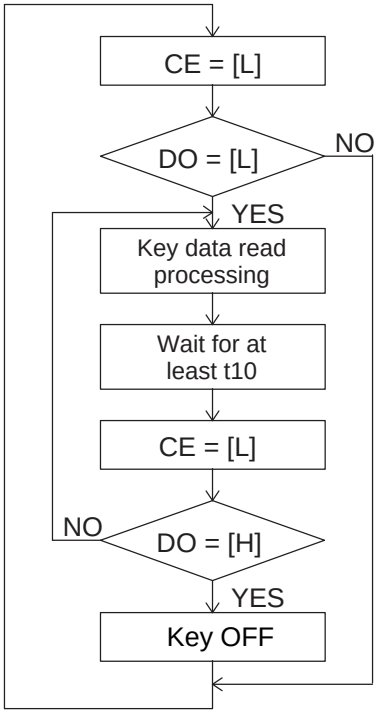
The period t9 in this technique must satisfy the following condition.

t9>t6+t7+t8

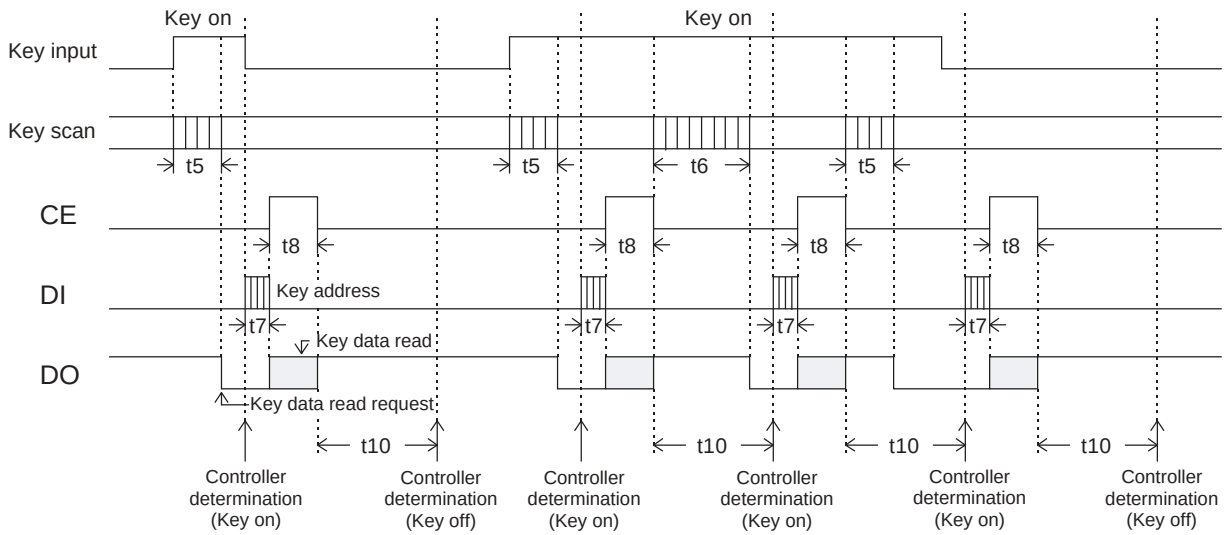
<u>If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.</u>

2. Interrupt based key data acquisition

(1) Flowchart



(2) Timing chart



t5: Key scan execution time when the key data agreed for two key scans. (615T(s))
t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230T(s))
t7: Key address (43H) transfer time
t8: Key data read time

$$T = \frac{1}{fosc} = \frac{1}{fCK}$$

(3) Explanation

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t10 has elapsed by checking the DO state when CE is low and reading the key data. The period t10 in this technique must satisfy the following condition.

t10 > t6

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.