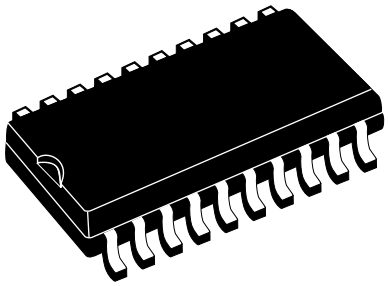
# ESDA6V1S3

## Transil™ array for ESD protection

**Datasheet - production data**



SO-20

## Features

- 18 unidirectional Transil™ functions
- Low leakage current: $I_R$ max. < 2 µA
- 200 W peak pulse power (8/20 µs)

### Benefits

- High ESD protection level: up to 25 kV
- High integration
- Suitable for high density boards

### Complies with the following standards:

- IEC 61000-4-2: Level 4
- MIL STD 883C - Method 3015-6: Class 3 (human body model)

## Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

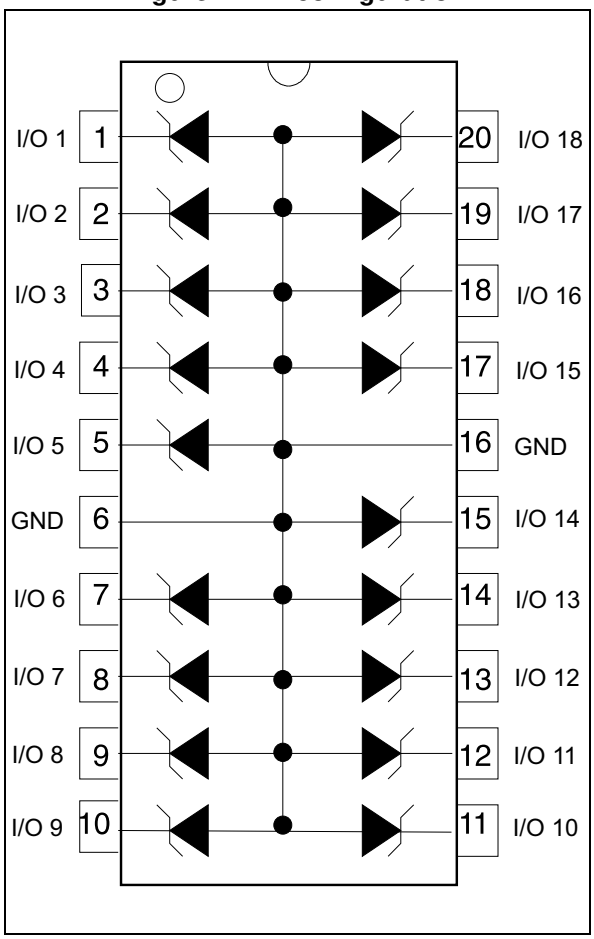
- Computers
- Printers
- Communication systems
- GSM handsets and accessories
- Other telephone sets

## Description

The ESDA6V1S3 is a monolithic voltage suppressors designed to protect components which are connected to data and transmission lines against ESD.

It clamp the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients.

**Figure 1. Pin configuration**



# 1 Characteristics

**Table 1. Absolute ratings ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{PP}$ | Peak pulse voltage | Electrostatics discharge: MIL STD 883C-Method 3015-6 | 25 | kV |
| $P_{PP}$ | Peak pulse power (8/20µs) | | 200 | W |
| $T_j$ | Maximum operating junction temperature | | +150 | °C |
| $T_{stg}$ | Storage temperature range | | -55 to +150 | °C |
| $T_L$ | Maximum lead temperature for soldering during 10 s | | 260 | °C |

**Figure 2. Electrical characteristics (definitions)**

Symbol Parameter
$V_{BR}$ = Breakdown voltage
$I_{RM}$ = Leakage current @ $V_{RM}$
$V_{RM}$ = Stand-off voltage
$V_{CL}$ = Clamping voltage
$I_{PP}$ = Peak pulse current
$I_F$ = Forward current
$V_F$ = Forward voltage
$R_d$ = Dynamic impedance
$C_{LINE}$ = Line capacitance

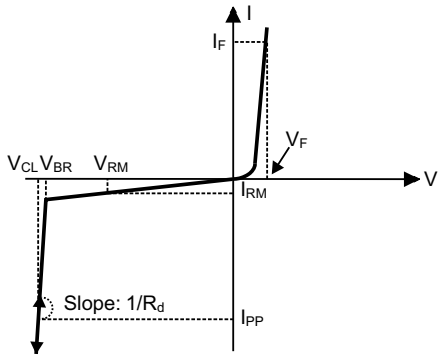



**Table 2. Electrical characteristics - values ($T_{amb}$ = 25 °C)**

| Types | $V_{BR}$ at $I_R$ | | | $I_{RM}$ at $V_{RM}$ | | $V_F$ at $I_F$ | | $\alpha T^{(1)}$ | $C_{line}$ at 0 V |
|---|---|---|---|---|---|---|---|---|---|
| | min. | max. | | max.(2) | | max. | | max. | typ. |
| | V | V | mA | µA | V | V | mA | $10^{-4}$/C | pF |
| ESDA6V1S3 | 6.1 | 7.2 | 1 | 2 | 5.25 | 1.25 | 200 | 6 | 120 |

1. $\Delta V_{BR} = \alpha T^* (T_{amb} - 25\ °C) * V_{BR}$ (25 °C)
2. Between any I/O pin and ground.

# 2 Calculation of the clamping voltage

## 2.1 Use of the dynamic resistance

The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage $V_{CL}$. This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

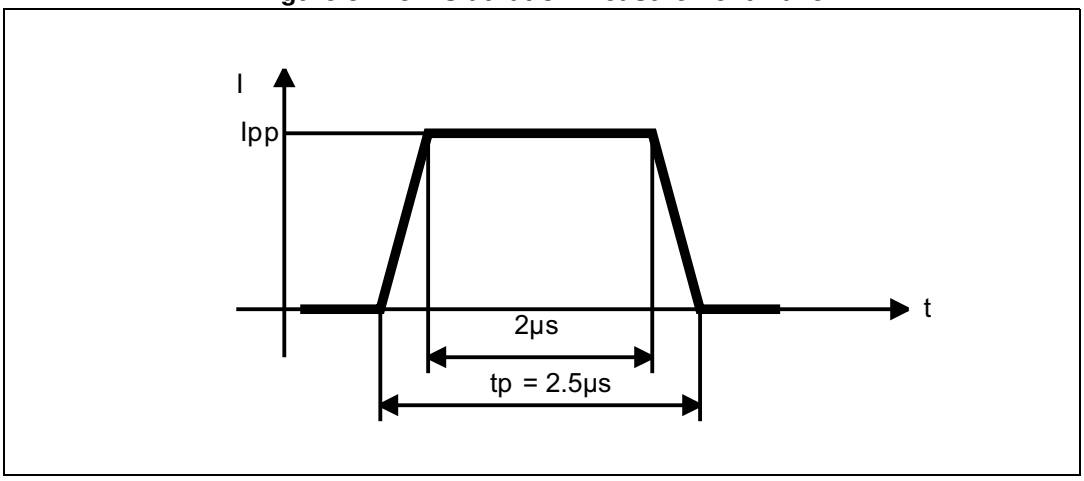
$V_{CL} = V_{BR} + Rd\ I_{PP}$

Where Ipp is the peak current through the ESDA cell.

## 2.2 Dynamic resistance measurement

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20 µs and 10/1000 µs surges.

**Figure 3. 2.5 ms duration measurement wave**




As the value of the dynamic resistance remains stable for a surge duration lower than 20 µs, the 2.5 µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.

**Figure 4. Peak power dissipation versus initial junction temperature ($T_j$ initial = 25 °C)**

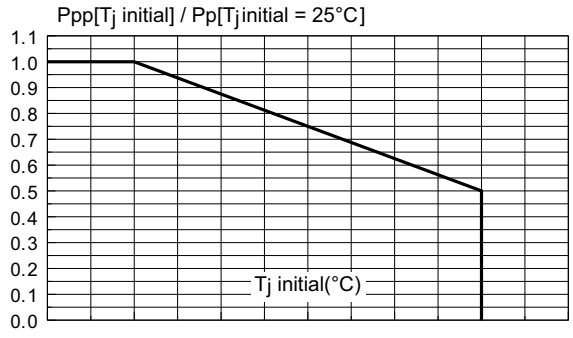



**Figure 5. Peak pulse power versus exponential pulse duration ($T_j$ initial = 25 °C)**

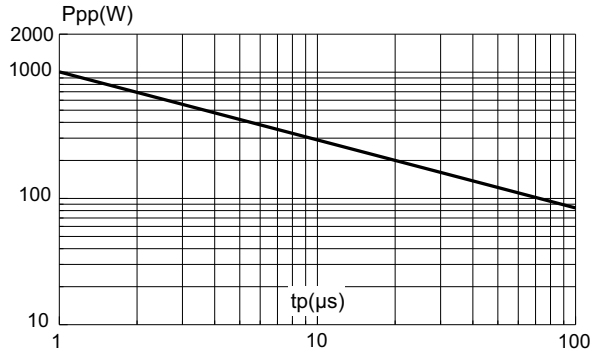



**Figure 6. Clamping voltage versus peak pulse current ($T_j$ initial = 25 °C), rectangular waveform**

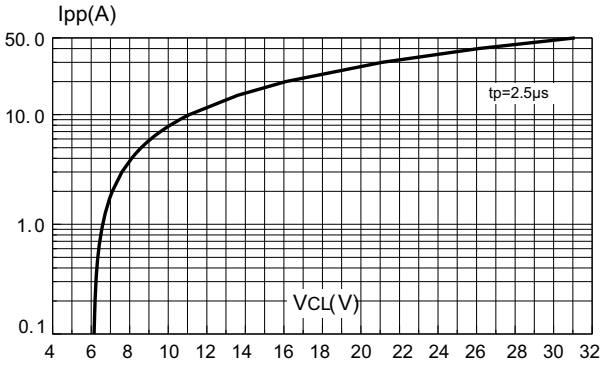



**Figure 7. Capacitance versus reverse applied voltage (typical values)**

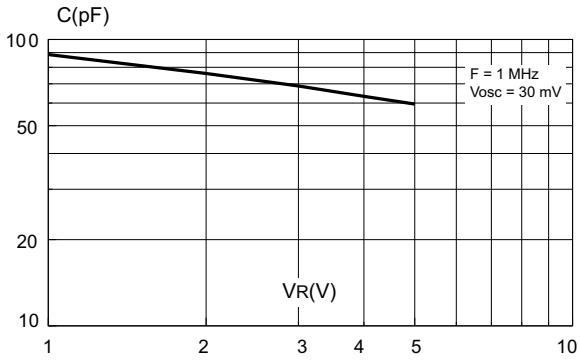



**Figure 8. Relative variation of leakage current versus junction temperature (typical values)**

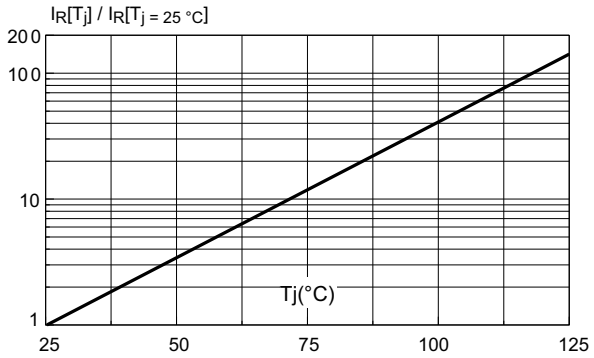
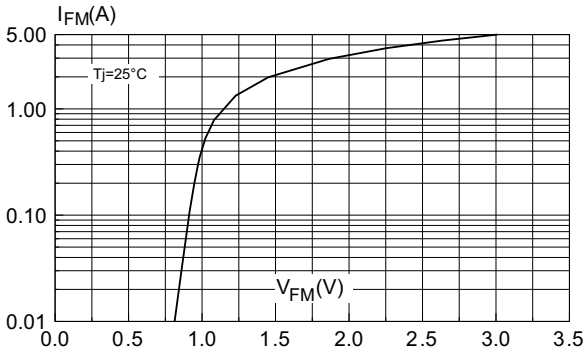



**Figure 9. Peak forward voltage drop versus peak forward current (typical values)**



# 3 Application example

**Figure 10. Protection of logic-level signals (ex: centronics junction)**

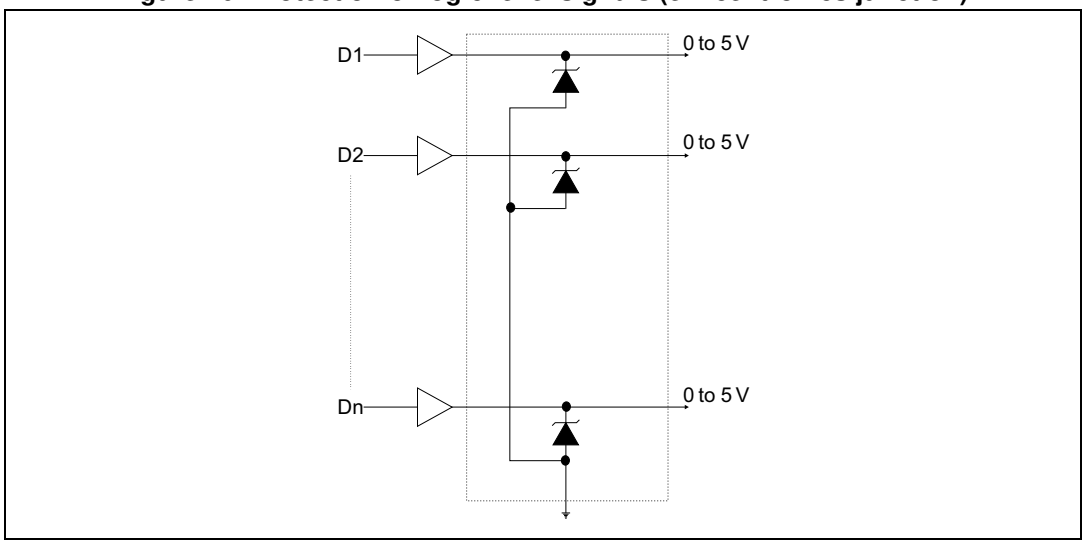
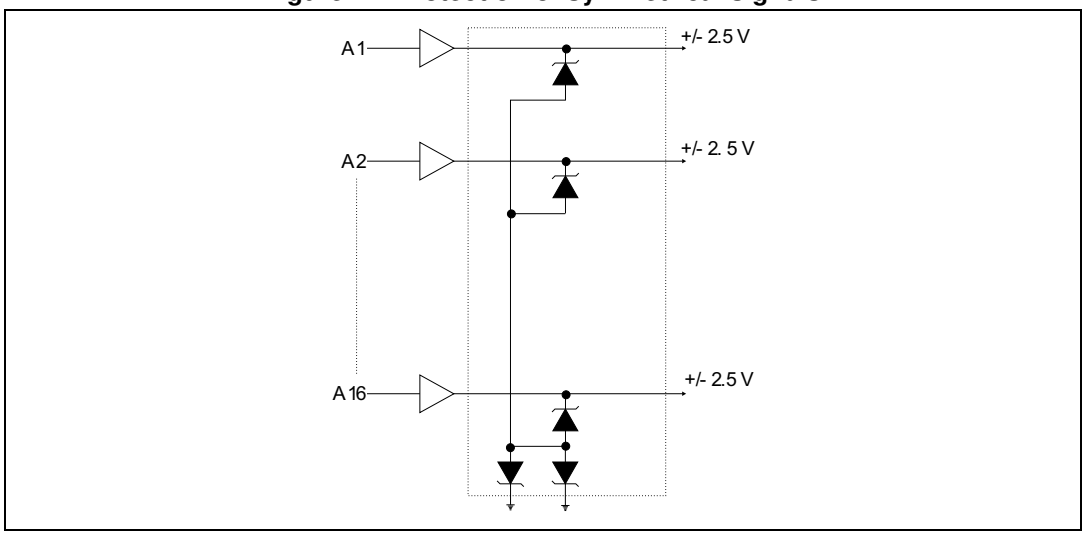



**Figure 11. Protection of symmetrical signals**




*Note: Capacitance value between any I/O pin and ground is divided by 2.*

Implementing its ASD™ technology, STMicroelectronics has developed a monolithic Transil™ diode array, which is a reliable protection against electrostatic overloads for computer I/O ports, modems, GSM handsets and accessories or other similar systems with data outputs. The ESDA6V1S3 integrates 18 Transil™ diodes in a compact package that can be easily mounted close to the circuitry to be protected, eliminating the assembly costs associated with the use of discrete diodes, and also increasing system reliability.

Each Transil™ has a breakdown voltage between 6.2 V (minimum) and 7.2 V (maximum). When the input voltage is lower than the breakdown voltage, the diodes present a high impedance to ground. For short overvoltage pulses, the fast-acting diodes provide an almost instantaneous response, clamping the voltage to a safe level.

# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 4.1 SO-20 package information

**Figure 12. SO-20 package outline**

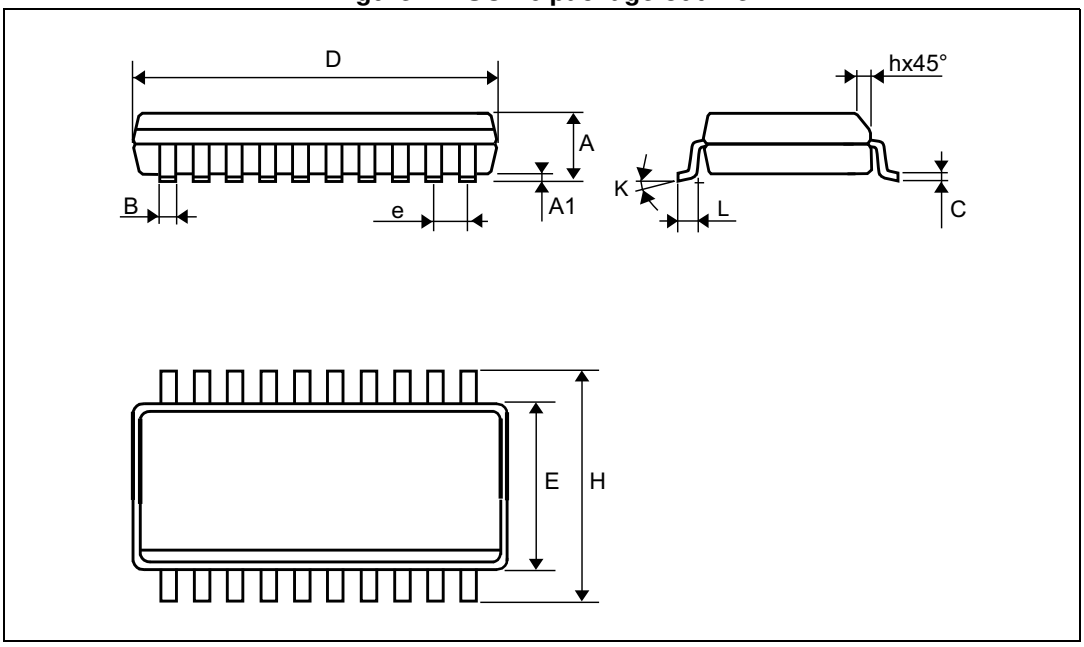



**Table 3. SO-20 package mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.35 | | 2.65 | 0.092 | | 0.104 |
| A1 | 0.10 | | 0.20 | 0.004 | | 0.008 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.23 | | 0.32 | 0.009 | | 0.013 |
| D | 12.6 | | 13.0 | 0.484 | | 0.512 |
| E | 7.40 | | 7.60 | 0.291 | | 0.299 |
| e | | 1.27 | | | 0.050 | |
| H | 10.0 | | 10.65 | 0.394 | | 0.419 |
| h | 0.25 | | 0.75 | 0.010 | | 0.029 |
| L | 0.50 | | 1.27 | 0.020 | | 0.050 |
| K | | | 8° | | | 8° |

# 5 Ordering information

**Figure 13. Ordering information scheme**

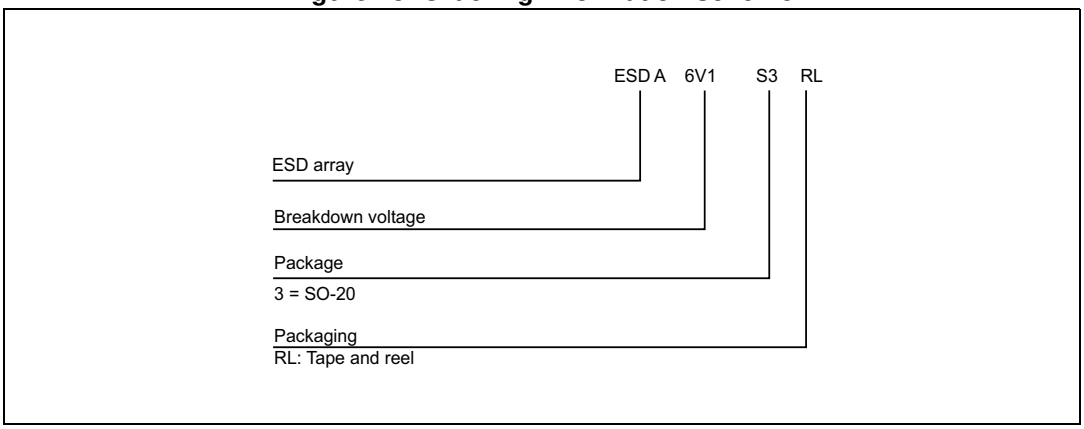



**Table 4. Ordering information**

| Order codes | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| ESDA6V1S3 | E6V1S3 | SO-20 | 0.55 g | 1000 | Tape and reel |

# 6 Revision history

**Table 5. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 18-Sep-2014 | 4 | |
| 13-Nov-2015 | 5 | Removed ESDA6V2S6 package information. |