19-3775; Rev 2; 5/06

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

General Description

The MAX4901–MAX4905 switches feature negative signal capability that allows signals below ground to pass through without distortion. The MAX4901/MAX4902 are a dual SPST (single-pole/single-throw) and the MAX4903/MAX4904/MAX4905 are a single SPDT (single-pole/double-throw) configuration. These analog switches operate from a single +1.8V to +5.5V supply and have low 0.6Ω on-resistance, making them ideal for switching audio signals.

The MAX4905 includes a comparator that can be used for headphone detection or mute/send key function. The MAX4902/MAX4904/MAX4905 have internal shunt resistors to automatically discharge any capacitance at the NO_ and NC connection points. This reduces click-and-pop sounds that occur when switching audio signals between pre-charged points. A break-before-make feature and auto-discharge also help to reduce popping.

These SPST and SPDT switches are available in space-saving 8-pin TDFN and 9-bump UCSP™ packages and operate over the -40°C to +85°C extended temperature range.

Applications

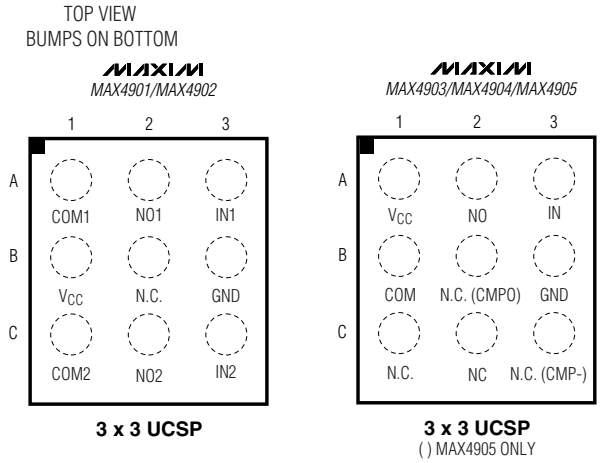
Cell Phones	Notebook Computers
PDAs and Handheld Devices	MP3 Players

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- **Distortion-Free Signal Throughput Down to V_{CC} - 5.5V**
- **Comparator for Headphone or Mute Detection (MAX4905)**
- **Clickless Switches with Internal Shunt Resistors (MAX4902/MAX4904/MAX4905)**
- **0.6Ω (typ) Low On-Resistance (R_{ON})**
- **0.25Ω On-Resistance Flatness**
- **+1.8V to +5.5V Supply Voltage**
- **0.04% THD**

Pin Configurations



Pin Configurations continued at end of data sheet.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	TOP MARK	CONFIGURATION	COMPARATOR	SHUNT	PKG CODE
MAX4901EBL-T	1.5mm x 1.5mm 9 UCSP-9	AEU	2 x SPST	No	No	B9-1
MAX4901ETA-T	8 TDFN-8	AOW	2 x SPST	No	No	T833-2
MAX4902EBL-T	1.5mm x 1.5mm 9 UCSP-9	AEV	2 x SPST	No	Yes	B9-1
MAX4902ETA-T	8 TDFN-8	AOX	2 x SPST	No	Yes	T833-2
MAX4903EBL-T	1.5mm x 1.5mm 9 UCSP-9	AEY	1 x SPDT	No	No	B9-1
MAX4903ETA-T	8 TDFN-8	AOY	1 x SPDT	No	No	T833-2
MAX4904EBL-T	1.5mm x 1.5mm 9 UCSP-9	AEW	1 x SPDT	No	Yes	B9-1
MAX4904ETA-T	8 TDFN-8	AOZ	1 x SPDT	No	Yes	T833-2
MAX4905EBL-T	1.5mm x 1.5mm 9 UCSP-9	AEX	1 x SPDT	Yes	Yes	B9-1
MAX4905ETA-T	8 TDFN-8	APA	1 x SPDT	Yes	Yes	T833-2

Note: *All devices operate over the -40°C to +85°C operating temperature range.*

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, IN_, CMP- ..... -0.3V to +6.0V
COM_, NO_, NC ..... (V_{CC} - 6V) to (V_{CC} + 0.3V)
CMPO ..... -0.3V to (V_{CC} + 0.3V)
Open-Switch Continuous Current NO_, NC
(MAX4902/MAX4904/MAX4905) ..... ±30mA
Closed-Switch Continuous Current COM_, NO_, NC ..... ±100mA
Peak Current COM_, NO_, NC
(Pulsed at 1ms, 50% duty cycle) ..... ±200mA
Peak Current COM_, NO_, NC
(Pulsed at 1ms, 10% duty cycle) ..... ±300mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 18.2mW/°C above +70°C) 1455mW
9-Bump UCSP (derate 5.2mW/°C above +70°C) 412mW
ESD Method 3015.7 ..... ±2kV
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Bump Temperature (soldering)
Infrared (15s) ..... +220°C
Vapor Phase (60s) ..... +215°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V_{CC}			1.8		5.5	V
Supply Current	I+	V_{CC} = 5.5V, $V_{IN\_}$ = 0V or V_{CC}	MAX4901–MAX4904		0.001	1	µA
			MAX4905		5	10	
ANALOG SWITCH							
Analog Signal Range	$V_{NO\_}$ V_{NC}, $V_{COM\_}$	(Note 2)		V_{CC} - 5.5		V_{CC}	V
On-Resistance	$R_{ON(NC)}$, $R_{ON(NO)}$	V_{CC} = 2.7V, V_{NC} or $V_{NO\_}$ = V_{CC} - 5.5V, -1V, 0, 1V, 2V, V_{CC}; I_{COM} = 100mA (Notes 3, 4)	T_A = +25°C		0.6	1.0	Ω
			T_A = T_{MIN} to T_{MAX}			1.2	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 2.7V, $I_{NO\_}$ or I_{NC} = 100mA or $V_{NO\_}$ (Notes 3, 4, 5)	T_A = +25°C		0.01	0.25	Ω
			T_A = T_{MIN} to T_{MAX}			0.30	
On-Resistance Flatness	R_{FLAT}	V_{CC} = 2.7V, V_{NC} or $V_{NO\_}$ = V_{CC} - 5.5V, -1V, 0, 1V, 2V, V_{CC}; I_{COM} = 100mA (Notes 4, 6)	T_A = +25°C		0.25	0.5	Ω
			T_A = T_{MIN} to T_{MAX}			0.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shunt Resistance	R_{SH}	$I_{NO\_}$ or I_{NC} = 10mA, V_{CC} = 2.7V (MAX4902/MAX4904/MAX4905)	T_A = T_{MIN} to T_{MAX}		30	50	Ω
NO_, NC Off-Leakage Current	$I_{NO\_(OFF)}$, $I_{NC\ (OFF)}$	V_{CC} = 2.7V, switch open; V_{NC} or $V_{NO\_}$ = -2.5V, +2.5V; $V_{COM\_}$ = +2.5V, -2.5V (MAX4901/MAX4903) (Notes 3, 7)	T_A = +25°C	-6		+6	nA
			T_A = T_{MIN} to T_{MAX}	-50		+50	
COM_ Off-Leakage Current	$I_{COM\_(OFF)}$	V_{CC} = 2.7V, switch open; V_{NC} or $V_{NO\_}$ = -2.5V, +2.5V; $V_{COM\_}$ = -2.5V, +2.5V (MAX4901) (Note 3)	T_A = +25°C	-6		+6	nA
			T_A = T_{MIN} to T_{MAX}	-50		+50	
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V_{CC} = 2.7V, switch closed; V_{NC} or $V_{NO\_}$ = -2.5V, +2.5V, or unconnected; $V_{COM\_}$ = -2.5V, +2.5V or unconnected (Note 3)	T_A = +25°C	-6		+6	nA
			T_A = T_{MIN} to T_{MAX}	-50		+50	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	V_{CC} = 2.7V, V_{NO} = 1.5V, $V_{IN\_}$ = 0V to V_{CC}; V_{NC} = 1.5V, $V_{IN\_}$ = V_{CC} to 0; R_L = 50Ω, C_L = 5pF (Figure 1)			25	100	ns
Turn-Off Time	t_{OFF}	V_{CC} = 2.7V, $V_{NO\_}$ = 1.5V, $V_{IN\_}$ = V_{CC} to 0; V_{NC} = 1.5V, $V_{IN\_}$ = 0 to V_{CC}; R_L = 50Ω, C_L = 5pF (Figure 1)			15	100	ns
Break-Before-Make Time Delay (MAX4903/MAX4904/MAX4905)	t_{BBM}	V_{CC} = 2.7V, $V_{NO\_}$ = 1.5V, $V_{IN\_}$ = V_{CC} to 0; V_{NC} = 1.5V, $V_{IN\_}$ = 0 to V_{CC}; R_L = 50Ω, C_L = 5pF (Figure 2)	T_A = +25°C	2	10		ns
			T_A = T_{MIN} to T_{MAX}	1			
Charge Injection	Q	$V_{COM\_}$ = 0V, R_S = 0Ω, C_L = 1.0nF (Figure 3)			125		pC
Off-Isolation (Note 8)	V_{ISO}	f = 100kHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF (Figure 4)			-70		dB
Crosstalk	V_{CT}	f = 100kHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF (Figure 4)			-75		dB
Power-Supply Rejection Ratio	PSRR	f = 10kHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF			60		dB
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, R_L = 50Ω, C_L = 5pF (Figure 4)			27		MHz
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V_{COM} = $0.5V_{P-P}$, DC bias = 0, R_L = 32Ω			0.04		%

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NO_, NC Off-Capacitance	$C_{NO\_(OFF)}$ $C_{NC(OFF)}$	f = 1MHz, V_{COM} = 0.5V_{P-P}, DC bias = 0 (Figure 5)		40		pF
COM On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, V_{COM} = 0.5V_{P-P}, DC bias = 0 (Figure 5)		200		pF
DIGITAL I/O (IN_)						
Input Logic-High Voltage	V_{IH}	V_{CC} = 2.7V to 3.6V	1.4			V
		V_{CC} = 4.2V to 5.5V	2.0			
Input Logic-Low Voltage	V_{IL}	V_{CC} = 2.7V to 3.6V			0.5	V
		V_{CC} = 4.2V to 5.5V			0.8	
Input Leakage Current	I_{IN}	$V_{IN\_}$ = 0V or V_{CC}	-1		+1	µA
COMPARATOR (MAX4905)						
Comparator Threshold				V_{CC} / 3		V
Comparator Output-High Voltage		I_{SOURCE} = 1mA	V_{CC} - 0.4V			V
Comparator Output-Low Voltage		I_{SINK} = 1mA			0.4	V
Comparator Input Leakage		V_{CMP-} = 0 to 2.7V	-100		+100	nA
Comparator Switching Time		V_{CC} = 2.7V, V_{CMP-} = 0V to V_{CC}, from 50% of V_{CMP-} to 50% of V_{CMPO}		1	2	µs

Note 1: UCSP and TDFN parts are 100% tested at T_A = +25°C only, and guaranteed by design over the specified temperature range.

Note 2: Signals on COM_, NO_, or NC exceeding V_{CC} are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 3: Guaranteed by design.

Note 4: I_{COM} for UCSP is 10mA.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

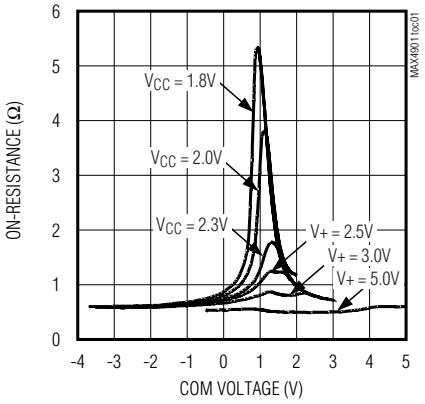
Note 7: The MAX4902/MAX4904/MAX4905 have an internal shunt resistor when, in off-state, will determine off-current.

Note 8: Off-Isolation = $20\log_{10}$ (V_{COM} / V_{NO}), V_{COM} = output, V_{NO} = input to off switch.

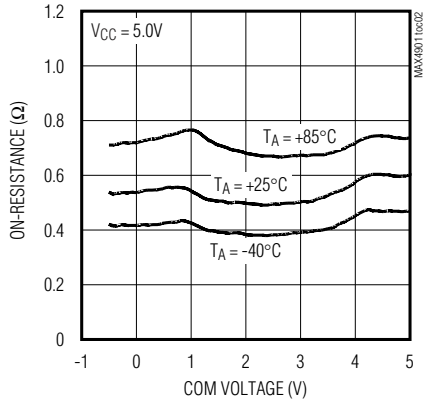
Typical Operating Characteristics

(T_A = +25°C, V_{CC} = 3.0V, unless otherwise noted.)

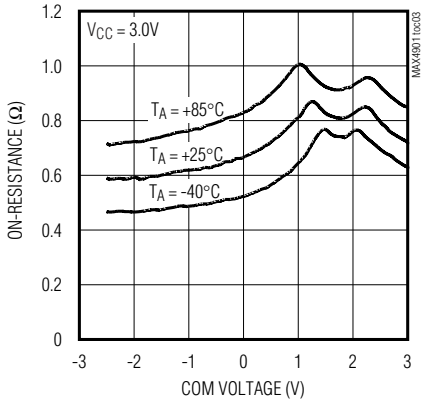
ON-RESISTANCE vs. COM VOLTAGE



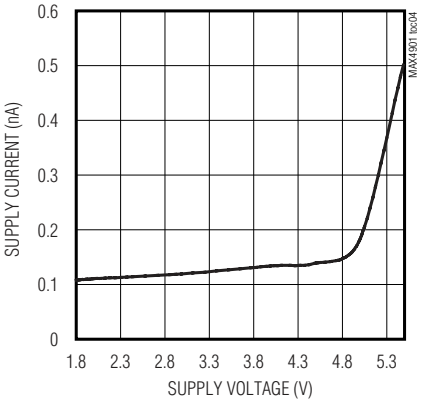
ON-RESISTANCE vs. COM VOLTAGE



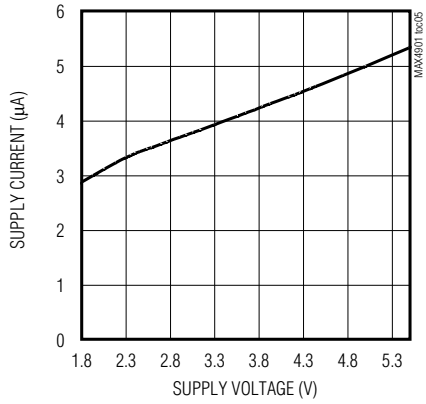
ON-RESISTANCE vs. COM VOLTAGE



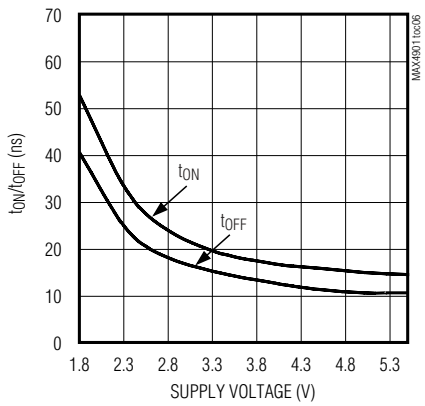
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX4901–MAX4904)



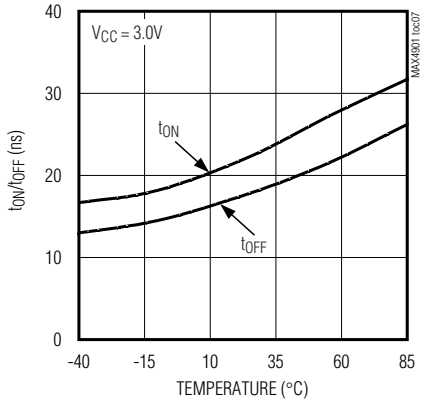
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX4905)



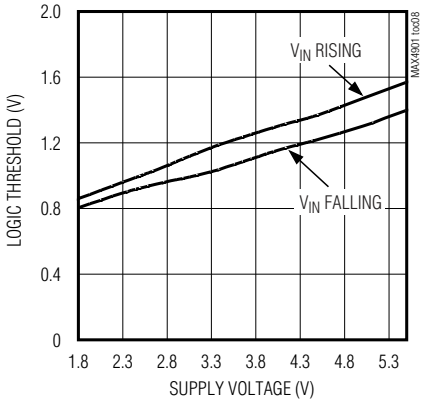
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



TURN-ON/TURN-OFF TIME vs. TEMPERATURE



LOGIC THRESHOLD vs. SUPPLY VOLTAGE

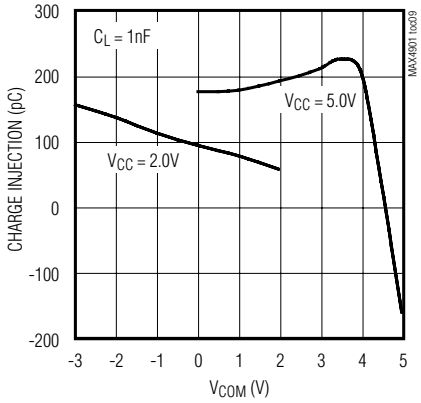


Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

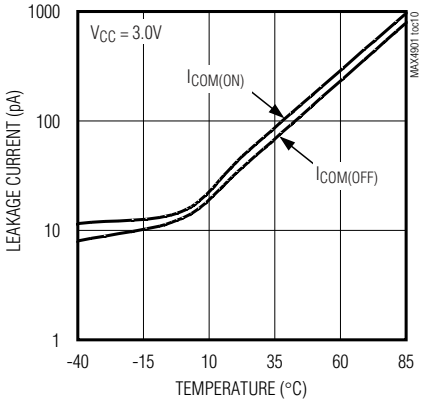
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{CC} = 3.0V, unless otherwise noted.)

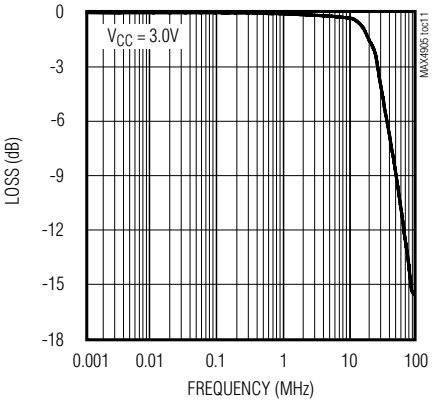
CHARGE INJECTION vs. V_{COM}



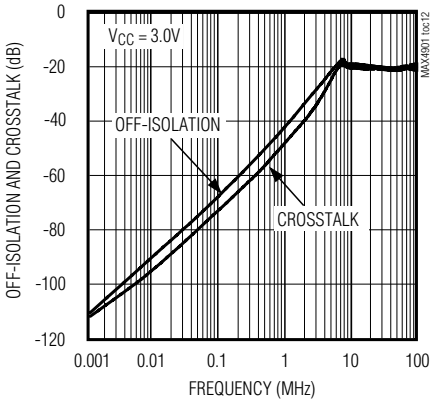
ON-/OFF-LEAKAGE CURRENT vs. TEMPERATURE



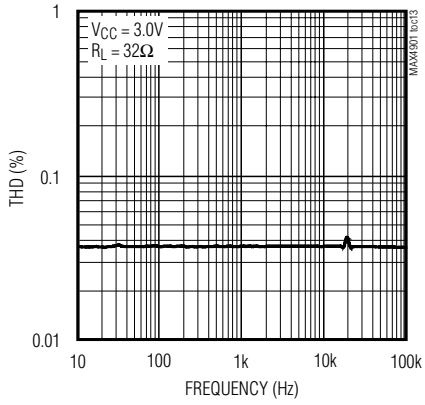
FREQUENCY RESPONSE



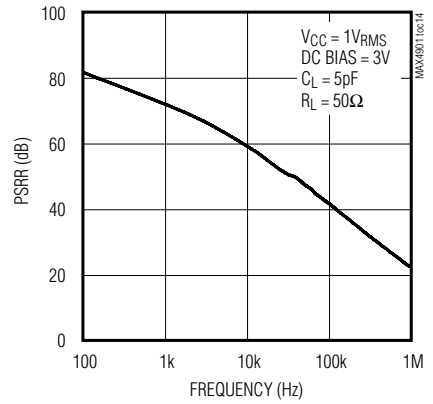
OFF-ISOLATION AND CROSSTALK vs. FREQUENCY



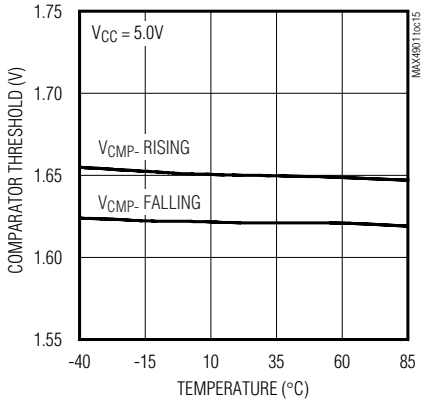
TOTAL HARMONIC DISTORTION vs. FREQUENCY



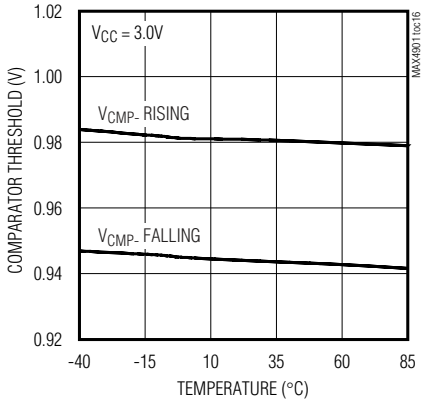
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



COMPARATOR THRESHOLD vs. TEMPERATURE



COMPARATOR THRESHOLD vs. TEMPERATURE



Pin Description (MAX4901/MAX4902 Dual-SPST Switches)

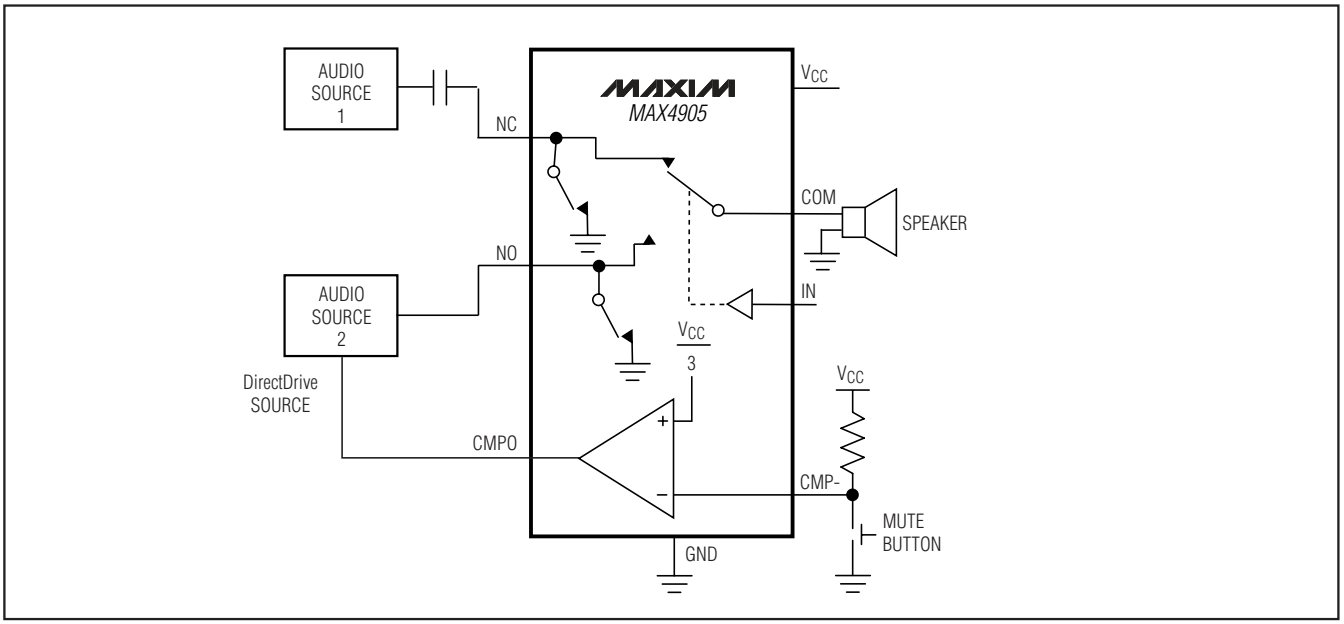
PIN		NAME	FUNCTION
TDFN	UCSP		
1	B1	V_{CC}	Positive Supply-Voltage Input. Bypass V_{CC} to GND with a 0.1µF capacitor as close to V_{CC} as possible.
2	A1	COM1	Analog Switch 1, Common Terminal
—	B2	N.C.	No Connection. Leave N.C. unconnected.
3	A2	NO1	Analog Switch 1, Normally Open Terminal. NO1 (MAX4902) has a shunt resistor to GND when the switch is in open position.
4	A3	IN1	Digital Control Input for Analog Switch 1. A logic high on IN1 connects COM1 to NO1 and a logic low opens the switch.
5	B3	GND	Ground
6	C3	IN2	Digital Control Input for Analog Switch 2. A logic high on IN2 connects COM2 to NO2 and a logic low opens the switch.
7	C2	NO2	Analog Switch 2, Normally Open Terminal. NO2 has a shunt resistor to GND when the switch is in open position (MAX4902).
8	C1	COM2	Analog Switch 2, Common Terminal
EP	—	EP	Exposed Pad. Connect exposed pad to GND.

Pin Description (MAX4903/MAX4904/MAX4905 SPDT Switches)

PIN		NAME	FUNCTION
TDFN	UCSP		
1	A1	V_{CC}	Positive Supply-Voltage Input. Bypass V_{CC} to GND with a 0.1µF capacitor as close to V_{CC} as possible.
2	A2	NO	Analog Switch, Normally Open Terminal. NO has a shunt resistor to GND when the switch is in open position (MAX4904/MAX4905).
3	A3	IN	Digital Control Input. Logic low on IN connects COM to NC and logic high connects COM to NO.
4	B2	N.C.	No Connection. Leave N.C. unconnected (MAX4903/MAX4904).
		CMPO	Comparator Output (MAX4905)
5	B3	GND	Ground
6	C3	N.C.	No Connection. Leave N.C. unconnected (MAX4903/MAX4904).
		CMP-	Comparator Input (MAX4905)
7	C2	NC	Analog Switch, Normally Closed Terminal. NC has a shunt resistor to GND when the switch is in open position (MAX4904/MAX4905).
8	B1	COM	Analog Switch, Common Terminal
—	C1	N.C.	No Connection. Leave N.C. unconnected (MAX4903/MAX4904/MAX4905)
EP	—	EP	Exposed Pad. Connect exposed pad to GND.

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Typical Operating Circuit



Detailed Description

The MAX4901–MAX4905 are low on-resistance, low-voltage, dual-SPST and single-SPDT analog switches that operate from a +1.8V to +5.5V supply and are fully specified for nominal 3.0V applications. The devices feature a negative signal capability that allows signals below ground to pass through without distortion and have break-before-make switching (MAX4903/MAX4904/MAX4905).

The MAX4905 features a comparator that can be used for headphone or mute detection. The comparator threshold is internally generated to be approximately 1/3 of V_{CC}. The MAX4902/MAX4904/MAX4905 feature an internal shunt resistor to discharge any capacitance at NO_ and NC connection points. This reduces the click-and-pop sounds that occur when switching audio signals.

Applications Information

Digital Control Inputs

The MAX4901–MAX4905 logic inputs accept up to +5.5V, regardless of supply voltage. For example, with a +3.3V supply, IN_ can be driven low to GND and high to +5.5V, allowing for mixing of logic levels in a system. Driving IN_ rail-to-rail minimizes power consumption. For a +1.8V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high). For a +5V supply voltage, the logic thresholds are 0.8V (low) and 2.0V (high).

Analog Signal Levels

The on-resistance of the MAX4901–MAX4905 changes very little for analog input signals across the entire supply-voltage range (see the *Typical Operating Characteristics*). The switches are bidirectional.

The MAX4901–MAX4905 pass signals as low as V_{CC} - 5.5V, including signals below ground with minimal distortion. Note that there are shunt resistors on NO_ and NC when they are unconnected to COM_ for the MAX4902/MAX4904/MAX4905.

Comparator (MAX4905)

The MAX4905 includes a comparator that can be used for mute and headphone detection functions. The positive terminal of the comparator is internally set to V_{CC} / 3. When the negative terminal (CMP-) is below the threshold, the comparator output (CMPO) is a logic high.

The comparator threshold of V_{CC} / 3 allows for detection of headphones because headphone audio signals are typically biased to V_{CC} / 2.

Shunt Resistor (MAX4902/MAX4904/MAX4905)

The 50Ω shunt resistors on the MAX4902/MAX4904/MAX4905 automatically discharge any capacitance at the NC or NO_ terminals when they are unconnected to COM_. This reduces audio click-and-pop sounds that occur when switching between audio sources.

Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_{CC} before applying analog signals, especially if the analog signal is not current-limited.

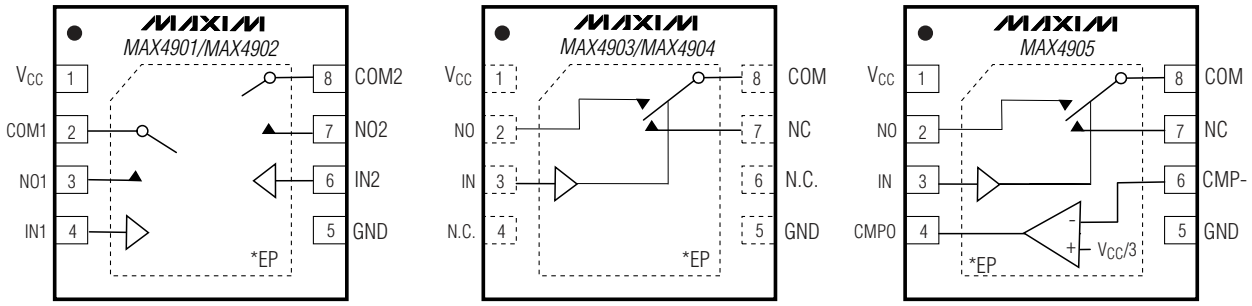
UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note: *UCSP—A Water-Level Chip-Scale Package* on Maxim's web site at www.maxim-ic.com/ucsp.

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

NOTE: N.C. IS NO CONNECTION (SEE *PIN DESCRIPTION TABLE*)



TDFN
*EXPOSED PAD CONNECTED TO GND

TDFN
*EXPOSED PAD CONNECTED TO GND

*EXPOSED PAD CONNECTED TO GND

MAX4901–MAX4905		
IN	NC	NO
0	ON	OFF
1	OFF	ON

MAX4904/ MAX4905	
NCS*	NOS*
OFF	ON
ON	OFF

*NCS AND NOS REFER TO NORMALLY CLOSED SHUNT REGISTER

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Test Circuits/Timing Diagrams

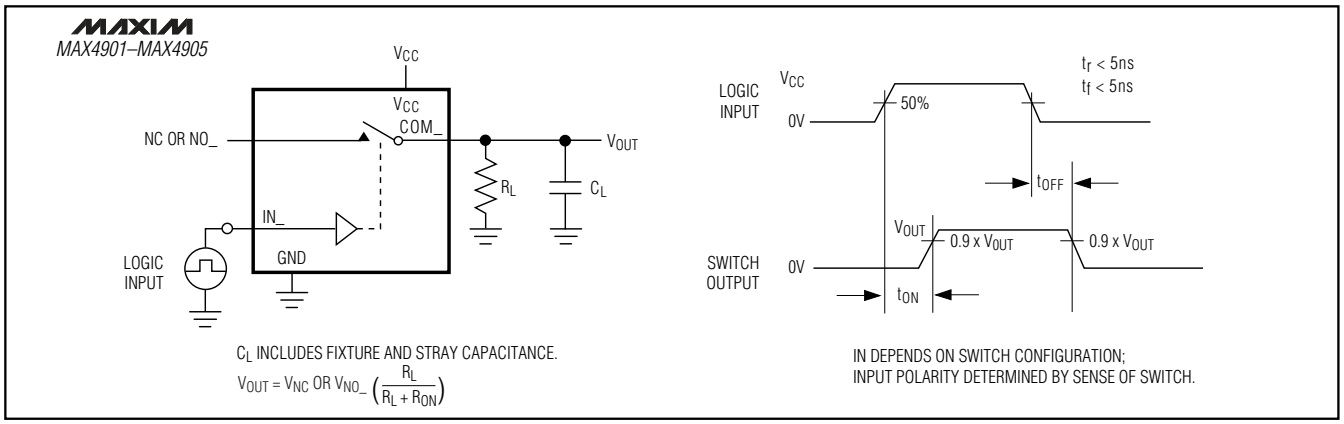


Figure 1. Switching Time

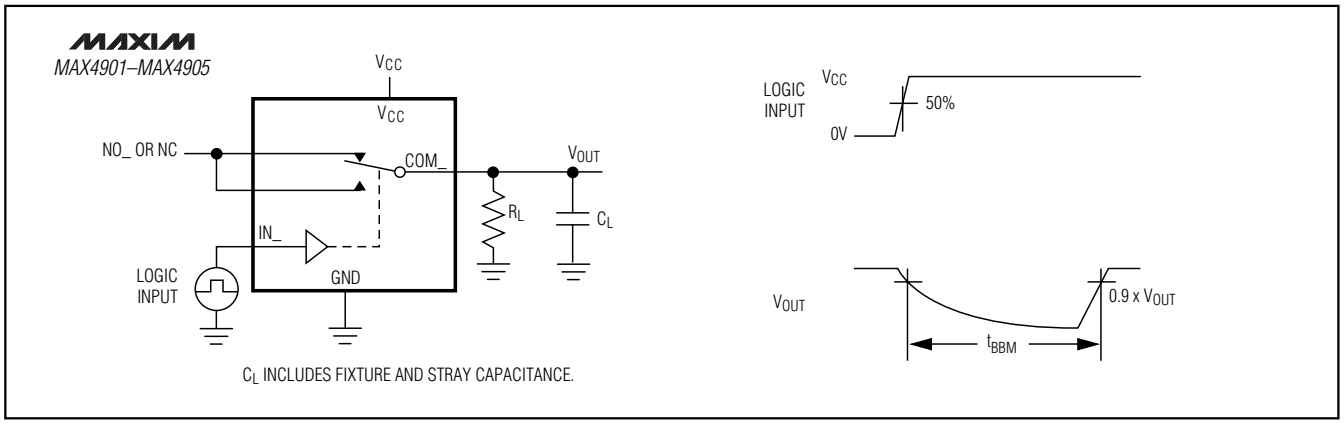


Figure 2. Break-Before-Make Interval

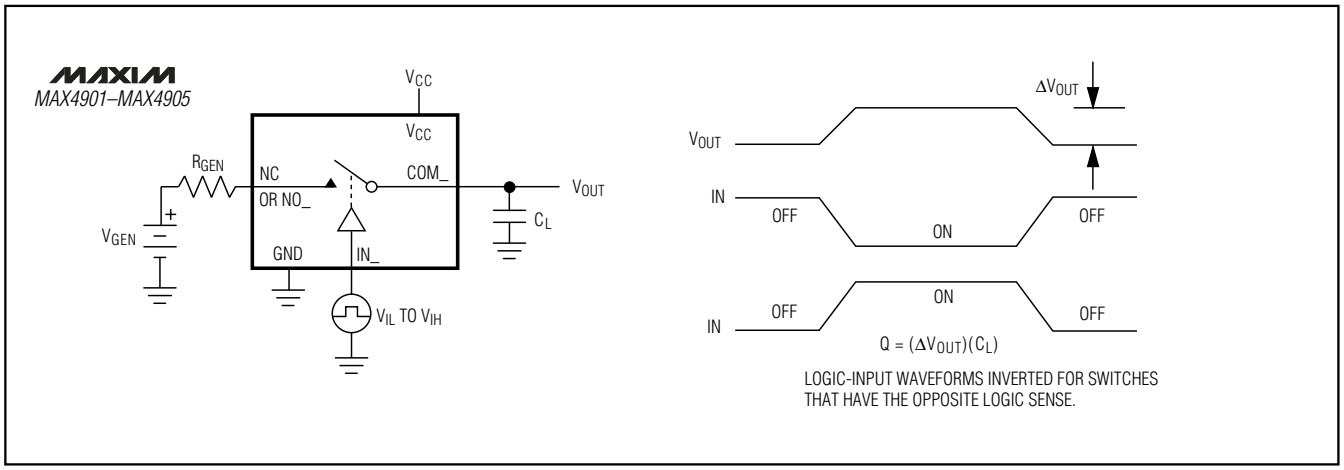


Figure 3. Charge Injection

Test Circuits/Timing Diagrams (continued)

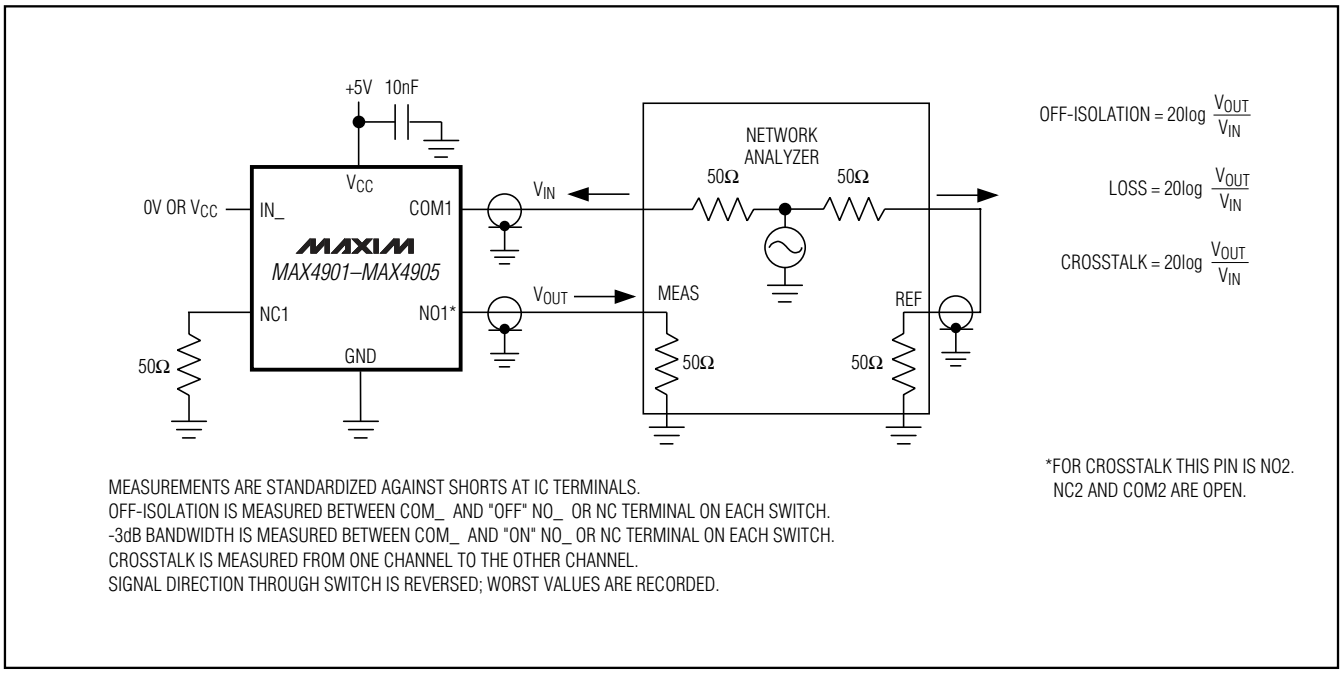


Figure 4. -3dB Bandwidth, Off-Isolation, and Crosstalk

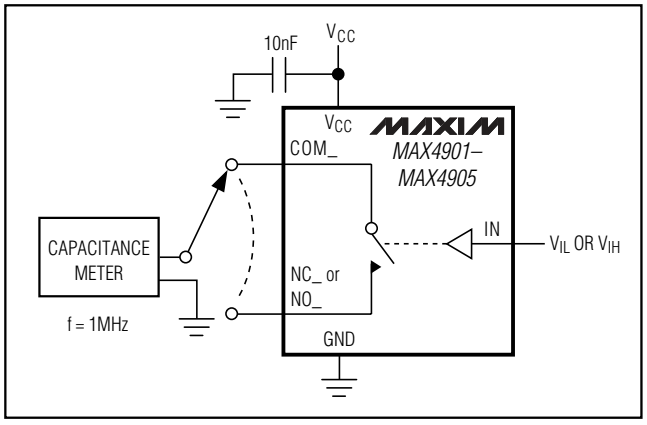


Figure 5. Channel Off-/On-Capacitance

Chip Information

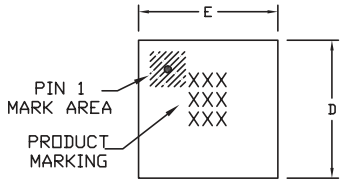
PROCESS: BiCMOS

Low-RON, Dual-SPST/Single-SPDT Clickless Switches with Negative Rail Capability

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

9LUCSP, 3x3.EPS

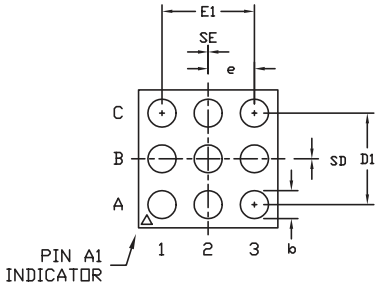


TOP VIEW

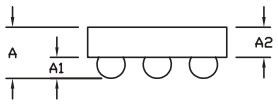
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

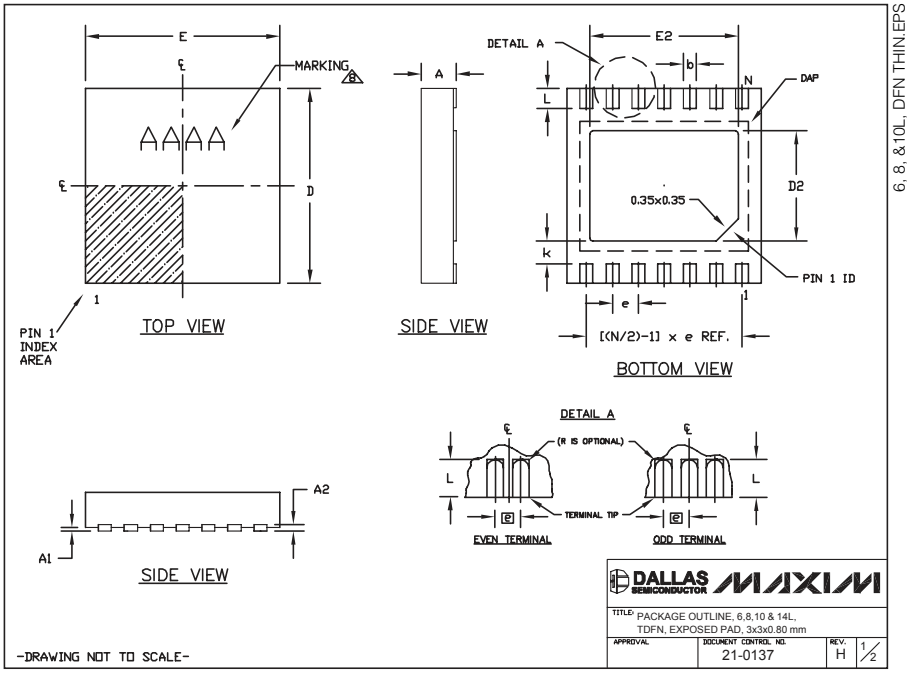
TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0093	K	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6, 8, &10L, DFN THIN.EPS



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. H
2/2