AN3213
Application note

ST7570 S-FSK power line networking system-on-chip design guide for AMR

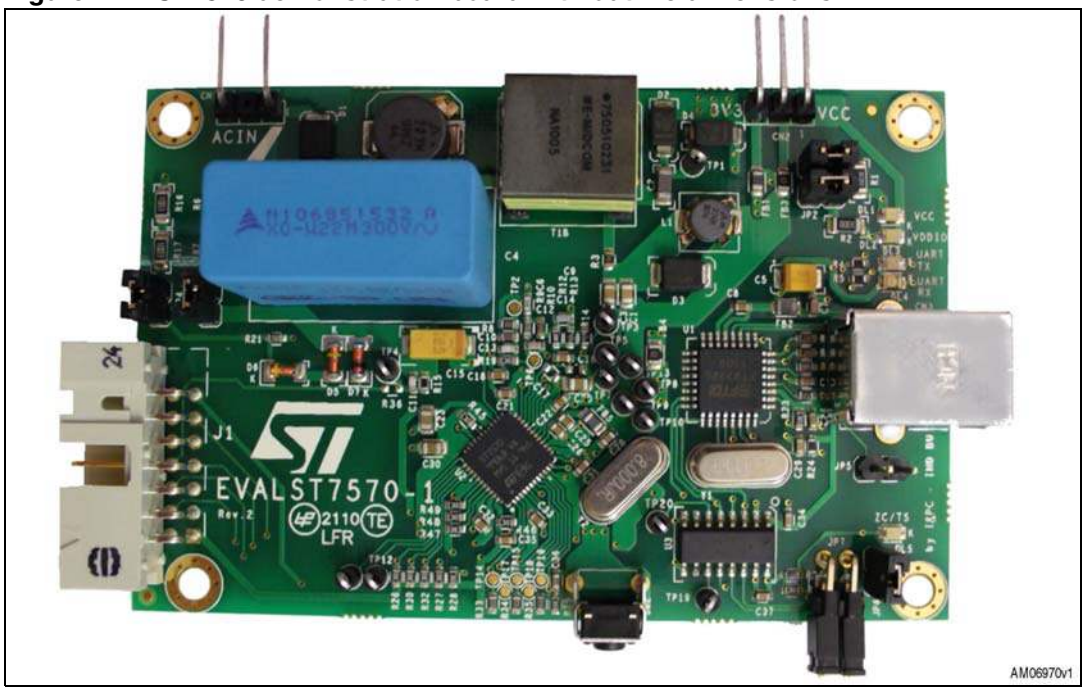
Introduction

The ST7570 demonstration board has been realized as a useful tool which exploits the performance capability of the ST7570 S-FSK power line networking system-on-chip (*References 1*).

With this demonstration board, it is possible to evaluate the ST7570 features and its transmitting and receiving performance directly on the power line.

The coupling interface is designed to allow the ST7570 device to transmit and receive on the mains using a spread-spectrum FSK signal with 63.3 and 74 kHz tone frequencies, within the European CENELEC EN50065-1 standard A-band, specified for automatic meter reading (*References 4*).

Figure 1. ST7570 demonstration board with outline dimensions



As can be seen from *Figure 1*, special effort has been made to make the demonstration board as compact as possible, while including all the features which enable the ST7570 to perform at its best.

Note: The information provided in this application note refers to the EVALST7570-1 demonstration board.

Contents

List of tables

List of figures

1 Abbreviations used in this document

- AC = alternate current
- AFE = analog front end
- AMR = automated meter reading
- AWGN = additive white gaussian noise
- BER = bit error rate
- BOM = bill of material
- CE = conducted emissions
- DC = direct current
- EMC = electro-magnetic compliance
- EMI = electro-magnetic immunity
- GUI = graphical user interface
- MAC = medium access control layer (as per IEC61334-5-1 protocol stack definition - *References 5*)
- NBI = narrow-band interferer
- LISN = line impedance stabilization network
- PA = power amplifier
- PCB = printed circuit board
- PHY = physical layer (as per IEC61334-5-1 protocol stack definition - *References 5*)
- PLC = power line communication
- PSU = power supply unit
- RBW = resolution bandwidth
- SBW = signal bandwidth
- S-FSK = spread frequency shift keying
- SNR = signal-to-noise ratio
- SSD = start subframe delimiter (as per IEC61334-5-1 physical layer definition - *References 5*)

2 Electrical characteristics

Table 1. Electrical and thermal characteristics of the ST7570 demonstration board

Parameter	Value			Notes
	Min	Typ	Max	
Thermal data				
Ambient operating temperature	-40 °C		85 °C	
ST7570 thermal resistance			50 °C/W ((1))	Measured on the ST7570 demonstration board 2-side PCB with thermal pad and 4x4 thermal via array
Transceiver section				
Transmitting specifications (Tx mode)				
Transmitted signal Tone “1” frequency		63.3 kHz		
Transmitted signal Tone “0” frequency		74 kHz		
Transmitted signal -20 dB bandwidth		19 kHz		2400 BAUD
Transmitted output current limit		1 A rms		R15 = 130 Ω
Receiving specifications (Rx mode)				
Minimum detectable received signal		46 $dB\mu V_{rms}$		1200 BAUD, BER<10^{-3}, SNR > 20 dB
Reception filter -3 dB bandwidth		50 kHz		
Mains coupling specifications				
Transformer isolation	4 kV ((2))			
Power supply requirements				
AC mains voltage range	85 V_{AC}		265 V_{AC}	
Mains frequency		50-60 Hz		
VCC power supply voltage	8 V	13 V	18 V	
VCC power supply current absorption – RX mode		12 mA		DL1 on (7 mA typ.)

Table 1. Electrical and thermal characteristics of the ST7570 demonstration board (continued)

Parameter	Value			Notes
VCC power supply current absorption – TX mode	20 mA		500 mA	VCC = 8 to 18 V, I(PA_OUT) = 0 to 1 A rms
VDDIO digital supply voltage	-10 %	3.3 V	+10 %	
VDDIO digital supply current absorption		40 mA		DL2 on (5 mA typ.), no external microcontroller connection through J1
Maximum required power (typical application)		7 W		VCC = 13 V

1. Measured over a continuous transmission period of 3000 seconds (steady-state thermal dissipation).
2. Note that STMicroelectronics does not guarantee transformer isolation. STMicroelectronics assumes no responsibility for the consequences that may arise from that risk.

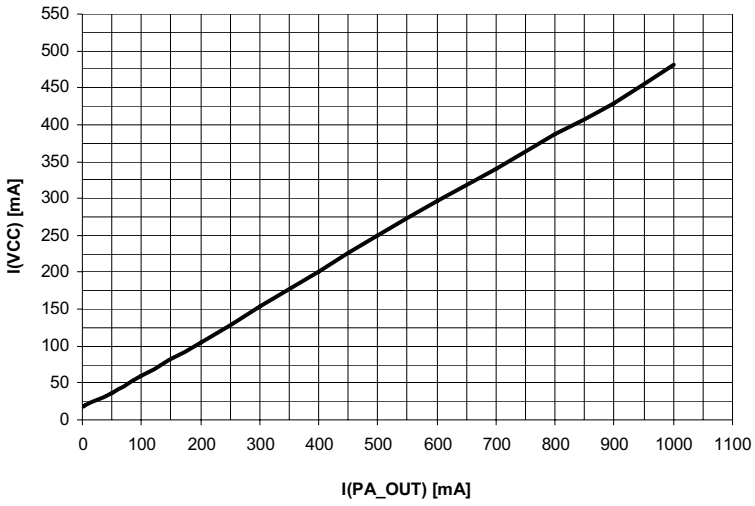
Table 2. TX_OUT level vs. TX_GAIN - typical values

TX_GAIN	TX_OUT	
	[dBµV rms]	[V rms]
31	123	1.420
30	122	1.265
29	121	1.128
28	120	1.005
27	119	0.896
26	118	0.798
25	117	0.712
24	116	0.634
23	115	0.565
22	114	0.504
21	113	0.449
20	112	0.400
19	111	0.357
18	110	0.318
17	109	0.283
16	108	0.252
15	107	0.225
14	106	0.201

Table 2. TX_OUT level vs. TX_GAIN - typical values (continued)

TX_GAIN	TX_OUT	
13	105	0.179
12	104	0.159
11	103	0.142
10	102	0.127
9	101	0.113
8	100	0.101
7	99	0.090
6	98	0.080
5	97	0.071
4	96	0.063
3	95	0.057
2	94	0.050
1	93	0.045

Figure 2. I(VCC) vs. I(PA_OUT) curve - typical values



3 Safety recommendations

The board must be used by expert technicians only. Due to the high voltage (85-265 V_{AC}) present on the non-isolated parts, special care must be taken in order to avoid electrical risks regarding user safety.

There is no protection against accidental human contact with high voltages.

After disconnecting the board from the mains, no live parts must be touched immediately because of the energized capacitors.

It is mandatory to use a mains insulation transformer to perform any tests on the high voltage sections, using test instruments such as, spectrum analyzers or oscilloscopes.

Do not connect any probe to high voltage sections if the board is not isolated from the mains supply, in order to avoid damaging instruments and demo tools.

Warning: STMicroelectronics assumes no responsibility for the consequences arising from any improper use of this development tool.

4 ST7570 S-FSK power line networking system-on-chip description

The ST7570 is a powerful power line networking system-on-chip, combining a high-performing PHY processor core and a protocol controller core with a fully integrated analog front end (AFE) and line driver, for a scalable future-proof, cost effective single chip narrow-band power line communication solution based on IEC61334-5-1 S-FSK technology (*References 5*).

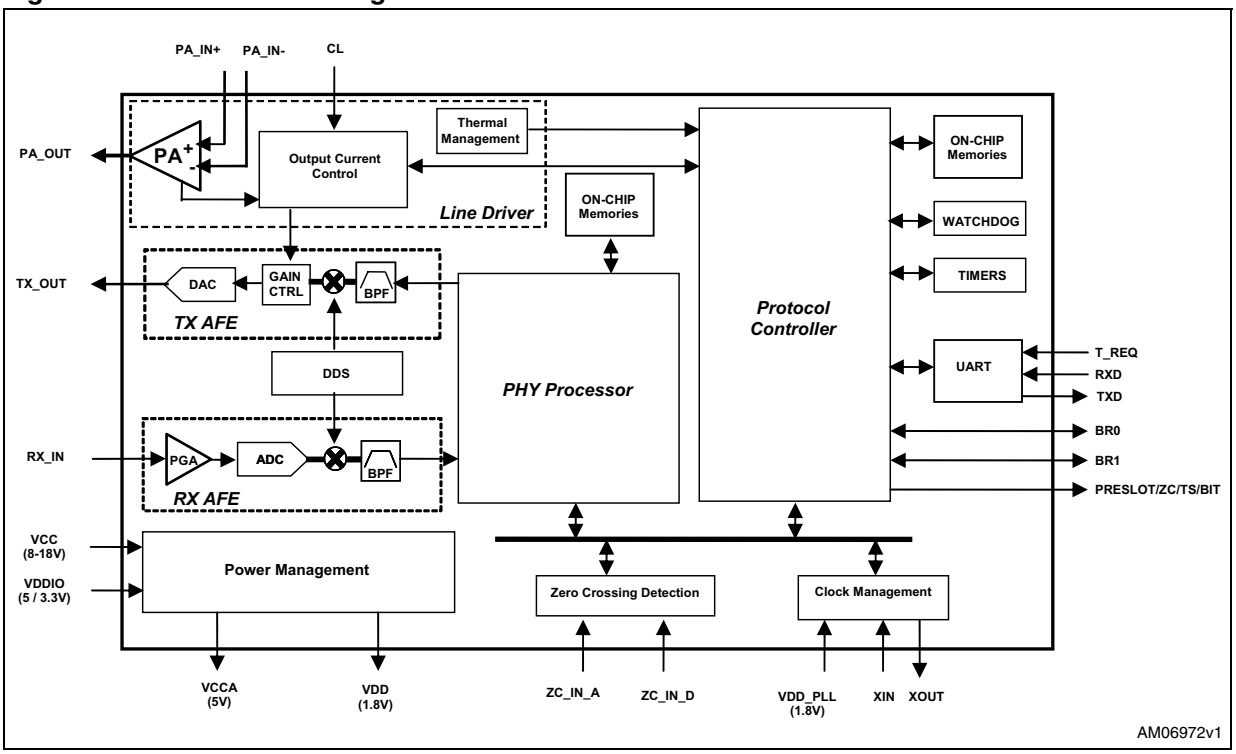
The ST7570 comes with a dedicated FW implementing full PHY and MAC protocol layers and services compliant with the open standard IEC 61334-5-1, mainly developed for smart metering applications in EN50065-1 A band, but also usable for other command and control applications and remote load management in B band (*References 4*).

The on-chip analog front end, featuring analog-to-digital and digital-to-analog conversion and automatic gain control, plus the integrated power amplifier delivering up to 1 A rms output current, makes the ST7570 the first complete system-on-chip for power line communication.

The line coupling network design is also simplified, leading to a very low cost BOM. Safe performance operations are guaranteed while keeping power consumption and distortion levels very low, therefore making ST7570 an ideal platform for the most stringent application requirements and regulatory standard compliance.

For further details, please refer to *References 1* and *2*.

Figure 3. ST7570 block diagram



5 Demonstration tools

The minimum set of evaluation tools required to test the ST7570 power line communication is two communication nodes, each made up of the following elements:

- A PC running the ST7570 GUI software tool
- One EVALST7570-1 board
- One ALTAIR04-900 demonstration board as the power supply unit (PSU).

For further details regarding the ST7570 GUI software and the available evaluation tools, please visit http://www.st.com/powerline.

6 Test and measurement tools

- Spectrum/network/impedance analyzer
  - Agilent 4395A: 10 Hz - 500 MHz
  - Agilent 43961A Impedance test kit
- Differential active probe
  - Agilent 1141A differential probe: 1 MΩ, 7 pF
- Agilent 1142A probe control and power module:
  - DC reject 0.05 Hz
- EMC analyzer
  - Agilent E7402A: 100 Hz - 3 GHz
- Two-line V-network (LISN)
  - Rohde&Schwarz ENV216
- Isolation transformer
  - 1000 VA, 0 - 250 V variable output
- Oscilloscope
  - Tektronik TDS 754D: 500 MHz, 2 GS/s
- Surge/burst generator
  - Volta UCS 500-M

7 ST7570 demonstration board description

The ST7570 demonstration board is made up of the following sections:

- ST7570 supply and digital connections
- Line coupling section, including four subsections:
  - Transmission active filter
  - Reception passive filter
  - Power line coupling
  - Zero crossing coupling.

The board has also four external connections:

- AC mains (line and neutral) on CN1 connector
- VCC (8 to 18 V) and VDDIO (3.3 or 5 V) supply voltages on CN2 connector
- USB interface for PC connectivity on CN3 USB type B connector
- Digital interface on J1 7x2 connector, collecting all the signals required to interface an external microcontroller board.

Figure 4. Board drawing with indication of the various sections

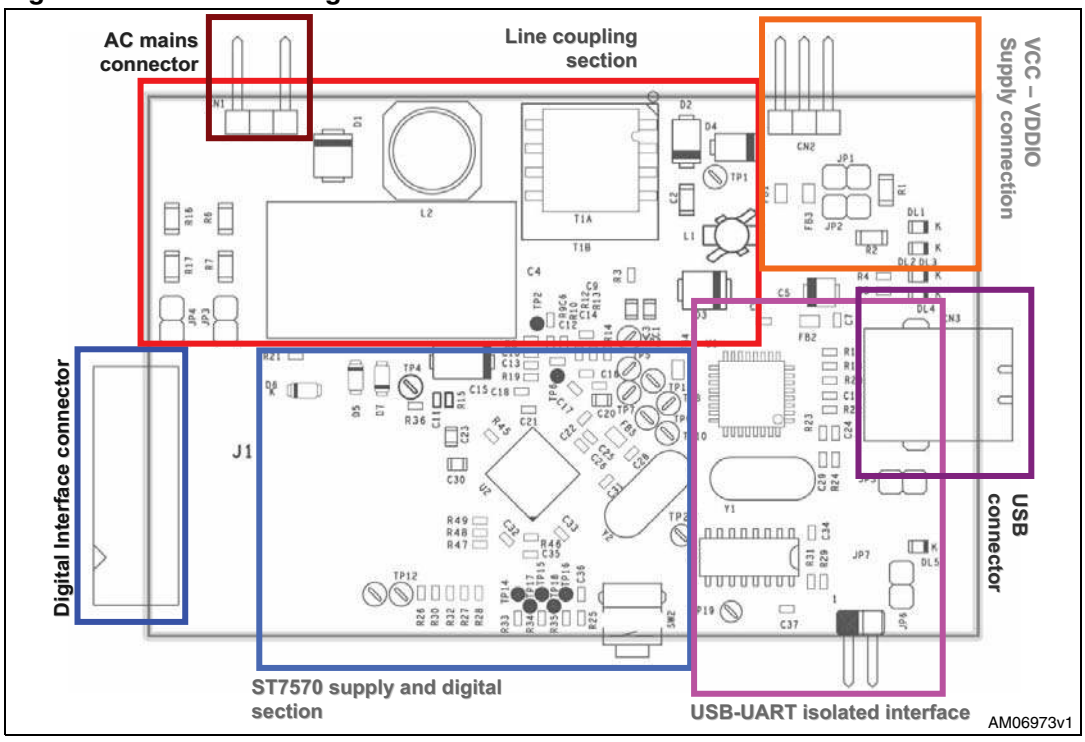


Figure 5 gives a global view of the demonstration board. *Figure 6* shows the ST7570 and the line coupling circuits, while *Figure 10* represents the USB to UART connection circuit.

Table 3 lists the components chosen to realize the demonstration board. All the parts have been selected to obtain good performance in a real case application.

The layout of the printed circuit board is given in *Appendix A: Board layout* - *Figure 53*, *Figure 54* and *Figure 55*.

Figure 5. Global view of the ST7570 demonstration board

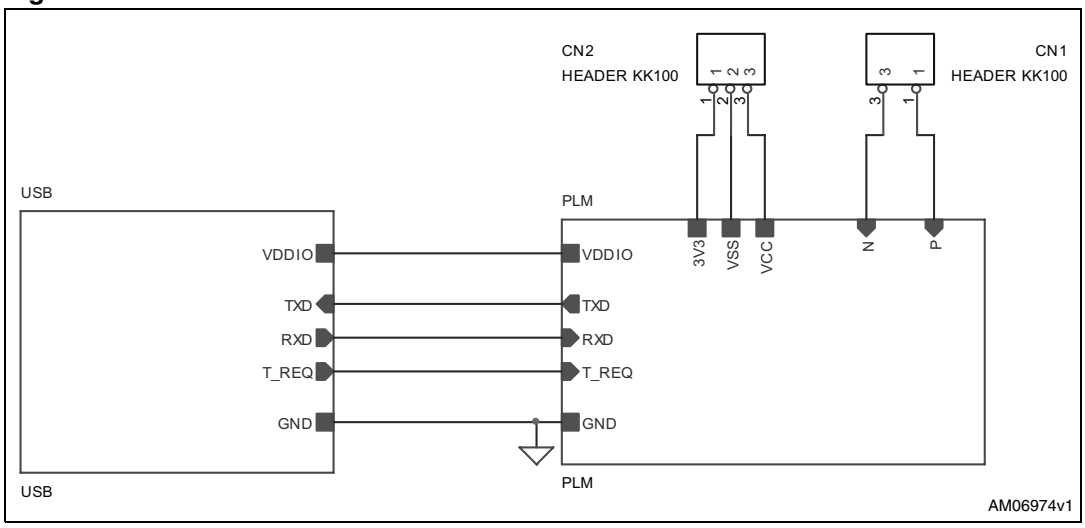


Figure 6. ST7570 schematic circuit (part 1)

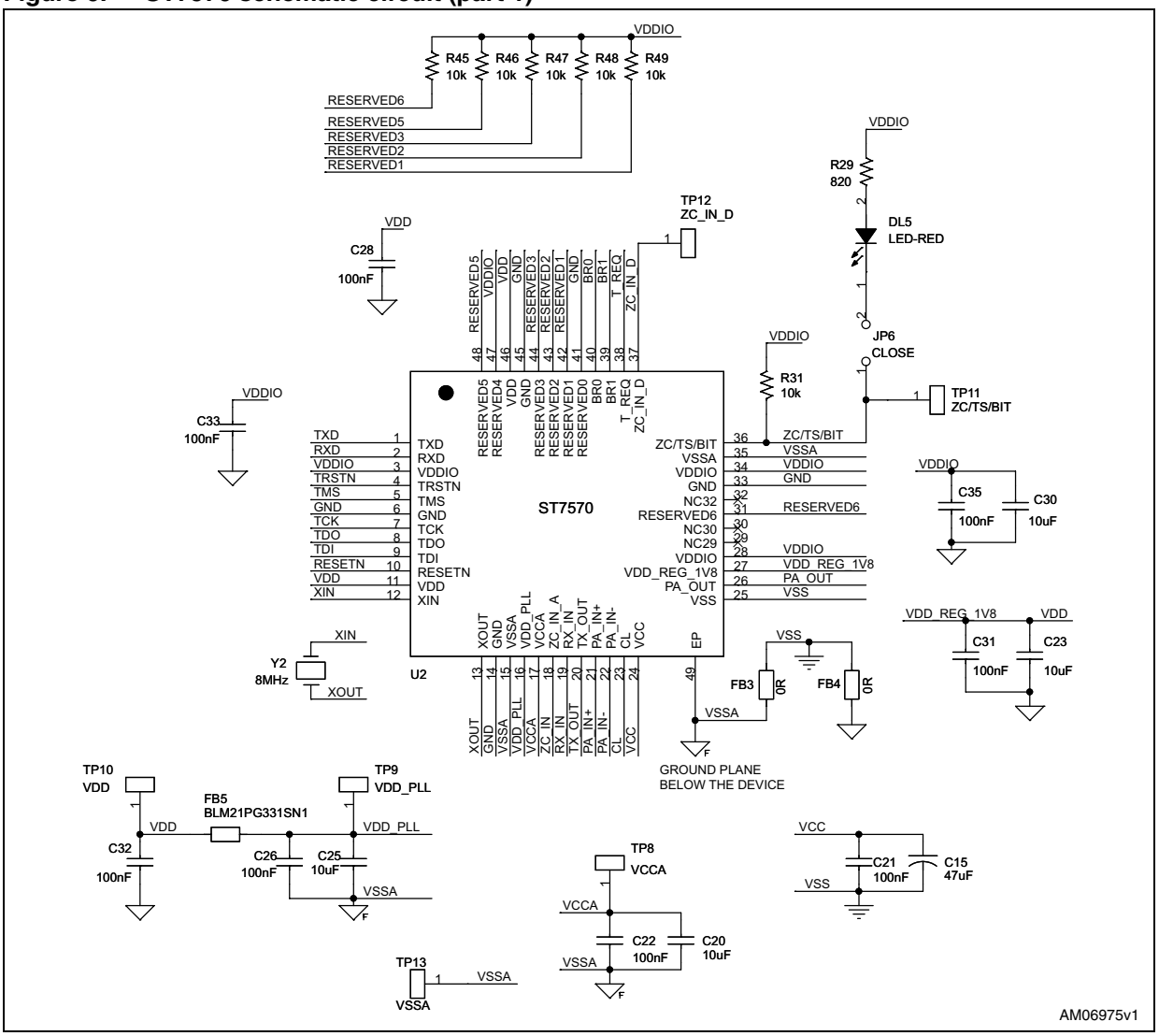


Figure 7. Power supply section

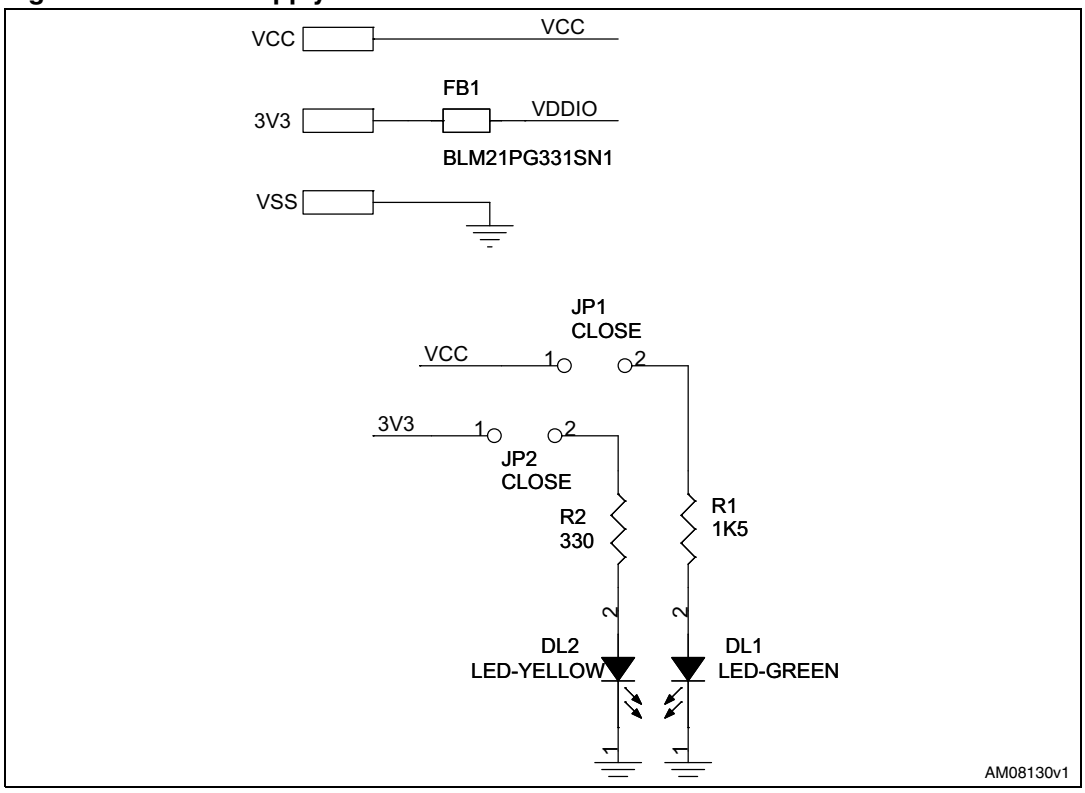


Figure 8. UART interface section

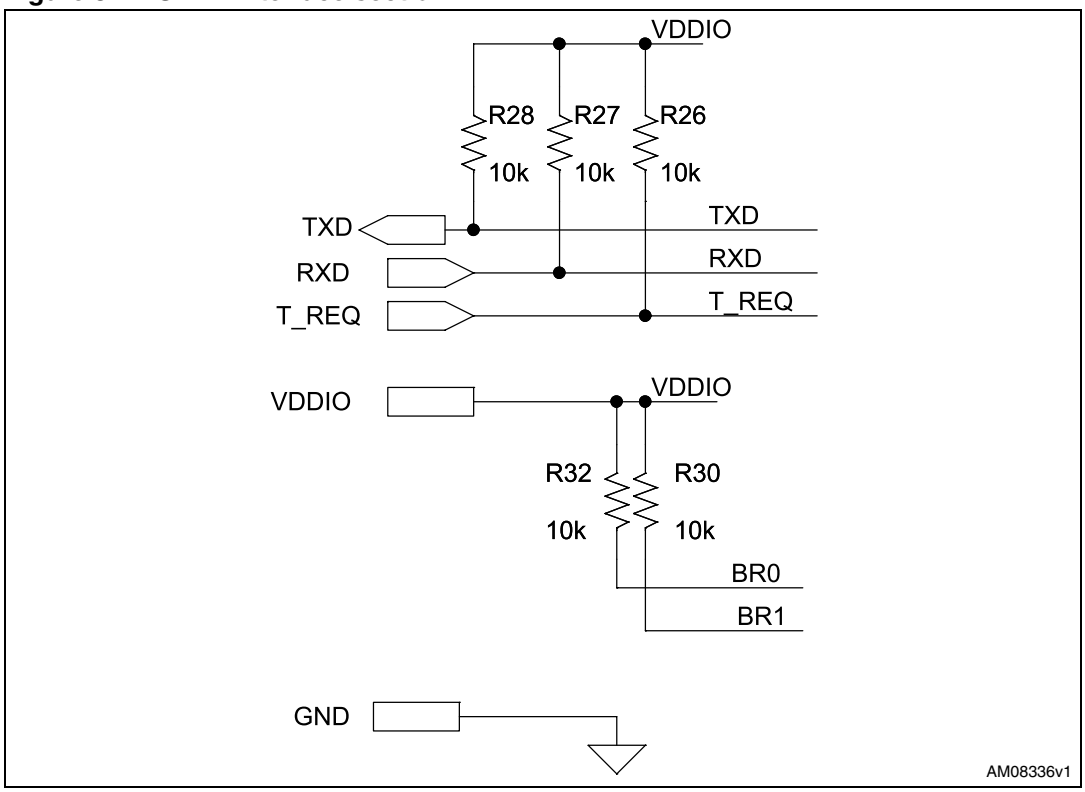


Figure 9. External microcontroller connection section

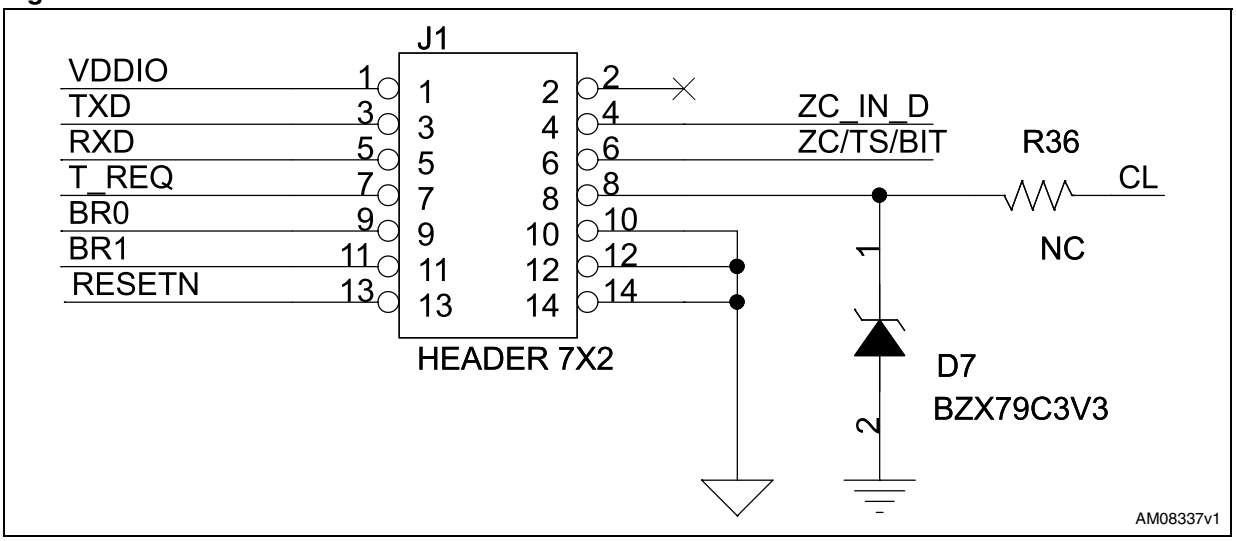


Figure 10. ST7570 schematic circuit

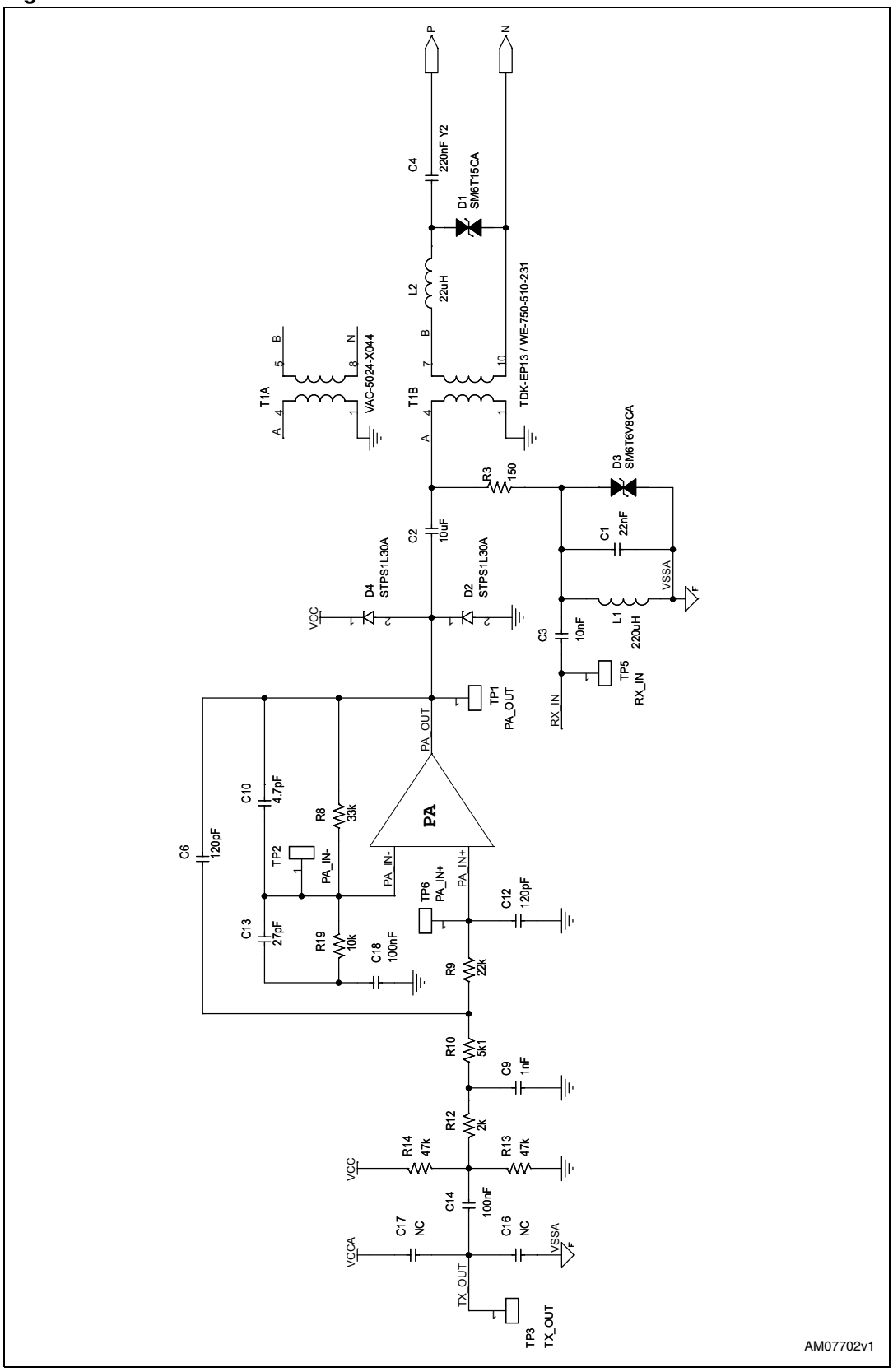


Figure 11. Reset circuit section

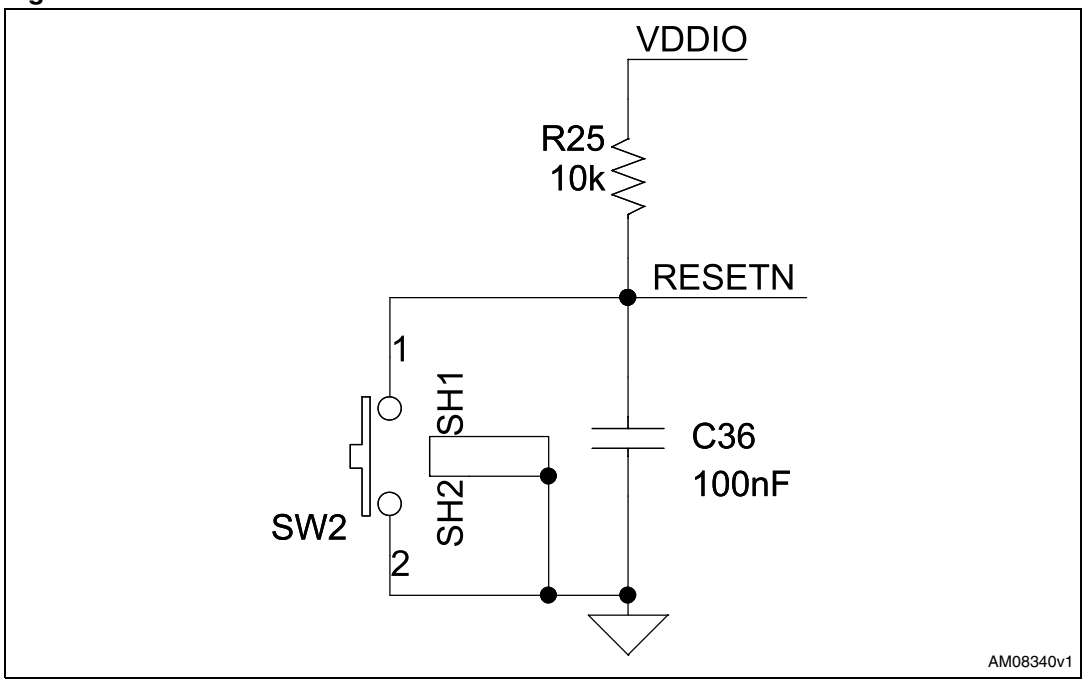


Figure 12. JTAG lines

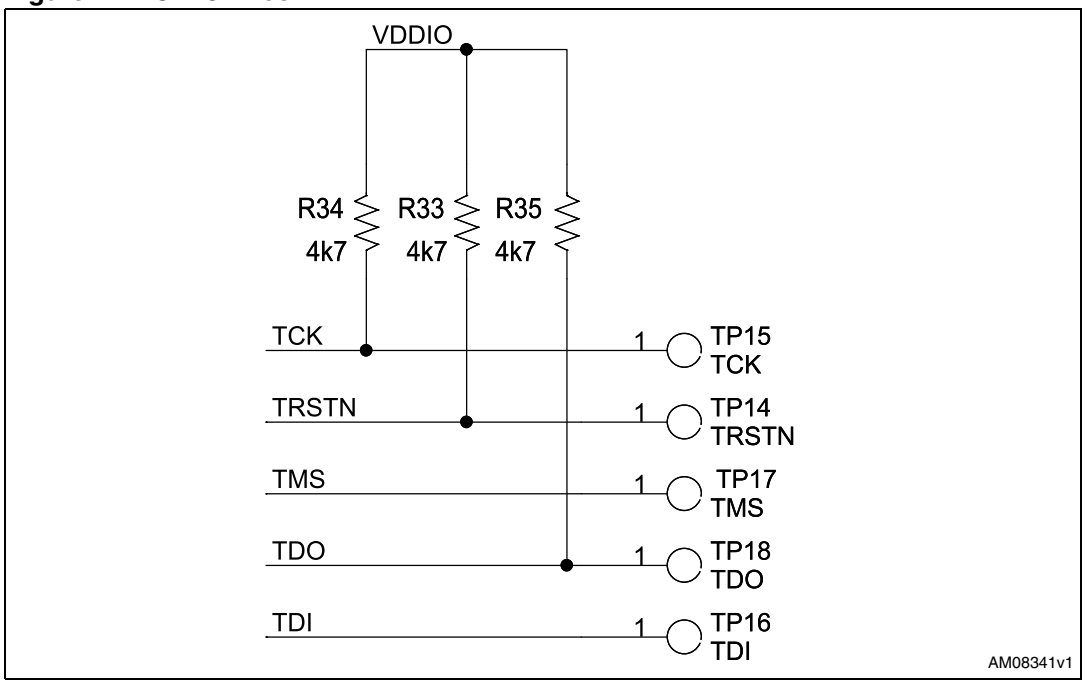


Figure 13. Current limit setting

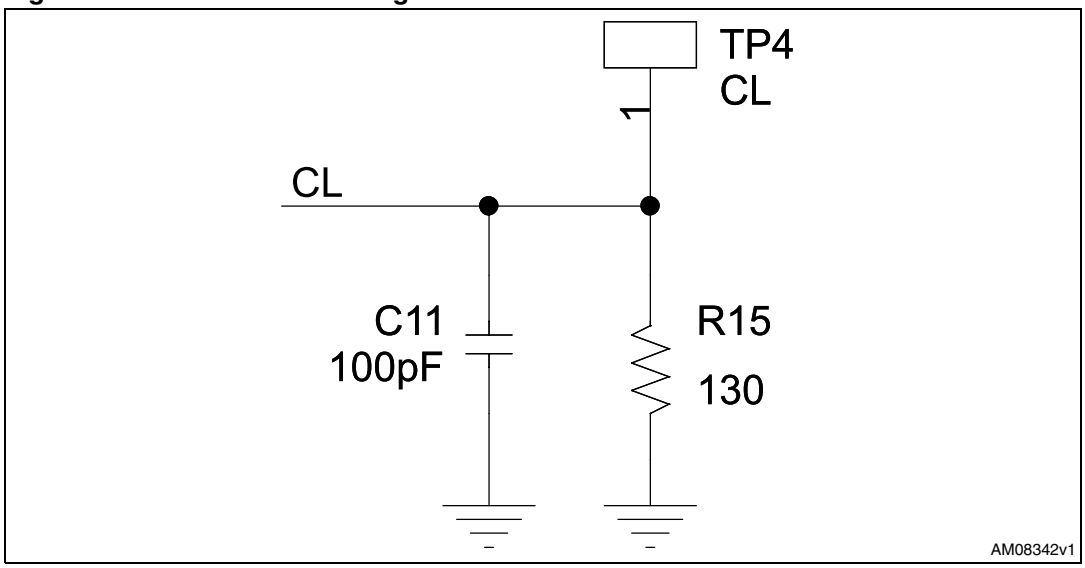


Figure 14. Non-isolated zero crossing

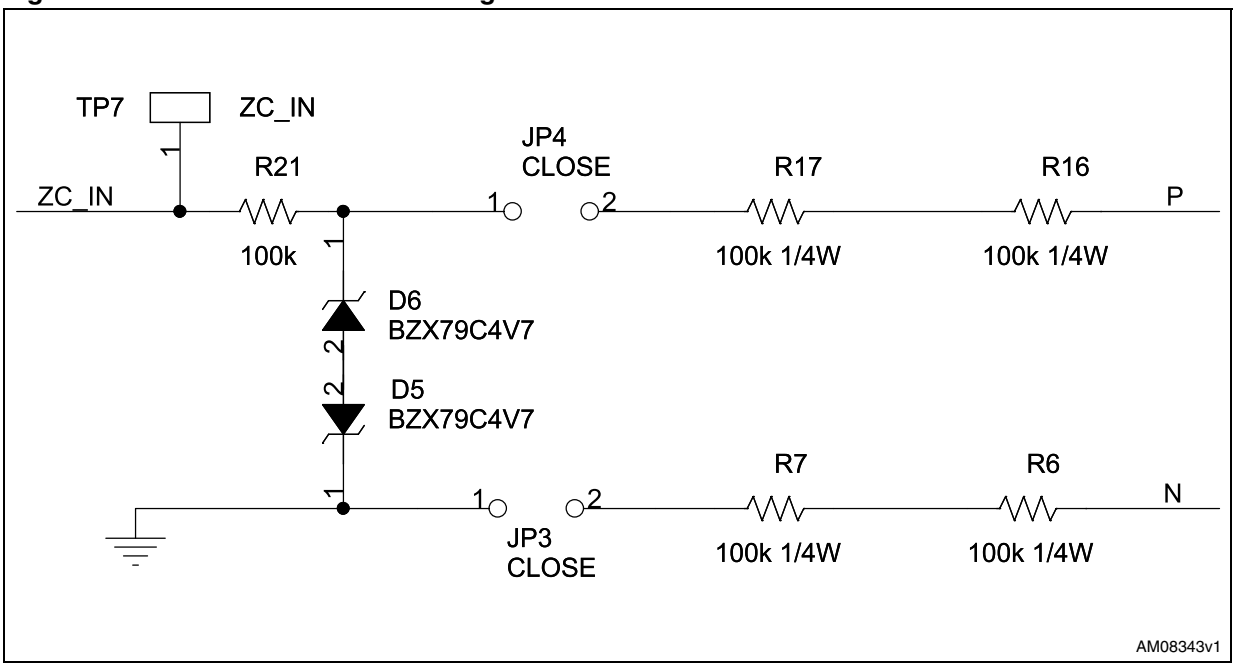


Figure 15. USB to UART connection

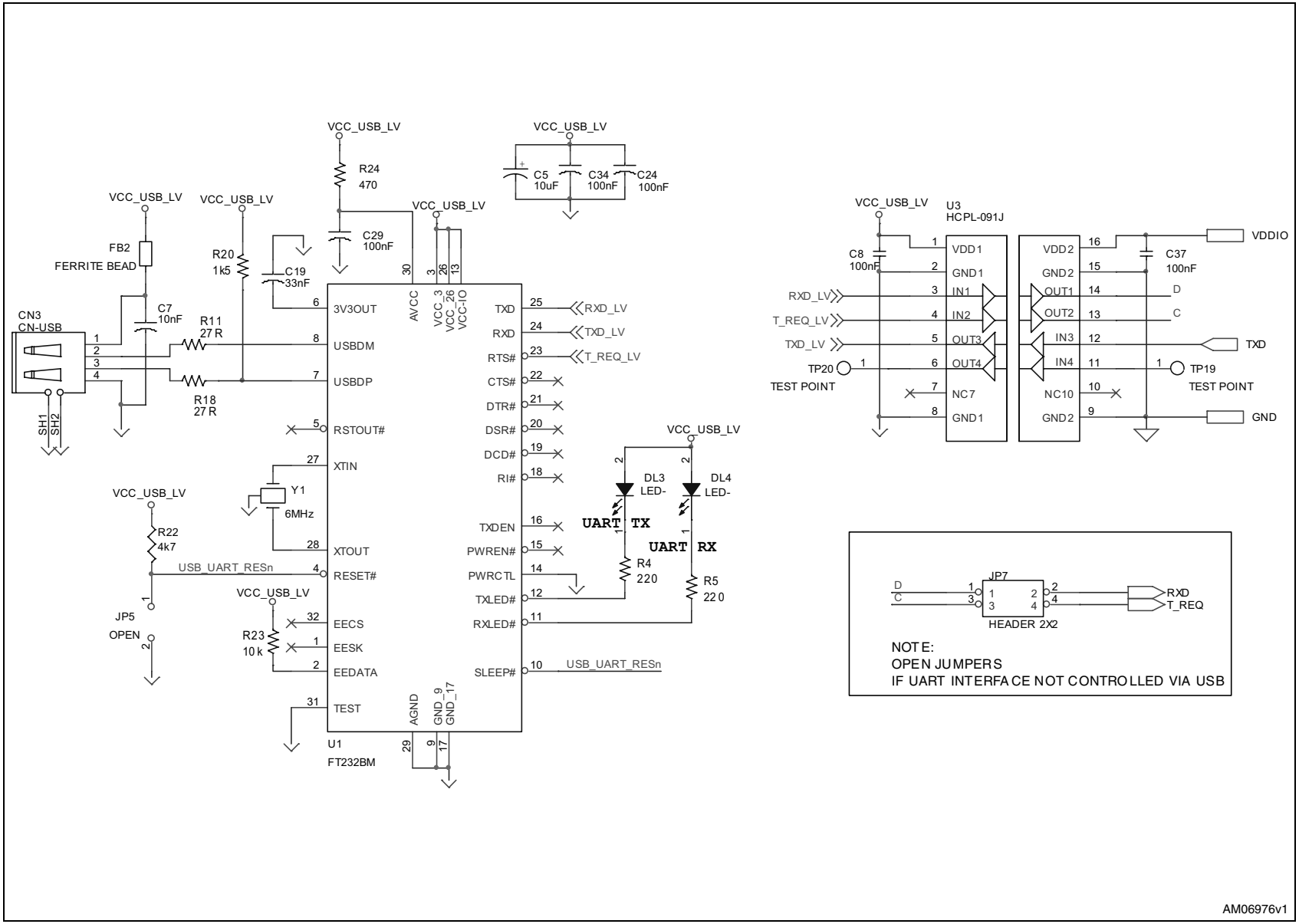


Table 3. BOM list

Part	Value	Description
CN1	Connector 2x1	Molex KK 100, 3-pole, right angle, p=2.54 mm (central pin removed)
CN2	Connector 3x1	Molex KK 100, 3-pole, right angle, p=2.54 mm
CN3	USB connector	USB type B
C1	22 nF	SMD 0805 X7R 50 V
C2	10 µF	SMD 1206 X5R 25 V
C3	10 nF	SMD 0805 X7R 50 V
C4	220 nF Y2	Epcos B32023-B3224K p=22.5 mm
C5	10 µF	SMD 3528 Tantalum 16 V
C6, C12	120 pF	SMD 0603 NP0 50 V
C7	10 nF	SMD 0603 X7R 50 V
C8, C14, C18, C21, C22, C24, C26, C28, C29, C31:C37	100 nF	SMD 0603 X7R 50 V
C9	1 nF	SMD 0603 X7R 50 V
C10	4.7 pF	SMD 0603 NP0 50 V
C11	100 pF	SMD 0603 NP0 50 V
C13	27 pF	SMD 0603 NP0 50 V
C15	47 µF	SMD 6032 Tantalum 16 V
C16, C17	NC	SMD 0603
C19	33 nF	SMD 0603 X7R 50 V
C20, C23, C30	10 µF	SMD 0805 X7R 10 V
C25	10 µF	SMD 0603 X5R 6.3 V
DL1	Green LED	SMD 0805
DL2	Yellow LED	SMD 0805
DL4	Blue LED	SMD 0805
DL3, DL5	Red LED	SMD 0805
D1	SM6T15CA	Bi-directional Transil diode, SMB
D2, D4	STPS1L30A	Schottky diode, SMA
D3	SM6T6V8CA	Bi-directional Transil diode, SMB
D5, D6	BZX79C4V7	Zener diode, SOD80
D7	BZX79C3V3	Zener diode, SOD80
FB1, FB5	BLM21PG331SN1	Ferrite bead, 0805
FB3, FB4	0	Ferrite bead not mounted, 0805
FB2	MI0805K400R-10	Ferrite bead, 0805

Table 3. BOM list (continued)

Part	Value	Description
JP1, JP4, JP6	Jumper	Close
JP5	Jumper	Open
JP7	Strip 2x2	Right angle - Close 1-2, 3-4
J1	Connector 7x2	Flex connector, male, right angle
L1	220 µH	Epcos B82462-A4224K
L2	22 µH	Epcos B82464-A4223K
R1	1.5 kΩ	SMD 1206
R2	330 Ω	SMD 1206
R3	150 Ω	SMD 0603
R4, R5	220 Ω	SMD 0603
R6, R7, R16, R17	100 kΩ	SMD 1206 ¼ W
R8	33 kΩ	SMD 0603
R9	22 kΩ	SMD 0603
R10	5.1 kΩ	SMD 0603
R11, R18	27 Ω	SMD 0603
R12	2 kΩ	SMD 0603
R13, R14	47 kΩ	SMD 0603
R15	130 Ω	SMD 0603
R19, R23, R25:R28, R30:R32, R45:R49	10 kΩ	SMD 0603
R20	1.5 kΩ	SMD 0603
R21	100 kΩ	SMD 0603
R22, R33:R35	4.7 kΩ	SMD 0603
R24	470 Ω	SMD 0603
R29	820 Ω	SMD 0603
R36	NC	SMD 0603
SW2	Reset button	Right angle
T1A	Line transformer - A	VAC 5024-X044
T1B	Line transformer - B	WE 750-510-231 / TDK SRW13EP-X05H002
U1	FT232BM	USB to UART converter
U2	ST7570	Power line communication SoC, QFN48
U3	HCPL-091J	Quad digital isolator, 16-pin SOIC narrow body
Y1	6 MHz	HC49U

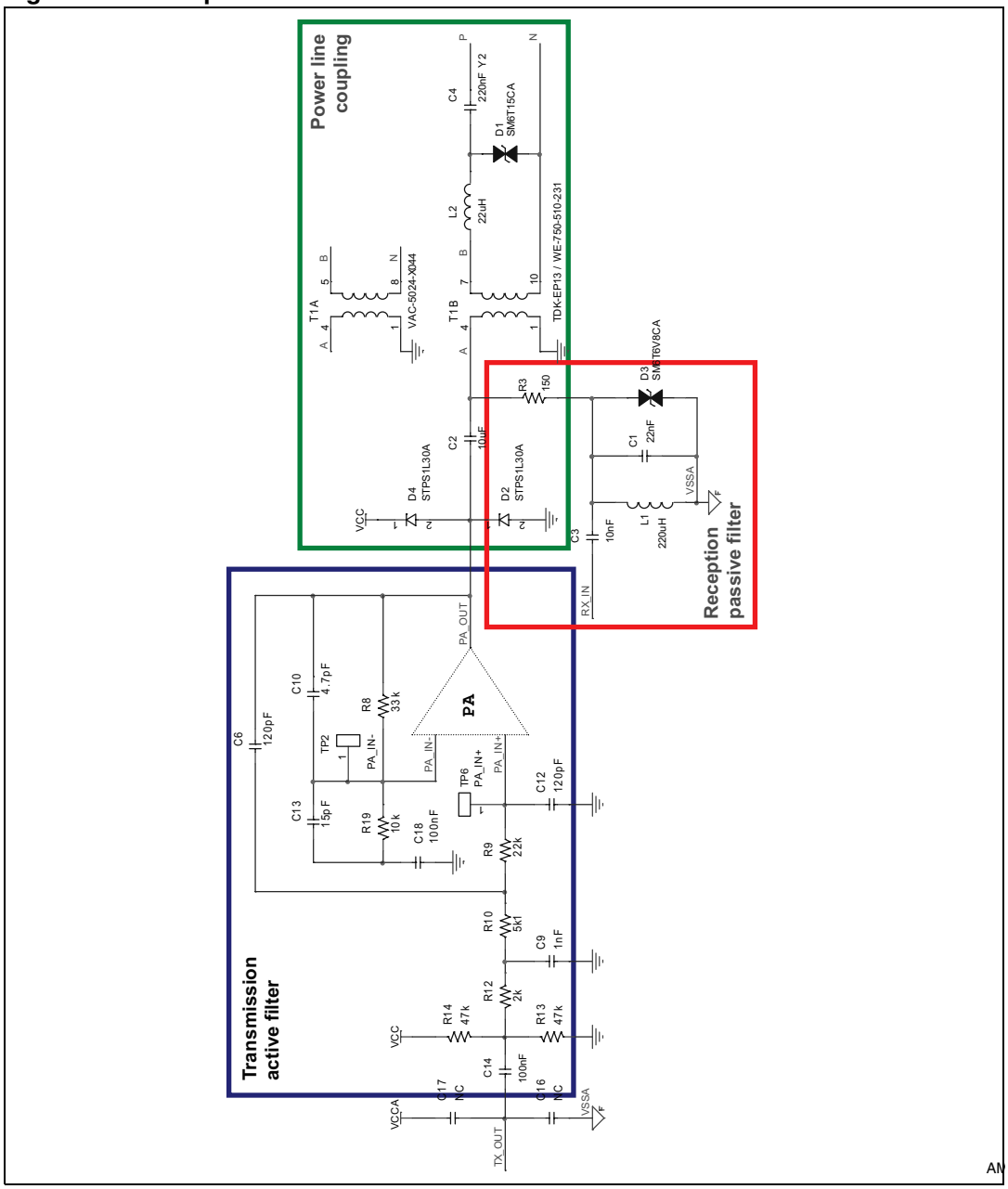
Table 4. ST parts on board

Part	Value	Description
D1	SM6T15CA	Bi-directional Transil diode, SMB
D2, D4	STPS1L30A	Schottky diode, SMA
D3	SM6T6V8CA	Bi-directional Transil diode, SMB
U2	ST7570	Power line communication SoC, QFN48

7.1 Line coupling section

The line coupling section is composed of four different circuits; the transmission active filter, the reception passive filter, the power line coupling, and the zero crossing coupling. All four sections are described below. For each section, calculations and measured behavior are reported. The frequency response of the filters is usually sensitive to the component value tolerance. Actual components used in the ST7570 demonstration board have the following tolerances: +/-10 % for coils and for the Y2 capacitor, +/-1 % for SMD resistors, and +/-5 % for SMD ceramic capacitors. To evaluate the sensitivity to these possible variations, simulated responses are also included with Montecarlo statistical analysis of response variation vs. spread of component value.

Figure 16. Reception and transmission filter schematics



7.1.1 Transmission active filter

The transmission active filter is based on the ST7570 internal Power Amplifier (PA), with input and output pins externally available to allow a filtering network tailored around the amplifier. For the ST7570 demonstration board, a 3-pole low-pass filter has been realized by cascading a simple R-C low-pass stage and a Sallen-Key 2-pole cell. The R12-C9 low-pass stage is aimed at having a corner frequency of nearly 80 kHz, just above the higher S-FSK tone, for a first filtering of the TX_OUT harmonics. The 1 nF value of C9 has been found to be the optimal value to obtain a good filtering action without yielding unwanted capacitive load distortion on the TX_OUT line. The transfer function of the 2nd order Sallen-Key cell is:

Equation 1

$$A(s) = \frac{A_0}{\frac{s^2}{\omega_C^2} + \frac{s}{\omega_C \cdot Q} + 1}$$

Where

Equation 2

$$A_0 = \left(1 + \frac{R_8}{R_{19}}\right) = 4.3 = 12.7\text{dB}$$

Equation 3

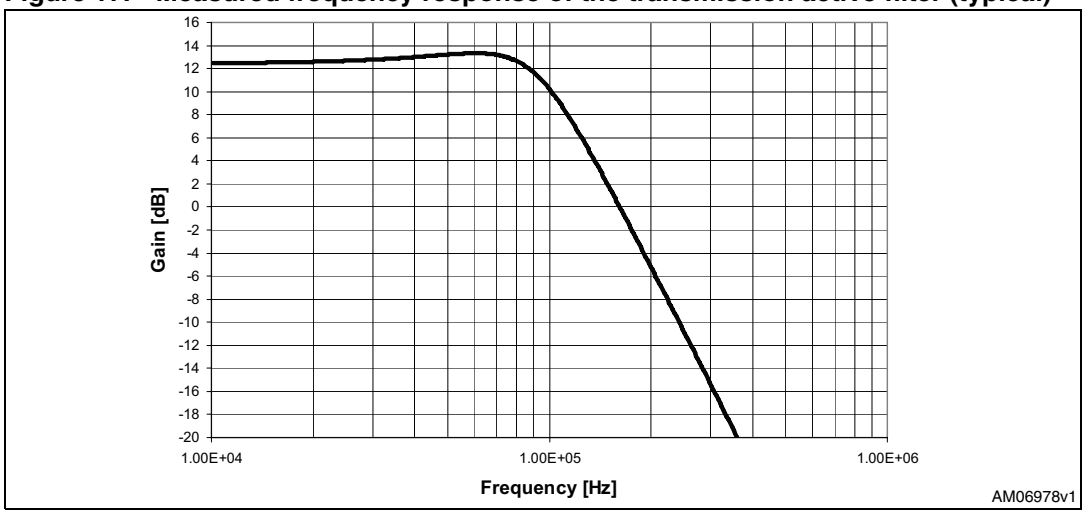
$$f_C = \frac{1}{2\pi \cdot \sqrt{R_9 \cdot R_{10} \cdot C_6 \cdot C_{12}}} = 125\text{kHz}$$

Equation 4

$$Q = \frac{\sqrt{R_9 \cdot R_{10} \cdot C_6 \cdot C_{12}}}{R_{10}C_{12} + R_9C_6 + R_{10}C_6(1 - A_0)} = 1.03$$

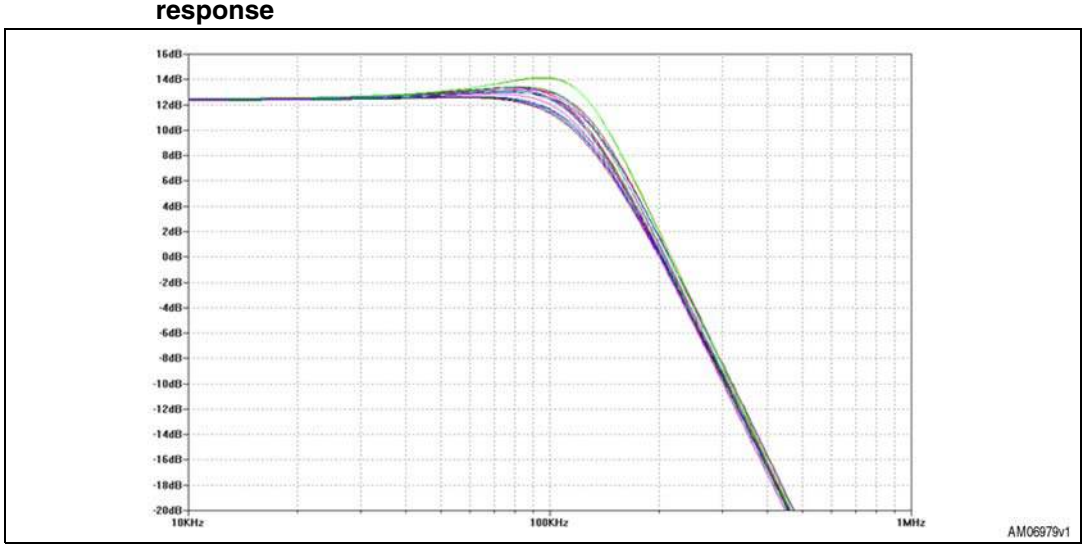
Figure 17 represents measured transfer function of the transmission active filter. It shows good rejection at signal harmonic frequencies.

Figure 17. Measured frequency response of the transmission active filter (typical)



Simulation of the Tx active filter response against component tolerance, depicted in *Figure 18*, shows +/-1 dB variation in gain module within the signal bandwidth, while the Q variation is more sensitive around 100 kHz.

Figure 18. Montecarlo simulation of the transmission active filter frequency response



7.1.2 Reception passive filter

The reception filter is made up of the series of a resistor and a parallel L-C resonant. The transfer function of the filter can be written as:

Equation 5

$$R(s) = \frac{\frac{s \cdot L_1 + R_L}{R_3 L_1 C_1'}}{s^2 + \frac{R_3 R_L C_1' + L_1}{R_3 L_1 C_1'} \cdot s + \frac{R_3 + R_L}{R_3 L_1 C_1'}}$$

Where

- R_L is the DC series resistance of the inductor (in this case, about 2 Ω)
- C_1' is the parallel of C_1 with the reverse capacitance of the transil diode D_3, which is about 2 nF.

The center frequency and the quality factor of the filter can be expressed as:

Equation 6

$$fc = \frac{1}{2\pi} \cdot \omega_C = \frac{1}{2\pi} \sqrt{\frac{R_3 + R_L}{R_3 L_1 C_1'}} \cong \frac{1}{2\pi \sqrt{L_1 C_1'}} = 69 \text{ kHz}$$

Equation 7

$$Q = \frac{R_3 L_1 C_1'}{R_3 R_L C_1' + L_1} \cdot \omega_C = 1.4$$

It is quite evident that the quality factor and the filter selectivity depend not only on the R_3 value, but also on R_L. A higher R_L leads to lower steepness of the resonance, while a higher R_3 gives higher selectivity.

The R_L value impacts in a more evident way on insertion losses. To evaluate the relationship between R_L and the received signal loss, the following simplified expression of $|R(s)|$ at $f=f_C$ can be used:

Equation 8

$$\left|R(j\cdot 2\pi f_C)\right| \cong Q\cdot\frac{\omega_C\cdot L_1}{R_3} = \frac{1}{1+R_L\cdot R_3\cdot\frac{C_1}{L_1}}$$

With actual values of the components, a loss of about 1 dB is obtained. The same calculation gives unitary transfer if R_L is set to zero.

When looking at the first way to express the module of the transfer function, it can be seen that a higher Q can help to keep the losses to a minimum. On the other hand, it would bring the response to a higher sensitivity to component tolerance.

Figure 19 shows the measured frequency response of the Rx passive filter. The filter shows a -3 dB bandwidth equal to 50 kHz and an attenuation of less than 1 dB at f_C.

Figure 19. Measured frequency response of the reception passive filter (typical)

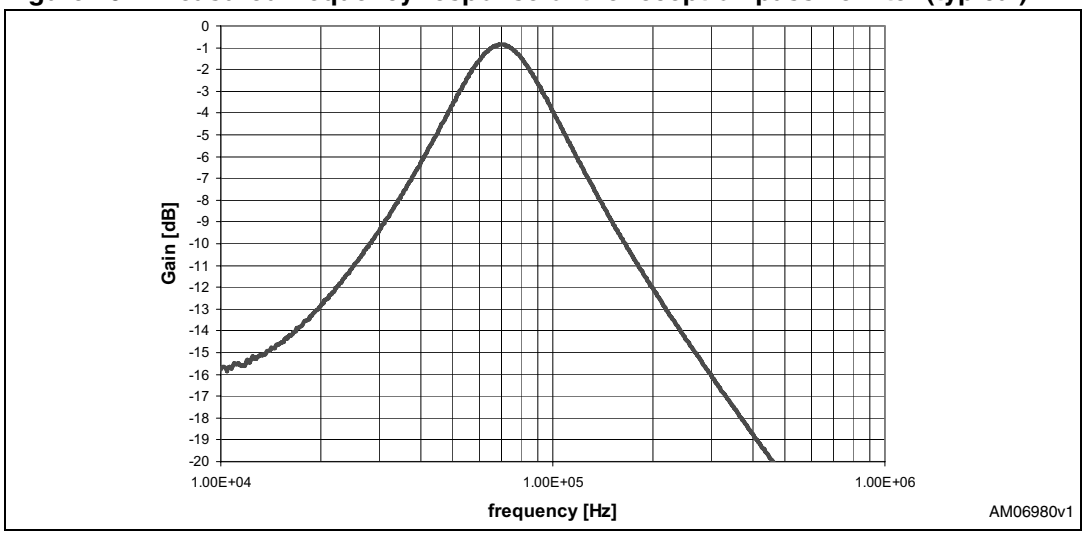
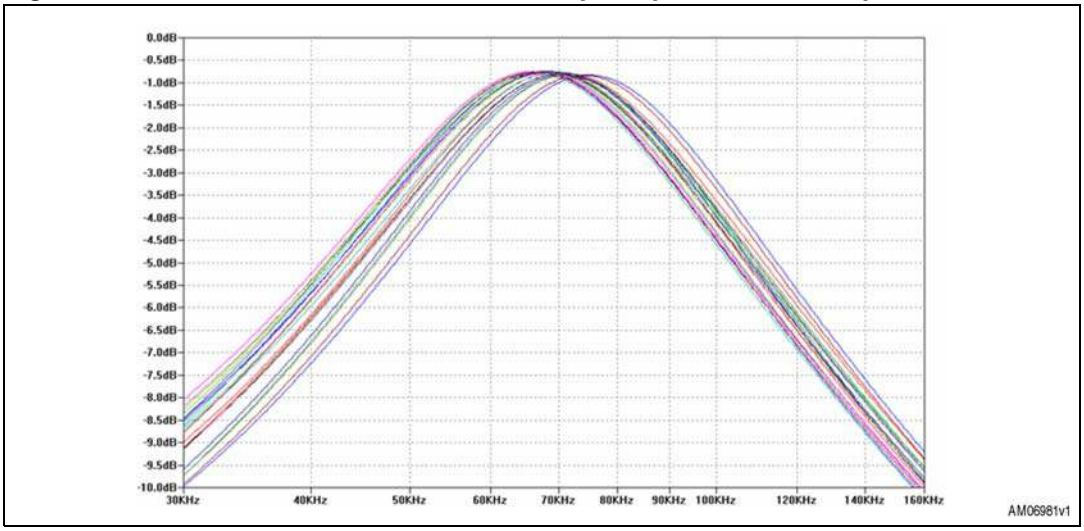


Figure 20 shows the simulation of the response of the Rx passive filter with the components tolerance effect. The shift on the center frequency gives a worst-case loss of nearly 0.5 dB around 68 kHz.

Figure 20. Montecarlo simulation of the reception passive filter response



7.1.3 Power line coupling

The coupling to the power line requires some passive components in addition to the active filtering stage. In particular, it includes the DC decoupling capacitor C2, the line transformer T1, the power inductor L2, and the Y2 safety capacitor C4.

L2 has been accurately chosen to have high saturation current (> 2 A) and very low equivalent series resistance (< 0.1 Ω), to limit distortion and insertion losses even with heavy line load.

Center frequency for the series resonance can be calculated at first approximation as:

Equation 9

$$fc = \frac{1}{2\pi\sqrt{L_2' \cdot C_4}} = 71 \text{ kHz}$$

provided that the capacitance of C2 is much greater than the C4 capacitance. L_2 is the series of L2 and the leakage inductance of the coupling transformer T1, adding about 1 µH to L2. The Q factor of this coupling circuit is driven by the mains line impedance: the choice of the L2 and C4 values leads to 3 dB maximum attenuation when line impedance modulus goes down to 5 Ω.

Particular attention has been paid to choosing the line transformer. The required characteristics are listed in *Table 5*.

In order to have a good signal transfer and minimize the insertion losses, it is recommended to choose a transformer with a primary (shunt) inductance of 1 mH or greater, a leakage inductance much smaller than L2, and a total DC resistance lower than 0.5 Ω.

The 4 kV insulation voltage requirement, the last specified parameter, is described and codified by the EN50065-4-2 CENELEC document (*References 4*).

Table 5. Line coupling transformer specifications

Parameter	Value
Turn ratio	1:1
Shunt inductance	≥ 1 mH
Leakage inductance	≤ 1.5 µH
DC total resistance	≤ 0.5 Ω
DC saturation current	≥ 15 mA
Inter-winding capacitance	< 30 pF
Withstanding voltage	≥ 4 kV

In *Figure 21* the measured response of the whole transmission coupling, loaded with the LISN impedance as set by the EN50065-1 document, is given. The image highlights a further filtering effect added by the passive L-C series resonant combined with the LISN reactive load.

Figure 21. Measured frequency response of the Tx active + passive filter loaded with the EN50065-1 LISN impedance (typical)

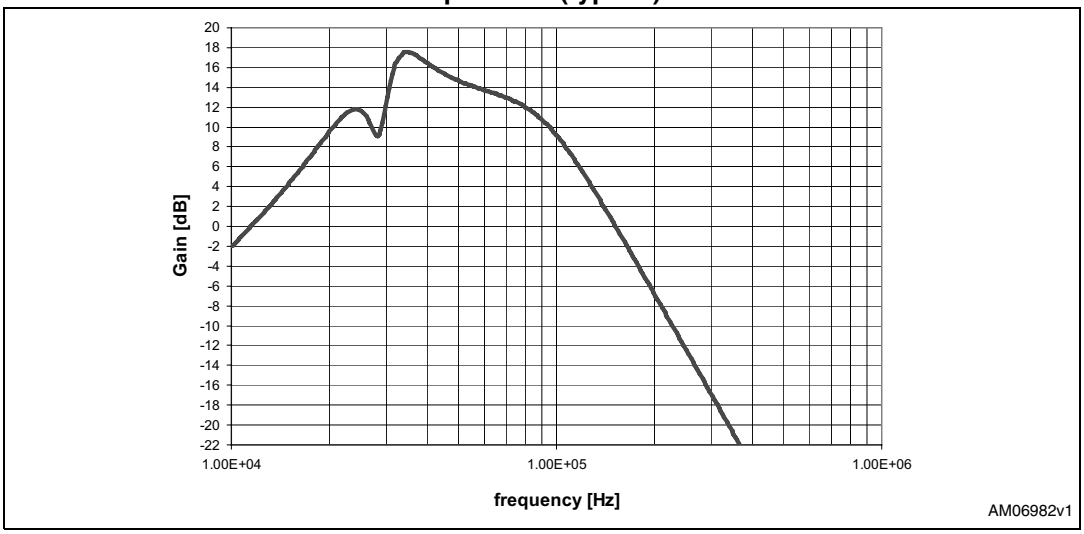
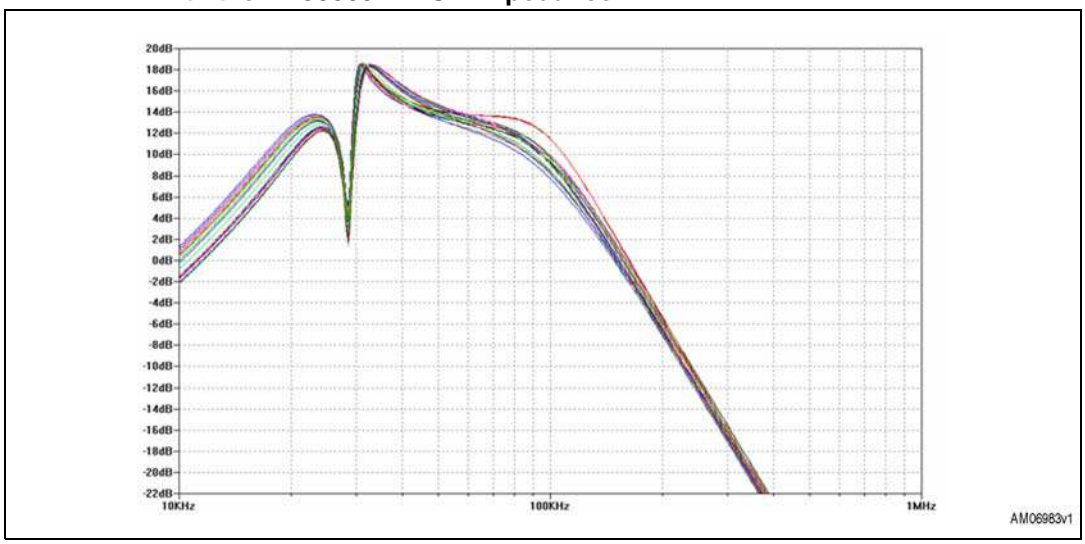


Figure 22 represents the Montecarlo simulation of the cumulated response of transmission active and passive filters, loaded with the LISN impedance, as set by the EN50065-1 document (*References 3*). Due to the response slope and the effect of power components, the in-band variation is within +/-1.5 dB.

Figure 22. Montecarlo simulation of the transmission line coupling response loaded with the EN50065-1 LISN impedance



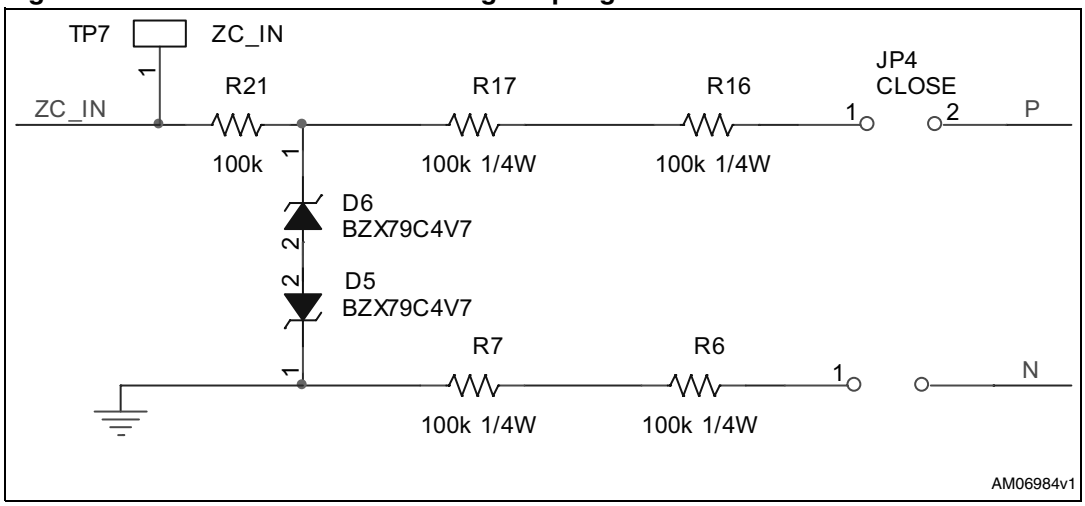
7.1.4 Zero crossing coupling

The zero crossing coupling circuit is aimed at providing an analog signal to the ZC_IN_A pin synchronous with the mains network voltage. This signal must be centered on VSS and limited to ±5 V peak (*References 1*).

The zero crossing circuit is realized through a non-isolated resistive coupling to both neutral and phase lines, as represented in *Figure 23*.

The two Zener diodes clamp the mains voltage at ±4.7 V, keeping the same slope as the mains voltage around the zero crossing. The four 100 kΩ series resistors limit the Zener current to 1.5 mA rms. Having two resistors per line helps prevent short-circuits in the case of resistor degradation.

Figure 23. Non-isolated zero crossing coupling circuit



This circuit introduces a delay of nearly 30 µs between the mains zero crossing and the ZC_IN_A input pin, as represented in *Figure 24*. *Figure 25* shows an oscilloscope infinite persistence snapshot showing an overall jitter lower than 10 µs.

Figure 24. ZC_IN_A vs. mains voltage - delay measurement

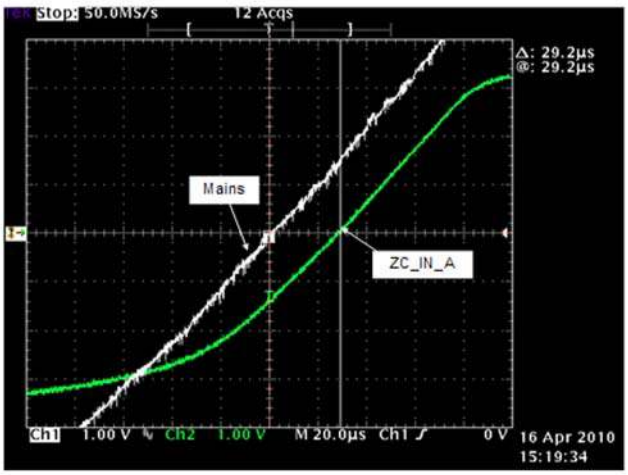
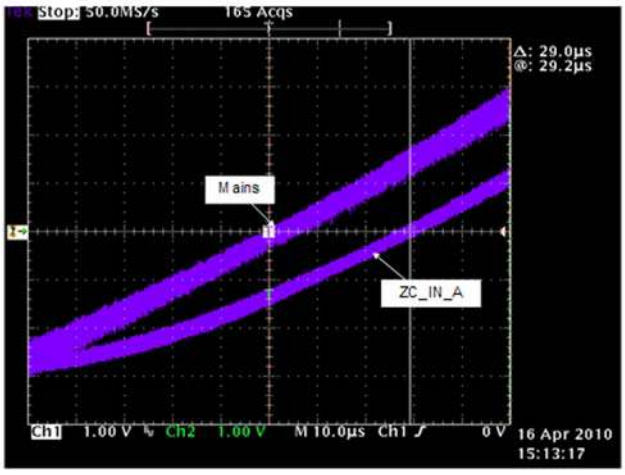


Figure 25. ZC_IN_A vs. mains voltage - jitter measurement



7.1.5 Input impedance

The input impedance of a power line communication node is another critical point. According to the network impedance measurements carried out in some European distribution networks (Italy, Germany and France) the following characteristics can be associated to the impedance of a typical low-voltage (LV) power line:

- Typical impedance magnitude is around 5 Ω
- Nearly 90 % of measured values range between 0.5 and 10 Ω
- The impedance value depends on the measurement point
- The measured value changes over time.

The reasons for these characteristics can be described as follows:

- The LV distribution network has a “tree” structure, with many branches and sub-branches acting as parallel impedances
- Several electronic devices connected to the LV network offer a very low impedance, mostly because of the EMI input filters installed at their mains connection
- The type and number of electronic loads connected to the mains network varies over time

For all these reasons, particular attention must be paid to the impedance of the ST7570 line coupling circuit. Specifically:

- In receiving (idle) mode, the coupling impedance must be high enough to make the power line source impedance negligible and to minimize the mutual interference between different PLC nodes connected to the same network
- In transmitting mode, the coupling impedance must be very low inside the signal bandwidth but high enough for out-of-band frequencies.

According to these requirements, the EN50065-7 standard document fixes the following constraints for the PLC node operating in the A band:

- Tx mode:
  - free in the range 3 to 95 kHz
  - 3 Ω from 95 to 148.5 kHz
- Rx mode:
  - 10 Ω from 3 to 9 kHz
  - 50 Ω between 9 and 95 kHz only inside the signal bandwidth (free for frequencies outside the signal bandwidth)
  - 5 Ω from 95 to 148.5 kHz

Figure 26 and *27* show the input impedance magnitude vs. frequency measured in transmission and reception mode.

The impedance magnitude values prove that the ST7570 demonstration board is compliant with the EN50065-7 requirements. At the same time, the line interface gives an efficient signal coupling both in transmission and reception.

Figure 26. Measured input impedance modulus of the line coupling - reception mode (typical)

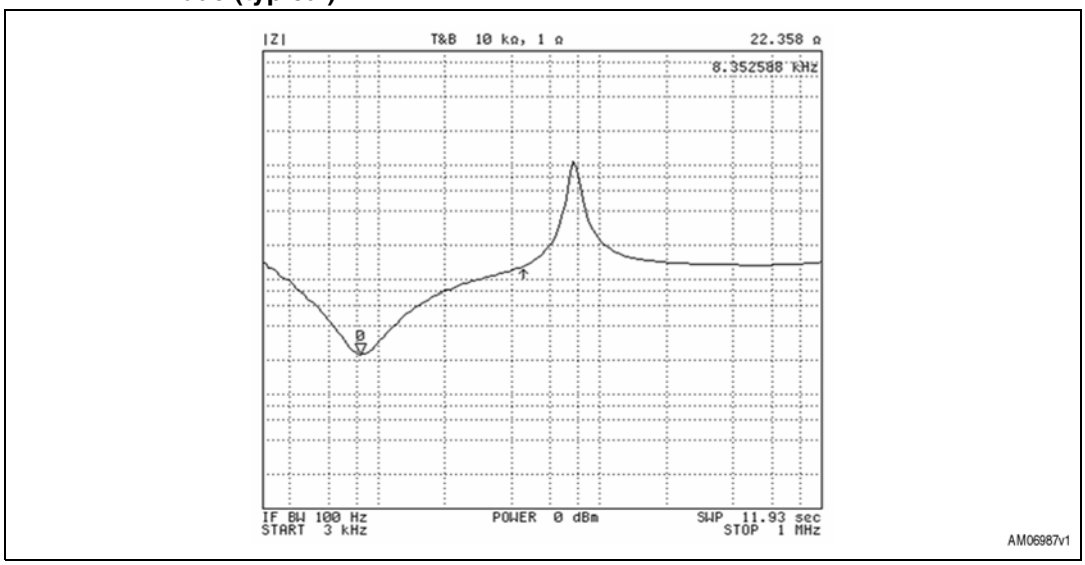
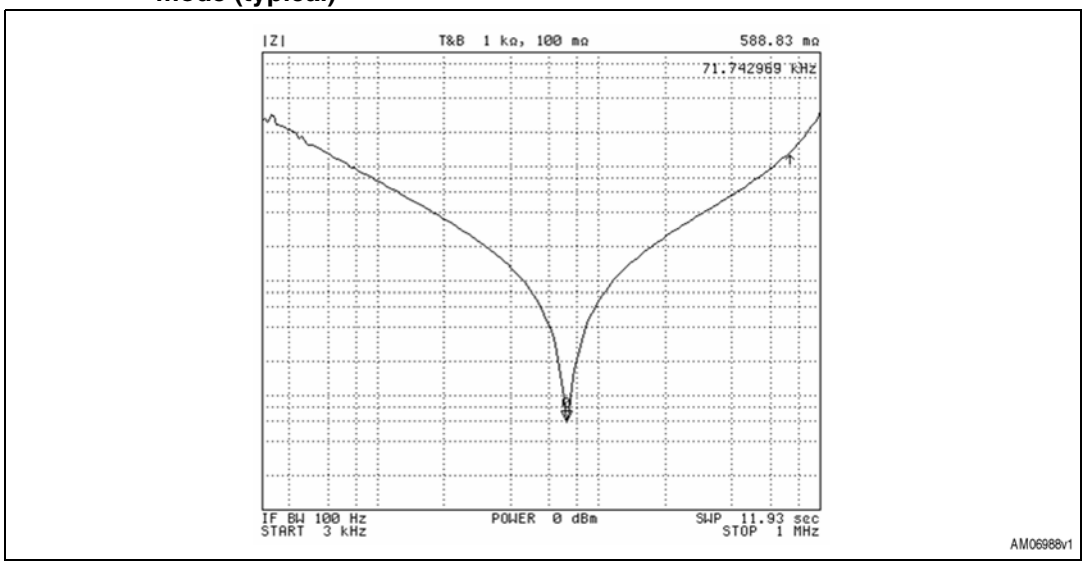


Figure 27. Measured input impedance modulus of the line coupling - transmission mode (typical)



7.2 Conducted disturbances

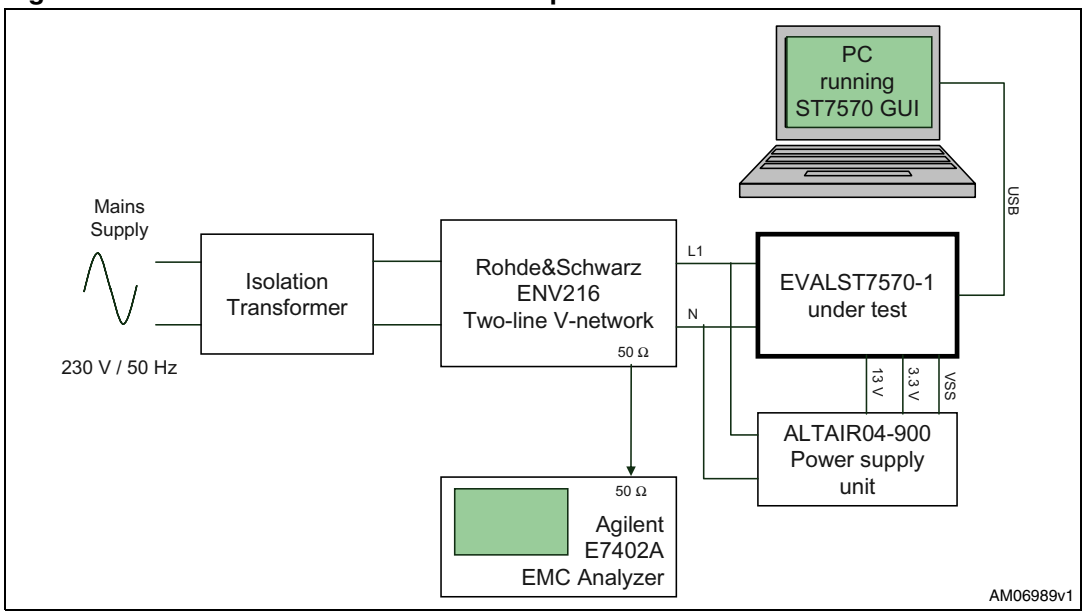
7.2.1 Conducted emission (CE) measurements

The EN50065-1 standard describes the test setup and procedures for these kinds of tests.

The compliance tests have been performed with 230 V AC isolated supply. The test pattern consists of a continuous transmission of the two S-FSK tones, alternating at 2400 baud.

The output signal level has been set to 2.5 V rms (ST7570 TX_GAIN parameter = 23), corresponding to 122 dBµV rms measured at the standard two-line V-network (also called line impedance stabilization network, or LISN) measurement port.

Figure 28. Conducted emissions test setup



The conducted emissions measurement results are reported below. Quasi-peak measurements have been performed, as required by the EN50065-1 standard document. The measured spectrum is always compared to the EN50065-1 compliance limit mask (*References 3*).

Figure 29, *30*, *31*, and *32* show the full set of transmission spectrum measurements.

Figure 29. Conducted emissions: transmission spectrum, quasi-peak measurement, 3 kHz - 150 kHz, line-to-earth, as per EN50065-1

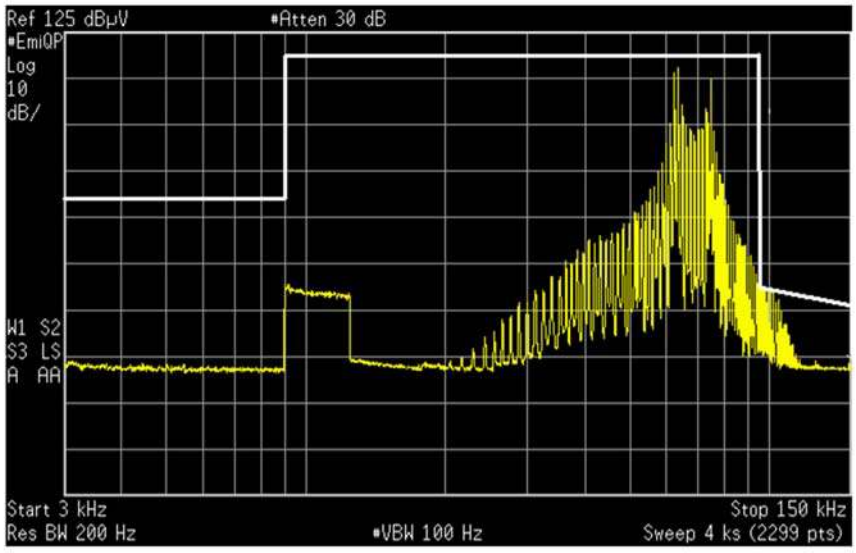


Figure 30. Conducted emissions: transmission spectrum, quasi-peak measurement, 3 kHz - 150 kHz, neutral-to-earth, as per EN50065-1

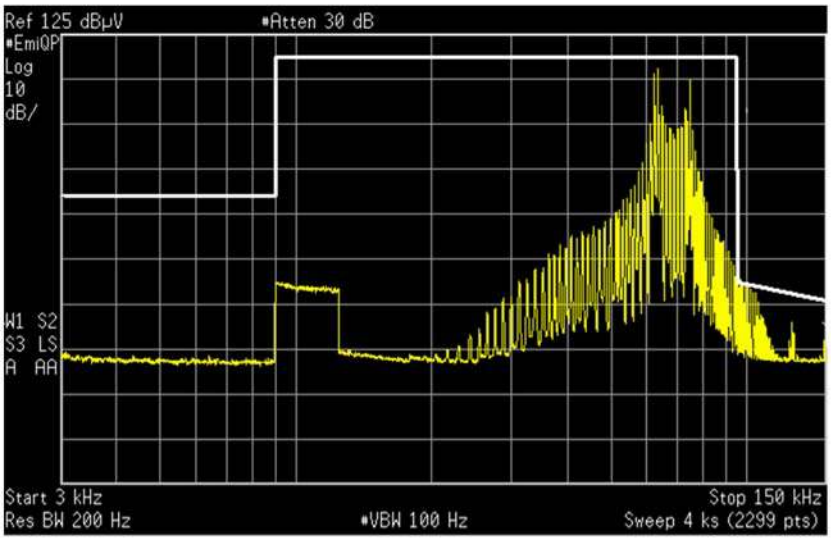


Figure 31. Conducted emissions: transmission spectrum, quasi-peak measurement, 150 kHz - 30 MHz, line-to-earth, as per EN50065-1

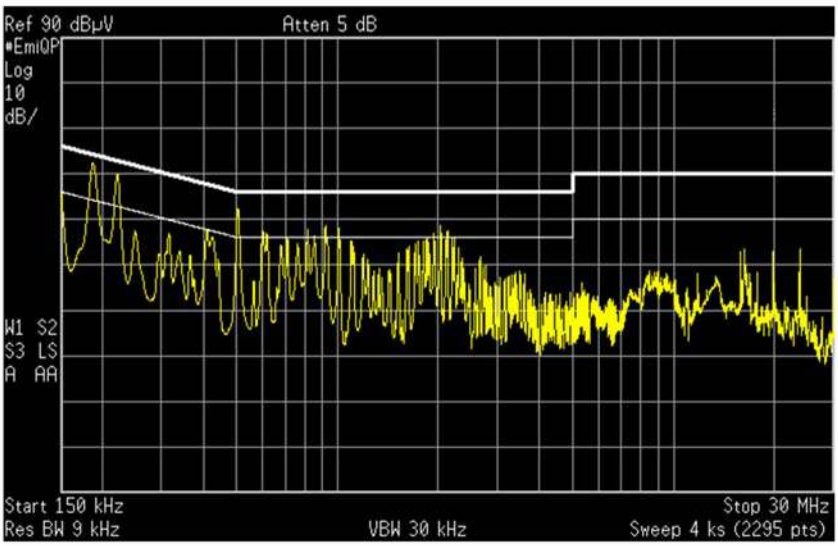
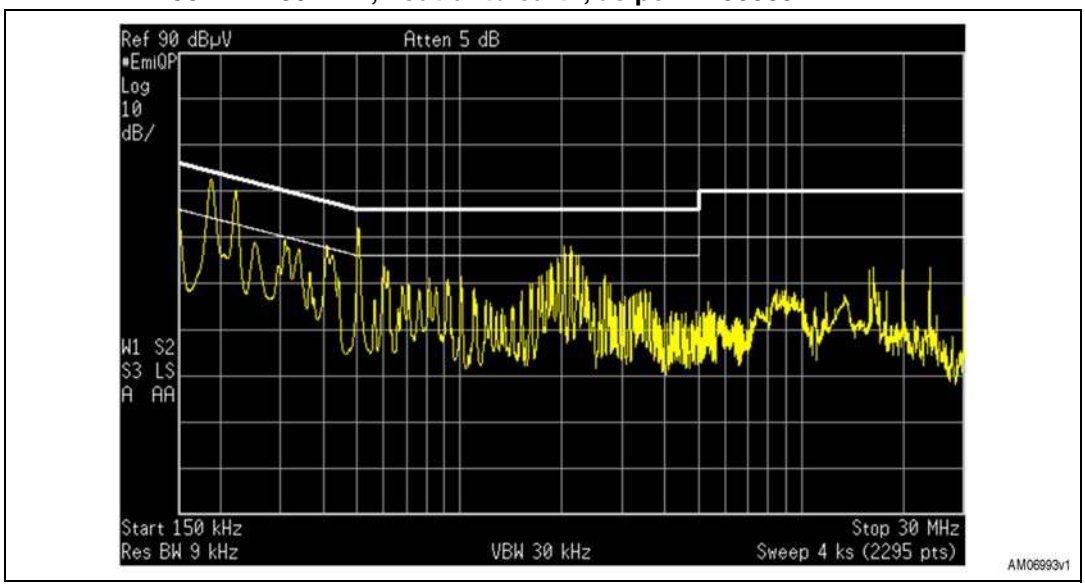


Figure 32. Conducted emissions: transmission spectrum, quasi-peak measurement, 150 kHz - 30 MHz, neutral-to-earth, as per EN50065-1



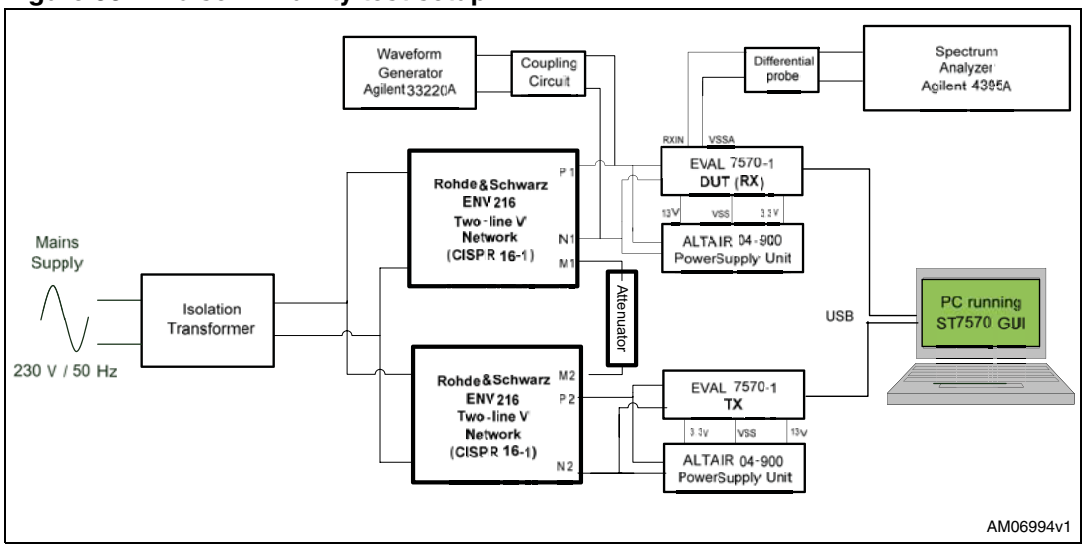
7.2.2 Noise immunity

The tests on immunity against white noise (AWGN) and narrow-band interferers (NBI) are based on two ST7570 demonstration boards, performing a unidirectional point-to-point communication. The first board transmits a message with a known bit pattern, while the receiving board passes the received message to the ST7570 GUI software, which calculates the percentage of wrong bits (BER). The tests have been performed at 1200 and 2400 baud.

Figure 33 shows the test environment used to perform noise immunity tests.

The noise (AWGN or NBI) is produced by a waveform generator and injected into the network through an AC coupling circuit; this circuit is mandatory to protect the waveform generator output.

Figure 33. Noise immunity test setup



Noise and signal are measured independently on the RX_IN pin of the ST7570 through a spectrum analyzer with a differential 1 MΩ probe. When measuring the signal level S_S (expressed in dBµV rms), the transmitting ST7570 device is set in continuous transmission of a single sine tone, allowing the measurement of the signal level to be performed with a resolution bandwidth (RBW) of 100 Hz. The probe was removed during communication tests to avoid any interference.

7.2.3 AWGN tests

These tests are aimed at testing the demonstration board performance against AWGN and guaranteeing compliance with IEC61334-5-1 requirements (*References 5*).

The value of injected noise has been kept constant during all performance tests; different SNR values have been set by changing the signal level on the transmitting ST7570 device.

The measured noise level has been obtained with an RBW equal to 3 kHz. As the spectrum analyzer is integrating the noise spectral density over its RBW, the actual noise level S_N (expressed in dBµV rms) can be obtained by scaling the measured value to the modulated signal bandwidth SBW (that is, 1200 or 2400 Hz according to the baud rate). *Equation 10* expresses the relationship between measured and actual noise level.

Equation 10

$$S_N[dB\mu Vrms] = \text{measured noise value}[dB\mu Vrms] \cdot 10Log(\frac{SBW}{RBW})$$

Table 6 gives the actual noise level at each S-FSK tone frequency in the test setup of *Figure 33*.

Table 6. Noise level S_{N0} and S_{N1} during AWGN tests

SBW [Hz]	S_{N0} [dBµV rms]	S_{N1} [dBµV rms]
1200	41.12	39.82
2400	44.13	42.83

The signal-to-noise ratio (SNR) values for the two S-FSK tones can be calculated as: $SNR_0 = \frac{S_{S0}}{S_{N0}}$ and $SNR_1 = \frac{S_{S1}}{S_{N1}}$. The average SNR_{AV} is calculated in accordance with *Equation 11* as in *References 3*:

Equation 11

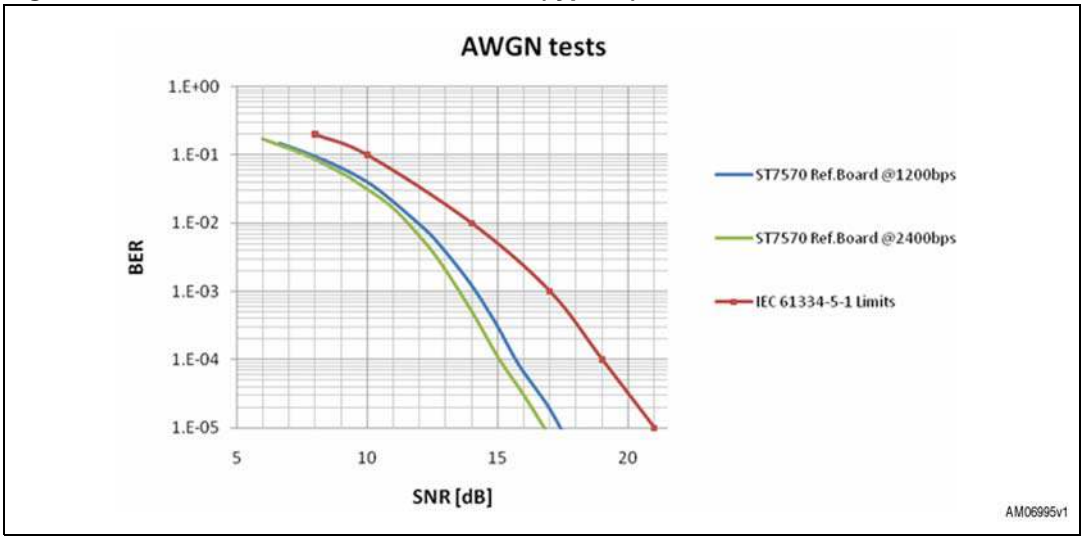
$$SNR_{AV} = \frac{2 \cdot SNR_1 \cdot SNR_0}{SNR_1 + SNR_0}$$

The difference found between noise levels on f_0 and f_1 frequencies is mostly due to non-flat response of transmission and reception filters. Nevertheless, these values can be considered as a real case for evaluating the ST7570 demonstration board performance in communication tests.

S_{S0} and S_{S1} have the same unbalancing, so the resulting difference between SNR_0 and SNR_1 is about 1 dB.

Figure 34 represents the BER vs. SNR curve in the presence of white noise for both 1200 bps and 2400 bps at 50 Hz in these conditions.

Figure 34. Measured BER vs. SNR curve (typical), white noise



7.2.4 NBI tests

In order to test the demonstration board immunity to a narrow-band interferer (NBI), the method described in the IEC61334-5-1 standard has been followed (*References 5*). It requires a sine wave interferer at a 20 kHz < f_N < 95 kHz frequency to be applied at the receiving device. Setting an rms interferer level equal to SN and an rms signal level equal to S_S, the BER of the receiving device must be lower than 10-5 with S_N/S_S < 30 dB.

The waveform generator has been used to provide the sine wave signal, whereas a second demonstration board was generating packet traffic compliant with IEC61334-5-1 at PHY layer (standard preamble and SSD sequence followed by a random payload) (*References 5*).

Table 7 shows the parameters setting the test conditions. Both signal and noise levels have been measured through a spectrum analyzer with differential probe. The resolution bandwidth RBW was equal to 100 Hz.

Table 7. Narrow-band interferer immunity test settings

Parameter	Value
Received signal level	69.5 dBµV rms
Received NBI level	100.0 dBµV rms
Signal bandwidth	2400 Hz

The test returned a BER value lower than 10^{-5} for all the interferer frequencies, proving that the demonstration board is compliant with IEC 61334-5-1 requirements on narrowband interferer tests.

7.3 PCB layout guidelines

7.3.1 Thermal performance

The ST7570 device can operate within the standard industrial temperature range, from -40 to 85 °C ambient temperature. Especially in high ambient temperature conditions, the effect of the power dissipation of the device must be considered to keep it operating in safe conditions.

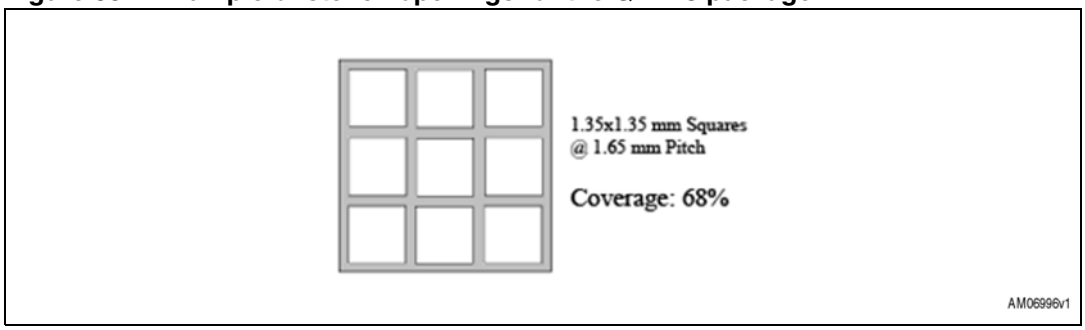
Even though the ST7570 features a built-in thermal shutdown circuitry which turns off the power amplifier (PA) when the die temperature (T_J) exceeds 170 °C, it is recommended not to exceed 125 °C during normal operation to ensure the functionality of the IC.

A QFN48 package with Exposed Pad has been chosen for the ST7570 device to achieve very good thermal performance. However, in order to take full advantage of this, the PCB must be designed to effectively conduct heat away from the package.

To obtain a low impedance thermal path to the PCB, a 5x5 mm thermal pad has been realized on the top layer under the device. In order to effectively remove the heat, the exposed pad must be well soldered to the PCB thermal pad. Therefore, the out-gassing phenomenon due to the soldering process must be controlled to reduce solder voids between the QFN48 exposed pad and the PCB thermal pad. To achieve this, smaller multiple openings in the solder paste stencil should be used instead of one big opening on the thermal pad region. This has also the advantage of reducing the amount of solder paste used, therefore avoiding bridges with perimeter pads.

A suitable example for the QFN48 package is shown in *Figure 35*.

Figure 35. Example of stencil openings for the QFN48 package



Another technique to improve heat conduction on the top layer is to fill all unused areas with copper tied to the dissipating ground plane.

In order to have an effective heat transfer from the top layer of the PCB to the bottom layer, thermal vias need to be included within the thermal pad area. If properly designed, thermal vias are the most efficient paths for removing heat from the device.

An array of 4 x 4 thermal vias at 1.0 mm pitch, with a via diameter of 0.3 mm, have been incorporated into the thermal pad, as shown in *Figure 36* and *37*.

To minimize solder wicking effect due to open vias, possibly leading to poor soldering of the QFN48 exposed pad, the via encroaching technique has been adopted (see bottom-side image in *Figure 37*). The bottom-side solder resist has only small openings (nearly 0.2 mm larger than the via drill diameter) around the vias; the reduced area of exposed copper on the bottom reduces the amount of solder paste flowing down the vias.

Figure 36. PCB copper dissipating area on top layer for the ST7570 demonstration board

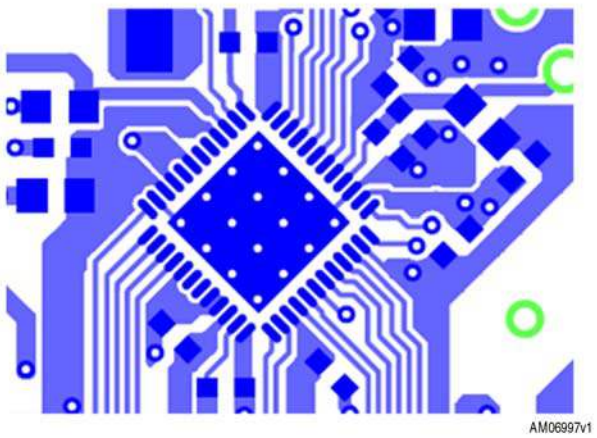
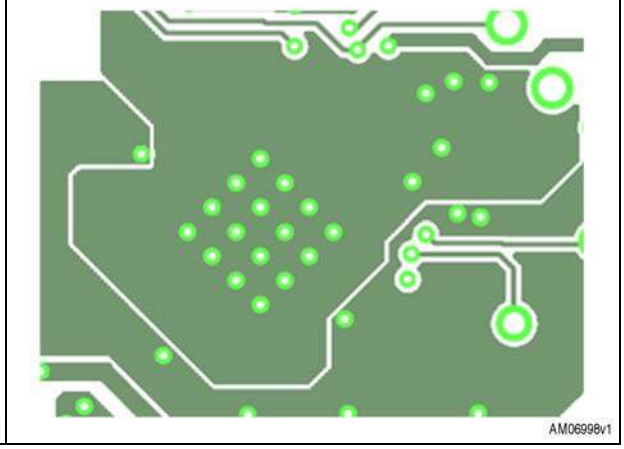


Figure 37. PCB copper dissipating area on bottom layer for the ST7570 demonstration board



Another important parameter for effective heat dissipation is the copper thickness for both top and bottom layers. 1 oz copper is considered as the minimum value to ensure good dissipation.

The bottom-side routing plays an important role too. The solid ground area of copper under the device must be as large as possible to minimize the thermal impedance. Therefore, traces on the bottom-side must run as far as possible from the device area.

7.3.2 Ground connections

Good soldering of the ST7570 exposed pad is also required to minimize ground noise. Being the exposed pad connected to VSSA, its cleanliness is directly related to the noise level detected by the receiving circuitry (i.e. to the actual sensitivity level) and to the PLL behavior.

It is very important to filter each supply to its respective ground: VCC to VSS, VCCA and VDD_PLL to VSSA, VDDIO and VDD to GND.

7.3.3 Oscillator

It is very important to keep the crystal oscillator and the load capacitors as close as possible to the device.

The resonant circuit must be far away from noise sources such as:

- Power supply circuitry
- Burst and surge protections
- Mains coupling circuits
- Any PCB track or via carrying an RF switching signal.

To properly shield and separate the oscillator section from the rest of the board, it is recommended to use a ground plane, on both sides of the PCB, filling all the area below the crystal oscillator. No tracks or vias, except for the crystal connections, should cross the ground plane.

Connecting the case to ground could be a good practice to reduce the effect of radiated signals on the oscillator.

7.4 Thermal impedance and power dissipation calculation

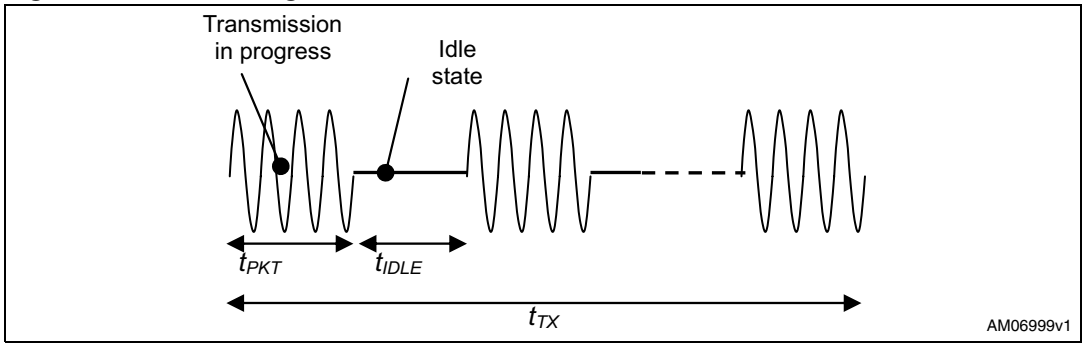
The relationship between junction temperature (T_J) and power dissipation during transmission (P_D) is described in the following formula:

Equation 12

$$T_J(t_{TX},d) = T_A + P_D \cdot Zth_{JA}(t_{TX},d)$$

where T_A is the ambient temperature (from -40 to +85 °C) and Zth_{JA} is the junction to ambient thermal impedance of the ST7570 IC, which is related to the length of the transmission (t_{TX}) and to the duty cycle $d = t_{PKT} / (t_{PKT} + t_{IDLE})$, assuming a packet-fragmented transmission as illustrated by *Figure 38*.

Figure 38. Packet-fragmented transmission

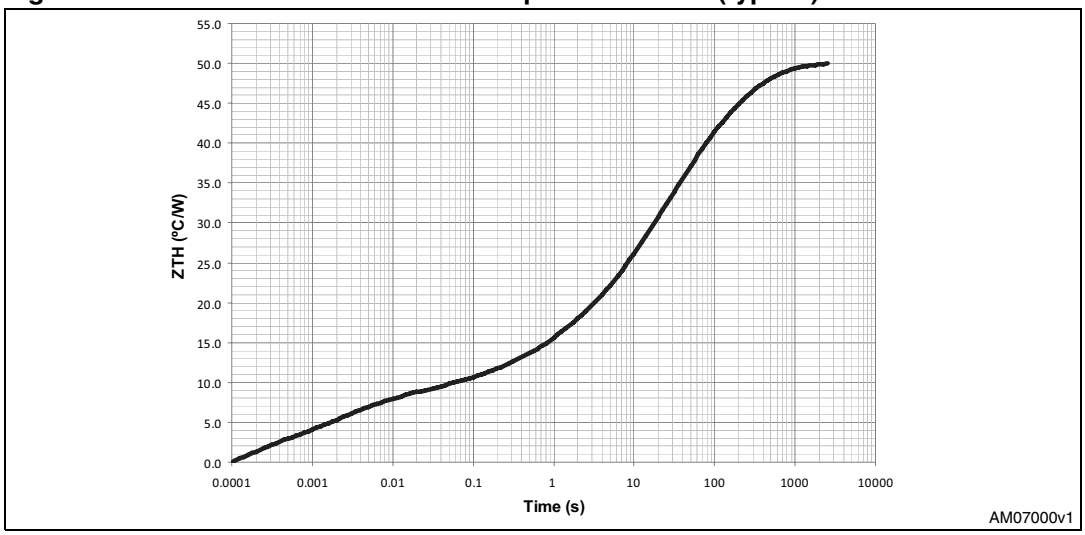


When soldered to a proper dissipating area on the PCB, as explained above, the ST7570 IC is characterized by a steady-state thermal resistance Rth_{JA} of about 50 °C/W. The thermal impedance curve obtained as the power dissipation step response is given in *Figure 39*.

It can be seen that the transient of Zth_{JA} takes some thousands of seconds, after which the static value of 50 °C/W is reached. This means that during the transient phase (i.e. if the transmission time t_{TX} is some seconds or even less) the IC is able to dissipate a power that is far higher than the one sustainable at steady-state.

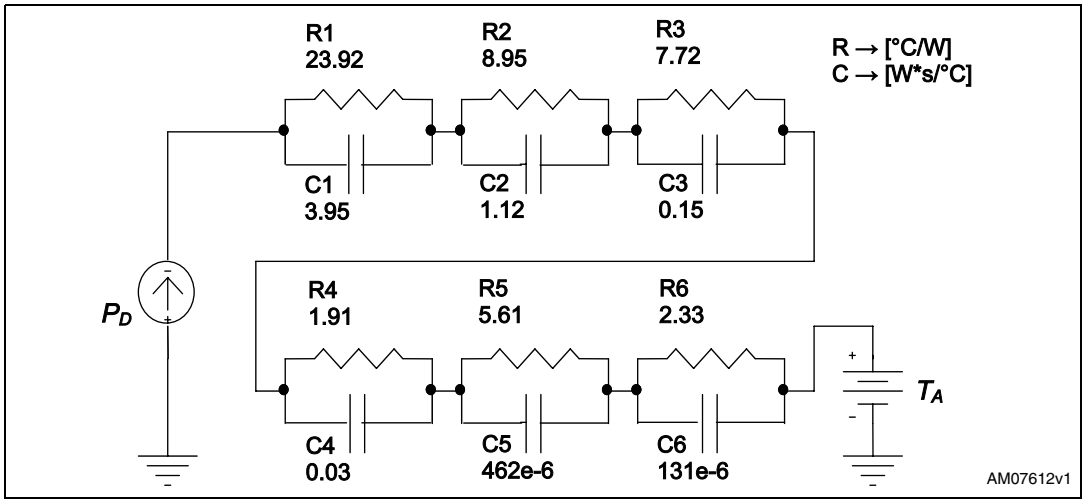
For this reason, a complete thermal analysis requires that the characteristics of the transmission are taken into account, i.e. duty cycle and duration, determining the value reached by the thermal impedance and then the allowed power dissipation.

Figure 39. Measured ST7570 thermal impedance curve (typical)



The thermal impedance, as a response to dissipation at different duty cycle and duration values, can be estimated by simulating a 6-cell equivalent model obtained by the curve fitting from *Figure 39*, as shown in *Figure 40*.

Figure 40. Simulation model of the thermal impedance Zth_{JA} of the ST7570 mounted on the demonstration board



The actual dissipated power PD can be calculated as:

Equation 13

$$P_D = P_{IN} - P_{OUT}$$

where $P_{IN} = V_{CC} \cdot I_{CC}$ and $P_{OUT} = V_{OUT\ rms} \cdot I_{OUT\ rms}$. Note that power consumption by receiving circuitry and linear regulators is considered negligible for thermal analysis purposes. The relationship between current absorption from the power supply (I_{CC}) and PA output current to the load (I_{OUT}) is shown in *Figure 2*.

The transmission output level $V_{OUT\ rms}$ of 2.5 V and the current limit $I_{OUT\ rms(LIMIT)}$ of 1 A, fixed for the ST7570 demonstration board, correspond to a maximum output power P_{OUT} of 2.5 W over a 2.5 Ω load. In these conditions, the required dissipation results as follows:

Equation 14

$$P_{D(LIMIT)} = P_{IN(LIMIT)} - P_{OUT(LIMIT)} \cong (13V \cdot 0.48A) - (2.5V \cdot 1A) = 3.7\ W$$

Referring to the relationship between dissipated power and temperature, it can be proved that in a continuous transmission, i.e. with Zth_{JA} at its steady-state value of 50 °C/W, with an ambient temperature of 25 °C, the maximum dissipation can be 2 W. However, controlling the transmission duty cycle and total duration it becomes possible to get higher dissipation.

A real IEC61334-5-1 standard protocol condition can be used as an example (*References 5*):

- Maximum length MAC frame with alarms: at 2400 bps and 50 Hz mains frequency, the packet time t_{PKT} is 150 ms, the duty cycle d is 100 % and the transmission duration t_{TX} is 1 second, corresponding to seven MAC sub-frames. According to *Figure 39*, in these conditions, Zth_{JA} would reach a maximum value of 16 °C/W only. This allows the power dissipation PD to reach 2.5 W over all the ambient temperature range of the ST7570, while $P_{D(LIMIT)}$ may be reached with an ambient temperature up to 66 °C.

7.5 Oscillator section

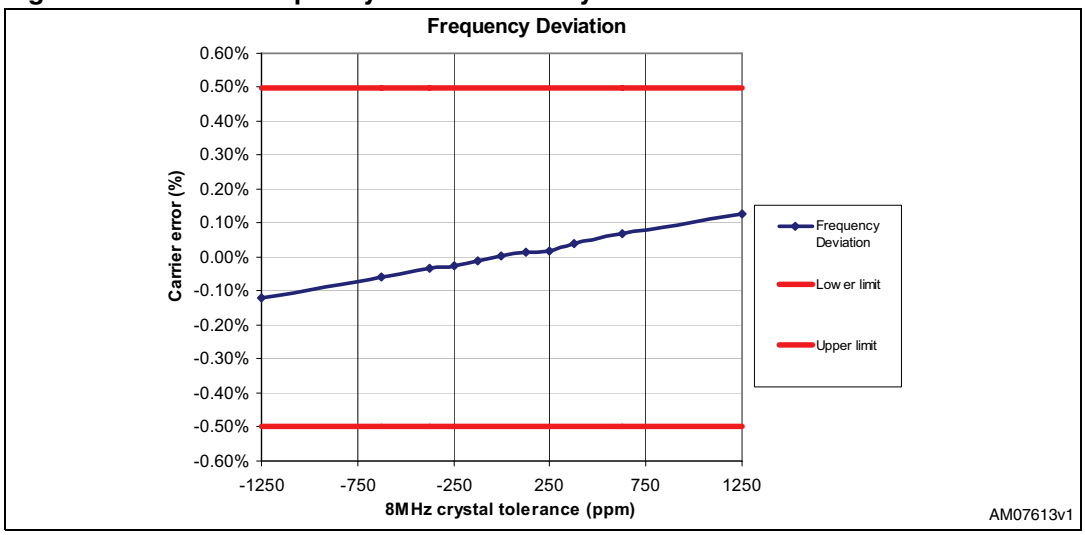
The ST7570 crystal oscillator circuitry requires a crystal having a maximum load capacitance of 20 pF and a maximum ESR of 100 Ω.

Moreover, the following requirements impacting on the quartz crystal choice are typically set by ST7570 metering applications:

- Communication frequencies: f_0 = 74 kHz, f_1 = 63.3 kHz with ±0.5 % tolerance
- Delay between mains zero-crossing and the beginning of the communication window: 120 µs, with tolerance equal to ± 20 µs.

Figure 41 shows the carrier frequency deviation vs. the quartz crystal tolerance, simulated through a waveform generator applying a square wave with frequency values around 8 MHz:

Figure 41. Carrier frequency deviation vs. crystal tolerance

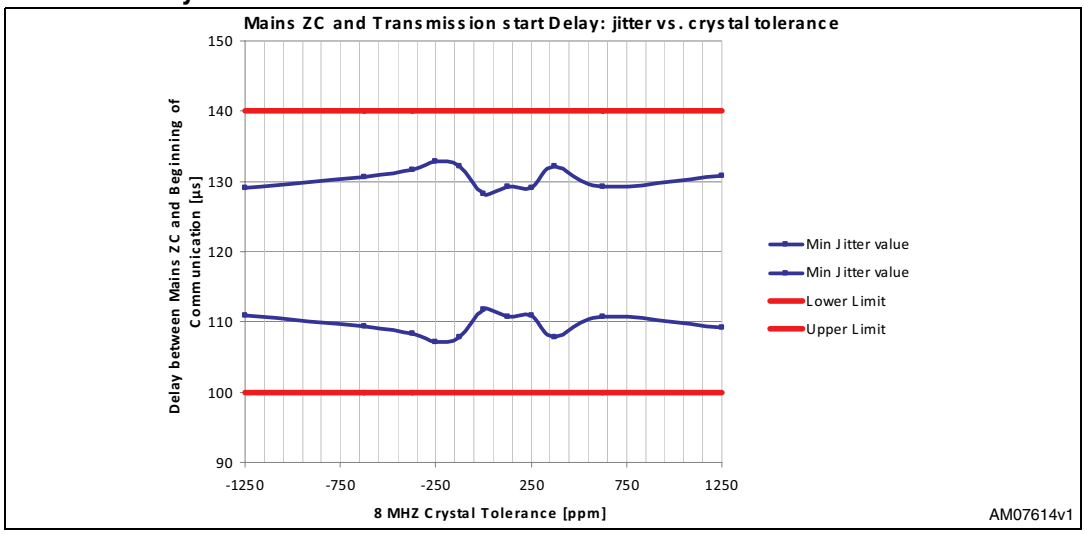


In order to evaluate the compliance, with the requirement of the delay between mains zero crossing and the beginning of the communication window, the zero crossing coupling circuit response needs to be considered, introducing a delay of 30 µs (typical) between mains zero crossing and ZC_IN_A signal (see *Section 7.1.4*).

The target delay equal to 120 µs can be achieved by adding an integer number of 13 µs steps to the circuit delay (*References 2*). In particular, with 7 steps the total delay is 7×13 µs + 30 µs ≈ 120 µs.

The jitter around the expected value changes in accordance with the crystal tolerance, as shown in *Figure 42*.

Figure 42. Delay between mains zero crossing and transmission start: jitter vs. crystal tolerance



The maximum tolerance for the HC49U crystal adopted for the ST7570 demonstration board, that is 150 ppm, allows the above requirements to be met.

7.6 Surge and burst protection

The specific structure of the coupling interface circuit of the application is a weak point against high voltage disturbances which may come from the external environment. In fact, an efficient coupling circuit with low insertion losses realizes, consequently, a low impedance path from the mains to the power line interface of the device.

For this reason it is recommended to add some specific protections on the mains coupling path, to prevent high energy disturbances coming from the mains from damaging the internal power circuitry of the ST7570.

The possible environments for this kind of application can be both indoor and outdoor; residential, commercial and light-industrial locations. To verify the immunity of the system to environmental electrical phenomena, a series of immunity specification standards and tests must be applied to the power line application.

The immunity requirements for any PLC metering application, communicating in the European A band (9-95 kHz), are listed in the EN50065-2-3 document, which refers to EN61000 and ENV50204 for tests to be applied (*References 3*).

These standards include surge tests, both common mode and differential mode (+/- 4 kV peak, t_R = 1.2 µs, t_N = 50 µs) and fast transient (burst) tests (+/- 2 kV peak, t_R = 5 ns, t_H = 50 ns, repetition frequency 5 kHz).

For the application to be able to withstand such a severe electrical overstress, the coupling capacitor C4 must be a Y2 type part, rated for 5 kV pulses.

In the case of non-metering applications, communicating outside the A band, the requirements are listed in the EN50065-2-1 document, which set lower pulse levels. In such a case, an X1 capacitor (e.g. Epcos B32912A3224K) can be used instead of a Y2 part.

Protection devices must also be included in the board design, as described below. *Figure 43* and *44* show the protection against common mode disturbances. D4 and D2 low-drop Schottky diodes are able to quickly absorb fast transient disturbances exceeding the supply rails. *Figure 45* describes the protection intervention in case of differential mode disturbances. A differential voltage higher than 15 V p-p is clamped by the D1 bi-directional Transil diode. D1 is the most robust protection and also the one which is able to absorb most of the energy of any incoming disturbance.

Figure 43. Common mode disturbance protection - positive disturbance

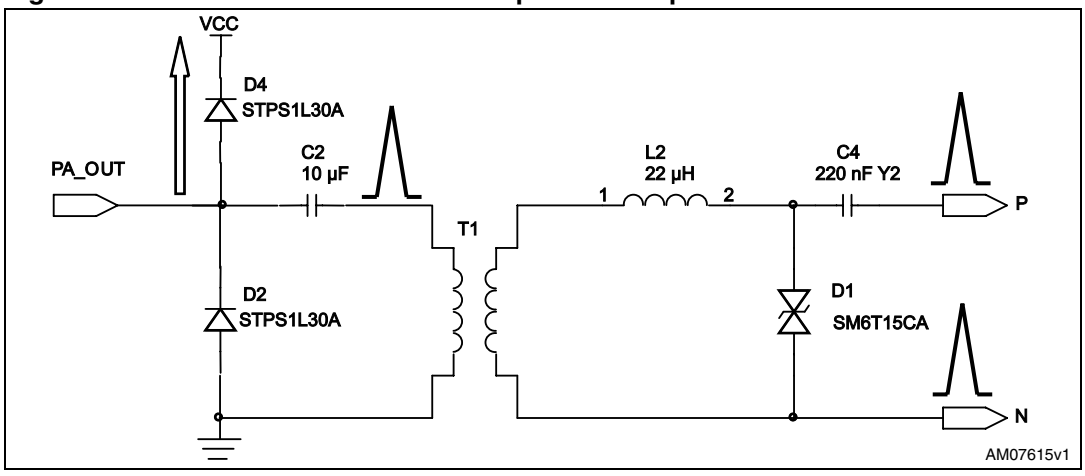


Figure 44. Common mode disturbance protection - negative disturbance

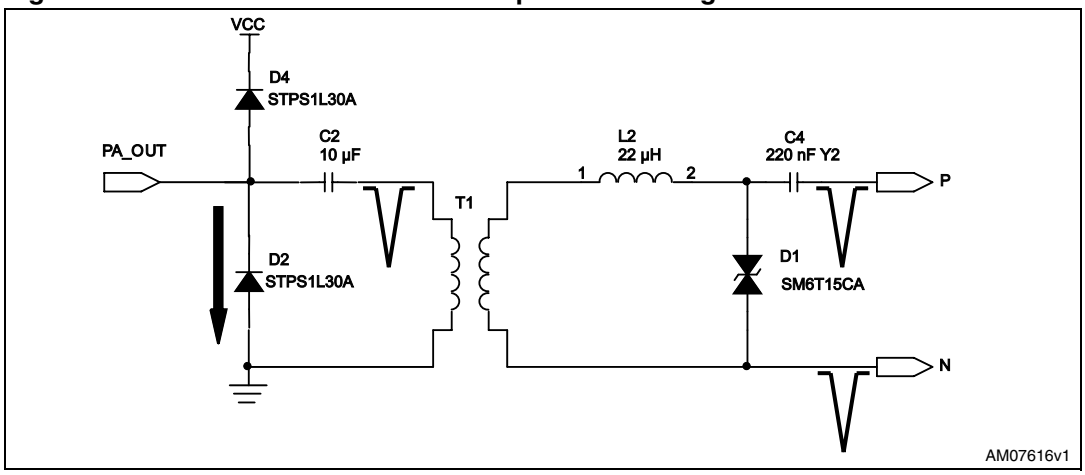
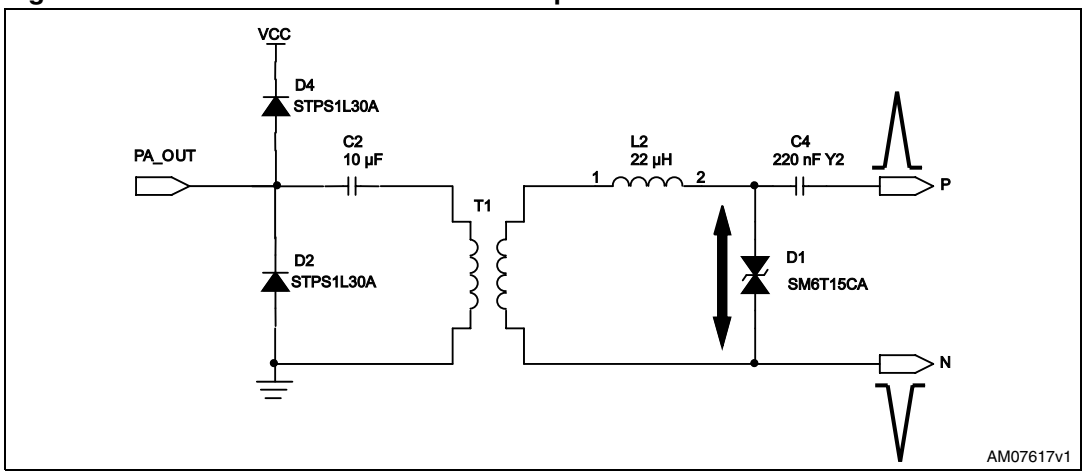


Figure 45. Differential mode disturbances protection



7.7 Power supply

The power supply requirements for the ST7570 demonstration board are listed in *Table 1*.

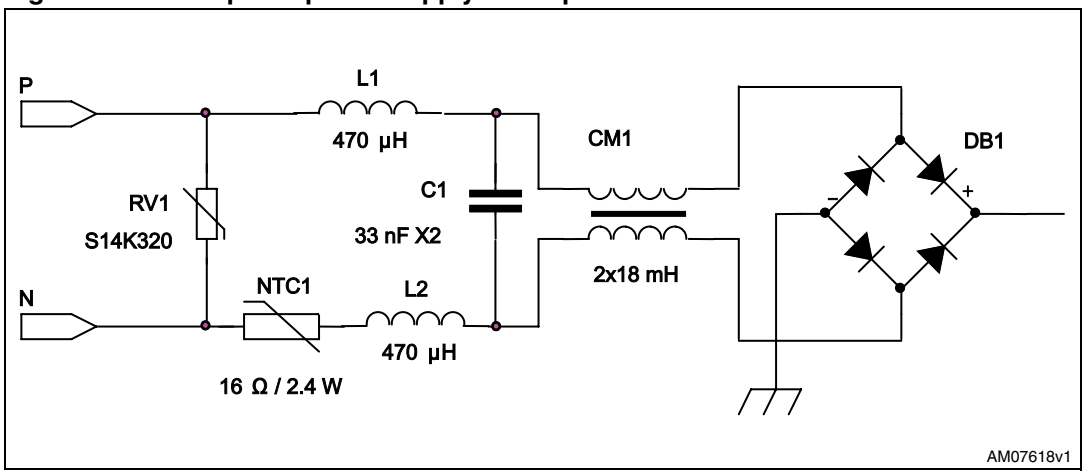
However, the power supply circuit design is not only relevant in terms of available power. Two points are particularly sensitive for a power line communication application:

- The noise injected on the line
- The input impedance of the power supply unit

For the first point, a quasi-resonant switching mode power supply based on the ALTAIR04-900 device has been chosen. This kind of switching controller spreads the switching disturbances over a wide frequency range, therefore minimizing the overall disturbance amplitude.

The second point involves the EMI input filter design. The suggested circuit in *Figure 46* has been designed to have minimum influence on the ST7570 line coupling circuit, in terms of load impedance and linearity. It is required to have a symmetrical circuit with two series inductors to minimize differential noise and avoid capacitive load from the X2 capacitor.

Figure 46. Example of power supply EMI input filter



8 Application ideas

8.1 Three-phase architecture

The ST7570 modem can be used to communicate on a three-phase network. This is especially required for low-voltage substation nodes (concentrators), collecting data from several energy meters all along the three phases of the distribution network.

In the example scheme of *Figure 47*, the line coupling circuit allows the signal to divide into the three phases via capacitive coupling. This structure has been designed to keep a similar impedance on each phase, therefore optimizing the signal distribution between the phases.

A critical point regarding this solution may be the total impedance the ST7570 power amplifier is required to drive, which is the result of the three phases in parallel. For concentrator nodes, however, the impedance per phase is likely to be considerably above the driving limit of the power amplifier, as all the electrical devices supplied by the power line are placed at a certain distance from the substation.

In the switched coupling scheme of *Figure 48*, a more complex circuit is shown, being the coupling to each phase selectable via opto-switches.

Only one phase at a time can be used to transmit. An incoming signal, however, can be received either from one phase at a time (J1 closed, J2 open) or from any phase at the same time (J1 open, J2 closed). Both solutions can work well: the first solution has the advantage of reducing crosstalk between the three phases, while the second allows listening to the whole network at the same time. The choice depends on electrical and performance tests as well as on specific protocol requirements.

For the zero crossing coupling, only one phase shall be used as reference, therefore keeping the same coupling circuit as in the ST7570 single-phase demonstration board.

Figure 47. Scheme of principle for non-switched three-phase architecture

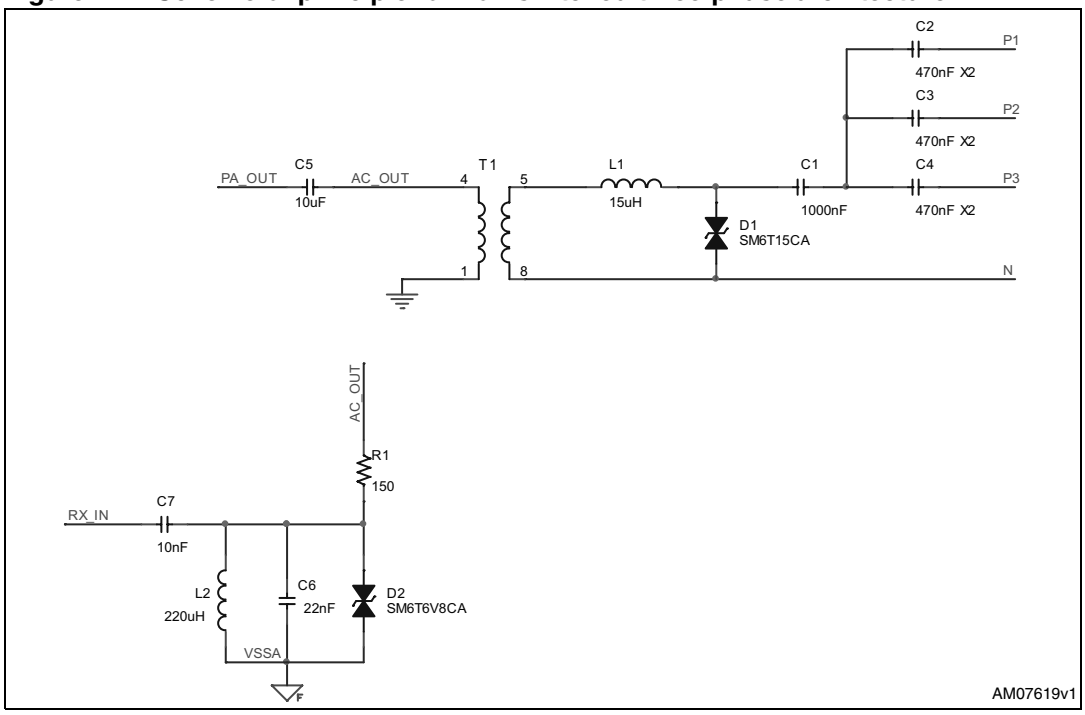
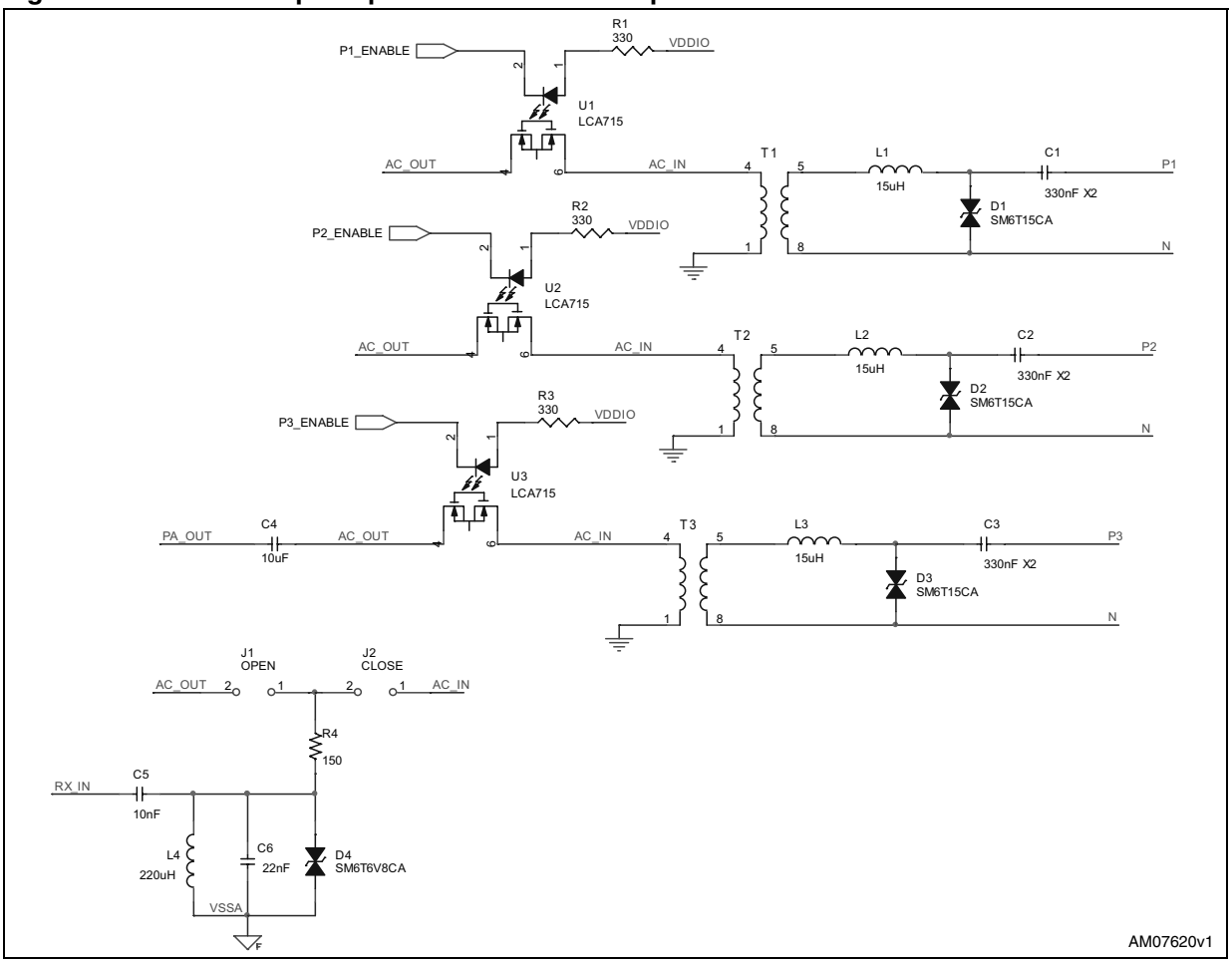


Figure 48. Scheme of principle for switched three-phase architecture



8.2 Received signal strength indication (RSSI)

In many application fields, measuring the strength of the incoming signal is useful to:

- Evaluate the SNR (signal-to-noise ratio) at the node
- Choose the best routing through the network (if repeaters are allowed).

As explained in *References 1* and *2*, the ST7570 embeds estimators for signal-to-noise ratio (SNR_0, SNR_1) values. These estimators are calculated during valid packet reception on each S-FSK spectrum frequency f_0 and f_1. The values are notified to the external host during each data indication message (*References 2*). In order to evaluate the robustness of ST7570 embedded estimators, the setup represented in *Figure 33* has been adopted and all the estimator values extracted from received packets have been compared to the values measured by the spectrum analyzer.

Figure 49, *50*, *51* and *52* show the error bars with standard deviation for SNR_0 and SNR_1 values, compared to the measured values for 1200 and 2400 baud.

Figure 49. SNR_0 estimator at 1200 bps

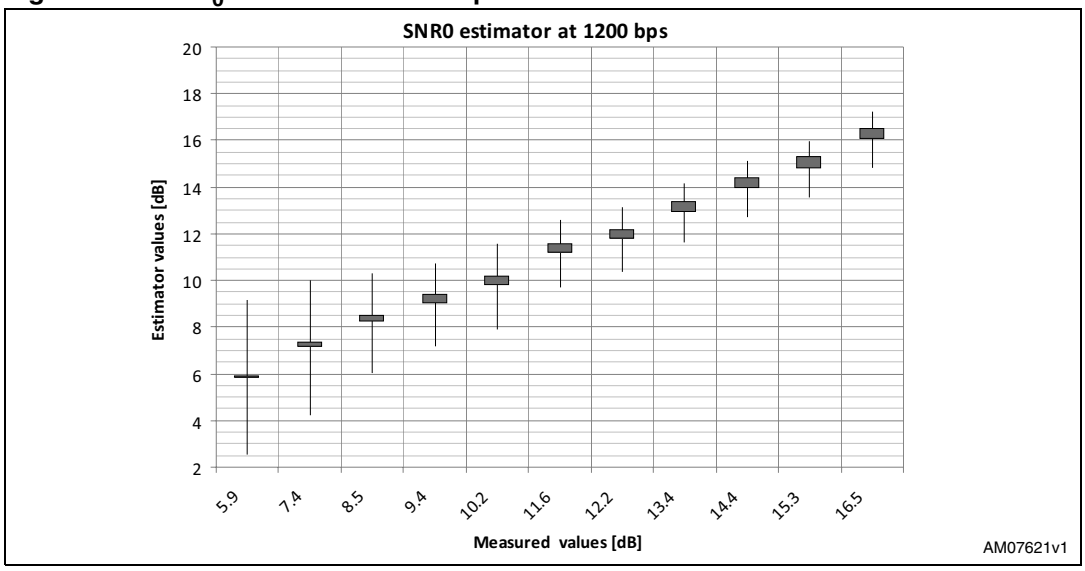


Figure 50. SNR_1 estimator at 1200 bps

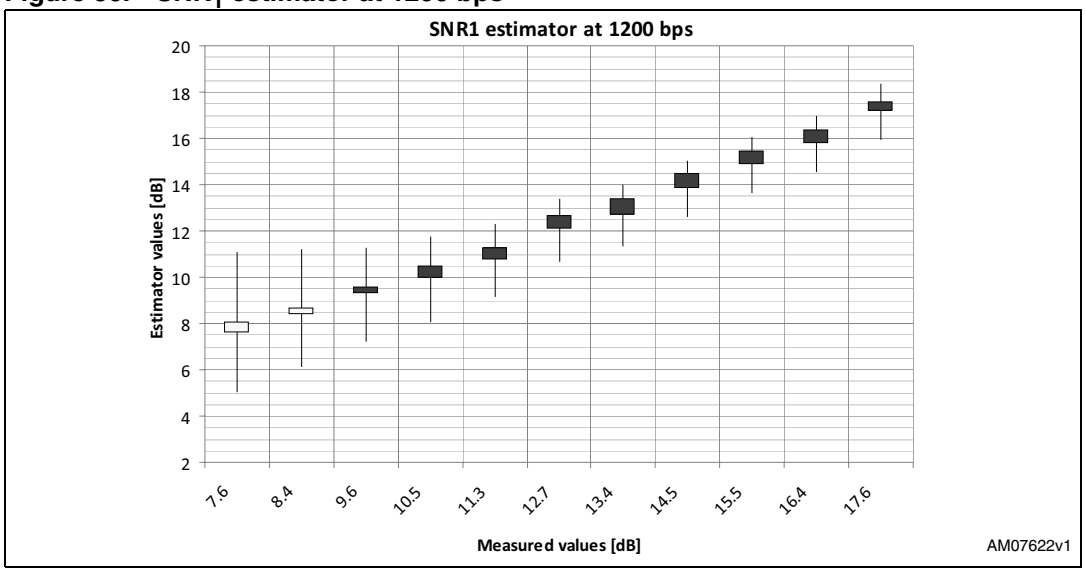


Figure 51. SNR_0 estimator at 2400 bps

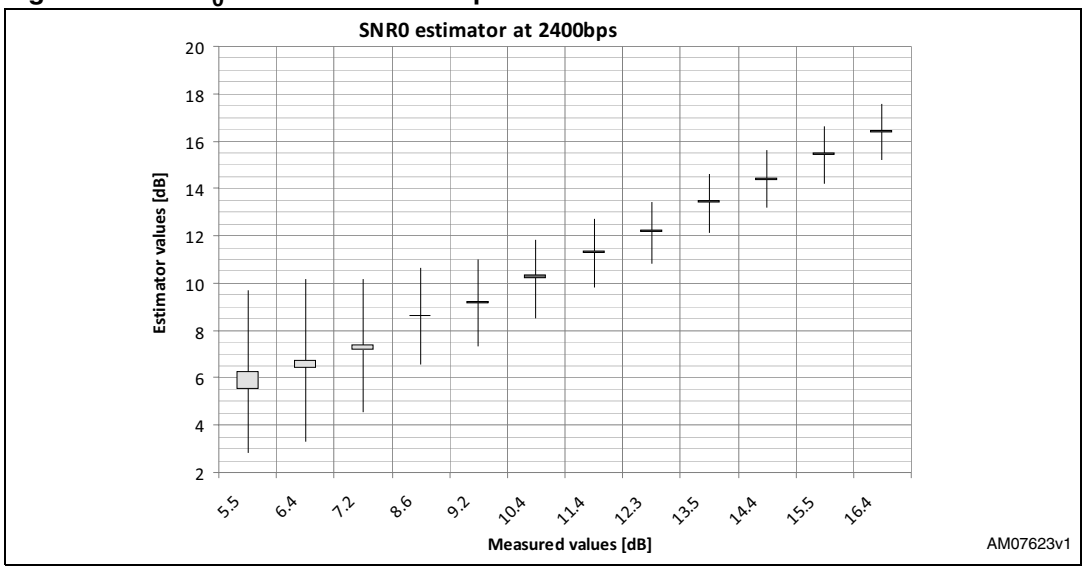
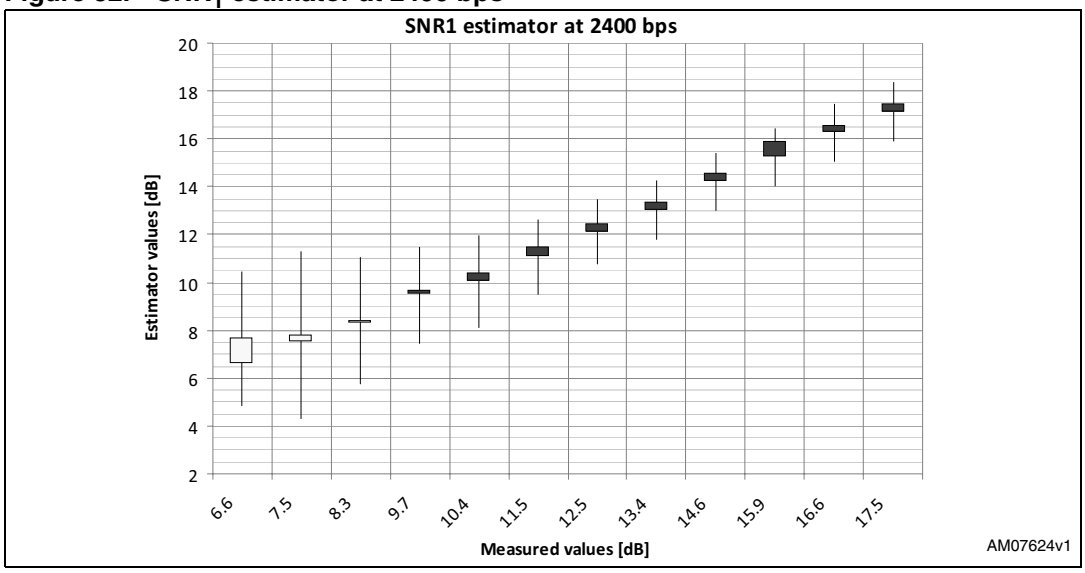


Figure 52. SNR_1 estimator at 2400 bps



9 FAQs and troubleshooting

In this section the most frequently asked questions and the solution to common ST7570 demonstration board usage problems are described.

9.1 FAQs

- Q: Is it possible to use ST power line transceivers on a medium or high voltage AC line?
  - A: Yes. The same circuit solution as for a low voltage AC line can be used, provided that coupling interface (and particularly line transformer, power inductor and Y2 capacitor) guarantees an adequate and safe isolation from the AC line.
- Q: Is it possible to use the ST7570 on a DC or de-energized line?
  - A: No, the ST7570 device requires the 50-60 Hz zero crossing detection to work.
- Q: Which kind of protocols can be used with the ST7570?
  - A: The embedded PHY and MAC protocol layers are mainly designed, but not limited, to interface with a IEC61334-4-32 compliant Logic Link Control (LLC) layer in applications targeting DLMS/COSEM, a widely-used European standard for the application layer of meters.
- Q: Does the ST7570 demonstration board meet FCC part 15 specs?
  - A: Yes. In fact, the EN50065 normative compliance intrinsically guarantees the compliance with FCC part 15 regulations as well.
- Q: What distance can a PLC signal cover?
  - A: Given a transmitted signal level of 2.5 V rms, at 1200 baud the ST7570 device is able to transmit through a channel attenuating up to 84 dB. This means that in a point-to-point link a distance of several km can be covered, according to the characteristics of the line. Nevertheless, the allowable distance can be reduced because of noisy devices and low-impedance loads connected on the power line; such elements impact on the actual SNR seen by the receiver.
- Q: Why with power line communication can I not get 100 % reachability even though the range is a few meters?
  - A: A probability lower than 100 % to reach a PLC node within such a small distance can depend on two main factors:

  a) attenuation or losses on the power line (for example because of some heavy capacitive load connected close to the transmitter)

  b) noise coming from electric or electronic equipment connected on the power line (for example SMPS, ballasts, or motors).

  It can be useful to measure the signal level at transmitter and receiver to understand if there are undesired losses. It is also important to measure the noise level and spectral distribution to see whether the PLC channel is somehow “jammed” by noise.
- Q: Does the power line communication work if a power distribution transformer is present between two nodes?
  - A: The communication could work, but the transformer impedance at the signal frequency must be taken into account, as it could introduce strong attenuation in

the signal level. A signal coupler (for example, a capacitive coupling) between the two sides of the distribution transformers may be required.

- Q: What method of coupling is preferred for medium voltage and low voltage mains line: capacitive or inductive?
  - A: For MV line, capacitive coupling is preferable for narrow-band PLC. In the case of an LV line, being the actual line impedance unpredictable because of the number of electrical devices connected on it, the solution should be an L-C series resonant circuit tuned at channel frequency, designed to have low Q even with very low line impedance (below 5 Ω).
- Q: Is it possible to detect the channel quality through the ST7570 device?
  - A: Yes. Using the ST7570 estimators for SNR_0 and SNR_1, always available for the external host, it is possible to evaluate the channel quality over the physical link between transmitter and receiver.
- Q: Why use zero crossing synchronization?
  - A: As defined in the IEC61334-5-1 document, the mains zero crossing information is used to define the bit and frame timing and ensure proper time slot management.
- Q: What is the minimum signal-to-noise ratio that the ST7570 can manage?
  - A: A bit error rate (BER) of 10^{-3} is used as reference. In this condition, the ST7570 shows good receiving performance with a signal-to-noise ratio down to 13 dB at 1200 baud, 50 Hz.
- Q: When data is being transmitted by the ST7570, is it encoded in some way?
  - A: No. The ST7570 has been developed according to the IEC61334-5-1 standard, which neither requires nor allows coding for PHY and MAC levels.
- Q: What could be the main sources of harmonic distortion in the ST7570 transmitted signal?
  - A: Generally, harmonics can rise up because of: high output current, due to low line impedance; saturation of magnetic components in the line coupling circuit, due to either poor dimensioning of the saturation current or to 50 Hz residual current; capacitive load applied to the power amplifier output; insufficient margin to the supply rails (low VCC or high output voltage).

9.2 Troubleshooting

1. Problem: the ST7570 demonstration board doesn't work at all.

- What to check:
  a) Check that the AC mains supply cable is well connected
  b) Check if the DL1 (VCC) and DL2 (VDDIO) are on
  c) Check the voltage on VCC, VDDIO, VCCA, VDD, and VDD_PLL lines. All these voltages must be present in order to turn on the ST7570.

2. Problem: the ST7570 demonstration board is not responding.

- What to check:
  a) Check if some activity on DL3 and DL4 is present when trying to communicate via USB with the board
  b) Try disconnecting and reconnecting the USB cable; sometimes the USB driver fails during COM port opening
  c) Verify if an 8 MHz clock is present on the XOUT pin (13) of the ST7570 device.

3. Problem: the ST7570 demonstration board does not transmit.

- What to check:
  a) Check the bias voltage on the PA_OUT test point (TP1) with the oscilloscope probe referred to VSS power ground. A DC voltage of VCC/2 must be measured during RX state
  b) Set the ST7570 in continuous transmission by setting TEST0 (higher frequency tone), TEST1 (lower frequency tone) or TEST2 (alternating tones) modes via the ST7570 GUI. A sinusoidal carrier should be detected by the oscilloscope probe,

with an amplitude equal to the TX_OUT programmed level multiplied by the PA gain (nearly 4.5). In this case, there is no problem regarding the AFE and PA

c) Check the ZC_IN_A (or ZC_IN_D, if it has been selected): a signal synchronous to the mains voltage must be present for the ST7570 to be able to transmit in operating mode

d) Verify, via the ST7570 GUI, if the node is synchronized.

4. Problem: the ST7570 demonstration board transmits only for a short while.

- What to check:

a) Verify the internal temperature of the ST7570, available inside the management information base (MIB), and accessible via the ST7570 GUI

b) Check if there is short-circuit (i.e. capacitive) impedance on the mains at the carrier frequency. It may lead to device overheating and PA thermal shutdown.

5. Problem: the ST7570 demonstration board does not receive.

- What to check:

a) Check if the transmitted signal reaches the ST7570 device by measuring the RX_IN line voltage (TP5) with the oscilloscope probe referred to VSSA signal ground

b) Check that the GUI is setting the transmitter and the receiver to use the same tone frequencies

c) Check the ZC_IN_A (or ZC_IN_D, if it has been selected): a signal synchronous to the mains voltage must be present for the ST7570 to be able to receive in operating mode

6. Problem: During a communication test, the ST750 GUI shows a high bit error rate (BER).

Note: (This point refers to a half-duplex communication involving two ST7570 demonstration boards communicating with each other).

- What to check:

a) Check that both demonstration boards have the same ST7570 GUI settings

b) Verify the SNR of the communication. If the signal is too low or the noise is too high with respect to each other, the communication performance is poor. Try to:

1. Check the S and N estimation of the receiving ST7570 device
2. Measure the signal level S and the noise level N on the RX_IN line (TP5) of the receiving board.

10 References

1. ST7570; *S-FSK power line networking system-on-chip*, datasheet
2. UM0934; *ST7570 S-FSK power line networking System-on-Chip*, user manual
3. “Spread Frequency Shift Keying”, IEEE transactions on communications, vol. 42, no. 2/3/4, February/March/April 1994

11 Normative references

4. EN50065: Signaling on low voltage electrical installations in the frequency range 3 kHz to 148.5 kHz
   - Part 1: General requirements, frequency bands, and electromagnetic disturbances
   - Part 2-3: Immunity requirements
   - Part 4-2: Low voltage decoupling filters - Safety requirements
   - Part 7: Equipment impedance
5. IEC61334: Distribution automation using distribution line carrier systems
   - Part 5-1: Lower layer profiles - the spread frequency shift keying (S-FSK) profile

Appendix A Board layout

Figure 53. PCB layout - component placing

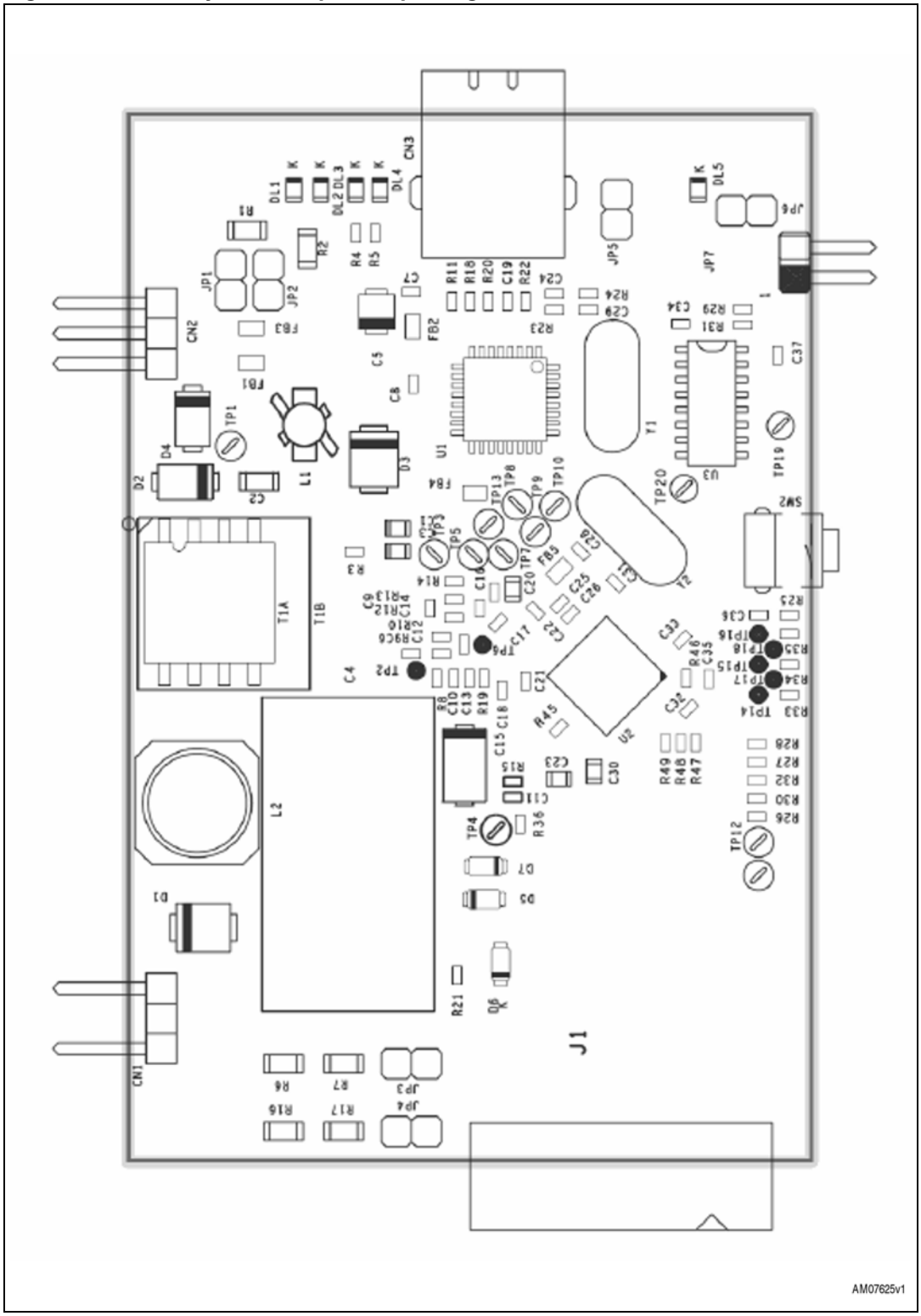


Figure 54. PCB layout - top view

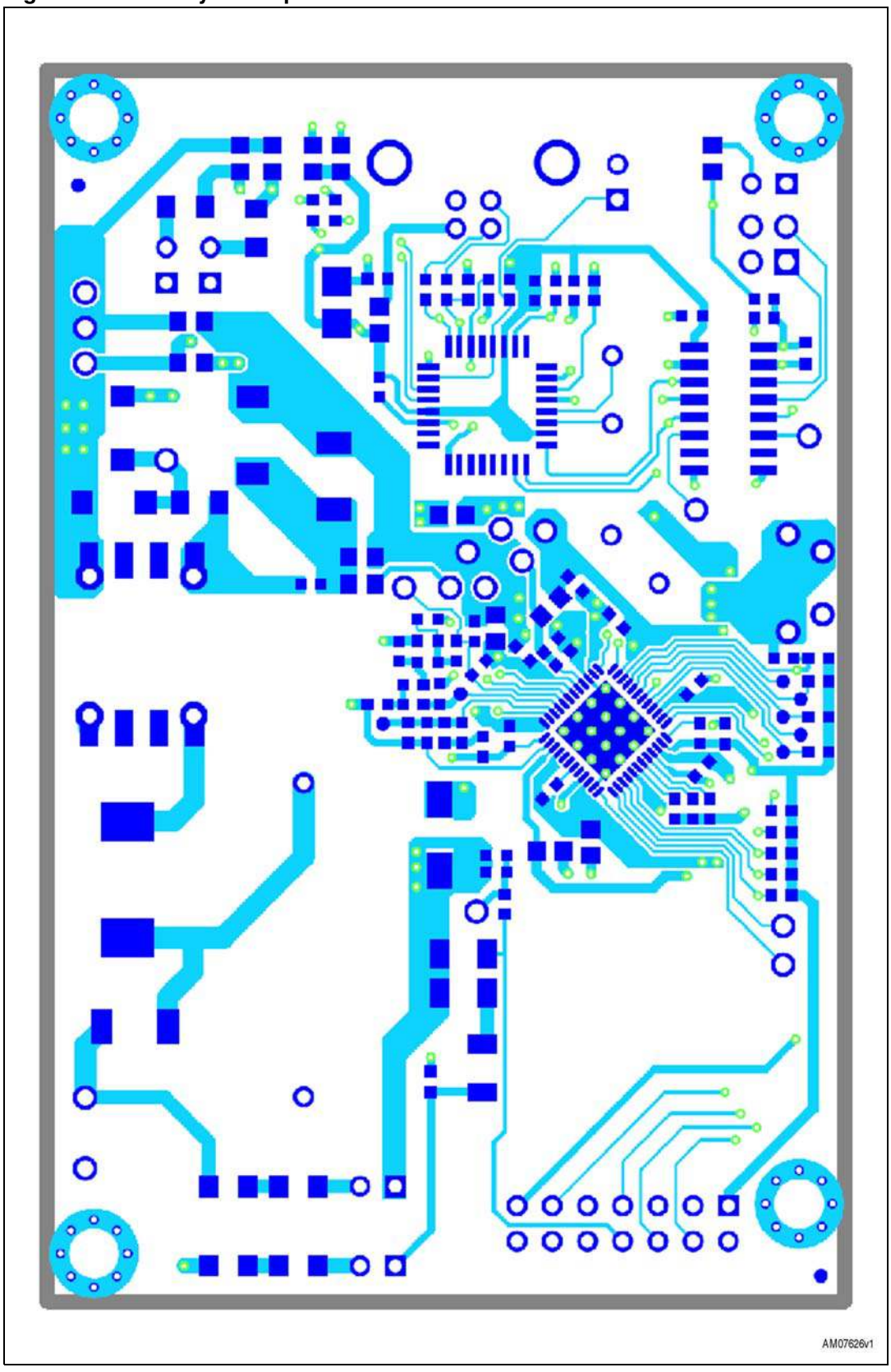
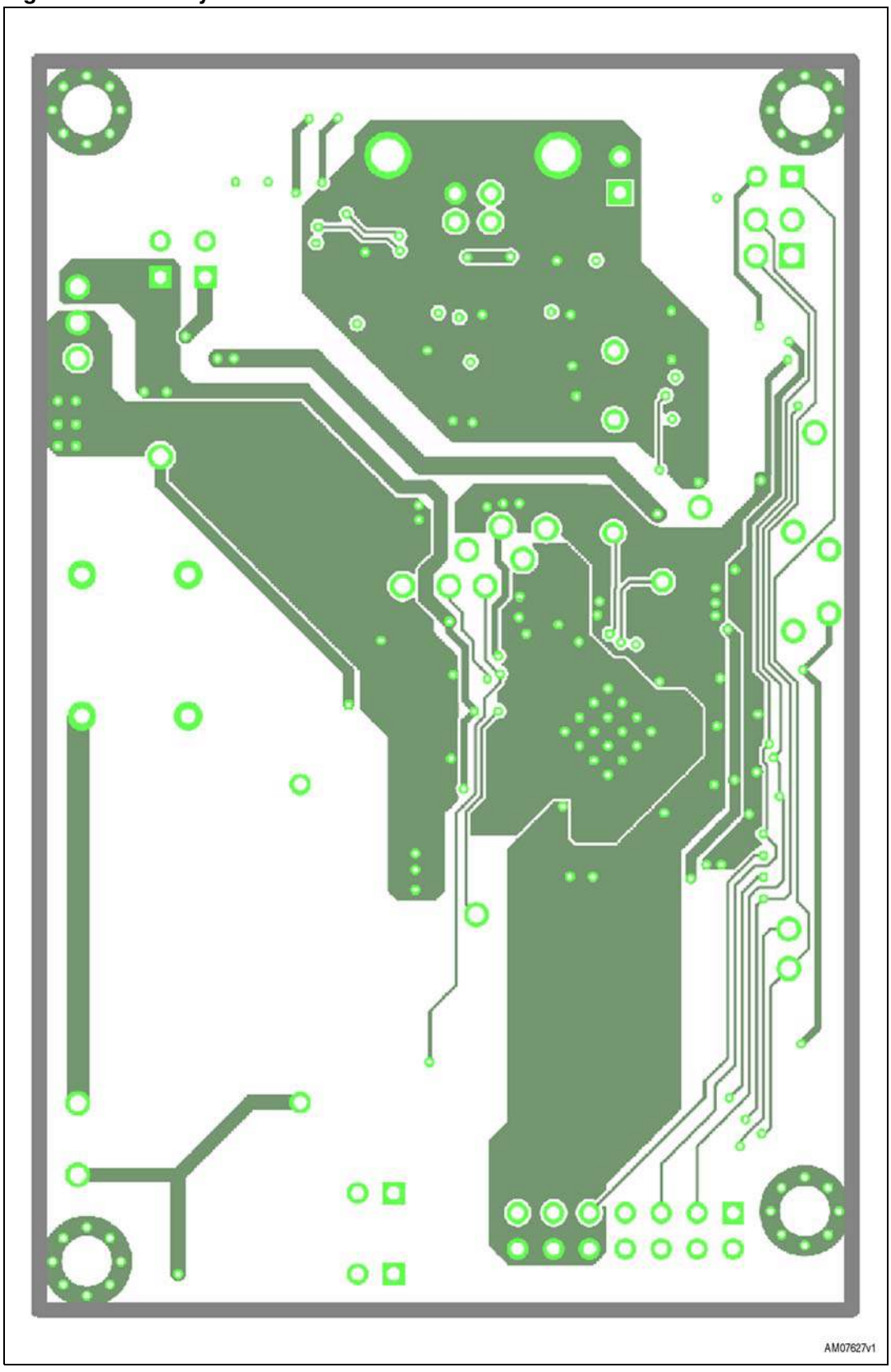


Figure 55. PCB layout - bottom view



Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Oct-2010	1	Initial release.