Freescale Semiconductor
Technical Data

Document Number: MW5IC970NBR1
Rev. 1, 5/2006

RF LDMOS Wideband 2-Stage Power Amplifiers

MW5IC970NBR1

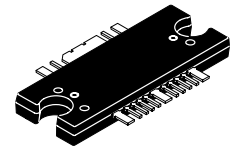
**800-900 MHz, 70 W, 28 V
RF LDMOS WIDEBAND
2-STAGE POWER AMPLIFIERS**

Designed for broadband commercial and industrial applications with frequencies from 132 MHz to 960 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 28 volt base station equipment. The device has a 2-stage design with off-chip matching for the input, interstage and output networks to cover the desired frequency band.

- Typical Performance: 800 MHz, 28 Volts, I_{DQ1} = 80 mA, I_{DQ2} = 650 mA, P_{out} = 70 Watts PEP
  Power Gain — 30 dB
  Drain Efficiency — 48%
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 850 MHz, 70 Watts CW Output Power

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



**CASE 1329-09
TO-272 WB-16
PLASTIC**

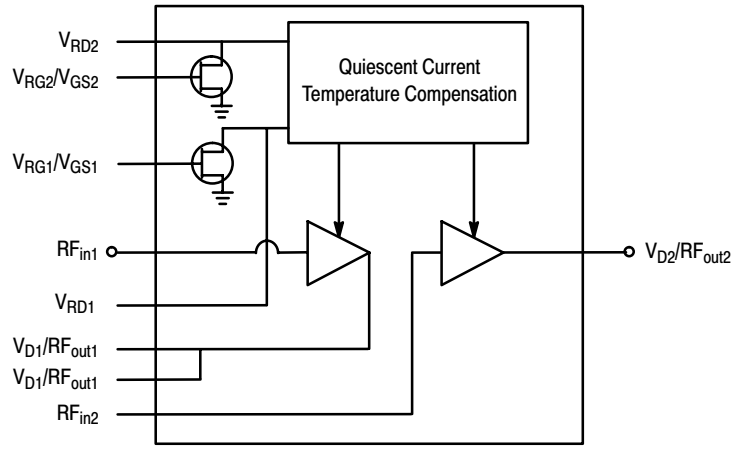
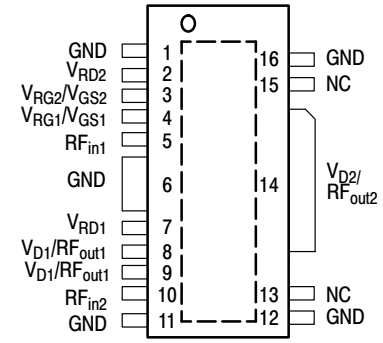


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside flag is source terminal for transistors.

Figure 2. Pin Connections

1. Refer to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +200	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic		Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
Final Application (P_{out} = 70 W CW)	Stage 1, 28 Vdc, I_{DQ} = 80 mA		5.2	
	Stage 2, 28 Vdc, I_{DQ} = 650 mA		0.8	
EDGE Application (P_{out} = 35 W CW)	Stage 1, 28 Vdc, I_{DQ} = 80 mA		5.3	
	Stage 2, 28 Vdc, I_{DQ} = 650 mA		0.8	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

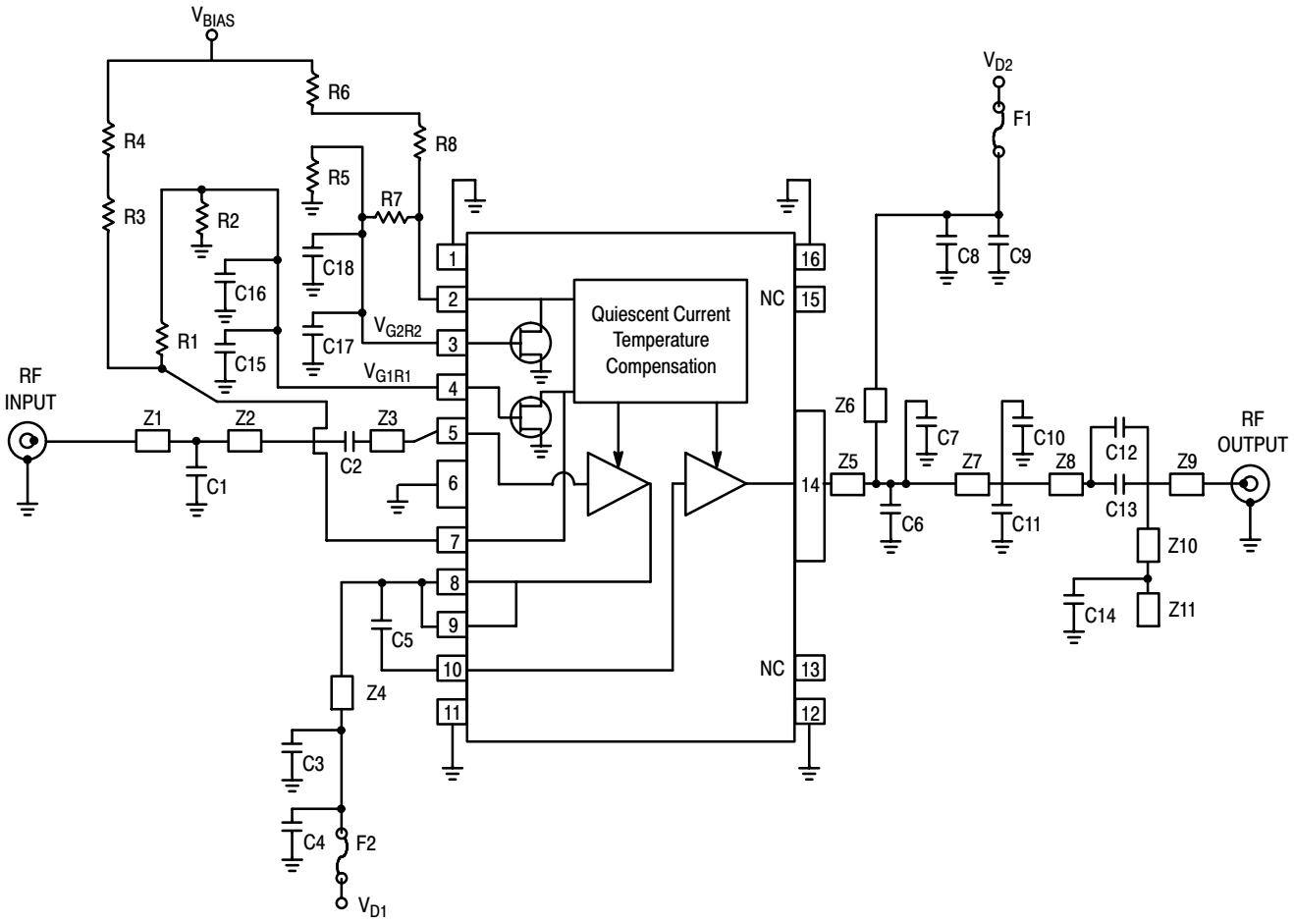
Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28.5 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 650 mA, P_{out} = 70 W PEP, f1 = 870.0 MHz, f2 = 870.1 MHz					
Power Gain	G_{ps}	26.5	30	34.5	dB
Drain Efficiency	η_D	40	48	—	%
Input Return Loss	IRL	—	-12	-10	dB
Intermodulation Distortion	IMD	—	-33	-28	dBc
Typical 800/900 MHz Performances (In Freescale 800/900 MHz Reference Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 650 mA, 740-870 MHz, 870-960 MHz					
Gain Flatness in 30 MHz Bandwidth @ P_{out} = 70 W CW	G_F	—	2	—	dB
Gain Flatness in 30 MHz Instantaneous Bandwidth @ P_{out} = 70 W CW	G_F	—	0.2	—	dB
Delay @ P_{out} = 70 W CW Including Output Matching	Delay	—	4.5	—	ns
Part-to-Part Phase Variation @ P_{out} = 70 W CW	$\Delta\Phi$	—	±15	—	°

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)



Z1	0.485″ x 0.066″ Microstrip	Z7	0.040″ x 0.233″ Microstrip
Z2	0.270″ x 0.040″ Microstrip	Z8	0.450″ x 0.120″ Microstrip
Z3	0.068″ x 0.020″ Microstrip	Z9	0.100″ x 0.066″ Microstrip
Z4	0.950″ x 0.040″ Microstrip	Z10	1.000″ x 0.040″ Microstrip
Z5	0.131″ x 0.233″ Microstrip	Z11	0.148″ x 0.040″ Microstrip
Z6	0.797″ x 0.050″ Microstrip	PCB	Rogers 4350B, 0.030″, ε_r = 3.5

Figure 3. MW5IC970NBR1 Test Circuit Schematic

Table 6. MW5IC970NBR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C10, C11	3.9 pF Chip Capacitor	600S3R9BT	ATC
C2	56 pF Chip Capacitor	600S560JW	ATC
C3, C8, C14, C15, C17	39 pF Chip Capacitors	GRM40001C0G390J050BD	Murata
C4, C9	10 μF Chip Capacitors	ECJ4YF1H106Z	Panasonic
C5	24 pF Chip Capacitor	600F240JT	ATC
C6, C7	15 pF Chip Capacitors	600F150JT	ATC
C12	4.7 pF Chip Capacitor	600F4R7BT	ATC
C13	0.4 pF Chip Capacitor	600F0R4BT	ATC
C16, C18, C19, C20	0.015 μF Chip Capacitors	GRM400X7R153J050BD	Murata
F1	5A Surface Mount Fuse	1FT5A	Little Fuse
F2	1A Surface Mount Fuse	1FT1A	Little Fuse
R1, R7	681 Ω, Chip Resistors		
R2, R5	4.75 kΩ, Chip Resistors		
R3, R4, R8	1.21 kΩ, Chip Resistors		
R6	267 Ω, Chip Resistor		

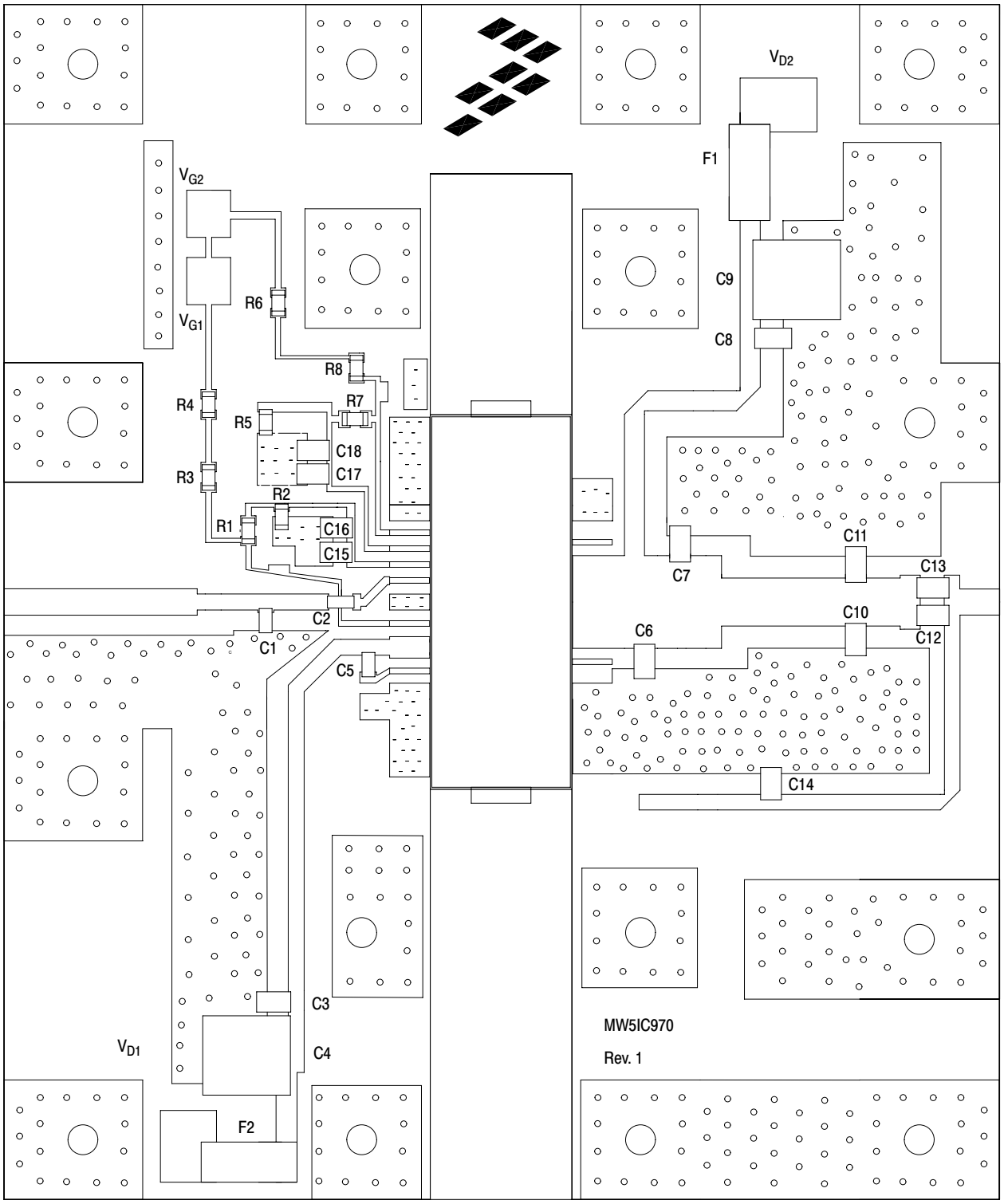


Figure 4. MW5IC970NBR1 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

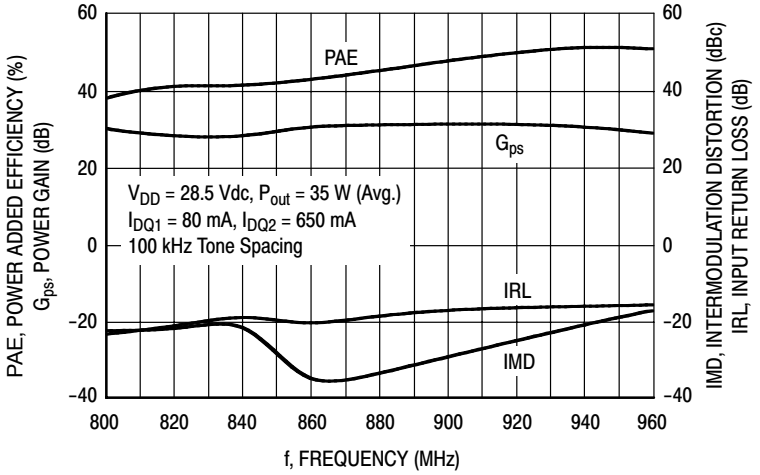


Figure 5. Two-Tone Wideband Performance @ P_{out} = 35 Watts (Avg.)

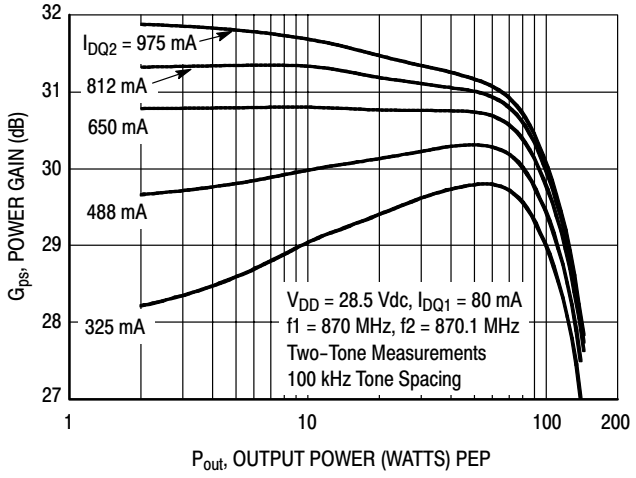


Figure 6. Two-Tone Power Gain versus Output Power

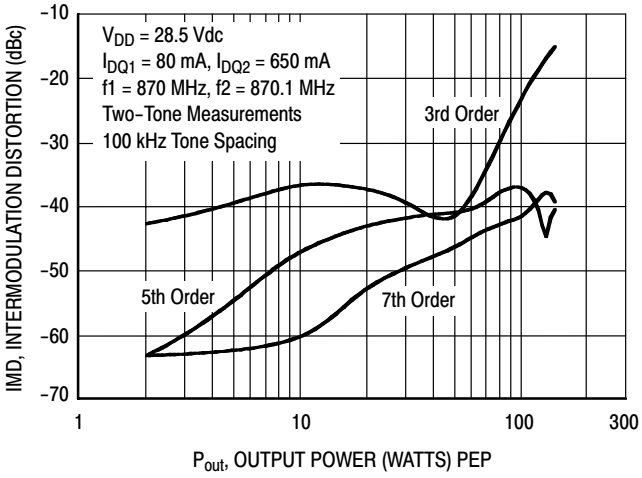


Figure 7. Intermodulation Distortion Products versus Output Power

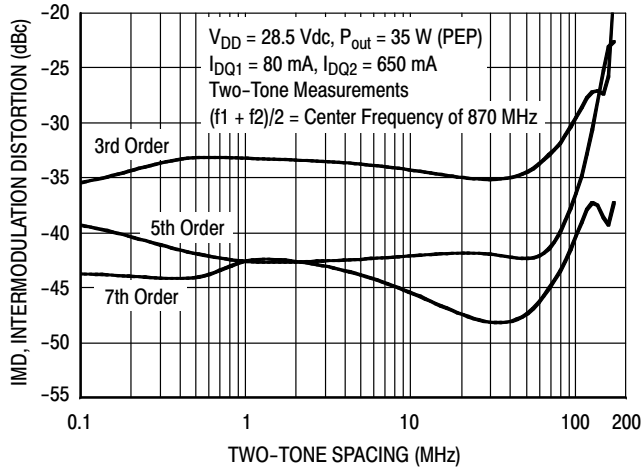


Figure 8. Intermodulation Distortion Products versus Tone Spacing

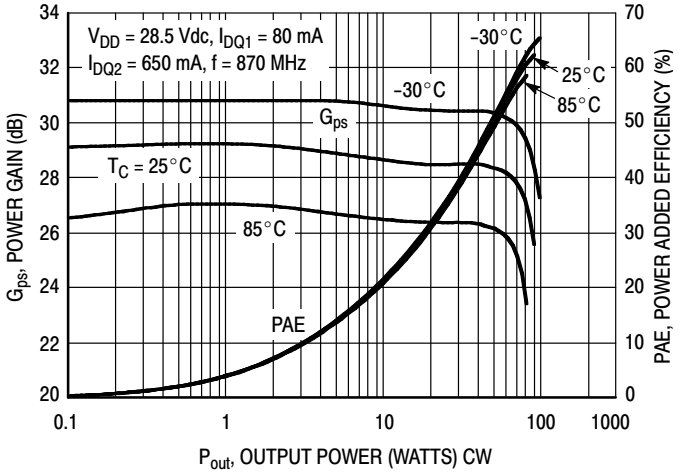


Figure 9. Power Gain and Power Added Efficiency versus CW Output Power

TYPICAL CHARACTERISTICS

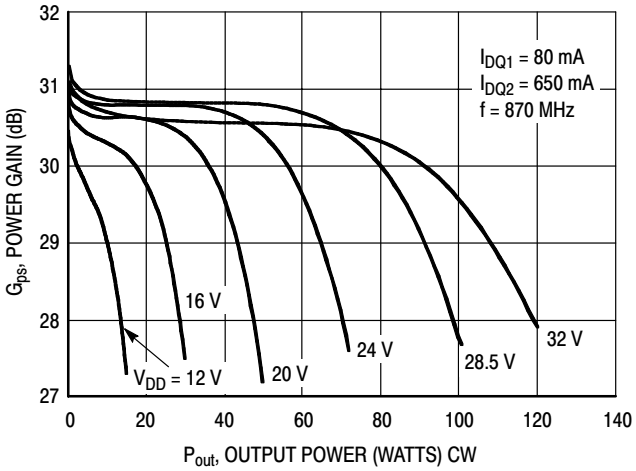
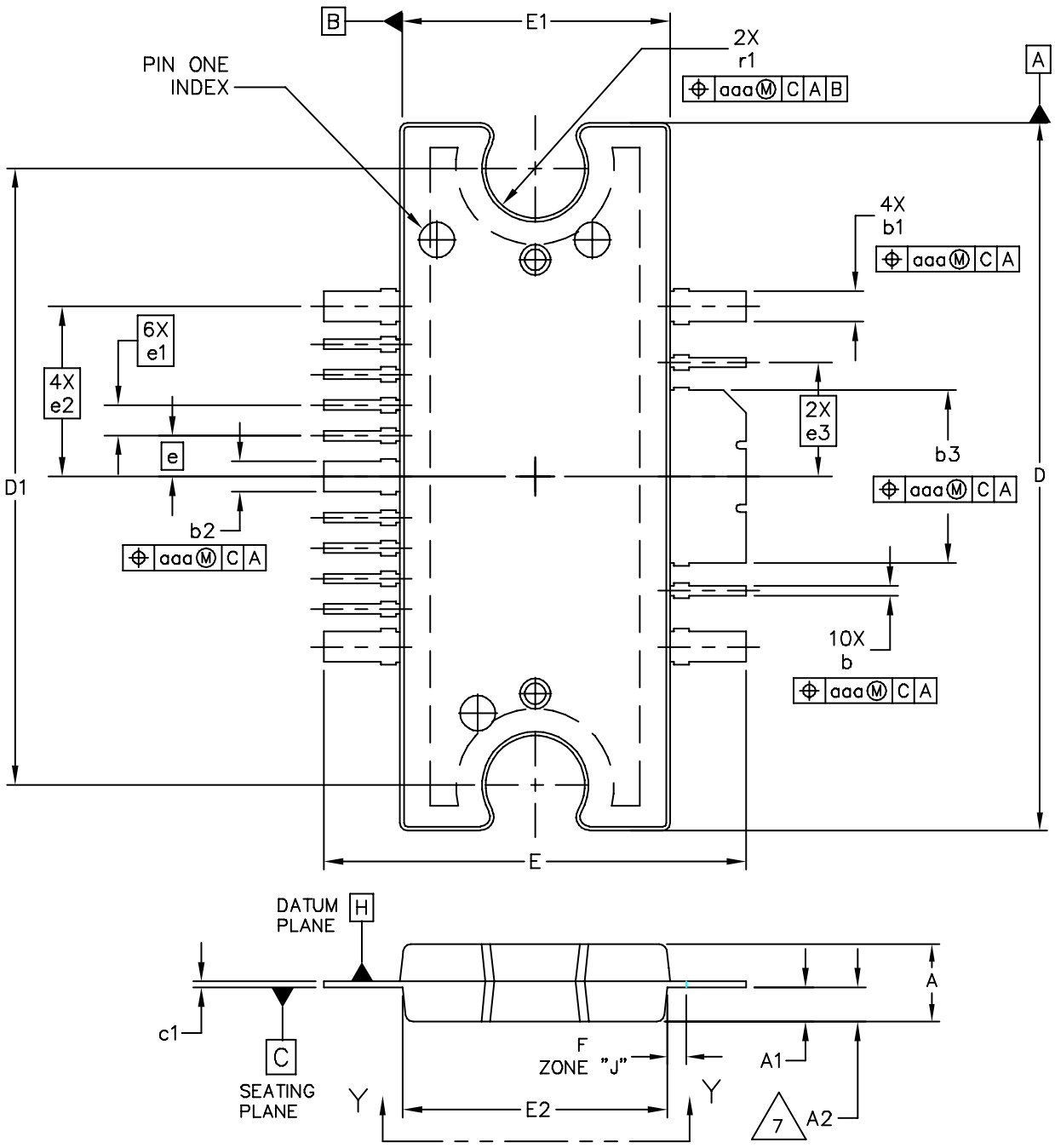


Figure 10. Power Gain versus Output Power

NOTES

NOTES

PACKAGE DIMENSIONS



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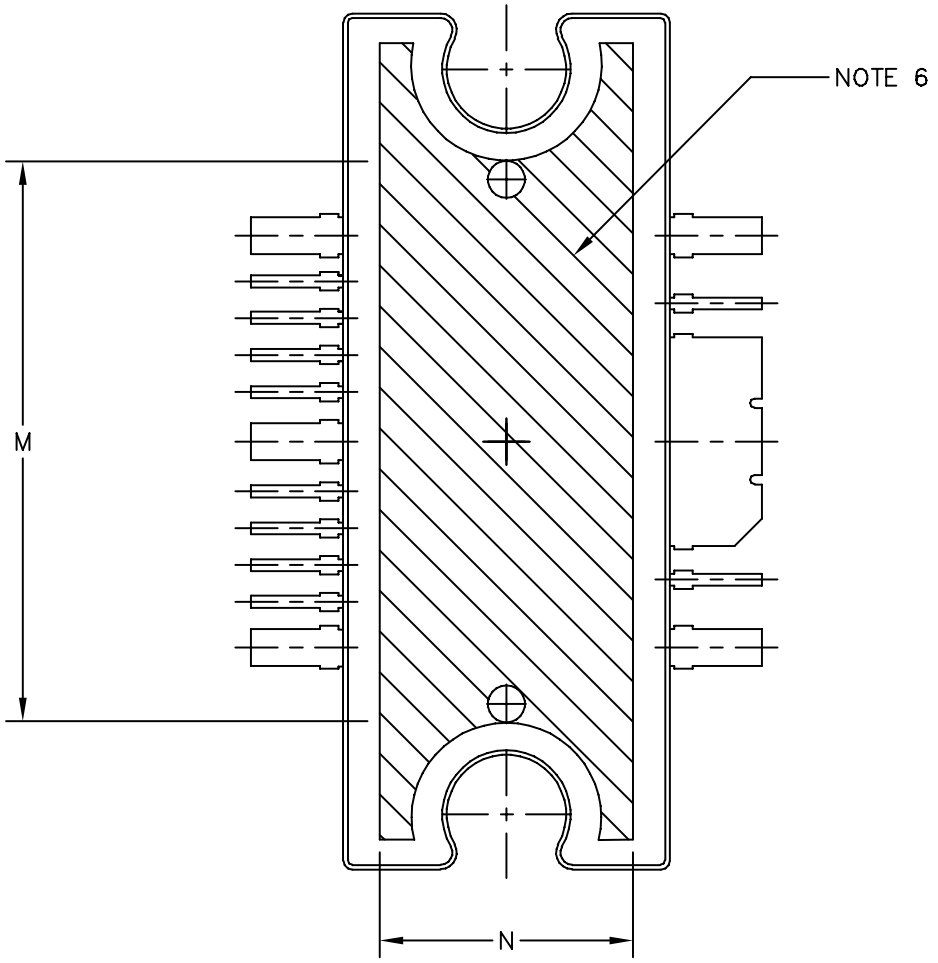
	CASE NUMBER: 1329-09	13 MAR 2006
	STANDARD: NON-JEDEC	



VIEW Y–Y

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	CASE NUMBER: 1329–09	13 MAR 2006
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----					
					aaa	.004		.10	

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