

Hex Inverting Schmitt Trigger

MM74HCT14

Description

The MM74HCT14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HCT logic family is functionally and pinout-compatible with the standard 74LS logic family. Inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 10 ns
- Wide Power Supply Range: 4.5 V – 5.5 V
- Low Quiescent Current: 10 μ A Maximum
- Low Input Current: 1 μ A Maximum
- Fanout of 10 LS-TTL Loads
- Typical Hysteresis Voltage: 0.6 V at $V_{CC} = 4.5$ V
- TTL, LS Pin-out and Input Threshold Compatible
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Connection Diagram

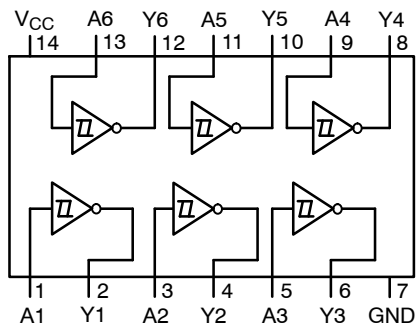


Figure 1. Pin Assignments

Schematic Diagram

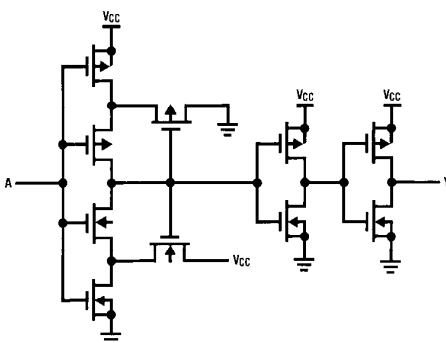
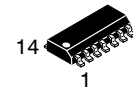
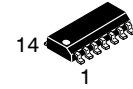


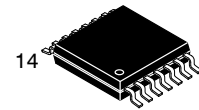
Figure 2. Schematic



SOIC-14 NB
CASE 751A-03

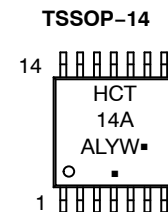
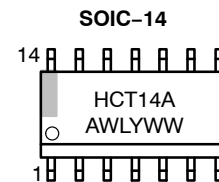


SOIC-14
CASE 751EF



TSSOP-14 WB
CASE 948G

MARKING DIAGRAMS



- HCT14A = Specific Device Code
- A = Assembly Location
- WL, L = Wafer Lot Number
- Y = Year
- WW, YW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

MM74HCT14

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Min	Max	Unit
V _{CC}	Supply Voltage	-0.5	+7.0	V
V _{IN}	DC Input Voltage	-0.5	V _{CC} + 0.5	V
V _{OUT}	DC Output Voltage	-0.5	V _{CC} + 0.5	V
I _{IK} , I _{OK}	Clamp Diode Current		±20	mA
I _{OUT}	DC Output Current, Per Pin		±25	mA
I _{CC}	DC V _{CC} or GND Current, Per Pin		±50	mA
T _{STG}	Storage Temperature Range	-65	+150	°C
T _L	Lead Temperature (Soldering 10 second)		+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	4.5	5.5	V
V _{IN} , V _{OUT}	DC Input or Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range	-40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC}	T _A = +25°C		T _A = -40 to +85°C		Unit
				Typ	Guaranteed Limits			
V _{T+}	Positive-Going Threshold Voltage	Minimum	4.5	1.5	1.2	1.2	V	
			5.5	1.7	1.4	1.4		
		Maximum	4.5	1.5	1.9	1.9		
			5.5	1.7	2.1	2.1		
V _{T-}	Negative-Going Threshold Voltage	Minimum	4.5	0.9	0.5	0.5	V	
			5.5	1.0	0.6	0.6		
		Maximum	4.5	0.9	1.2	1.2		
			5.5	1.0	1.4	1.4		
V _H	Hysteresis Voltage	Minimum	4.5	0.6	0.4	0.4	V	
			5.5	0.7	0.4	0.4		
		Maximum	4.5	0.6	1.4	1.4		
			5.5	0.7	1.5	1.5		
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 20 μA	4.5	V _{CC}	V _{CC} - 0.1	V _{CC} - 0.1	V	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4.0 mA	4.5	4.20	3.98	3.84		
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4.8 mA	5.5	5.20	4.98	4.98		
V _{OL}	Maximum LOW Level Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 20 μA	4.5	0	0.1	0.1	V	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4.0 mA	4.5	0.2	0.26	0.33		
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4.8 mA	5.5	0.2	0.26	0.33		
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}	5.5		±0.1	±1.0	μA	

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DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V _{CC}	T _A = +25°C		T _A = -40 to +85°C		Unit
				Typ	Guaranteed Limits			
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0 μA	5.5		1.0	10.0	μA	
		V _{IN} = 2.4 V or 0.5 V			2.4	2.4	mA	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns)

Symbol	Parameter	Typ	Guaranteed Limit	Unit
t _{PHL} , t _{PLH}	Maximum Propagation Delay	10	18	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC} = 5.0 V ±10%, C_L = 50 pF, t_r = t_f = 6 ns)

Symbol	Parameter	Conditions	T _A = +25°C		T _A = -40 to +85°C		Unit
			Typ	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay			20	25	ns	
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		9	15	19	ns	
C _{PD}	Power Dissipation Capacitance (Note 1)	Per Gate		25		pF	
C _{IN}	Maximum Input Capacitance		5	10	10	pF	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. C_{PD} determines the no-load dynamic power consumption, P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

Typical Applications

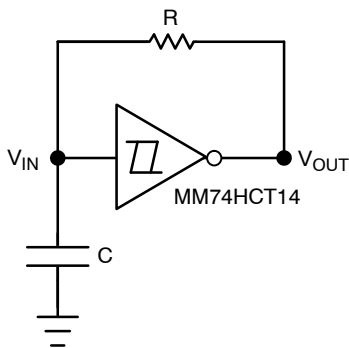


Figure 3. Low Power Oscillator

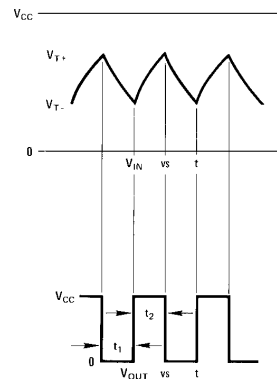


Figure 4. Oscillator Input and Output Waveforms

The following equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$:

$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}} \quad (\text{eq. 1})$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}} \quad (\text{eq. 2})$$

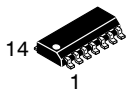
MM74HCT14

ORDERING INFORMATION

Device	Package	Shipping [†]
MM74HCT14M	SOIC-14 NB, Case 751A-03 (Pb-Free and Halide Free)	55 Units / Tube
MM74HCT14MX	SOIC14, Case 751EF (Pb-Free and Halide Free)	2500 Units / Tape & Reel
MM74HCT14MTCX	TSSOP-14 WB, Case 948G (Pb-Free and Halide Free)	2500 Units / Tape & Reel

For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

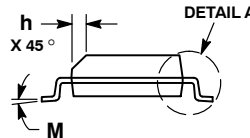
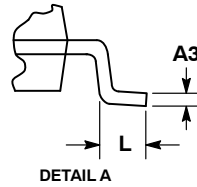
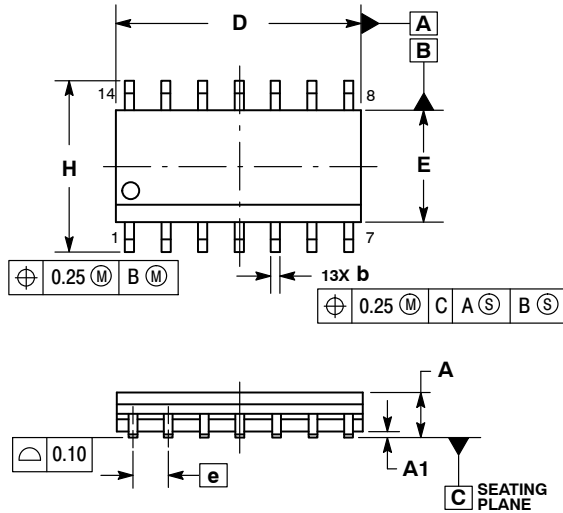
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

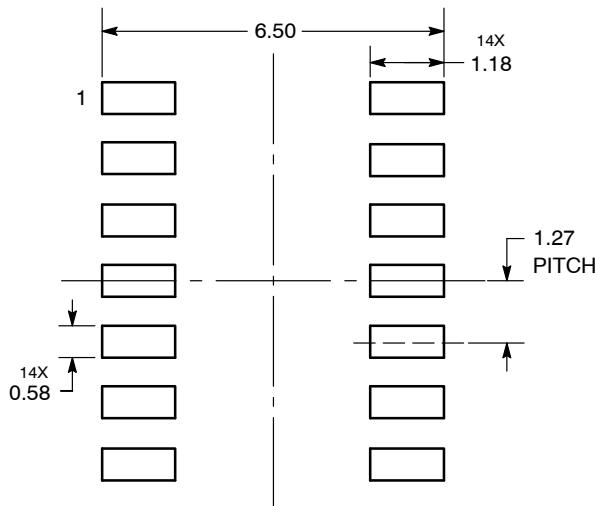


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

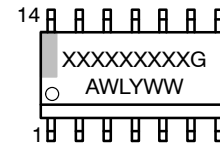
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
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 7. ANODE/CATHODE
 8. ANODE/CATHODE
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 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
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 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
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 9. ANODE/CATHODE
 10. ANODE/CATHODE
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 14. COMMON CATHODE

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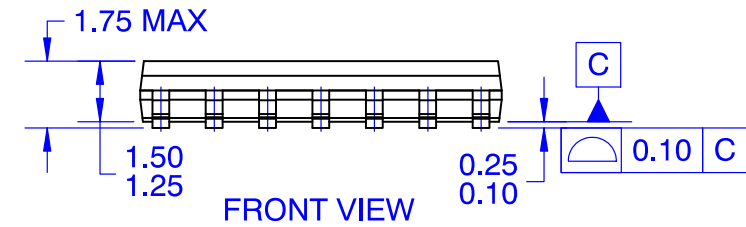
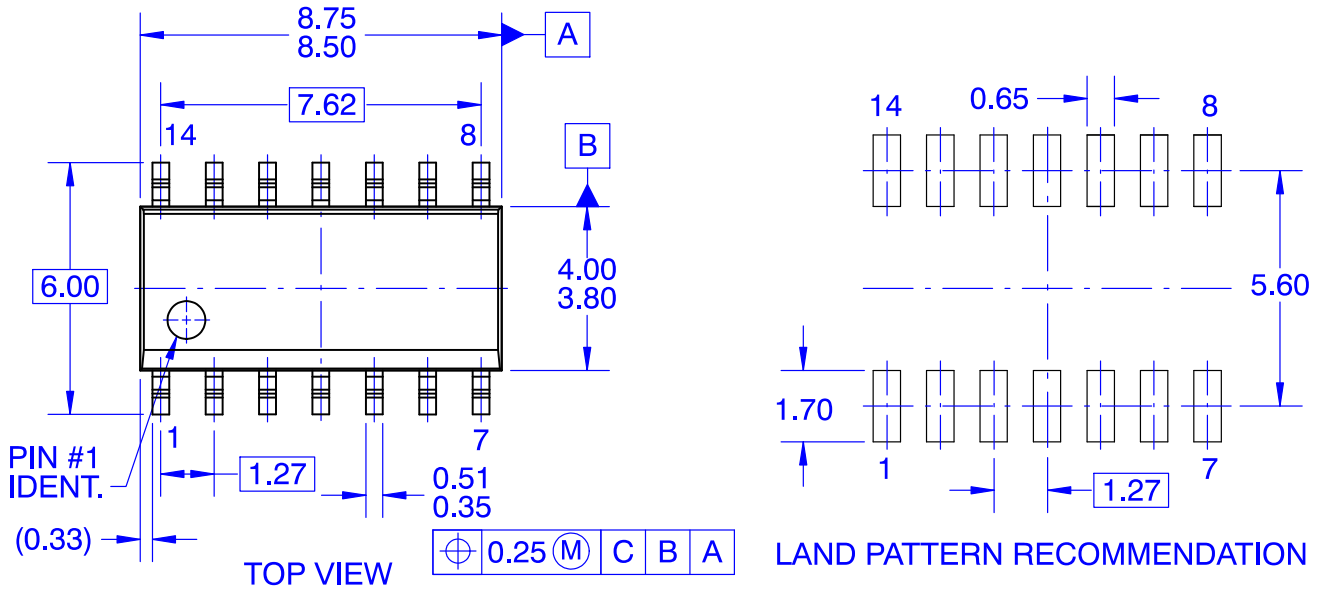
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



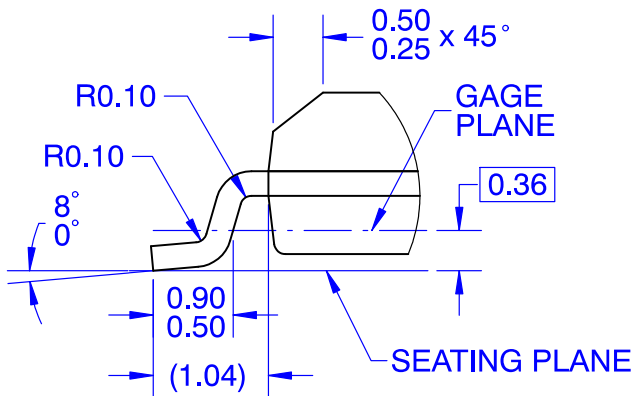
SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



NOTES:

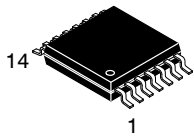
- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009



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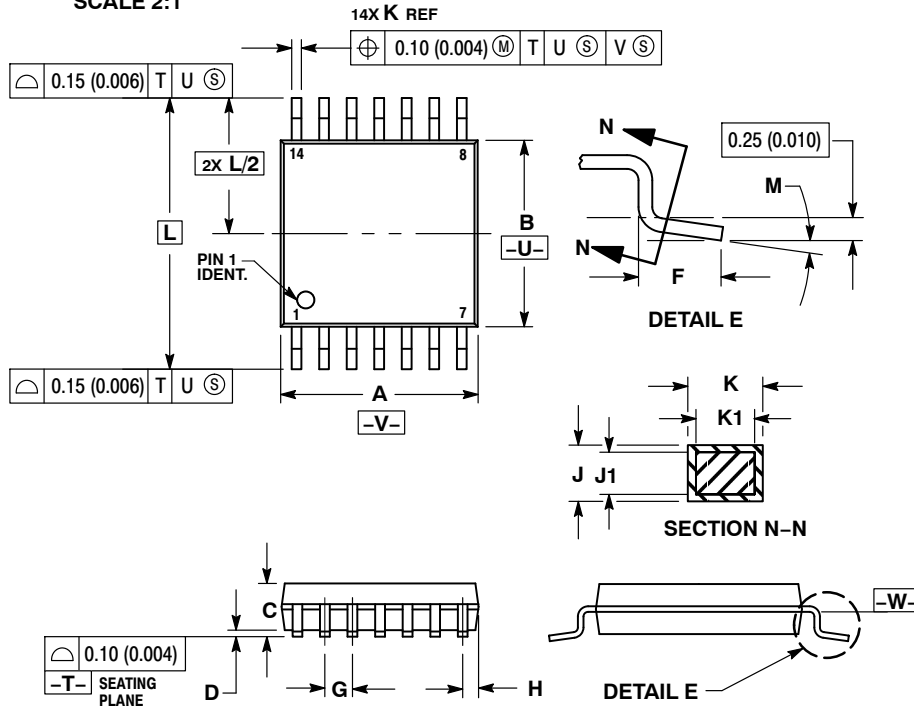
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

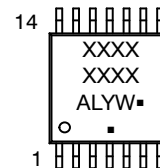


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*

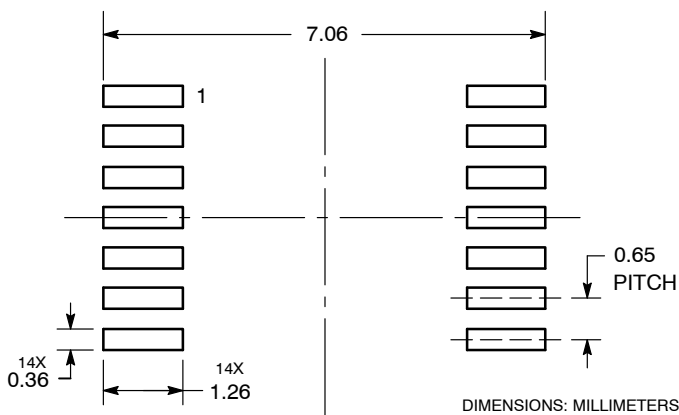


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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