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December 1, 2005 FN9135.4

Multi-Phase PWM Controller with Precision $r_{DS(ON)}$ or DCR Current Sensing for VR10.X Application

The ISL6565A, ISL6565B controls microprocessor core voltage regulation by driving up to 3 synchronous-rectified buck channels in parallel. Multi-phase buck converter architecture uses interleaved timing to multiply channel ripple frequency and reduce input and output ripple currents.

The difference between the ISL6565A and the ISL6565B is that the ISL6565A utilizes $r_{DS(ON)}$ current sensing, while the ISL6565B utilizes DCR current sensing for each phase. These cost and space saving methods of current sensing are used for adaptive voltage positioning (droop), channel-current balancing, and overcurrent protection. To ensure the accuracy of droop, a programmable internal temperature compensation function is implemented to compensate the effect of $r_{DS(ON)}$ and DCR temperature sensitivity.

A unity gain, differential amplifier is provided for remote voltage sensing. Any potential difference between remote and local grounds is eliminated using the remote-sense amplifier. The precision threshold-sensitive enable input is available to accurately coordinate the start up of the ISL6565A, ISL6565B with Intersil MOSFET driver ICs. Dynamic-VID™ technology allows seamless on-the-fly VID changes. The offset pin allows accurate voltage offset settings that are independent of VID setting.

Features

- Multi-Phase Power Conversion
  - 2 or 3 Phase Operation
- Precision Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Temperature and Life
  - Adjustable Reference-Voltage Offset
- Precision $r_{DS(ON)}$ or DCR Current Sensing
  - Integrated Programmable Temperature Compensation
  - Accurate Load-Line Programming
  - Accurate Channel-Current Balancing
  - Low-Cost, Lossless Current Sensing
- Input Voltage: 12V or 5V Bias
- Microprocessor Voltage Identification Input
  - Dynamic VID® Technology
  - 6-Bit VID Input
  - 0.8375V to 1.600V in 12.5mV Steps
- Threshold Enable Function for Precision Sequencing
- Overcurrent Protection
- Overvoltage Protection
- Digital Soft-Start
- Operation Frequency up to 1.5MHz per Phase
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package Footprint, which Improves PCB Efficiency and Has a Thinner Profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Ordering Information

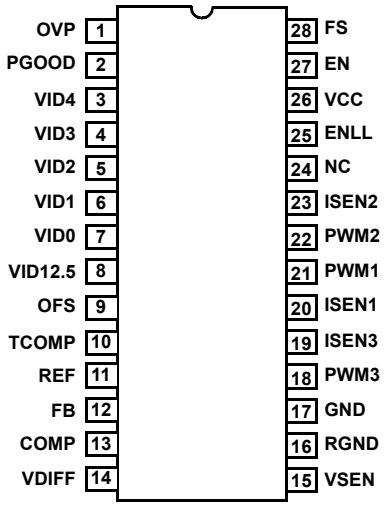
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6565ACB	ISL6565ACB	0 to 105	28 Ld SOIC	M28.3
ISL6565ACBZ (Note)	ISL6565ACBZ	0 to 105	28 Ld SOIC (Pb-free)	M28.3
ISL6565ACR	ISL6565ACR	0 to 105	28 Ld 5x5 QFN	L28.5x5
ISL6565ACRZ (Note)	ISL6565ACRZ	0 to 105	28 Ld 5x5 QFN (Pb-free)	L28.5x5
ISL6565ACV	ISL6565ACV	0 to 105	28 Ld TSSOP	M28.173
ISL6565ACVZ (Note)	ISL6565ACVZ	0 to 105	28 Ld TSSOP (Pb-free)	M28.173
ISL6565BCB	ISL6565BCB	0 to 105	28 Ld SOIC	M28.3
ISL6565BCBZ (Note)	ISL6565BCBZ	0 to 105	28 Ld SOIC (Pb-free)	M28.3
ISL6565BCR	ISL6565BCR	0 to 105	28 Ld 5x5 QFN	L28.5x5
ISL6565BCRZ (Note)	ISL6565BCRZ	0 to 105	28 Ld 5x5 QFN (Pb-free)	L28.5x5
ISL6565BCV	ISL6565BCV	0 to 105	28 Ld TSSOP	M28.173
ISL6565BCVZ (Note)	ISL6565BCVZ	0 to 105	28 Ld TSSOP (Pb-free)	M28.173

*Add "-T" suffix for tape and reel.

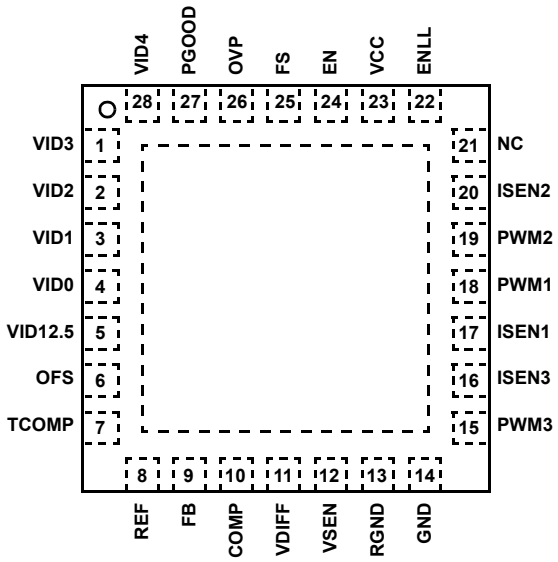
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

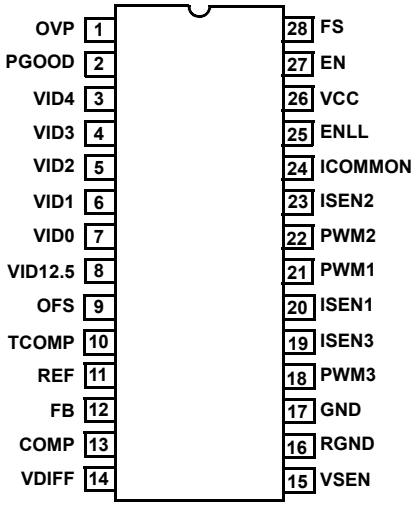
ISL6565ACB (SOIC), ISL6565ACV (TSSOP)
TOP VIEW



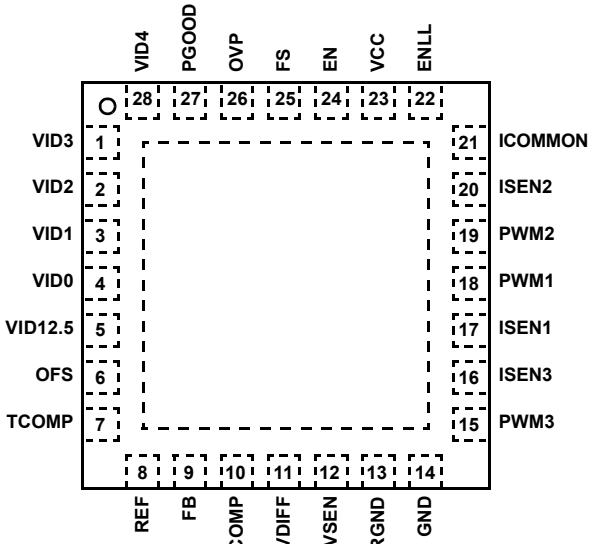
ISL6565ACR (QFN)
TOP VIEW



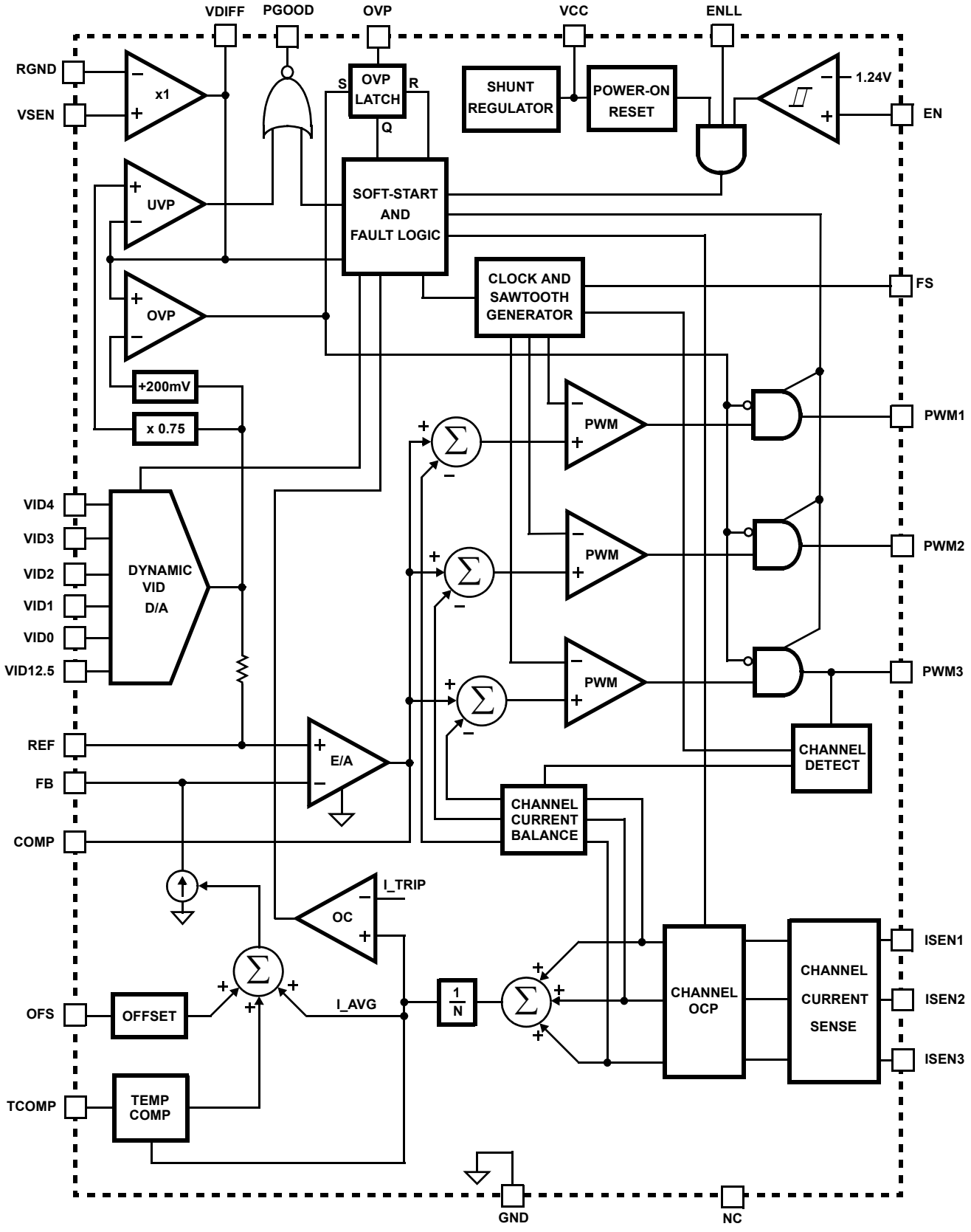
ISL6565BCB (SOIC), ISL6565BCV (TSSOP)
TOP VIEW



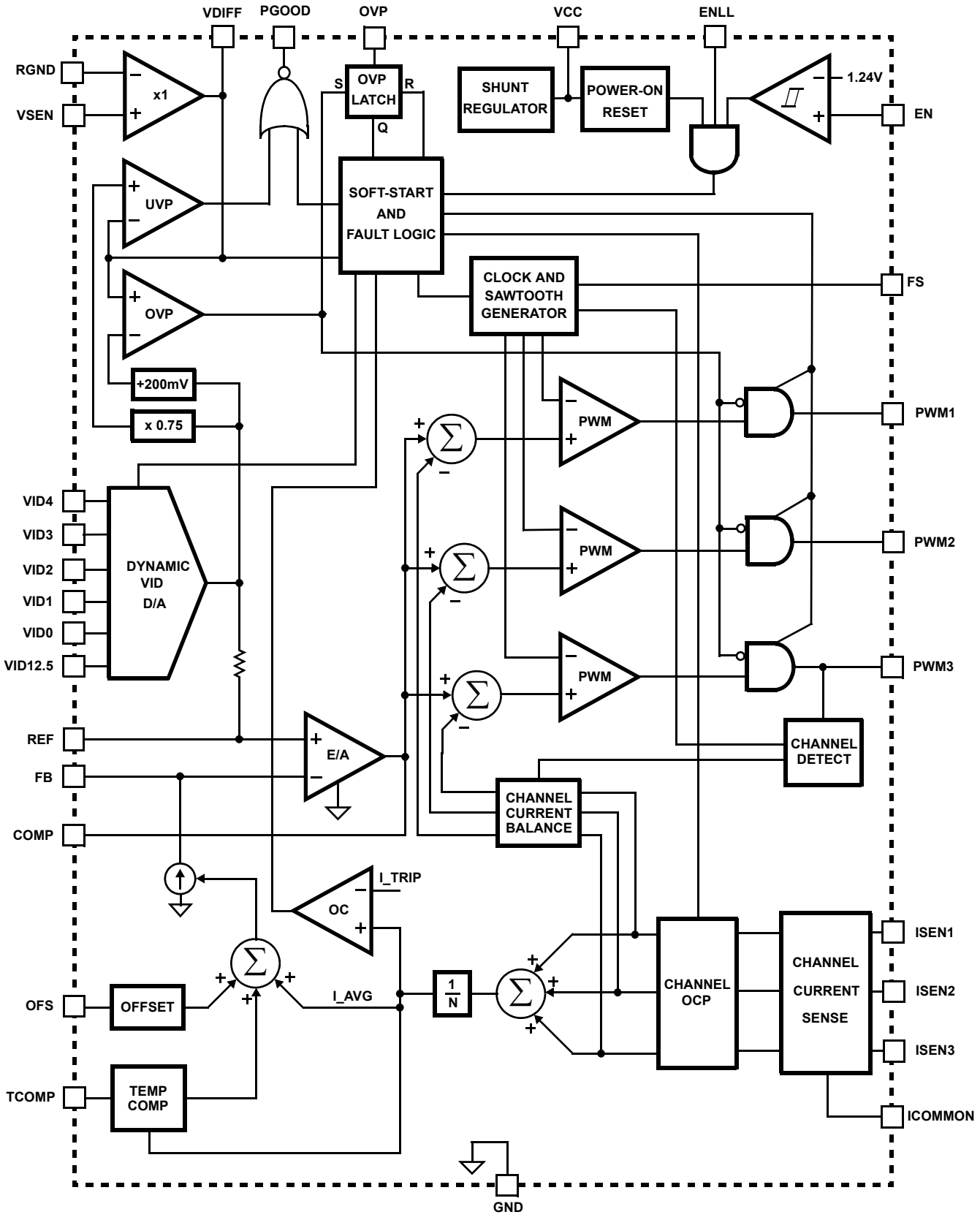
ISL6565BCR (QFN)
TOP VIEW



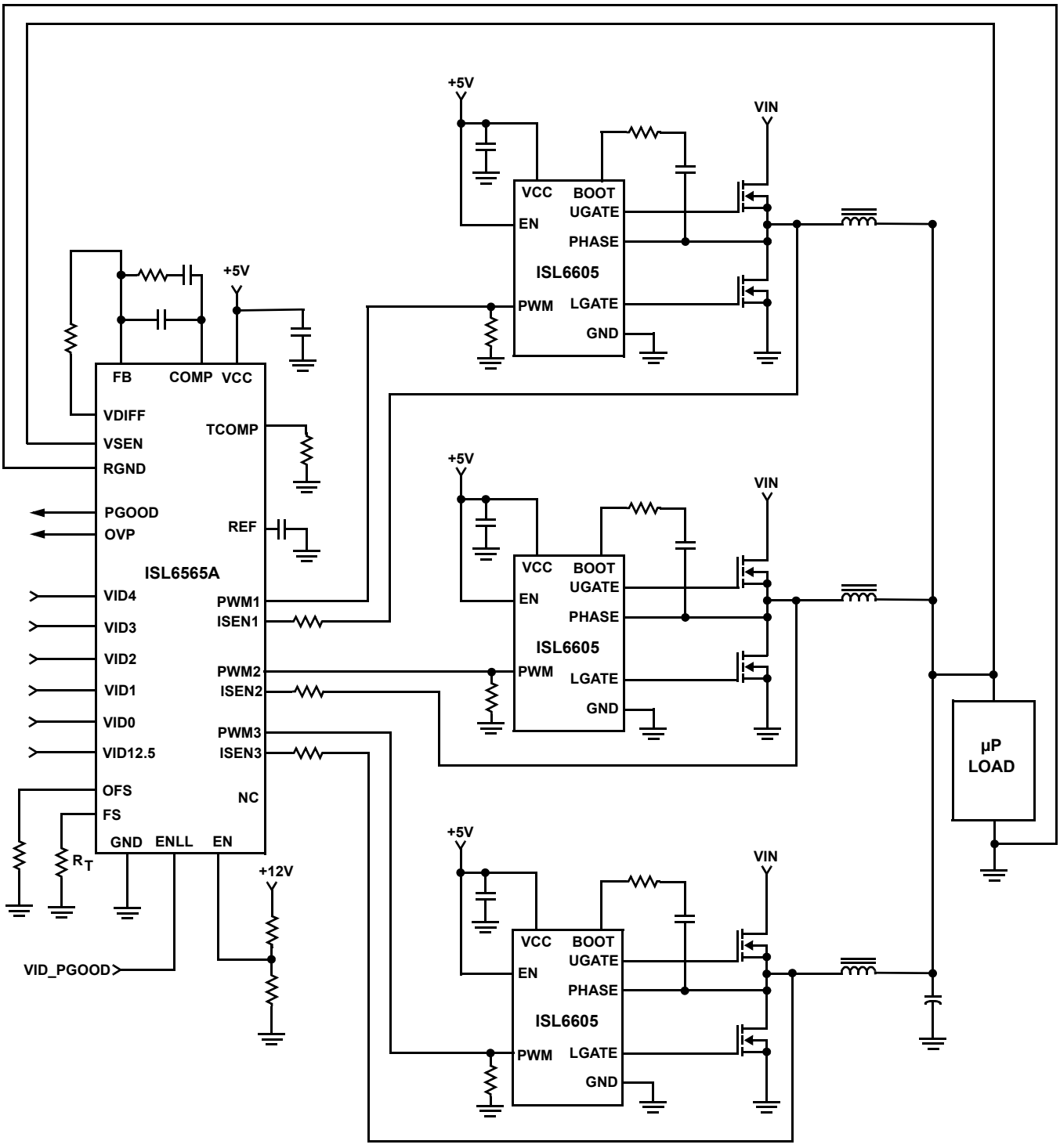
ISL6565A Block Diagram



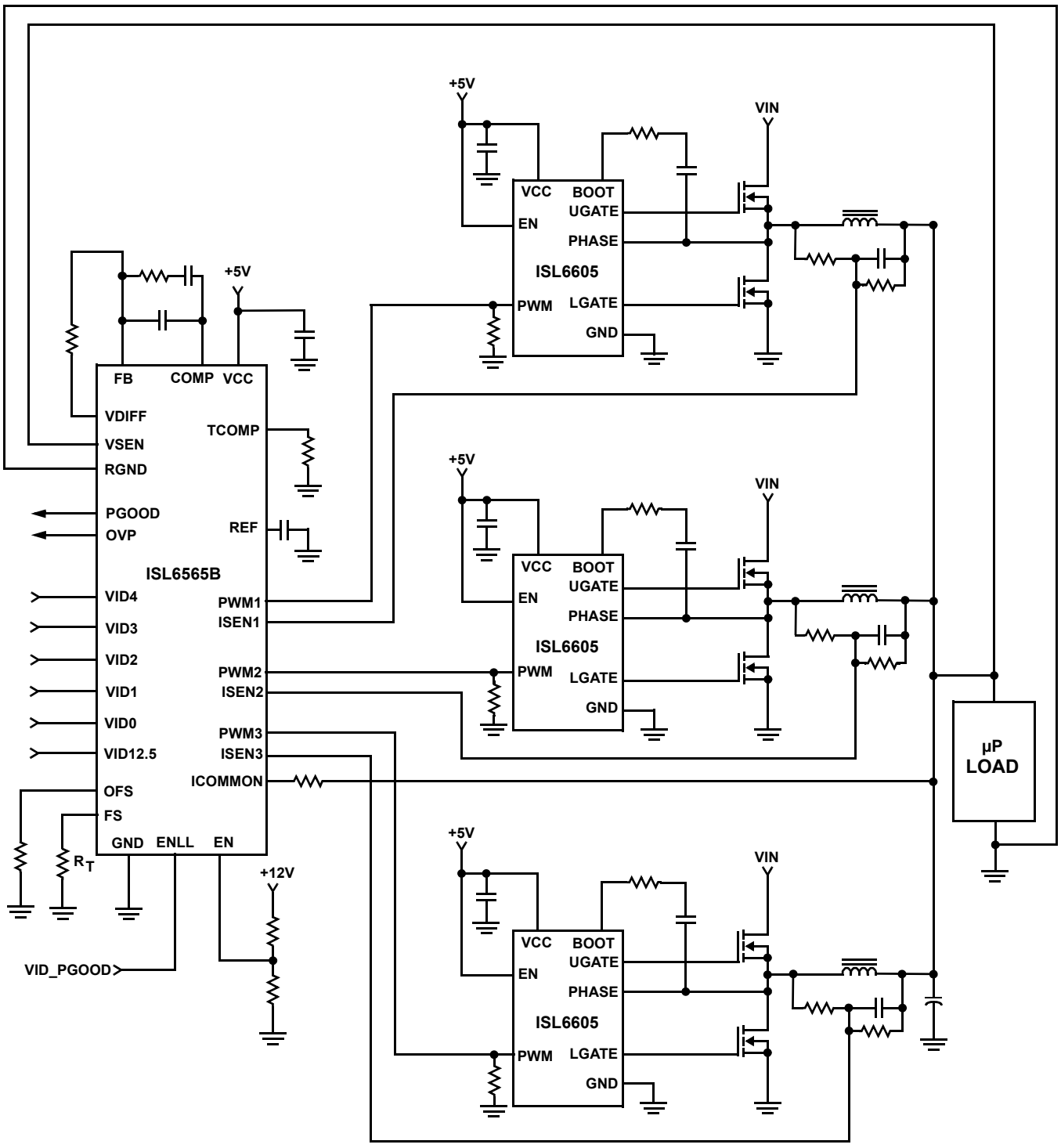
ISL6565B Block Diagram



Typical Application - ISL6565A



Typical Application - ISL6565B



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . .+7V
Input, Output, or I/O Voltage (except OVP) . .GND -0.3V to V_{CC} + 0.3V
OVP Voltage . . . . . .+15V
ESD (Human body model) . . . . . .>4kV
ESD (Machine model) . . . . . .>300V
ESD (Charged device model) . . . . . .>2kV

Operating Conditions

Supply Voltage, VCC (5V bias mode) . . . . . +5V ±5%
Junction Temperature . . . . . 0°C to 125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	62	N/A
QFN Package (Notes 2, 3)	33	3.5
TSSOP Package (Note 1)	85	N/A

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V or ICC < 25mA (Note 4), T_J = 0°C to 105°C. Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT					
Nominal Supply	VCC = 5VDC; EN = 5VDC; R_T = 100kΩ, ISEN1 = ISEN2 = ISEN3 = -70µA	-	14	18	mA
Shutdown Supply	VCC = 5VDC; EN = 0VDC; R_T = 100kΩ	-	10	14	mA
SHUNT REGULATOR					
VCC Voltage	VCC tied to 12VDC thru 300Ω resistor, R_T = 100kΩ	5.6	5.9	6.2	V
VCC Sink Current	VCC tied to 12VDC thru 300Ω resistor, R_T = 100kΩ	-	-	25	mA
POWER-ON RESET AND ENABLE					
POR Threshold	VCC Rising	4.2	4.31	4.50	V
	VCC Falling	3.7	3.82	4.00	V
ENABLE Threshold	EN Rising	1.29	1.31	1.33	V
	Hysteresis	-	150	-	mV
	Fault Reset	1.10	1.14	1.18	V
ENLL Input Logic Low Level		-	-	0.4	V
ENLL input Logic High Level		0.8	-	-	V
ENLL Leakage Current	ENLL = 5V	-	-	1	µA
REFERENCE VOLTAGE AND DAC					
System Accuracy (VID = 1.2V-1.6V, T_J = 0°C to 85°C)		-0.5	-	0.5	%VID
System Accuracy (VID = 0.8375V-1.1875V T_J = 25°C)		-0.7	-	0.7	%VID
System Accuracy (VID = 0.8375V-1.1875V, T_J = 0°C to 85°C)		-0.8	-	0.8	%VID
VID Pull Up		-65	-50	-35	µA
VID Input Low Level		-	-	0.4	V
VID Input High Level		0.8	-	-	V
DAC Source/Sink Current	VID = 010100	-200	-	200	µA
REF Source/Sink Current		-50	-	50	µA
PIN-ADJUSTABLE OFFSET					
Voltage at OFS Pin	Offset resistor connected to ground	485	500	515	mV
	Voltage below VCC, offset resistor connected to VCC	1.97	2.03	2.09	V

Electrical Specifications Operating Conditions: VCC = 5V or ICC < 25mA (Note 4), T_J = 0°C to 105°C. Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Accuracy	R_T = 100kΩ	-10	-	10	%
Adjustment Range		0.08	-	1.5	MHz
Sawtooth Amplitude		-	1.5	-	V
Max Duty Cycle		-	66.7	-	%
ERROR AMPLIFIER					
Open-Loop Gain (Note 7)	R_L = 10kΩ to ground	-	80	-	dB
Open-Loop Bandwidth (Note 7)	C_L = 100pF, R_L = 10kΩ to ground	-	18	-	MHz
Slew Rate	C_L = 100pF	4.5	6.0	7.5	V/μs
Maximum Output Voltage		4.0	4.3	-	V
Output High Voltage @ 2mA		3.7	-	-	V
Output Low Voltage @ 2mA		-	-	1.35	V
REMOTE-SENSE AMPLIFIER					
Bandwidth (Note 7)		-	20	-	MHz
Output High Current	VSEN - RGND = 2.5V	-500	-	500	μA
Output High Current	VSEN - RGND = 0.6	-500	-	500	μA
PWM OUTPUT					
PWM Output Voltage LOW Threshold	Iload = ±500μA	-	-	0.3	V
PWM Output Voltage HIGH Threshold	Iload = ±500μA	4.3	-	-	V
TEMPERATURE COMPENSATION					
Temperature Compensation Current @ 40°C and Tcomp = 0.5V		10	15	20	μA
Temperature Compensation Transconductance (Note 7)		-	2	-	μA/V/°C
SENSE CURRENT					
Sensed Current Tolerance	ISEN1 = ISEN2 = ISEN3 = 80μA, 0°C to 105°C	74	81	91	μA
Overcurrent Trip Level		95	110	130	μA
POWER GOOD AND PROTECTION MONITORS					
PGOOD Low Voltage	I_{PGOOD} = 4mA	-	-	0.4	V
Undervoltage Offset From VID	VSEN Falling	72	74	76	%VID
Overvoltage Threshold	Voltage above VID, After Soft-Start (Note 6)	180	200	220	mV
	Before Enable	-	1.63	-	V
	VCC < POR Threshold	1.7	1.8	1.87	V
Overvoltage Reset Voltage	VCC ≥ POR Threshold, VSEN Falling	-	0.6	-	V
	VCC < POR Threshold	-	1.5	-	V
OVP Drive Voltage	I_{OVP} = -100mA, VCC = 5V	-	1.9	-	V
Minimum VCC for OVP		1.4	-	-	V

NOTES:

4. When using the internal shunt regulator, VCC is clamped to 6.02V (max). Current must be limited to 25mA or less.
5. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
6. During soft-start, VDAC rises from 0 to VID. The overvoltage trip level is the higher of 1.7V and VDAC + 0.2V.
7. Parameter magnitude guaranteed by design. Not 100% tested.

Functional Pin Description

VCC - Supplies all the power necessary to operate the chip. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply or through a series 300Ω resistor to a +12V supply.

GND - Bias and reference ground for the IC.

EN - This pin is a threshold-sensitive enable input for the controller. Connecting the 12V supply to EN through an appropriate resistor divider provides a means to synchronize power-up of the controller and the MOSFET driver ICs. When EN is driven above 1.31V, the ISL6565A, ISL6565B is active depending on status of ENLL, the internal POR, and pending fault states. Driving EN below 1.14V will clear all fault states and prime the ISL6565A, ISL6565B to soft-start when re-enabled.

ENLL - This pin is a logic-level enable input for the controller. When asserted to a logic high, the ISL6565 is active depending on status of EN, the internal POR, VID inputs and pending fault states. Deasserting ENLL will clear all fault states and prime the ISL6565A, ISL6565B to soft-start when re-enabled.

FS - A resistor, placed from FS to ground, will set the switching frequency. Refer to Equation 45 for proper resistor calculation.

VID4, VID3, VID2, VID1, VID0, and VID12.5 - These are the inputs to the internal DAC that provides the reference voltage for output regulation. Connect these pins either to open-drain outputs with or without external pull-up resistors or to active-pull-up outputs. VID4-VID12.5 have 20µA internal pull-up current sources that diminish to zero as the voltage rises above the logic-high level.

VDIFF, VSEN, and RGND - VSEN and RGND are inputs to the precision differential remote-sense amplifier. This amplifier converts the differential voltage of the remote output to a single-ended voltage referenced to local ground. VDIFF is the amplifier's output and the input to the regulation and protection circuitry. Connect VSEN and RGND to the sense pins of the remote load.

FB and COMP - Inverting input and output of the error amplifier respectively. FB is connected to VDIFF through a resistor. A negative current, proportional to output current is present on the FB pin. A properly sized resistor between VDIFF and FB sets the load line (droop). The droop scale factor is set by the ratio of the ISEN resistors and the lower MOSFET $r_{DS(ON)}$ or inductor DCR. COMP is tied back to FB through an external R-C network to compensate the regulator.

REF - The REF input pin is the positive input of the Error Amp. It is internally connected to the DAC output through a 1kΩ resistor. A capacitor is used between the REF pin and ground to smooth the voltage transition during Dynamic VID™ operations.

TCOMP - Temperature compensation scaling input. A resistor from this pin to ground sets the gain of the internal thermal sense circuitry. The temperature sensed by the controller is utilized to modify the droop current output to the FB pin, adjusting for MOSFET $r_{DS(ON)}$ and Inductor DCR variations with temperature.

PWM1, PWM2, PWM3 - Pulse-width modulation outputs. Connect these pins to the PWM input pins of the Intersil driver ICs. The number of active channels is determined by the state of PWM3. Tie PWM3 to VCC to configure for 2-phase operation.

ISEN1, ISEN2, ISEN3, ICOMMON (ISL6565B only) - These pins are used for sensing individual phase output currents. The sensed current is used for channel balancing, protection, and load line regulation. ISEN3 should be left open for 2-phase operation.

For $r_{DS(ON)}$ current sensing using the ISL6565A, connect a resistor between the ISEN1, ISEN2, and ISEN3 pins and their respective phase node. This resistor sets a current proportional to the current in the lower MOSFET during it's conduction interval.

For DCR sensing using the ISL6565B, connect a resistor from VCORE to the ICOMMON pin. Then connect ISEN1, ISEN2, and ISEN3 to the node between the RC sense elements surrounding the inductor of their respective phase.

PGOOD - PGOOD is used as an indication of the end of soft-start. It is an open-drain logic output that is low impedance until the soft-start is completed. It will be pulled low again once the undervoltage point is reached.

OFS - The OFS pin provides a means to program a DC current for generating an offset voltage across the droop resistor between FB and VDIFF. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unconnected.

OVP - Overvoltage protection pin. This is an open drain device, which can be externally configured with a resistor to control an SCR to shut down the regulator.

Operation

Multi-Phase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multi-phase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter that is both cost-effective and thermally viable have forced a change to the cost-saving approach of multi-phase. The ISL6565A, ISL6565B controller helps simplify implementation by integrating vital functions and requiring minimal output components. The block diagrams on pages 3 and 4 provide top level views of multi-phase power conversion using the ISL6565A and ISL6565B controllers.

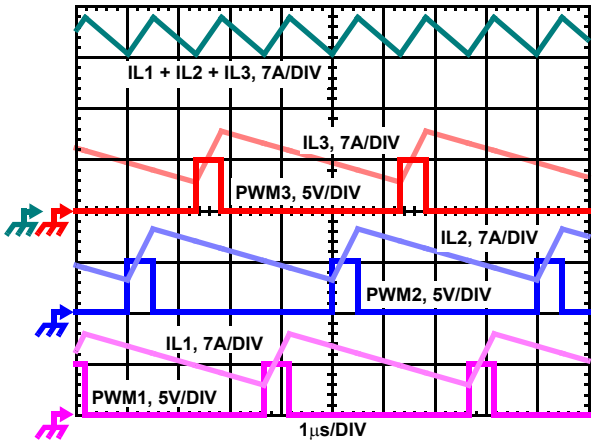


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine the equation representing an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{Lf_S V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N V_{OUT})V_{OUT}}{Lf_S V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

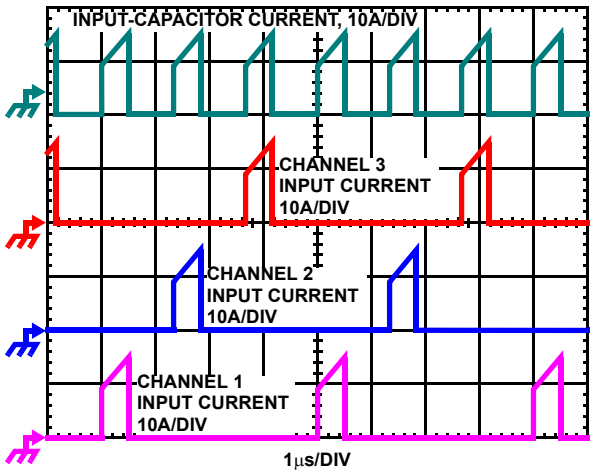


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Figures 19 and 20 in the section entitled *Input Capacitor Selection* can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution.

PWM Operation

The timing of each converter leg is set by the number of active channels. The default channel setting for the ISL6565A, ISL6565B is three. One switching cycle is defined as the time between PWM1 pulse termination signals. The pulse termination signal is the internally generated clock signal that triggers the falling edge of PWM1. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FS pin and ground. Each cycle begins when the clock signal commands PWM1 to go low. The PWM1 transition signals the channel-1 MOSFET driver to turn off the channel-1 upper MOSFET and turn on the channel-1 synchronous MOSFET. In the default channel configuration, the PWM2 pulse terminates 1/3 of a cycle after the PWM1 pulse. The PWM3 pulse terminates 1/3 of a cycle after PWM2.

If PWM3 is connected to VCC, two channel operation is selected and the PWM2 pulse terminates 1/2 of a cycle after the PWM1 pulse terminates.

Once a PWM pulse transitions low, it is held low for a minimum of 1/3 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the sawtooth ramp as illustrated in Figure 6. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Current Sampling

During the forced off-time, following a PWM transition low, the current-sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. No matter which current-sense method is employed, the sense current (I_{SEN}) is simply a scaled version of the inductor current. The sample window opens exactly 1/6 of the switching period, t_{SW}, after the PWM transitions low. The sample window then stays open for a fixed amount of time, t_{SAMPLE}, and is equal to 1/6 of the switching period, t_{SW} as illustrated in Figure 3.

$$t_{SAMPLE} = \frac{t_{SW}}{6} = \frac{1}{6 \cdot f_{SW}} \quad \text{(EQ. 3)}$$

The sampled current, at the end of the t_{SAMPLE}, is proportional to the inductor current and is held until the next switching period sample. The sampled current is used for current balance, load-line regulation, and overcurrent protection.

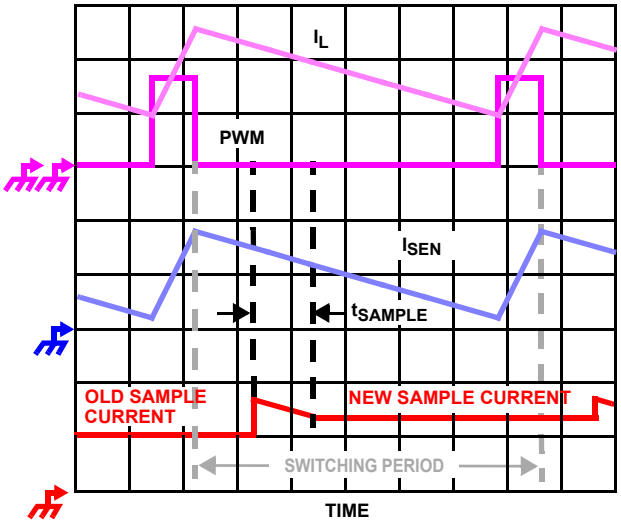


FIGURE 3. SAMPLE AND HOLD TIMING

Current Sensing

The ISL6565A supports MOSFET $r_{DS(ON)}$ current sensing, while the ISL6565B supports inductor DCR current sensing. The internal circuitry, shown in Figures 4 and 5, represent channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on the status of the PWM3 pin, as described in the *PWM Operation* section.

MOSFET $r_{DS(ON)}$ SENSING (ISL6565A ONLY)

The ISL6565A senses the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, as shown in Figure 4. A ground-referenced operational amplifier, internal to the ISL6565A, is connected to the PHASE node through a resistor, R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN pin is proportional to the channel current, I_L. The ISEN current is sampled and held as described in the *Current Sampling* section. From Figure 4, the following equation for I_n is derived where I_L is the channel current.

$$I_n = I_L \frac{r_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 4)}$$

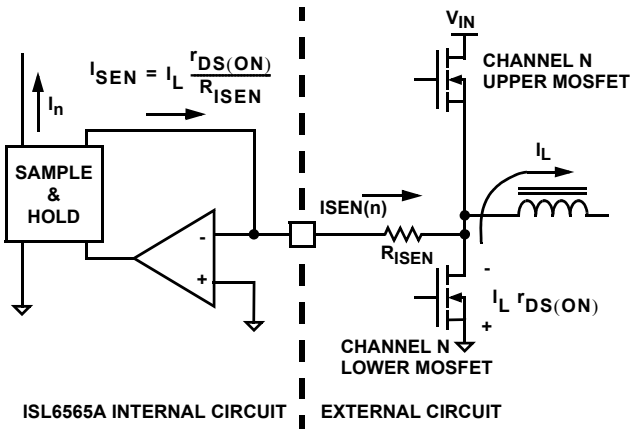


FIGURE 4. ISL6565A INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY

INDUCTOR DCR SENSING (ISL6565B ONLY)

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 5. The channel current I_L, flowing through the inductor, passes through the DCR. Equation 5 shows the s-domain equivalent voltage, V_L, across the inductor.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 5)}$$

A simple R-C network across the inductor (R_1 and C) extracts the DCR voltage, as shown in Figure 5. The voltage across the sense capacitor, V_C, can be shown to be proportional to the channel current I_L, shown in Equation 6.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot R_1 \cdot C + 1)} \cdot DCR \cdot I_L \quad \text{(EQ. 6)}$$

In some cases it may be necessary to use a resistor divider R-C network to sense the current through the inductor. This can be accomplished by placing a second resistor, R_2, across the sense capacitor. In these cases the voltage across the sense capacitor, V_C, becomes proportional to the channel current I_L, and the resistor divider ratio, K.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{\left(s \cdot \frac{(R_1 \cdot R_2)}{R_1 + R_2} \cdot C + 1\right)} \cdot K \cdot DCR \cdot I_L \quad \text{(EQ. 7)}$$

$$K = \frac{R_2}{R_2 + R_1} \quad \text{(EQ. 8)}$$

If the R-C network components are selected such that the RC time constant matches the inductor L/DCR time constant, then V_C is equal to the voltage drop across the DCR multiplied by the ratio of the resistor divider, K. **If a resistor divider is not being used, the value for K is 1**.

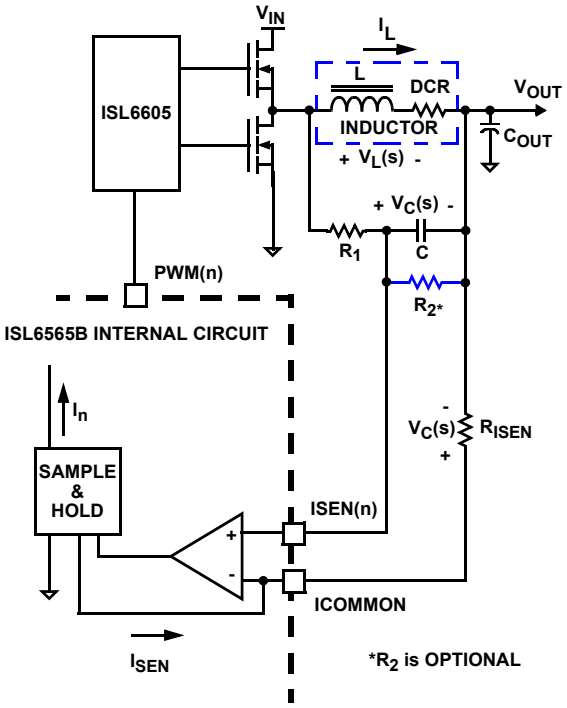


FIGURE 5. DCR SENSING CONFIGURATION

The capacitor voltage V_C, is then replicated across the sense resistor R_{ISEN}. **The regulator should have only one R_{ISEN} resistor connected from the V_{OUT} plane to the ICOMMON pin**. The current through R_{ISEN} is proportional to the inductor current. Equation 9 shows that the proportion between the channel current and the sensed current (I_{SEN}) is driven by the value of the sense resistor chosen, the resistor divider ratio, and the DCR of the inductor.

$$I_n = K \cdot I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 9)}$$

Channel-Current Balance

The sampled currents, I_n, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, I_{AVG}, provides a measure of the total load-current demand on the converter during each switching cycle. Channel-current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 6, with error correction for channel 1 represented. In the figure, the cycle average current combines with the channel 1 sample, I_1, to create an error signal I_{ER}.

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.

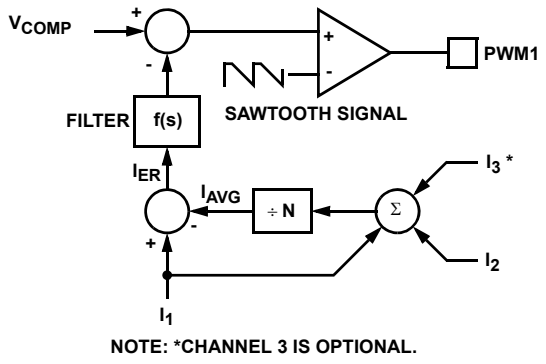


FIGURE 6. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Channel-current balance is essential in realizing the thermal advantage of multi-phase operation. The heat generated in conversion is dissipated over multiple devices and a large area. The designer avoids the complexity of driving multiple parallel MOSFETs, and the expense of using heat sinks and non-standard magnetic materials.

Voltage Regulation

The integrating compensation network shown in Figure 7 insures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6565A, ISL6565B to include the combined tolerances of each of these elements.

The output of the error amplifier, V_{COMP}, is compared to the sawtooth waveform to generate the PWM signals. The PWM signals control the timing of the Intersil MOSFET drivers and regulate the converter output to the specified reference voltage. The internal and external circuitry that controls voltage regulation is illustrated in Figure 7.

The ISL6565 incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The remote-sense output, V_{DIFF}, is connected to the inverting input of the error amplifier through an external resistor.

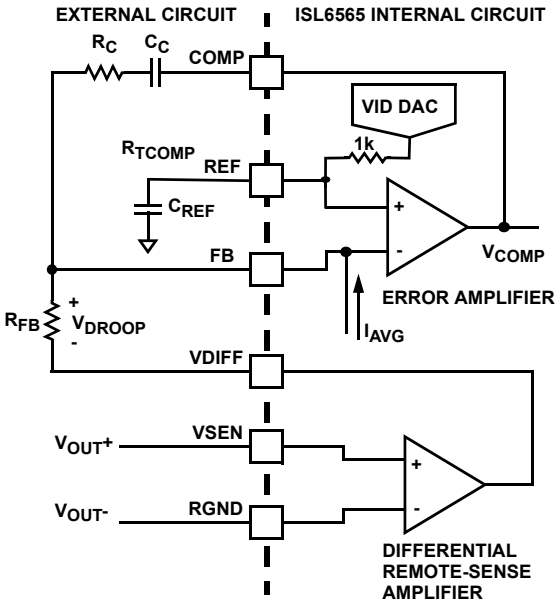


FIGURE 7. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADUJUSTMENT

A digital to analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID4 through VID12.5. The DAC decodes the 6-bit logic signal (VID) into one of the discrete voltages shown in Table 1. Each VID input offers a 20μA pull-up to an internal 2.5V source for use with open-drain outputs. The pull-up current diminishes to zero above the logic threshold to protect voltage-sensitive output devices. External pull-up resistors can augment the pull-up current sources in case leakage into the driving device is greater than 20μA.

TABLE 1. VOLTAGE IDENTIFICATION (VID) CODES

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.8500V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.8750V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.9000V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.9250V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.9500V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V0
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.0000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.0250v
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.0500V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.0750V
0	0	0	0	0	0	1.0875V
1	1	1	1	1	1	OFF
1	1	1	1	1	0	OFF
1	1	1	1	0	1	1.1000V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.1250V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.1500V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.1750V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.2000V
1	1	0	1	0	0	1.2125V
1	1	0	0	1	1	1.2250V
1	1	0	0	1	0	1.2475V
1	1	0	0	0	1	1.2500V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.2750V
1	0	1	1	1	0	1.2875V

TABLE 1. VOLTAGE IDENTIFICATION (VID) CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID12.5	VDAC
1	0	1	1	0	1	1.3000V
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.3250V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.3500V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.3750V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.4000V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.4250V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.4500V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.4750V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.5000V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.5250V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	1	1.5500V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.5750V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.600V

Load-Line Regulation

Some microprocessor manufacturers require a precisely-controlled output impedance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation.

As shown in Figure 7, a current proportional to the average current in all active channels, I_{AVG}, flows from FB through a load-line regulation resistor, R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as:

$$V_{DROOP} = I_{AVG} R_{FB} \quad \text{(EQ. 10)}$$

In most cases, each channel uses the same component values to sense current. If this is the case you can derive a more complete equation for V_{DROOP} for each current sense method being used.

$$V_{DROOP} = \frac{I_{OUT}}{N} \frac{r_{DS(ON)}}{R_{ISEN}} R_{FB} \quad \text{(EQ. 11)}$$

$r_{DS(ON)}$ SENSING (ISL6565A ONLY)

$$V_{DROOP} = \frac{I_{OUT}}{N} \cdot K \cdot \frac{DCR}{R_{ISEN}} R_{FB} \quad \text{(EQ. 12)}$$

DCR SENSING (ISL6565B ONLY)

Output-Voltage Offset Programming

The ISL6565A, ISL6565B allows the designer to accurately adjust the offset voltage by connecting a resistor, R_{OFS}, from the OFS pin to VCC or GND. When R_{OFS} is connected between OFS and VCC, the voltage across it is regulated to 2.0V. This causes a proportional current (I_{OFS}) to flow into the OFS pin and out of the FB pin. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.5V, and I_{OFS} flows into the FB pin and out of the OFS pin. The offset current flowing through the resistor between VDIFF and FB will generate the desired offset voltage which is equal to the product (I_{OFS} x R_{FB}). These functions are shown in Figures 8 and 9.

Once the desired output offset voltage has been determined, use the following formulas to set R_{OFS}:

For Positive Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.5 \times R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 13)}$$

For Negative Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{2 \times R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 14)}$$

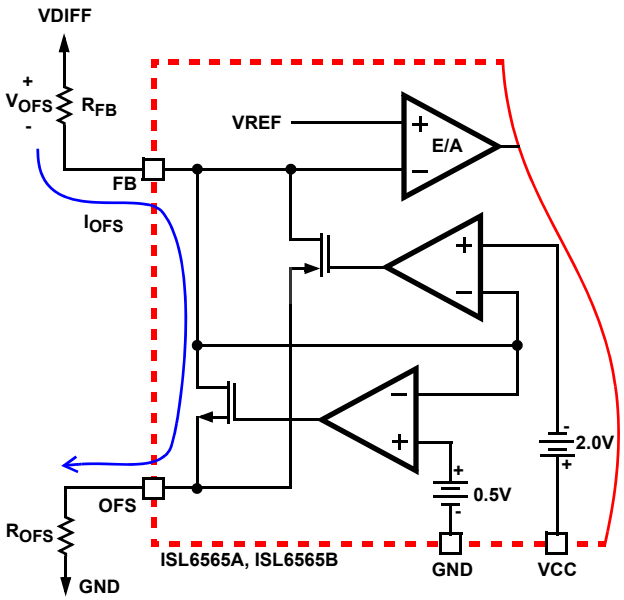


FIGURE 8. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

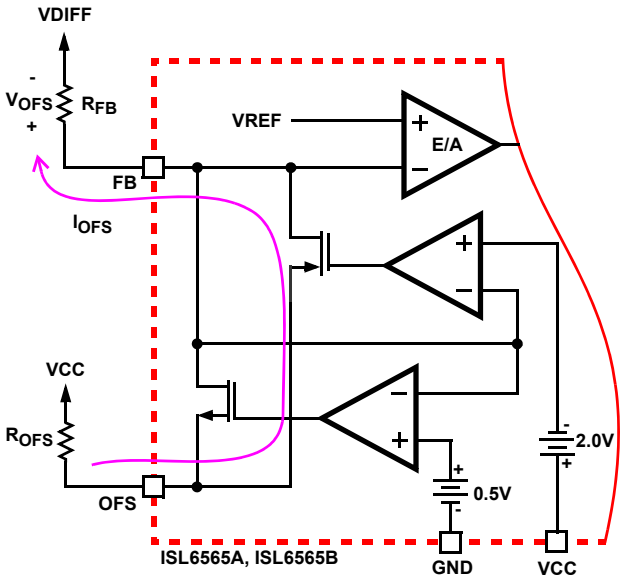


FIGURE 9. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the core-voltage regulator to do this by making changes to the VID inputs. The core-voltage regulator is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner supervising a safe output voltage transition without discontinuity or disruption.

The ISL6565A, ISL6565B checks the VID inputs six times every switching cycle. If the VID code is found to have changed, the controller waits half of a complete cycle before executing a 12.5mV change. If during the half-cycle wait period, the difference between the DAC level and the new VID code changes sign, no change is made. If the VID code is more than 1 bit higher or lower than the DAC (not recommended), the controller will execute 12.5mV changes six times per cycle until VID and DAC are equal. It is important to carefully control the rate of VID stepping in 1-bit increments.

In order to ensure the smooth transition of output voltage during VID change, a VID step change smoothing network is required for an ISL6565A, ISL6565B based voltage regulator. This network is composed of a 1kΩ internal resistor between the output of DAC and the capacitor C_{REF}, between the REF pin and ground. The selection of C_{REF} is based on the time duration for 1 bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1 bit every T_{VID}, the relationship between C_{REF} and T_{VID} is given by Equation 15.

$$C_{REF} = 0.004 X T_{VID} \quad \text{(EQ. 15)}$$

As an example, for a VID step change rate of 5µs per bit, the value of C_{REF} is 22nF based on Equation 15.

Temperature Compensation

MOSFET $r_{DS(ON)}$ and inductor DCR are both susceptible to changes in value due to temperature. Since output voltage positioning is derived from the channel current sensed across these two elements, any variation in resistance results in a corresponding error in the output voltage.

The temperature coefficient, α, of the $r_{DS(ON)}$ or DCR is the parameter that determines how much the resistance varies with temperature. As temperature increases above ambient, the average sensed current, I_{AVG}, changes in proportion to the temperature coefficient and temperature rise as shown in Equation 16.

$$I_{AVG} = I_{AVG(T_{AMBIENT})} \cdot [1 + \alpha(T - T_{AMBIENT})] \quad \text{(EQ. 16)}$$

With this resulting error, I_{AVG} can now be described as the sum of two parts, the average sensed current at ambient temperature and the resulting error current, I_{ERR}, due to the temperature rise.

$$I_{ERR(T)} = I_{AVG(T_{AMBIENT})} \cdot \alpha \cdot (T - T_{AMBIENT}) \quad \text{(EQ. 17)}$$

In order to compensate for this error current, the ISL6565A, ISL6565B includes a temperature compensation circuit that injects a current, I_{TCOMP}, into the FB pin. This current is created by pushing the average sense current through a selectable external resistor, R_{TCOMP}.

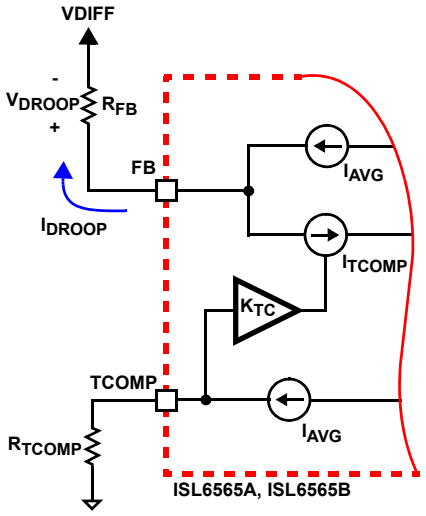


FIGURE 10. TEMPERATURE COMPENSATION CIRCUITRY

As shown in Figure 10, the voltage drop developed across R_{TCOMP} is then sensed and multiplied by a known gain, K_{TC}, which is determined by the internal IC temperature. This gain creates the temperature compensation current, I_{TCOMP}, that is injected into the FB pin.

$$I_{TCOMP} = K_{TC} \cdot (T - 25) \cdot I_{AVG} \cdot R_{TCOMP} \quad \text{(EQ. 18)}$$

Select R_{TCOMP} such that I_{TCOMP} equals I_{ERR} over the entire range of operating temperature. The resulting droop current accurately represents the load current; achieving a linear, temperature-independant load line.

Initialization

Prior to initialization, proper conditions must exist on the enable inputs and VCC. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts PGOOD.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state to assure the drivers remain off. The following input conditions must be met before the ISL6565A, ISL6565B is released from shutdown mode.

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6565A, ISL6565B is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6565A, ISL6565B will not inadvertently turn off unless the bias voltage drops substantially (see *Electrical Specifications*).

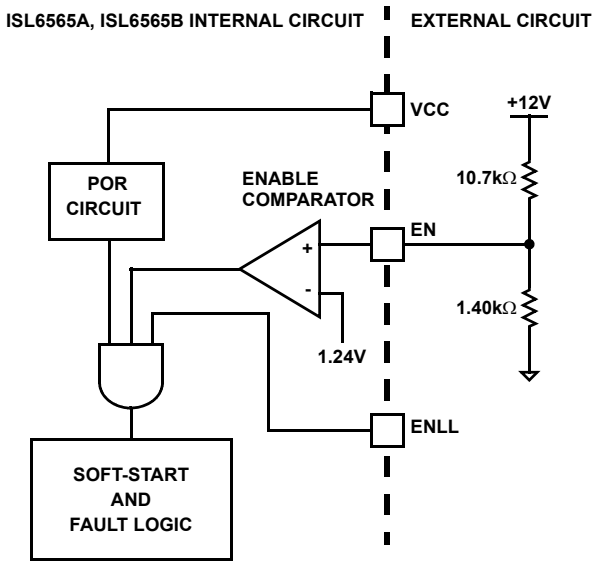


FIGURE 11. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

2. The voltage on EN must be above 1.31V. The EN input allows for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6565A, ISL6565B in shutdown until the voltage at EN rises above 1.31V. The enable comparator has about 100mV of hysteresis to prevent bounce. It is important that the driver ICs reach their POR level before the ISL6565A, ISL6565B becomes enabled. The schematic in Figure 11 demonstrates sequencing the ISL6565A, ISL6565B with the HIP660X family of Intersil MOSFET drivers, which require 12V bias.
3. The voltage on ENLL must be logic high to enable the controller. This pin is typically connected to the VID_PGOOD.
4. The VID code must not be 111111 or 111110. These codes signal the controller that no load is present. The controller will enter shut-down mode after receiving either of these codes and will execute soft-start upon receiving any other code. These codes can be used to enable or disable the controller but it is not recommended. After receiving one of these codes, the controller executes a 2-cycle delay before changing the overvoltage trip level to the shut-down level and disabling PWM. Overvoltage shutdown cannot be reset using one of these codes.

When each of these conditions is true, the controller immediately begins the soft-start sequence.

Soft-Start

During soft-start, the DAC voltage ramps linearly from zero to the programmed VID level. The PWM signals remain in the high-impedance state until the controller detects that the ramping DAC level has reached the output-voltage level. This protects the system against the large, negative inductor currents that would otherwise occur when starting with a pre-existing charge on the output as the controller attempted to regulate to 0V at the beginning of the soft-start cycle. The soft-start time, t_{SS}, begins with a delay period equal to 64 switching cycles followed by a linear ramp with a rate determined by the switching period, $1/f_{SW}$.

$$t_{SS} = \frac{64 + 1280 \cdot VID}{f_{SW}} \quad \text{(EQ. 19)}$$

For example, a regulator with a 250kHz switching frequency, having VID set to 1.35V, has t_{SS} equal to 6.912ms.

A 100mV offset exists on the remote-sense amplifier at the beginning of soft-start and ramps to zero during the first 640 cycles of soft-start (704 cycles following enable). This prevents the large inrush current that would otherwise occur should the output voltage start out with a slight negative bias.

During the first 640 cycles of soft-start (704 cycles following enable) the DAC voltage increments the reference in 25mV steps. The remainder of soft-start sees the DAC ramping with 12.5mV steps.

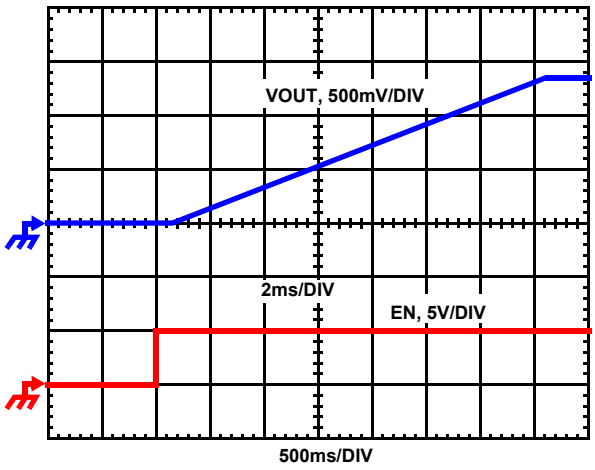


FIGURE 12. SOFT-START WAVEFORMS WITH AN UN-BIASED OUTPUT. FSW = 500kHz

Fault Monitoring and Protection

The ISL6565A, ISL6565B actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 13 outlines the interaction between the fault monitors and the power good signal.

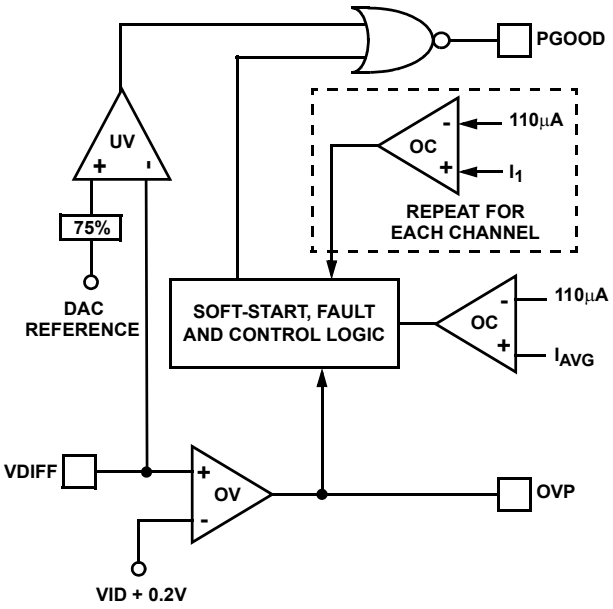


FIGURE 13. POWER GOOD AND PROTECTION CIRCUITRY

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output that transitions high when the converter is operating after soft-start. PGOOD pulls low during shutdown and releases high after a successful soft-start. PGOOD only transitions low when an undervoltage condition is detected or the controller is disabled by a reset from EN, ENLL, POR, or one of the no-CPU VID codes. After an undervoltage event, PGOOD will return high unless the controller has been disabled. PGOOD does not automatically transition low upon detection of an overvoltage condition.

Undervoltage Detection

The undervoltage threshold is set at 75% of the VID code. When the output voltage at VSEN is below the undervoltage threshold, PGOOD gets pulled low. No other action is taken by the controller.

Overvoltage Protection

When VCC is above 1.4V, but otherwise not valid as defined under **Power on Reset** in *Electrical Specifications*, the overvoltage trip circuit is active using auxiliary circuitry. In this state, an overvoltage trip occurs if the voltage at VSEN exceeds 1.8V.

With valid VCC, the overvoltage circuit is sensitive to the voltage at VDIFF. In this state, the trip level is 1.7V prior to valid enable conditions being met as described in *Enable and Disable*. The only exception to this is when the IC has been disabled by an overvoltage trip. In that case the overvoltage trip point is VID plus 200mV. During soft-start, the overvoltage trip level is the higher of 1.7V or VID plus 200mV. Upon successful soft-start, the overvoltage trip level is 200mV above VID. Two actions are taken by the ISL6565A, ISL6565B to protect the microprocessor load when an overvoltage condition occurs.

At the inception of an overvoltage event, all PWM outputs are commanded low until the voltage at VSEN falls below 0.6V with valid VCC or 1.5V otherwise. This causes the Intersil drivers to turn on the lower MOSFETs and pull the output voltage below a level that might cause damage to the load. The PWM outputs remain low until VDIFF falls to the programmed DAC level at which time they enter a high-impedance state. The Intersil drivers respond to the high-impedance input by turning off both upper and lower MOSFETs. If the overvoltage condition reoccurs, the ISL6565A, ISL6565B will again command the lower MOSFETs to turn on. The ISL6565A, ISL6565B will continue to protect the load in this fashion as long as the overvoltage condition recurs.

Simultaneous to the protective action of the PWM outputs, the OVP pin pulls to VCC delivering up to 100mA to the gate of a crowbar MOSFET or SCR placed either on the input rail or the output rail. Turning on the MOSFET or SCR collapses the power rail and causes a fuse placed further up stream to blow. The fuse must be sized such that the MOSFET or SCR will not overheat before the fuse blows. The OVP pin is tolerant to 12V (see *Absolute Maximum Ratings*), so an external resistor pull up can be used to augment the driving capability. If using a pull up resistor in conjunction with the internal overvoltage protection function, care must be taken to avoid nuisance trips that could occur when VCC is below 2V. In that case, the controller is incapable of holding OVP low.

Once an overvoltage condition is detected, normal PWM operation ceases until the ISL6565A, ISL6565B is reset. Cycling the voltage on EN, ENLL, or VCC below the POR-falling threshold will reset the controller. Cycling the VID codes will not reset the controller.

Overcurrent Protection

ISL6565A, ISL6565B has two levels of overcurrent protection. Each phase is protected from a sustained overcurrent condition on a delayed basis, while the combined phase currents are protected on an instantaneous basis.

In instantaneous protection mode, the ISL6565A, ISL6565B takes advantage of the proportionality between the load current and the average current, I_{AVG}, to detect an overcurrent condition. See the *Channel-Current Balance* section for more detail on how the average current is measured. The average current is continually compared with a constant 110μA reference current as shown in Figure 6. Once the average current exceeds the reference current, a comparator triggers the converter to shutdown.

In individual overcurrent protection mode, the ISL6565A, ISL6565B continuously compares the current of each channel with the same 110μA reference current. If any channel current exceeds the reference current continuously for eight

consecutive cycles, the comparator triggers the converter to shutdown.

At the beginning of overcurrent shutdown, the controller places all PWM signals in a high-impedance state commanding the Intersil MOSFET driver ICs to turn off both upper and lower MOSFETs. The system remains in this state for a period of 4096 switching cycles. If the controller is still enabled at the end of this wait period, it will attempt a soft-start (as shown in Figure 14). If the fault remains, the trip-retry cycles will continue indefinitely until either the controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard.

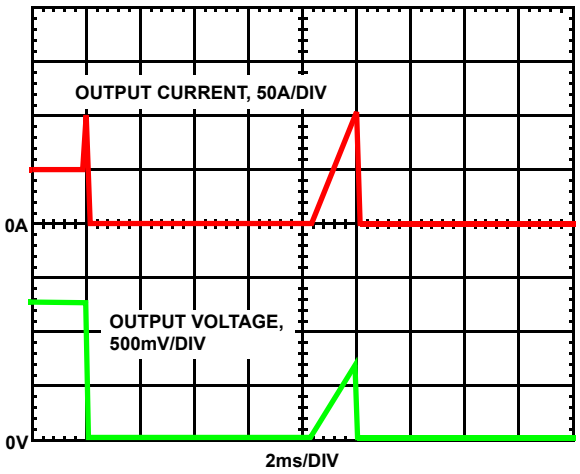


FIGURE 14. OVERCURRENT BEHAVIOR IN HICCUP MODE F_{SW} = 500kHz

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which each phase handles between 25A and 30A. All surface-mount designs will tend toward the lower end of this current range.

If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETS

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for power loss in the lower MOSFET is simple, since virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 20, I_M is the maximum continuous output current, I_{PP} is the peak-to-peak inductor current (see Equation 1), and d is the duty cycle (V_{OUT}/V_{IN}).

$$P_{LOW,1} = r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2(1-d) + \frac{I_{L,PP}^2(1-d)}{12}\right] \quad \text{(EQ. 20)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$, the switching frequency, f_S, and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} f_S\left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right) t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right) t_{d2}\right] \quad \text{(EQ. 21)}$$

The total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times, the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 22,

the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{PP}}{2}\right)\left(\frac{t_1}{2}\right)f_S \quad \text{(EQ. 22)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 23, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{PP}}{2}\right)\left(\frac{t_2}{2}\right)f_S \quad \text{(EQ. 23)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET's body diode can recover all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP,3}$.

$$P_{UP,3} = V_{IN} Q_{rr} f_S \quad \text{(EQ. 24)}$$

Finally, the resistive part of the upper MOSFETs is given in Equation 25 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 d + \frac{I_{PP}^2}{12}\right] \quad \text{(EQ. 25)}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 22, 23, 24 and 25. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Current Sensing Component Selection

The ISL6565A supports MOSFET $r_{DS(ON)}$ current sensing, while the ISL6565B uses inductor DCR current sensing. The procedures for choosing the components for each method of current sensing are very different and are described in the next two sections.

MOSFET $r_{DS(ON)}$ SENSING (ISL6565A ONLY)

The ISL6565A senses the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, as shown in Figure 15. The ISEN pins are denoted ISEN1, ISEN2, and ISEN3. The resistors connected between these pins and the respective phase nodes determine the gains in the load-line regulation loop and the channel-current balance loop as well as setting the overcurrent trip point.

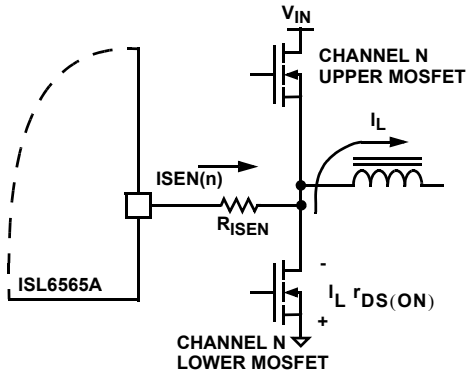


FIGURE 15. ISL6565A INTERNAL AND EXTERNAL CURRENT-SENSING CIRCUITRY

Select values for these resistors based on the room temperature $r_{DS(ON)}$ of the lower MOSFETs; the full-load operating current, I_{FL}; and the number of phases, N using Equation 26.

$$R_{ISEN} = \frac{r_{DS(ON)}}{70 \times 10^{-6}} \frac{I_{FL}}{N} \quad \text{(EQ. 26)}$$

In certain circumstances, it may be necessary to adjust the value of one or more ISEN resistor. When the components of one or more channels are inhibited from effectively dissipating their heat so that the affected channels run hotter than desired, choose new, smaller values of R_{ISEN} for the affected phases (see the section entitled *Voltage Regulation*). Choose $R_{ISEN,2}$ in proportion to the desired decrease in temperature rise in order to cause proportionally less current to flow in the hotter phase.

$$R_{ISEN,2} = R_{ISEN} \frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 27)}$$

In Equation 27, make sure that ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. While a single adjustment according to Equation 27 is usually sufficient, it may occasionally be necessary to adjust R_{ISEN} two or more times to achieve optimal thermal balance between all channels.

INDUCTOR DCR SENSING (ISL6565B ONLY)

The ISL6565B senses the channel load current by sampling the voltage across the output inductor DCR, as described in the *Current Sensing* section. As Figure 16 illustrates, an R-C network across the inductor is required to sense the channel current accurately.

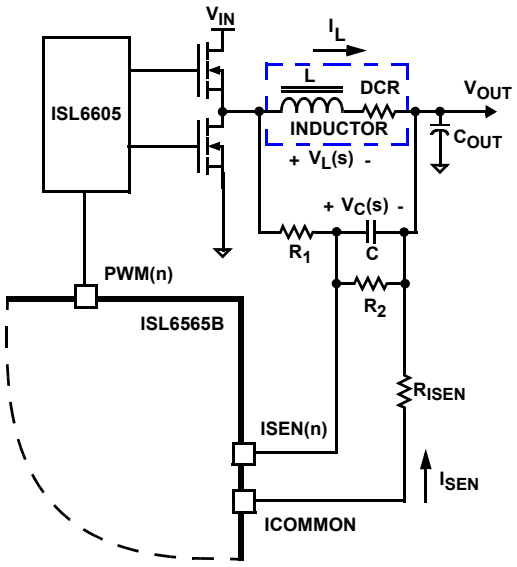


FIGURE 16. DCR SENSING CONFIGURATION

The time constant of this R-C network must match the time constant of the inductor L/DCR. Follow the steps below to choose the component values for this R-C network.

1. Choose an arbitrary value for C. The recommended value is 0.01µF.
2. Plug the Inductor L and DCR component values, and the values for C chosen in steps 1, into Equation 28 to calculate your value for R_1. Do not populate R_2.

$$R_1 = \frac{L}{DCR \cdot C} \quad \text{(EQ. 28)}$$

Due to errors in the inductance or DCR it may be necessary to adjust the value of R_1 for each phase to match the time constants correctly.

Once the R-C network components have been chosen, use Equation 29 to calculate the value of R_{ISEN}. In Equation 29, DCR is the DCR of the output inductor at room temperature, I_{FL} is the full load operating current, and N is the number of phases.

$$R_{ISEN} = \frac{DCR \cdot I_{FL}}{70 \times 10^{-6} \cdot N} \quad \text{(EQ. 29)}$$

Adjusting Phase Currents (ISL6565B Only)

Layout issues in the core-power regulator may cause the currents in each phase to be slightly unbalanced. This problem can be resolved without any changes to the layout or any significant cost increase. The solution requires populating R_2 in certain phases (as shown in Figure 16) to create a resistor divider ratio, K, for each phase. The time constant of each new resistor divider R-C sense network must match the time constant of the old sense network. Follow the steps below to choose the component values for the resistor divider R-C network for each phase.

1. Load the regulator to full load and allow the board to heat until the output voltage stabilizes (usually several minutes).
2. Measure the current flowing through each phase, labeling the highest phase current, I_{HIGH}, and the other, lower phase currents $I_{LOW}(1)$ and $I_{LOW}(2)$.
3. Individually, plug the values for each low phase current, $I_{LOW}(n)$, the highest phase current, I_{HIGH}, the full load current, I_{LOAD}, and the number of phases, N, into Equation 30 to calculate the resistor divider ratio, K_{LOW}, for each low phase. (NOTE: The phase with the highest phase current is the reference phase and it will not use a resistor divider network, keeping its resistor divider ratio equal to 1.)

$$K_{LOW}(n) = 1 + \frac{I_{LOW}(n) - I_{HIGH}}{I_{LOAD}/N} \quad \text{(EQ. 30)}$$

4. For each phase, calculate the values for the new R-C network sense resistors, $R_{1,new}$ and $R_{2,new}$, by plugging in each phase's new resistor divider ratio, K_{LOW}, and each phase's present sense resistor R_1, into Equations 31 and 32.

$$R_{1,new}(n) = \frac{R_1(n)}{K_{LOW}(n)} \quad \text{(EQ. 31)}$$

$$R_{2,new}(n) = \frac{R_1(n)}{1 - K_{LOW}(n)} \quad \text{(EQ. 32)}$$

After calculating the new resistor divider sense resistors, the phases will be balanced. It may be necessary to adjust the R_{ISEN} resistor slightly to correct for any changes in the desired I_{SEN} current that results from adding the resistor dividers.

The phase currents might also have to be adjusted if the components of one or more phases are inhibited from effectively dissipating their heat so that the affected phases run hotter than desired. In this case it may be necessary to adjust the resistor divider ratio of one or more of the R-C networks. Doing so adjusts the current through affected phases and can balance the temperatures of each phase. Choose $R_{1,new}$ and $R_{2,new}$ in relation to the desired change in temperature, as described in Equations 33 and 34, in order to cause less current to flow in the hotter phase.

$$R_{1,new} = R_1 \frac{\Delta T_2}{\Delta T_1} \quad \text{(EQ. 33)}$$

$$R_{2,new} = \frac{R_1 \cdot R_2}{R_1 + R_2 \cdot \left(1 - \frac{\Delta T_1}{\Delta T_2}\right)} \quad \text{(EQ. 34)}$$

In Equations 33 and 34, ΔT_2 is the desired temperature rise above the ambient temperature, and ΔT_1 is the measured temperature rise above the ambient temperature. It is

important to note that when using Equations 33 and 34 the resistor divider ratio of the corresponding phase RC network is being changed. In the phase being adjusted, this new ratio, K_{new} (described in Equation 35), can not exceed 1.0.

$$K_{new} = K\frac{\Delta T_1}{\Delta T_2} \quad \text{(EQ. 35)}$$

If this occurs, the current in the hot phase cannot be reduced any more. Instead of decreasing the current in the hot phase, the current must be increased in the colder phases. To accomplish this, use Equations 33 and 34 to get the desired temperature rise in the cold phases.

While a single adjustment, according to Equations 33 and 34, is usually sufficient, it may occasionally be necessary to adjust R_1 and R_2 in the corresponding channels two or more times to achieve optimal thermal balance between all phases.

Load-Line Regulation Resistor

The load-line regulation resistor is labeled R_{FB} in Figure 7. Its value depends on the desired full-load droop voltage (V_{DROOP} in Figure 7). Once the ISEN resistor has been chosen, the load-line regulation resistor can be calculated using Equation 36.

$$R_{FB} = \frac{V_{DROOP}}{70 \times 10^{-6}} \quad \text{(EQ. 36)}$$

If one or more of the ISEN resistors is adjusted for thermal balance, as in Equation 26, the load-line regulation resistor should be selected according to Equation 37 where I_{FL} is the full-load operating current and $R_{ISEN(n)}$ is the ISEN resistor connected to the n^{th} ISEN pin.

$$R_{FB} = \frac{V_{DROOP}}{I_{FL}\, r_{DS(ON)}} \sum_n R_{ISEN(n)} \quad \text{(EQ. 37)}$$

Temperature Compensation Resistor

By combining Equations 17 and 18 found in the *Temperature Compensation* section, the value of the TCOMP resistor can be determined using Equation 38.

$$R_{TCOMP} = \frac{\alpha}{K_T K_{TC}} \quad \text{(EQ. 38)}$$

In Equation 38, K_T is the temperature coupling coefficient between the ISL6565A and the closest lower MOSFET, or the ISL6565B and the output inductor. It represents how closely the controller temperature tracks the lower MOSFET or inductor temperature. The value of K_T is typically between 75% and 100%. K_{TC} is the temperature dependant transconductance of the internal compensation circuit. Its value is designed as 2µA/V/°C. The temperature coefficient of MOSFET $r_{DS(ON)}$ or inductor DCR is given by α. This is the ratio of the change in resistance to the change in temperature. Resistance is normalized to the value at 25°C and the value of α is typically between 0.35%/°C and 0.50%/°C.

According to Equation 38, a voltage regulator with 80% thermal coupling coefficient between the controller and lower MOSFET and 0.4%/°C temperature coefficient of MOSFET $r_{DS(ON)}$ requires a 2.5kΩ TCOMP resistor.

If the exact value for K_T and α are not known, Equation 38 can give an incorrect value for R_{TCOMP}. If this is the case, follow the steps below to obtain an accurate value for R_{TCOMP}. This procedure works by making two output voltage measurements. The first is made by using too much temperature compensation, and the second with too little. Each of the measurements produces an error and a linear interpolation is used to find a TCOMP resistor value to produce zero error. Make all measurements using a digital multimeter accurate to 100µV or better.

1. Install a 5kΩ resistor (R_1) for R_{TCOMP}.
2. Start the regulator at room temperature and apply full load current. Record the output voltage, V_1, immediately after loading the regulator.
3. Allow the board to heat until the output voltage stabilizes (usually several minutes). Record the output voltage, V_2.
4. Install a 1kΩ resistor (R_2) for R_{TCOMP}.
5. Start the regulator at room temperature and apply full load current. Record the output voltage, V_3, immediately after loading the regulator.
6. Allow the board to heat until the output voltage stabilizes (usually several minutes). Record the output voltage, V_4.
7. Calculate the correct value for R_{TCOMP} using Equation 39.

$$R_{TCOMP} = R_1 - (R_1 - R_2)\frac{(V_2 - V_1)}{(V_2 - V_1) + (V_3 - V_4)} \quad \text{(EQ. 39)}$$

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed.

The load-line regulated converter behaves in a similar manner to a peak-current mode controller because the two poles at the output-filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

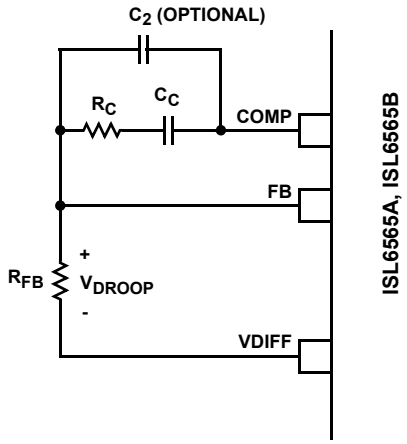


FIGURE 17. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6565A, ISL6565B CIRCUIT

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately, there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator, by compensating the L-C poles and the ESR zero of the voltage-mode approximation, yields a solution that is always stable with very close to ideal transient performance.

Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

Case 1:
$$\frac{1}{2\pi\sqrt{LC}} > f_0$$
$$R_C = R_{FB}\frac{2\pi f_0 V_{pp}\sqrt{LC}}{0.75V_{IN}}$$
$$C_C = \frac{0.75V_{IN}}{2\pi V_{PP}R_{FB}f_0}$$

Case 2:
$$\frac{1}{2\pi\sqrt{LC}} \le f_0 < \frac{1}{2\pi C(ESR)}$$
$$R_C = R_{FB}\frac{V_{PP}(2\pi)^2 f_0^2 LC}{0.75\,V_{IN}} \qquad \text{(EQ. 40)}$$
$$C_C = \frac{0.75V_{IN}}{(2\pi)^2 f_0^2 V_{PP}R_{FB}\sqrt{LC}}$$

Case 3:
$$f_0 > \frac{1}{2\pi C(ESR)}$$
$$R_C = R_{FB}\frac{2\pi f_0 V_{pp}L}{0.75\,V_{IN}(ESR)}$$
$$C_C = \frac{0.75V_{IN}(ESR)\sqrt{C}}{2\pi V_{PP}R_{FB}f_0\sqrt{L}}$$

In Equation 40, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in Figure 6 and *Electrical Specifications*.

Once selected, the compensation values in Equation 40 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from Equation 40 unless some performance issue is noted.

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 17). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading-edge jitter problem is noted.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must

have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 41)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see *Interleaving* and Equation 2), a voltage develops across the bulk-capacitor ESR equal to $I_{C,PP}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq (ESR)\frac{\left(V_{IN} - NV_{OUT}\right)V_{OUT}}{f_S V_{IN} V_{PP(MAX)}} \quad \text{(EQ. 42)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 43 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 44 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2NCV_O}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right] \quad \text{(EQ. 43)}$$

$$L \leq \frac{(1.25)NC}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I(ESR)\right]\left(V_{IN} - V_O\right) \quad \text{(EQ. 44)}$$

Input Supply Voltage Selection

The VCC input of the ISL6565 can be connected either directly to a +5V supply or through a current limiting resistor to a +12V supply. An integrated 5.8V shunt regulator maintains the voltage on the VCC pin when a +12V supply is used. A 300Ω resistor is suggested for limiting the current into the VCC pin to a worst-case maximum of approximately 25mA.

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper-MOSFET loss calculation. These effects are outlined in *MOSFETs*, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in *Output Filter Design*. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T (see the figures labeled *Typical Application* on pages 5 and 6). Figure 18 and Equation 45 are provided to assist in selecting the correct value for R_T.

$$R_T = 10^{[10.7 - 1.045\log(f_S)]} \quad \text{(EQ. 45)}$$

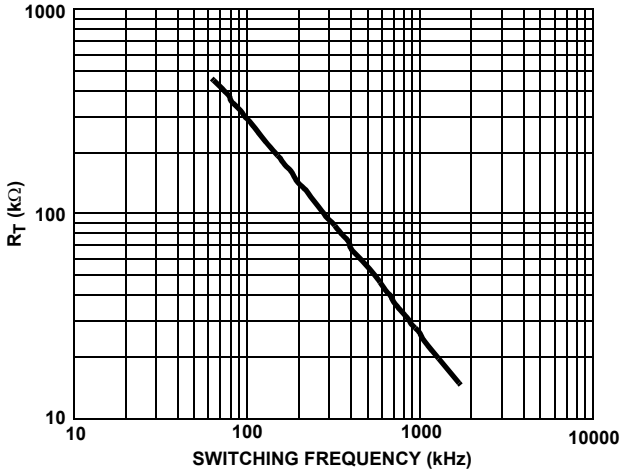


FIGURE 18. R_T vs SWITCHING FREQUENCY

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

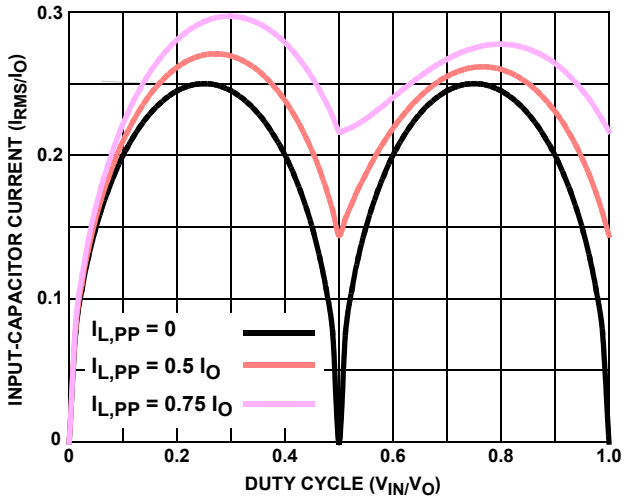


FIGURE 19. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 2-PHASE CONVERTER

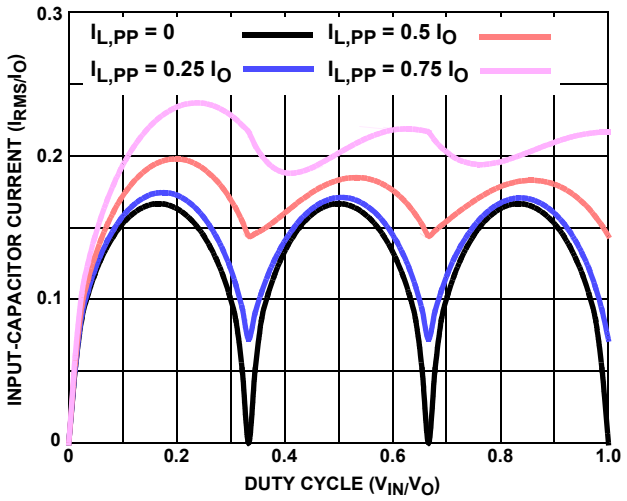
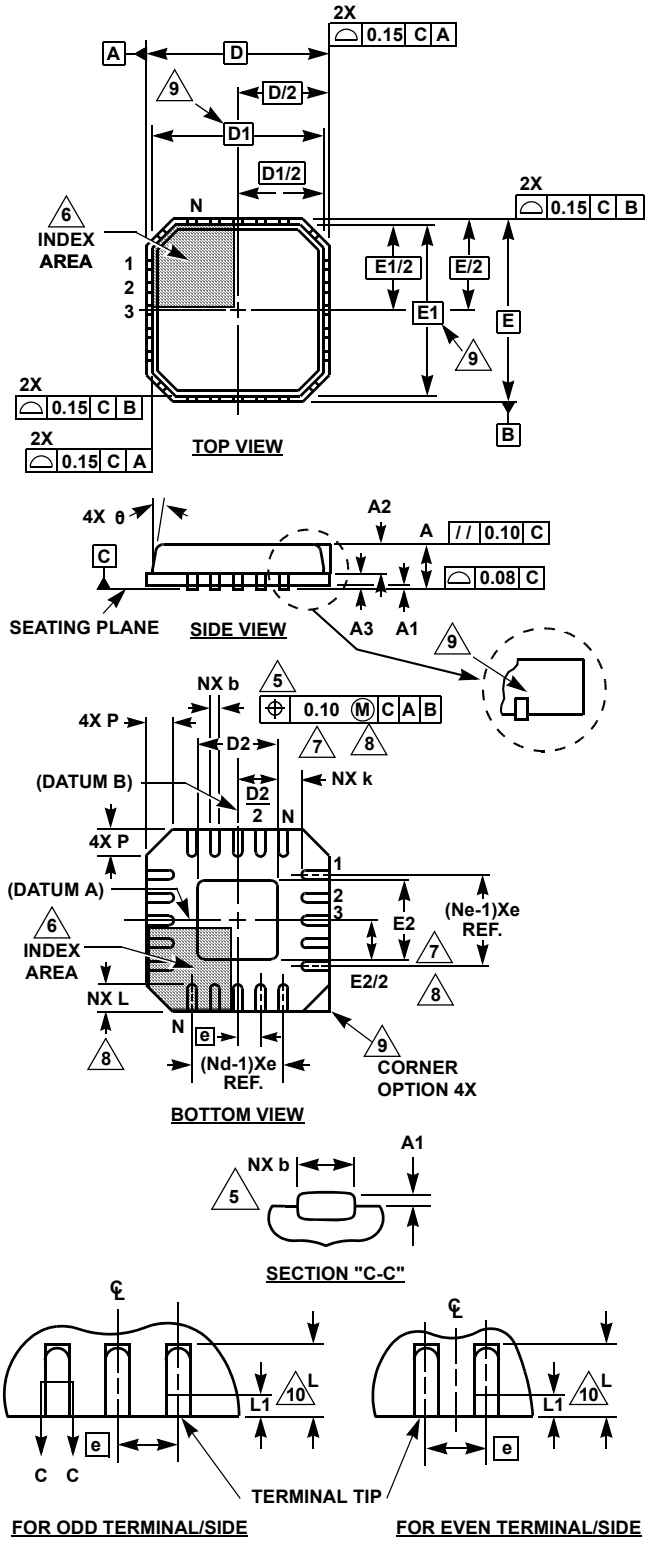


FIGURE 20. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

For a two-phase design, use Figure 19 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage. Figure 20 provides the same input RMS current information for three phase designs respectively. Use the same approach for selecting the bulk capacitor type and number.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L28.5x5

28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		28		2
Nd		7		3
Ne	8	7		3
P	-	-	0.60	9
θ	-	-	12	9

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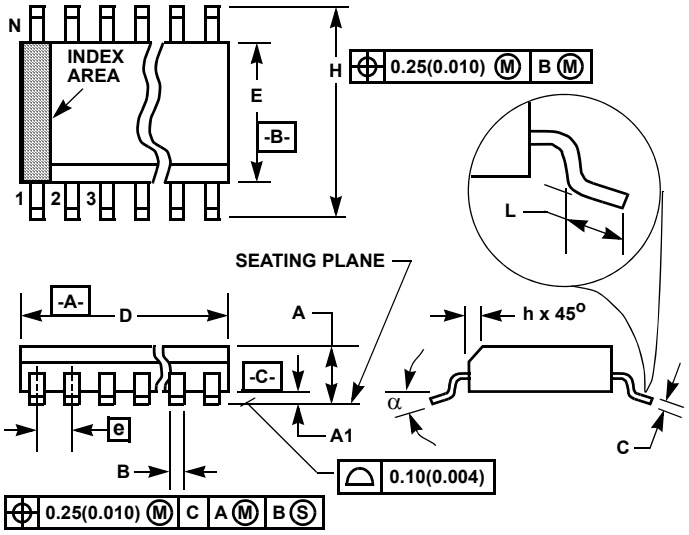
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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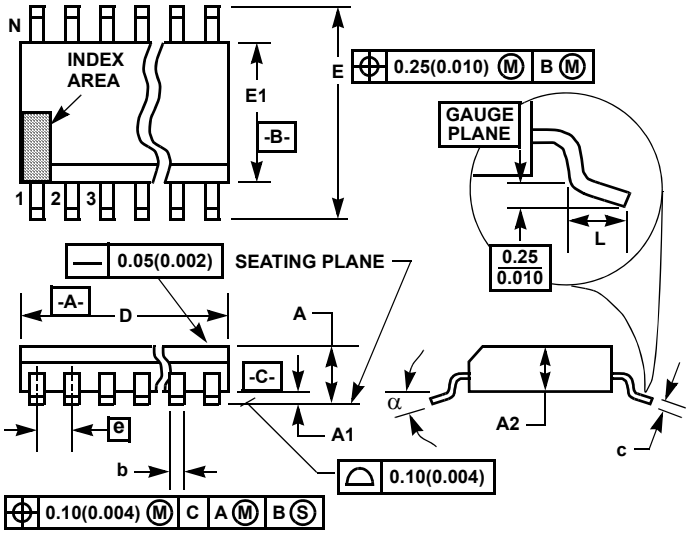
Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AE, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M28.173

28 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.378	0.386	9.60	9.80	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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