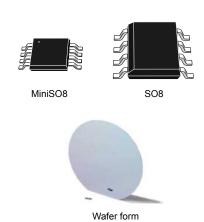


### Low-power dual operational amplifier



#### **Features**

- Frequency compensation implemented internally
- · Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain: 1.1 MHz temperature compensated)
- Very low-supply current per operator (500 μA)
- Low input bias current: 20 nA (temperature compensated)
- Low input offset current: 2 nA
- · Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to VCC 1.5 V
- · Internal ESD protection: 2 kV HBM, 200 V MM

#### **Description**

This circuit consists of two independent, high-gain, operational amplifiers that have frequency compensation implemented internally. The circuit is designed specifically for automotive and industrial control systems. It operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks, and all the conventional op-amp circuits which can now be more easily implemented in single-power supply systems. For example, these circuits can be directly supplied from standard 5 V which is used in logic systems and which easily provides the required interface electronics without requiring any additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground even though it is operated from a single-power supply.



# 1 Schematic diagram and pad locations

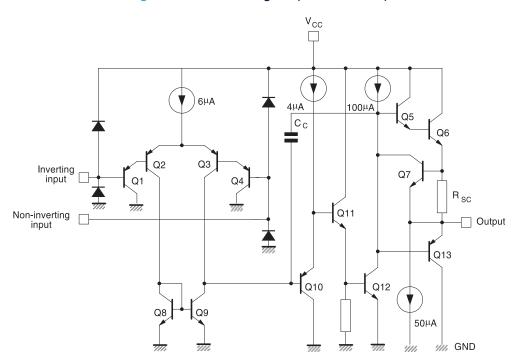
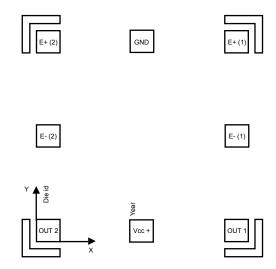


Figure 1. Schematic diagram (1/2 LM2904WH)

Figure 2. Pad locations



The origin coordinate is at the bottom left part of the OUT2 pin. All dimensions are specified in micrometers (µm).

DS3549 - Rev 9 page 2/14



**Table 1. Pad locations** 

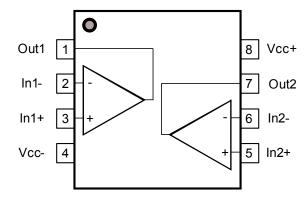
Name	Pad placement		Pad dim	ensions
Name	X	Y	x	Y
GND	480	1040		
E+1	940	1030		
E-1	1010	620	102 10	102
OUT1	910	55		
Vcc +	480	70		102
OUT2	55	55		
E-2	-30	620		
E+2	-30	1030		

DS3549 - Rev 9 page 3/14



# Package pin connections

Figure 3. MiniSO8 and SO8 package pin connections (top view)



DS3549 - Rev 9 page 4/14



### Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Parameter		
V <sub>CC</sub> +	Supply voltage	32		
V <sub>id</sub>	Differential input voltage		-0.3 to VCC + 0.3	V
V <sub>in</sub>	Input voltage		-0.3 to VCC + 0.3	
l <sub>in</sub>	Input current (1)		5	mA
	Output short-circuit to ground (2)		40	MA
T <sub>stg</sub>	Storage temperature range	Storage temperature range		
Tj	Maximum junction temperature	Maximum junction temperature		
R <sub>thja</sub> (3)	Thermal resistance junction to ambient	SO8	125	
ixnja	Thermal resistance junction to ambient	MiniSO8	190	°C/W
R <sub>thic</sub> (3)	Thormal resistance junction to case	SO8	40	C/VV
Tthjc **	Thermal resistance junction to case  MiniSO8		39	
	HBM: human body model (4)	2	kV	
ESD	MM: machine model (5)	200	V	
	CDM: charged device model (6)	1.5	kV	

- This input current only exists when the voltage value applied on the inputs is beyond the supply voltage line limits. This is not destructive if the current does not exceed 5 mA as indicated, and normal output is restored for input voltages above -0.3 V.
- Short-circuits from the output to VCC can cause excessive heating if VCC+ is < 15 V. The maximum output current is approximately 40 mA, independent of the magnitude of VCC. Destructive dissipation can result from simultaneous shortcircuits on all amplifiers
- 3. Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
- 4. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
- 6. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

**Table 3. Operating conditions** 

Symbol	Parameter	Value	Unit	
VCC+	Supply voltage	3 to 30		
			0 to (VCC+) - 1.5	V
Vicm	Input common-mode input voltage range (VCC+ = 30 V) (1)	Tmin ≤ Tamb ≤ Tmax	0 to (VCC+) - 2	
Toper	Operating free-air temperature range	-40 to 150	°C	

1. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is (VCC+) – 1.5 V, but either or both inputs can go to 32 V without damage.

DS3549 - Rev 9 page 5/14



## 4 Electrical characteristics

Table 4. VCC+ = 5 V, VCC- = ground, VO = 1.4 V, Tamb = 25 ° C (unless otherwise specified)

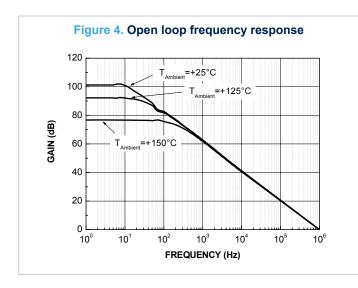
Parameter	Conditions	Min.	Тур.	Max.	Unit	
locate offs at walter as (1)			2	7	>/	
input oπset voltage (1)	Tmin ≤ Tamb ≤ Tmax			9	mV	
lanut affact aurrant			2	30		
input onset current	Tmin ≤ Tamb ≤ Tmax			40	nA	
			20	150	IIA	
input bias current (=)	Tmin ≤ Tamb ≤ Tmax			200		
Large signal voltage gain	VCC+ = 15 V, RL = 2 kΩ, VO = 1.4 V to 11.4 V	50	100		V/mV	
	Tmin ≤ Tamb ≤ Tmax	2.5				
Cumply valtage rejection ratio	VCC+ = 5 to 30 V, RS ≤ 10 kΩ	65	100		٩D	
Supply voltage rejection ratio	Tmin ≤ Tamb ≤ Tmax	65			dB	
Cupply ourrent all ampa no load	VCC+ = 5 V		0.7	1.2	mA	
Supply current, all amps, no load	Tmin ≤ Tamb ≤ Tmax, VCC = 30 V			2	MA	
Common model majorition matic	RS = 10 kΩ	70	85		٩D	
Common-mode rejection ratio	RS = 10 kΩ, Tmin ≤ Tamb ≤ Tmax	60			dB	
Output short-circuit current	VCC+ = 15 V, VO = 2 V, VID = 1 V	20	40	60		
	Tmin ≤ Tamb ≤ Tmax	10				
	VO = 2 V, VCC+ = 5 V	10	20		mA	
Output sink ourrent	VO = 2 V, VCC+ = 5 V, Tmin ≤ Tamb ≤ Tmax	5				
Output sink current	VO = 0.2 V, VCC+ = 15 V	12	50			
	VO = 0.2 V, VCC+ = 15 V, Tmin ≤ Tamb ≤ Tmax	10			μΑ	
Output valtage aving	RL = 2 kΩ	0		(VCC+) - 1.5		
Output voltage swing	RL = 2 kΩ, T <sub>min</sub> ≤ Tamb ≤ Tmax	0		(VCC+) - 2		
	VCC+ = 30 V, RL = 2 kΩ	26	27		V	
Llich level output voltere	VCC+ = 30 V, RL = 2 kΩ, Tmin ≤ Tamb ≤ Tmax	26			V	
nigh level output voltage	VCC+ = 30 V, RL = 10 kΩ	27	28			
	VCC+ = 30 V, RL = 10 kΩ, Tmin ≤ Tamb ≤ Tmax	27				
Low lovel output veltege	RL = 10 kΩ		5	20	mV	
Low level output voltage	RL = 10 kΩ. Tmin ≤ Tamb ≤ Tmax			20	IIIV	
Slew rate (unity gain)	VCC+ = 15 V, Vi = 0.5 to 3 V, RL = 2 kΩ, CL = 100 pF	0.3	0.6		V/µs	
	Tmin ≤ Tamb ≤ Tmax	0.2				
Gain bandwidth product	f = 100 kHz, VCC+ = 30 V, Vin = 10 mV, RL = 2 kΩ, CL = 100 pF	0.7	1.1		MHz	
	Supply voltage rejection ratio  Supply current, all amps, no load  Common-mode rejection ratio  Output short-circuit current  Output sink current  Output voltage swing  High level output voltage  Low level output voltage	$Tmin \le Tamb \le Tmax$ $Input offset current$ $Tmin \le Tamb \le Tmax$ $VCC+ = 15 \text{ V}, RL = 2 \text{ k}\Omega, VO = 1.4 \text{ V to} \\ 11.4 \text{ V}$ $Tmin \le Tamb \le Tmax$ $VCC+ = 5 \text{ to } 30 \text{ V}, RS \le 10 \text{ k}\Omega$ $Tmin \le Tamb \le Tmax$ $VCC+ = 5 \text{ V}$ $Tmin \le Tamb \le Tmax$ $VCC+ = 5 \text{ V}$ $Tmin \le Tamb \le Tmax$ $VCC+ = 5 \text{ V}$ $Tmin \le Tamb \le Tmax, VCC = 30 \text{ V}$ $RS = 10 \text{ k}\Omega$ $RS = 10 \text{ k}\Omega, Tmin \le Tamb \le Tmax$ $VCC+ = 15 \text{ V}, VO = 2 \text{ V}, VID = 1 \text{ V}$ $Tmin \le Tamb \le Tmax$ $VCC+ = 5 \text{ V}$ $Tmin \le Tamb \le Tmax, VCC = 30 \text{ V}$ $RS = 10 \text{ k}\Omega, Tmin \le Tamb \le Tmax$ $VCC+ = 15 \text{ V}, VO = 2 \text{ V}, VID = 1 \text{ V}$ $Tmin \le Tamb \le Tmax$ $VO = 2 \text{ V}, VCC+ = 5 \text{ V}$ $VO = 2 \text{ V}, VCC+ = 5 \text{ V}, Tmin \le Tamb \le Tmax}$ $VO = 0.2 \text{ V}, VCC+ = 15 \text{ V}, Tmin \le Tamb \le Tmax}$ $VO = 0.2 \text{ V}, VCC+ = 15 \text{ V}, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 2 \text{ k}\Omega$ $VCC+ = 30 \text{ V}, RL = 2 \text{ k}\Omega, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 2 \text{ k}\Omega, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega$ $RL = 10 \text{ k}\Omega$	$Tmin \le Tamb \le Tmax$ $Input offset current$ $Input bias current (2)$ $Tmin \le Tamb \le Tmax$ $VCC+ = 15 \text{ V}, RL = 2 \text{ k}\Omega, VO = 1.4 \text{ V to} \\ 11.4 \text{ V}$ $Tmin \le Tamb \le Tmax$ $VCC+ = 5 \text{ to } 30 \text{ V}, RS \le 10 \text{ k}\Omega$ $Supply voltage rejection ratio$ $Supply current, all amps, no load$ $Tmin \le Tamb \le Tmax$ $VCC+ = 5 \text{ to } 30 \text{ V}, RS \le 10 \text{ k}\Omega$ $Tmin \le Tamb \le Tmax, VCC = 30 \text{ V}$ $RS = 10 \text{ k}\Omega, Tmin \le Tamb \le Tmax$ $VCC+ = 15 \text{ V}, VO = 2 \text{ V}, VID = 1 \text{ V}$ $VO = 2 \text{ V}, VCC+ = 5 \text{ V}$ $VO = 2 \text{ V}, VCC+ = 5 \text{ V}$ $VO = 0.2 \text{ V}, VCC+ = 5 \text{ V}$ $VO = 0.2 \text{ V}, VCC+ = 15 \text{ V}$ $VO = 0.2 \text{ V}, VCC+ = 15 \text{ V}$ $VO = 0.2 \text{ V}, VCC+ = 15 \text{ V}$ $VO = 0.2 \text{ V}, VCC+ = 15 \text{ V}$ $VO = 0.2 \text{ V}, VCC+ = 15 \text{ V}$ $VO = 0.2 \text{ V}, VCC+ = 15 \text{ V}$ $VCC+ = 30 \text{ V}, RL = 2 \text{ k}\Omega$ $VCC+ = 30 \text{ V}, RL = 2 \text{ k}\Omega, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega$ $RL = 10 \text{ k}\Omega$ $Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 2 \text{ k}\Omega, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 2 \text{ k}\Omega, Tmin \le Tamb \le Tmax}$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega$ $Tmax$ $VCC+ = 30 \text{ V}, RL = 10 \text{ k}\Omega$ $Tmax$ $RL = 10 \text{ k}\Omega$	Input offset voltage (1)  Input offset current  Input bias current (2)  Input bias current (2)  Tmin ≤ Tamb ≤ Tmax   20  Tmin ≤ Tamb ≤ Tmax  VCC+ = 15 V, RL = 2 kΩ, VO = 1.4 V to 1.14	Input offset voltage   Input offset current   Tmin $\le$ Tamb $\le$ Tmax   9   2   30   150   160   150	

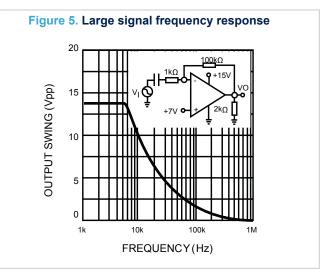
DS3549 - Rev 9 page 6/14

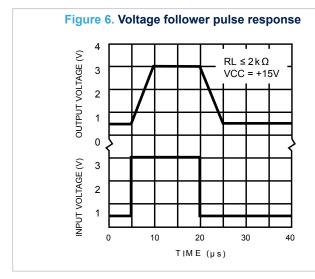


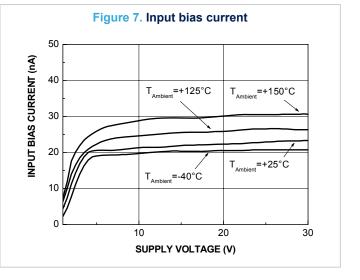
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
GBP	Gain bandwidth product	f = 100 kHz, Tmin ≤ Tamb ≤ Tmax	0.45			MHz
THD	Total harmonic distortion	f =1 kHz, Av = 20 dB, RL = 2 kΩ, VO = 2 Vpp, CL = 100 pF, VCC = 30 V		0.02		%
e <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz, RS = 100 Ω, VCC = 30 V		55		nV / √Hz
DVio	Input offset voltage drift			7	30	μV/°C
Dlio	Input offset current drift			10	300	pA/°C
VO1/VO2	Channel separation (3)	1 kHz ≤ f ≤ 20 kHz		120		dB

- 1. VO = 1.4 V,  $RS = 0 \Omega$ , 5 V < VCC + < 30 V, 0 V < Vic < (VCC +) 1.5 V.
- 2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so there is no change in the loading charge on the input lines.
- 3. Due to the proximity of external components, ensure that stray capacitance does not cause coupling between these external parts. Typically, this can be detected because this type of capacitance increases at higher frequencies.



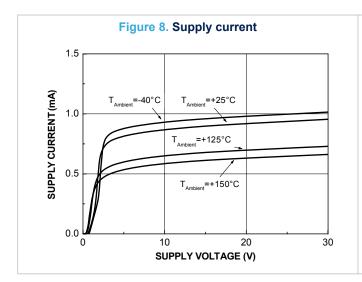






DS3549 - Rev 9 page 7/14





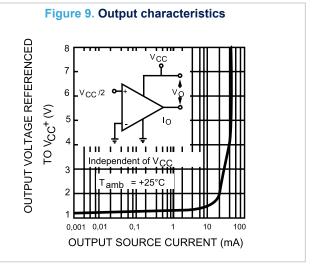


Figure 10. Output characteristics (sink)

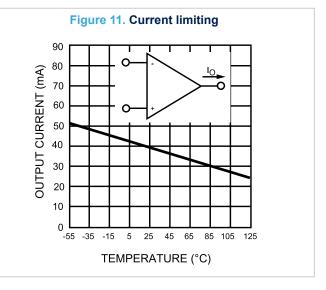
10

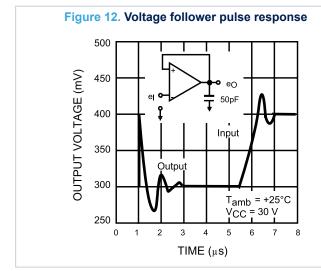
VCC = +5V

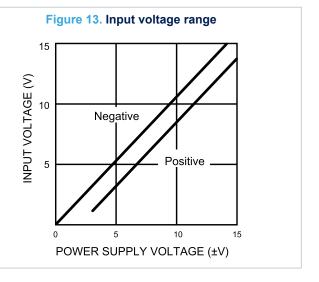
VCC = +15V

VCC = +30V

VCC = +30







DS3549 - Rev 9 page 8/14



Figure 14. Voltage gain

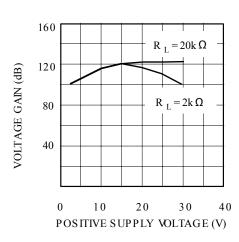


Figure 15. Gain bandwidth product

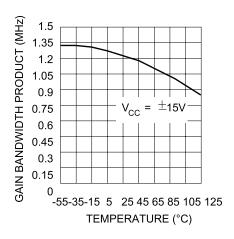


Figure 16. Power supply rejection ratio versus temperature

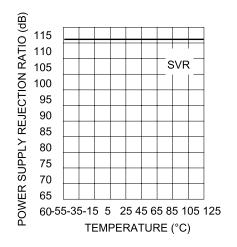
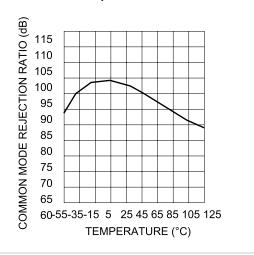


Figure 17. Common mode rejection ratio versus temperature



DS3549 - Rev 9 page 9/14



## 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

### 5.1 MiniSO8 package information

Figure 18. MiniSO8 package outline

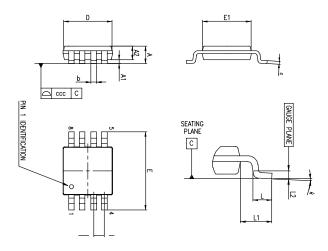


Table 5. MiniSO8 package mechanical data

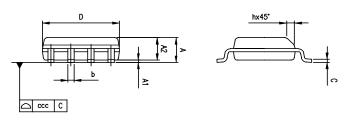
			Dime	nsions		
Ref.		Millimeters			Inches	
	Min.	Тур.	Max.	Min.	Тур.	Max.
А			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
С	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
е		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

DS3549 - Rev 9 page 10/14



## 5.2 SO8 package information

Figure 19. SO8 package outline



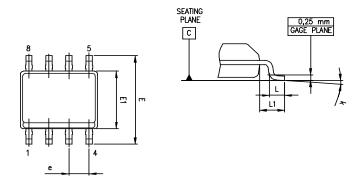


Table 6. SO8 package mechanical data

		Dimensions					
Ref.		Millimeters			Inches		
	Min.	Тур.	Max.	Min.	Тур.	Max.	
Α			1.75			0.069	
A1	0.10		0.25	0.004		0.010	
A2	1.25			0.049			
b	0.28		0.48	0.011		0.019	
С	0.17		0.23	0.007		0.010	
D	4.80	4.90	5.00	0.189	0.193	0.197	
E	5.80	6.00	6.20	0.228	0.236	0.244	
E1	3.80	3.90	4.00	0.150	0.154	0.157	
е		1.27			0.050		
h	0.25		0.50	0.010		0.020	
L	0.40		1.27	0.016		0.050	
L1		1.04			0.040		
k	0°		8°	0°		8°	
ccc			0.10			0.004	

DS3549 - Rev 9 page 11/14



# 6 Ordering information

Table 7. Order codes

Order code	Temperature range	Package	Packaging	Marking
JLM2904WH-CD1		Wafer	_	_
LM2904WHDT	40 4- 450 %	SO8	Tube or tone and real	2904WH
LM2904WHYDT (1)	-40 to 150 C	-40 to 150 °C Tube or tape and reel		2904WHY
LM2904WHYST (2)		MiniSO8	Tape and reel	K422

Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

DS3549 - Rev 9 page 12/14

<sup>2.</sup> Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q 002 or equivalent are on-going.



## **Revision history**

**Table 8. Document revision history** 

Date	Revision	Changes	
01-Sep-2003	1	Initial release	
01-Jul-2005	2	PPAP references inserted in the datasheet, see Section 6 Ordering information	
01-Oct-2005	3	Correction of error in AVD min. value in Table 4. VCC+ = 5 V, VCC- = ground, VO = 1.4 V, Tamb = 25 ° C (unless otherwise specified).	
		Minor grammatical and formatting changes throughout.	
27-Sep-2006	4	Correction of error in AVD min. value in Table 4. VCC+ = 5 V, VCC- = ground, VO = 1.4 V, Tamb = 25 ° C (unless otherwise specified).	
		ESD values added in Table 2. Absolute maximum ratings (AMR).	
20-Jul-2007	5	Equivalent input noise parameter added in Table 4. VCC+ = 5 V, VCC- = ground, VO = 1.4 V, Tamb = 25 $^{\circ}$ C (unless otherwise specified).	
		Electrical characteristics curves updated.	
		Package information updated.	
		Added Rthja and Rthjc parameters in Table 2. Absolute maximum ratings (AMR).	
07-Apr-2008	6	Updated format of package information for SO-8.	
		Corrected marking error in Table 7. Order codes (2904WHY, not 2904WY).	
04-Jul-2012	7	Removed commercial type LM2904WHYD.	
04-Jui-2012	7	Updated Table 7. Order codes.	
		Added MiniSO8 silhouette and package.	
01-Apr-2015	8	Table 2. Absolute maximum ratings (AMR): added MiniSO8 information for the parameters Rthja and Rthjc and updated the parameters Tstg and Tj.	
		Section 5.2 : added "L1" dimension.	
		Table 7. Order codes: added order code LM2904WHYST and removed obsolete order code LM2904WHD.	
24-Aug-2020	9	Added Section 2 Package pin connections.	

DS3549 - Rev 9 page 13/14



#### **IMPORTANT NOTICE - PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics - All rights reserved

DS3549 - Rev 9 page 14/14