STA1295, STA1275

Accordo5 - Automotive infotainment processors for display audio and cluster applications

Datasheet - production data

LFBGA529 19x19x1.7 mm

Features

- AEC-Q100 qualified Grade 3

Core and infrastructure

- ARM® Single or Dual Core Cortex® A7 up to 650 MHz with NEON instructions and FPU
- Memory organization
  - L1 Cache: 32 KB instruction, 32 KB data
  - L2 Cache: 256 KB
  - 768 KB embedded SRAM
  - 16/32-bit DDR3L interface at 660 MHz
  - Serial Quad IO NOR interface
  - 16-bit Parallel NAND Controller
- 32-bit watchdog timer
- 16-channels DMA
- 8x 32-bit free running timers/counters
- 5x 16-bit Extended Function Timer (EFT) with input capture/output compare and PWM
- Real Time Clock (RTC) with fraction readout
- Temperature sensor

Audio subsystem

- Sound processing DSP (450 MIPS)
- 6 stereo channels hardware sample rate converter
- 6x Audio DAC with 103 dB SNR A-weighted
- 6x Rx/Tx Audio interfaces (I2S/ multi-channel ports, with SPI mode)
- 1x stereo ADC for AUX IN/Tuner with internal switching logic (for 2 sources); 98 dB SNR A-weighted
- 2x differential Mono ADC for Voice/Tel-IN with internal switching logic; 98 dB SNR A-weighted

Media interfaces

- 3x secure-digital multimedia memory card interface (SD/MMC)
- 2x USB 2.0 Dual Role with integrated PHY (Fast charger function supported)
- 1x RMII/RGMII Ethernet AVB MAC
- SPDIF with CDROM block decoder support

Display subsystem

- Multi-layer TFT dRGB Controller: up to 1080p
- Resistive Touch screen controller
- Video input port, ITU-601/656
- 3D graphics acceleration (OpenGL® ES 2.0)
- 2D graphics Bit Blit/Blend engine
- H264 / Multi-Format Video Decoder

Embedded secure vehicle interface

- Dedicated ARM® Cortex® M3 MCU
- 256 KB isolated embedded memory
- Secured NOR interface
- CAN interfaces: 1x CAN, 2x CAN FD

I/O interfaces

- 1x 10 channels 10-bits ADC
- 1x 6 channels ADC for DC detection
- 3x I2C multi-master/slave interfaces
- 4x UART controller
- 3x Synchronous Serial Port (SSP/SPI)
- 5x 32-bit GPIO ports
- JTAG based In-Circuit Emulator (ICE) with Embedded Trace Module

Operating conditions

- ARM_VDD, VDD: 1.14 V - 1.26 V
- VDD_IO_3V3: 3.3 V ±10%
- DDR3L VDDQ: 1.35 V ±5%
- VDD_IO_ON: 3.3 V ±10%,
- Ambient temperature range: -40°C / +85°C
- Junction temperature range: -40°C / +125°C

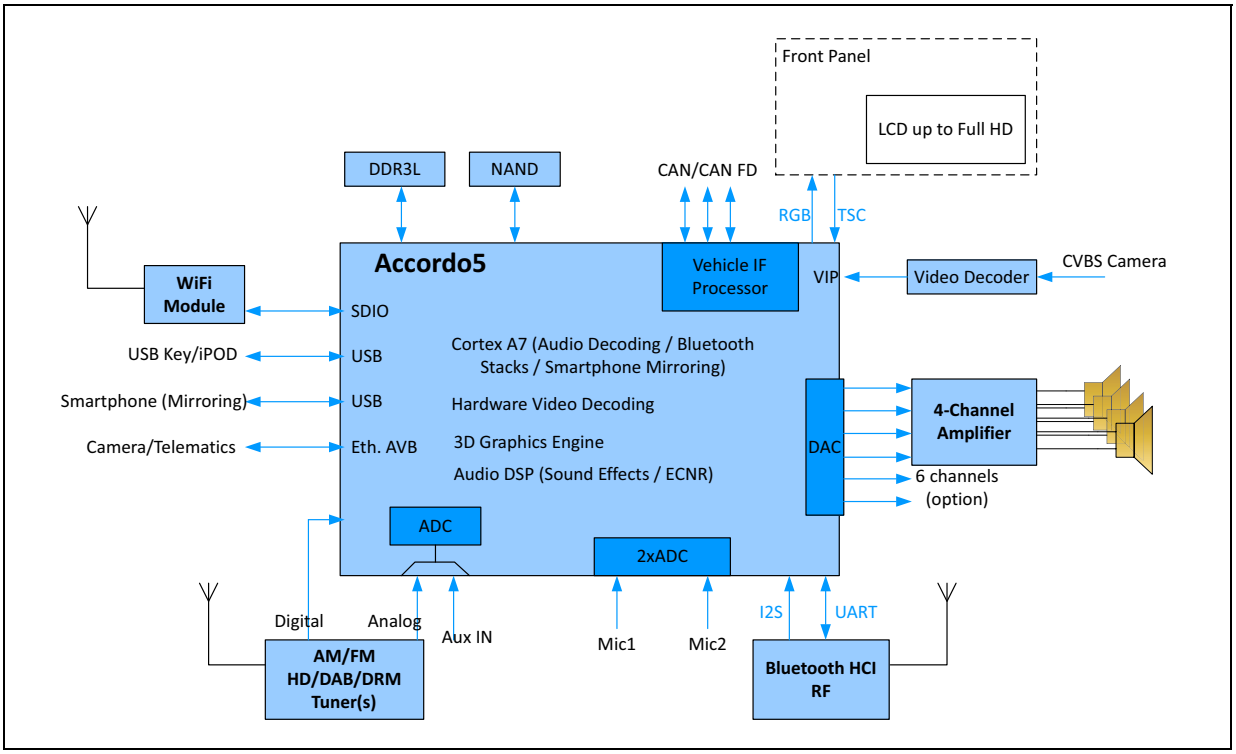
Contents

1 Description

STA1275 and STA1295 are fully automotive, power efficient Systems-On-Chip, targeting cost effective processing solution for modern Display Audio Systems.

They feature a powerful single or dual core Cortex® A7 processor (depending on the versions), a high performance 3D GPU engine, a multi-format video decoder engine, a multi-layer multi-format display controller, an audio DSP, a complete set of standard connectivity interfaces and a dedicated ARM® Cortex® M3 controller for real-time CAN / Vehicle Interface Processing.

Figure 1. Accordo5 block diagram



2 System description

2.1 Application processor

STA1275 and STA1295 processing capability relies on an ARM® Cortex® A7 (single or dual, according to the versions) running at up to 650 MHz, delivering 2500+ DMIPS with minimal heat dissipation requirements. The application processor has 32 KB of instruction cache and 32 KB of data cache, as well as 256 KB of L2 cache for high throughput and low latency tasks. The Cortex® A7 core implementation is equipped with a dedicated PLL and power domain, in order to achieve best thermal/MIPS performance compromise in all application scenarios.
The application processor is connected to the system via an efficient bus matrix infrastructure, implementing flexible QoS and trust zone features.

2.2 Memory architecture

2.2.1 Embedded memory

STA1275 and STA1295 embed 768 KB of 64 bits SRAM memory clocked at 200 MHz, which can be used for secure data storage.The whole embedded memory is also cacheable and can be accessed by DMA.

2.2.2 DDR controller

DDR controller supports DDR3L JEDEC interface 16 or 32 bits wide (depending on the versions), clocked at up to 660 MHz, allowing an optimal solution for throughput intensive applications.

Such memory is cacheable, and can be accessed by DMA, and is flexibly configurable as secure/non-secure.

2.2.3 SQI NOR interface

The SQIO controller allows interfacing Serial Quad I/O flash memories up to 125 MHz (SDR).

Main features are:

- Direct flash memory access
- Fast memory access through page buffer (256 bytes)
- Programmable single or quad I/O flash interface

SQI memory space can be partitioned in order to reserve a portion of the NOR device to the Secure CAN Subsystem.

2.2.4 Parallel memory interface

FSMC static memory controller provides a generic 16-bits parallel interface suitable to connect SRAM and NAND devices. This peripheral allows execution in-place from SRAMs, as well as DMA accesses. Such interface can be used to store boot code into NAND.

2.3 SD/MMC

STA1275 and STA1295 are equipped with 3 SDMMC controllers which allow interfacing to either mass storage devices, or to WiFi modems.

Two interfaces (SD/MMC1 and 2) implement the following specification:

- eMMC - MultiMedia Card 4.4
  - 26/52 MHz
  - 1, 4, 8 bit of data
- SD/SDIO 3.0
  - 4 bit interface
  - SDSC/SDHC/SDXC limited to 50 MHz SDR frequency

Both interfaces can be used in conjunction with DMA to efficiently implement data transfer with minimal CPU load for handling interrupts.

A third controller (SD/MMCM0) with dedicated DMA engine implementing:

- eMMC - MultiMedia Card 4.51
  - 26/52 MHz
  - 1, 4, 8 bit of data
- SD/SDIO 3.0
  - 4 bit interface
  - SDSC/SDHC/SDXC up to SDR50

2.4 USB

STA1275 and STA1295 have two Dual role USB HS controllers, both with embedded PHY, allowing to efficiently connect to mass storage devices, as well as portable devices (phones, pads). Along with USB connectivity, STA1275 and STA1295 fully support USB charger functionality, implementing CDP and SDP profiles from the BC 1.2 specifications. The controller supports HS 480-Mbps using an EHCI Host Controller, as well as FS and LS modes through an integrated OHCI interface.

USB controller implements a bootable interface, useful for production flashing, as well as to debug system post production.

2.5 Display controller

Display controller works simultaneously on multiple layers (up to 4), allowing an on-the-fly blending composition scheme from multiple frame buffers. Each buffer can have a different color format, and with each buffer user can specify cropping regions (windowing). A typical usage example is for blending a complex HMI rendered with 3D engine, on top of a video frame buffer and a rear-view camera buffer.

The controller can handle two symmetric display panels (only in WVGA mode), sharing the same data lane, with two separate frame buffer contents.

The main features are:

- Video overlay
- Supported color formats:
  RGB565, ARGB8888, YUV422, YUV 420 PLANAR
- Gamma correction (using independent look-up tables for R, G, B)
- Dithering
- Configurable alpha blending modes, with either buffer alpha or constant alpha

2.6 Touch screen controller

Embedded 10-bit resistive touch screen controller allows to control 7-inch display touch screens.

2.7 Video Input Port

The Video Input Port (VIP) allows to grab images from external devices, supporting parallel CCIR-656 interface up to 54 MHz. Both embedded synchronization and external synchronization are supported. VIP supports both interlaced or progressive modes.

The VIP is synchronized with display controller to prevent tearing effects, and is used in conjunction with SGA to implement on the fly YUV to RGB color conversion and bilinear interpolated re-scaling.

2.8 3D graphics engine

STA1275 and STA1295 come with a powerful 3D, allowing smooth HMI rendering with impressive transition effects quality, as well as navigation and instrument clusters rendering. The 3D engine is based on a unified shader architecture, based on an ultra-threaded SIMD processor that performs as both vertex shader and fragment shader with IEEE 32bit floating point full precision. When used as a vertex shader it performs geometry transformations and lighting computations. When used as a fragment shader it applies texture data and computes color values for each pixel.

The main features are:

- OpenGL® ES 2.0 / 1.1 compliance, including extensions; OpenVG™ 1.1
- IEEE 32-bit floating-point pipeline
- Ultra-threaded, unified vertex and fragment (pixel) shaders
- Low bandwidth at both high and low data rates
- Low CPU loading
- Up to 12 programmable elements per vertex
- Dependent texture operation with high-performance
- Alpha blending
- Depth and stencil compare
- Point sampling, bi-linear sampling, tri-linear filtering, and cubic textures
- Resolve and FastClear
- 8k x 8k texture size and 8k x 8k rendering target

- Vertex DMA streams

With a performance of up to:

- Vertex rate: 120 MVtx/sec
- Pixel Rate: 240 MPix/sec

2.8.1 Unified shader features

Table 1. Unified shader features

Features	GPU support
Shader type and execution units	Unified shader, SIMD4, SFP32 Trans
Swizzle capabilities	Full 32-bit word level swizzle in a 128-bit vector
GPR's per shader core	Up to 512 general purpose registers, 128 bits each
Uniform registers	Uniform total: 320 registers Vertex Shader: 128 registers, 128 bits each Fragment Shader: 128 registers, 128 bits each
FP denorm and rounding options	Denorms are set to zero. Supports rounding to zero.
Maximum number of data input attributes	Maximum of 12 vertex shader input elements Maximum of 8 fragment shader input elements
Sampler Count	Total: 12 (4 VS Samplers, 8 PS Samplers)
Maximum number of instructions	256
Maximum number of vertex streams	4
Maximum number of threads in flight per shader core	64
Subroutines	4 levels
Conditional branch support	GT, LT, EQ, GE, LE, NE
Shader instruction rate	1-cycle throughput for all shader instructions
Floating-point instruction precision	SIMD4 (vector): 23.5 bits
Fragment shader video	Supports video texture

2.8.2 Vertex processing features

Table 2. Vertex processing features

Features	GPU support
Vx D3D, OGL ES formats supported	BYTE, UBYTE, SHORT, USHORT, INT, UINT, DEC, UDEC, FLOAT, FLOAT16, D3DCOLOR, FIXED16DOT16
Vertex data size limits	256 bytes
Pre shader cache	1 kB
Post shader cache	8 vertices

2.8.3 Primitive processing features

Table 3. Primitive processing features

Features	GPU Support
Primitives supported	Triangle strip, fan and list; line strip and list; point list
Vertex/primitive geometry input index sizes	8-bit,16-bit and 32-bit indices
Setup parameters available to fragment shader	8 vec4 parameters; all available to fragment shader

2.8.4 Texture processing features

Table 4. Texture processing features

Features	GPU support								
Input texture formats (fixed point)	A8, L8, I8, A8L8, ARGB4, XRGB4, ARGB8, XRGB8, ABGR8, XBGR8, R5G6B5, A1RGB5, R8, R8G8, X1RGB5, YUY2, UYVY, D16, D24X8, A8_OES, DXT1, DXT2, DXT3, DXT4, DXT5, ETC1. All fixed-point formats are filtered.								
	Bits		**Format**		**Alpha**		**R**	**G**	**B**
	16		ARGB4444		4		4	4	4
	16		XRGB4444		4 (not used)		4	4	4
	16		ARGB1555		1		5	5	5
	16		XRGB1555		8 (not used)		5	5	5
	16		RGB565		0		5	6	5
	32		ARGB8888		8		8	8	8
	32		XRGB8888		8 (not used)		8	8	8
	32		ABGR8888		8		8	8	8
	32		XBGR8888		8 (not used)		8	8	8
	Planes	**Format**	**Mode**	**Y**	**U**	**V**	**UV**	**YUYV**	**UYVY**
	1	YUY2	4:2:2	—	—	—	—	1	—
	1	UYVY	4:2:2	—	—	—	—	—	1
Additional texture formats supported through resolve conversion	**Planes**	**Format**	**Mode**	**Y**	**U**	**V**	**UV**	**YUYV**	**UYVY**
	3	YV12	4:2:0	1	1	1	—	—	—
	2	NV12	4:2:0	1	—	—	1	—	—
Texture compression	4 bits and 8 bits per texel								
Compressed texture formats	DXT1, DXT2, DXT3, DXT4, DXT5, ETC1. All compressed formats are filtered.								
Compressed texture supertile	Supported								
Texture size maximum	8k x 8k								
Addressing modes	wrap, mirror, clamp								
Mipmap support	14 mipmap levels; programmable LOD biasing and replacement								
Shadow texture	Depth texture PCF filtering								

Table 4. Texture processing features (continued)

Features	GPU support
Texture cache size	32 cache lines, with 64 bytes per cache line; 2 KB texture cache total
Texture coordinate fraction bits	5 bits
Texture sampler units	8 samplers, indexable
Textures per fragment maximum	8 texture samplers
Dependent texture operation	High performance; unlimited dependent texture reads
Dependent texture per fragment max, relative sampling	No limit
Texture repeat max	256
Texture types	2D cube map, 1D, projected, depth, bump map, displacement map
Texture filters	Point sample, bi-linear, tri-linear
Texture component mapping: D3D, OGL ES options	Supports both D3D and OES options
Texture size types	Power-of-2, Non-square texture support

2.8.5 Rasterization

Table 5. Rasterization

Features	GPU support
Interpolant attributes	8
Render target size	8K x 8K
Clipping window	Clipping rectangle supported
Early Z	Yes

2.8.6 Fragment processing

Table 6. Fragment processing

Features	GPU support					
Fragment color, alpha, Z, stencil precision	**Bits**	**Format**	**Alpha**	**R**	**G**	**B**
	16	ARGB4444	4	4	4	4
	16	XRGB4444	4 (not used)	4	4	4
	16	ARGB1555	1	5	5	5
	16	XRGB1555	1 (not used)	5	5	5
	16	RGB565	0	5	6	5
	32	ARGB8888	8	8	8	8
	32	XRGB8888	8 (not used)	8	8	8
	32	ABGR8888	8	8	8	8
	32	XBGR8888	8 (not used)	8	8	8
	Bits	**Format**	**Depth**		**Stencil**	
	16	D16	16		0	
	32	D24S8	24		8	
Fragment storage	16-bit color and Z, 32-bit color and Z for each fragment Lossless compression, no storage reduction					
Alpha support	Individual fragment alpha masking					
Fragment cache	16 cache lines for color 16 cache lines for Z 16 bytes per cache line					

2.8.7 Z/Stencil buffer features

Table 7. Z/Stencil buffer features

Features	GPU support
Z/stencil formats	16-bit Z; 24-bit Z plus 8-bit stencil, with lossless compression support
Z/stencil buffer	16 cache lines; 64 bytes per line
Stencil support	Stencil compression, two-sided stencil

2.8.8 Render Target / Alpha blending

Table 8. Render Target / Alpha blending

Features	GPU support
Formats	16-bit and 32-bit, with lossless compression support
RT buffer cache	16 cache lines; 64 bytes per line RT caches are fully set associative

Table 8. Render Target / Alpha blending (continued)

Features	GPU support
Blend modes	Porter-Duff blending modes
Render target dithering support	Yes

2.8.9 Destination buffer color formats

Table 9. Destination buffer color formats

Features	GPU support					
	Bits	Format	Alpha	R	G	B
Destination color formats	16	ARGB4444	4	4	4	4
	16	ARGB1555	1	5	5	5
	16	RGB565	0	5	6	5
	32	ARGB8888	8	8	8	8
	32	ARGB8888	8	8	8	8

2.9 2D Smart Graphics Accelerator

The aim of the Smart Graphic Accelerator (SGA) is to provide an efficient 2D primitive drawing tool that breaks down the MIPS and power consumption related to bit blitting and composition tasks.

2D-Graphics features:

- 2D Rendering Speed: up to 208 MPixel/s
- Pixel, Line, Filled Triangle, Filled Rectangle primitives
- Line-Stippling, Filling Pattern
- Flat and Gradient colour fill (in triangles and rectangles)

Video Overlay features:

- Bit-Blitting on Rectangle, Triangle shapes
- Image Resizing (Bilinear Interpolation Filter or Sub/OverSampling)
- Image Rotation (with any angle)
- Colour Conversion (YUV-to-RGB or RGB-to-YUV, 16-235 clamping possible)
- Transparency extraction (exact Colour Keying or Colour Cube (triple interval)
- Colour Swap with Colour Keying
- Alpha-Blending of 3 sources to a destination, ROP boolean operations
- Dithering operator

2.10 Multi-format video decoder

The embedded video decoder is capable of decoding the following formats, with minimal CPU load:

- H.264 baseline, main and high profiles, levels 1–4.1
- SVC scalable baseline and high profiles, base layer only
- MPEG-4 simple and advanced simple profiles, levels 0–5
- H.263 Profile 0, levels 10–70
- Sorenson Spark–WMV9 / VC-1 simple, main and advanced profile, levels 0–3
- MPEG-1 and 2 main profile, levels low, medium and high–RealVideo8/9/10
- DivX®3/4/5/6 support – Home Theatre Profile Qualification
- On2 VP6, VP7 and VP8, Versions 0–3
- AVS JizhunProfile–JPEG, all common sampling formats

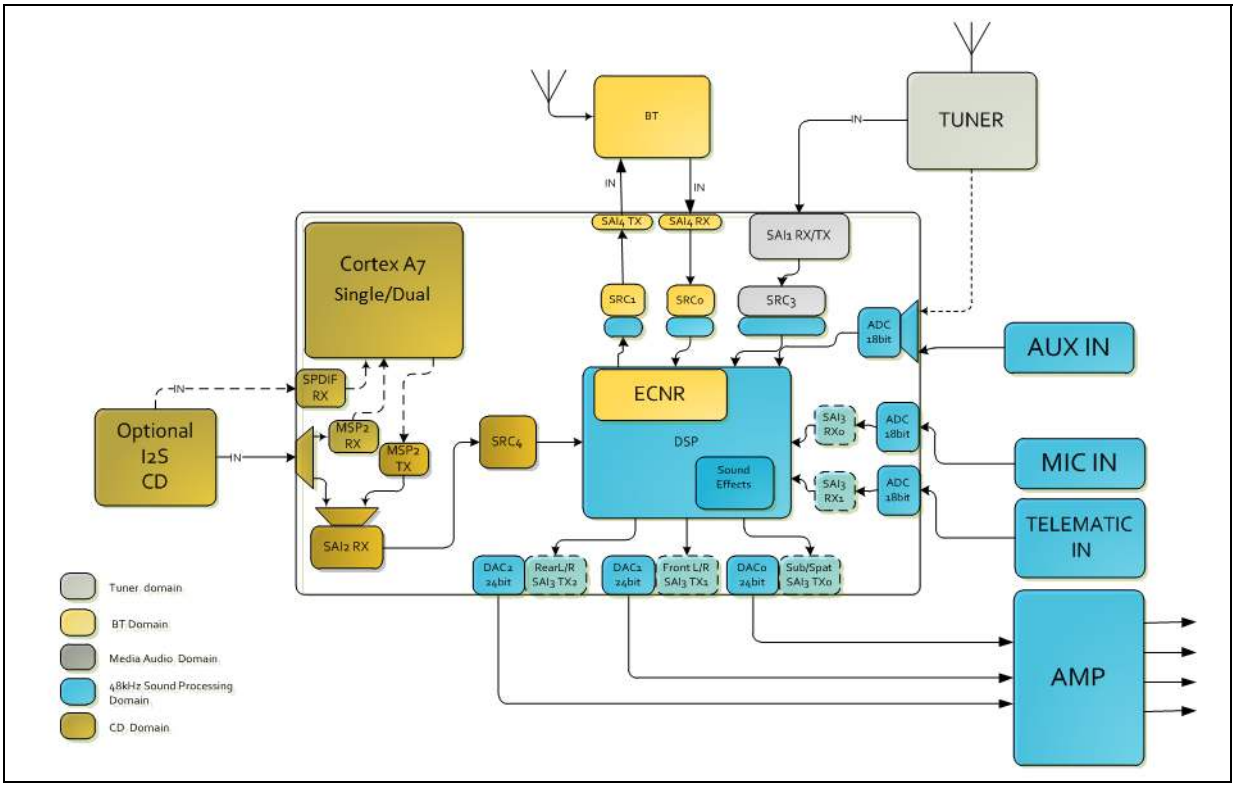
Along with video decoding features, the video decoder also implements video post processing functionality such as:

- Re-scaling, with high quality filtering
- Color conversion
- Gamma correction
- Dithering
- Image cropping
- Digital zoom
- Horizontal/vertical flip

2.11 Sound subsystem

STA1275 and STA1295 implement a sound subsystem which allows to efficiently handle sound processing tasks, such as spatialization and equalization, without loading the main CPU with interrupt intensive tasks. The sound subsystem is composed of a set of audio interfaces, an isochronous bus, a DSP delivering 450 MIPS, and a 3 stereo channels sample rate converter.

Figure 2. Accordo5 sound subsystem application example



2.11.1 Audio interfaces

A complete set of audio interfaces is provided, in order to simplify integration with amplifiers, and input sources. Each interface can be routed to the sound subsystem. A complete list of audio interfaces is provided below:

- 1x AUX ADC:
  - 18 bit Delta Sigma ADCs with 98 dB A-weighted
  - 83 dB THD internally
  - multiplexed between AUX line and tuner line
  - ADC inputs are single ended 3.3 V
- 2x Voice ADC (for MIC-IN and TEL-IN) for high quality hands-free at 8/16/24 kHz:
  - 18 bit Delta Sigma ADCs with 98 dB A-weighted
  - 83 dB THD
  - Both voice and TEL-IN lines are differential inputs
- 3x Stereo DAC delivering:
  - 103 dB A-weighted
  - 90 dB THD
  - DAC outputs are single ended 3.3 V
- 3x i2s IN
- 3x i2s OUT
- 1x MSP IN/OUT, TDM capable
- 1x SPDIF IN for CD/CDROM input with hardware block decoder for CDROM error correction

2.11.2 Routing and sample rate converter

Each audio interface can be routed in both directions (IN/OUT) through sample rate converters, which allow normalizing the sampling rate to the sound processing engine. The audio routing infrastructure is designed to deliver high quality sample rate conversion on multiple channels, allowing simultaneous audio streams, such as BlueTooth Hands Free and audio media playback, to be handled without CPU load.

In order to generate multiple sampling rate audio frequencies, a dedicated fractional PLL is also provided. This PLL also allows an efficient implementation of iPOD playback, by dynamically adjusting the reconstructed audio sampling rate without CPU overload.

2.11.3 Sound DSP

STA1275 and STA1295 are equipped with three (3) 150 MIPS 24-bit fixed point Harvard architecture DSPs (for a total of 450 MIPS) dedicated to sound processing, fully integrated with the sound subsystem with a specific isochronous bus. DSPs are provided with an integrated sound processing library implementing effects like gain, balancing and equalizer.

- STA1275 and STA1295 are equipped with 2 DSPs configured as:
  - 6 k x 32 bit program PRAM
  - 4 k x 24 bit data XRAM
  - 4 k x 24 bit data YRAM

- And a third DSP configured as:
  - 8k x 32 bit program PRAM
  - 32k x 24 bit data XRAM
  - 16k x 24 bit data YRAM

Each DSP is connected to other DSPs and audio peripherals by means of a programmable isochronous bus infrastructure which guarantees a controlled throughput and latency for all audio transfers.

2.12 Ethernet MAC Controller

Connection to Ethernet infrastructure is supported by the ETH MAC, which can be connected to an external PHY with either RGMII or RMII interfaces. Ethernet MAC also implements AVB features, and is compatible with the following standards:

- IEEE 1588-2008 for precision networked clock synchronization
- IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic
- RGMII/RTBI specification version 2.6 from HP/Marvell
- RMII specification version 1.2 from RMII consortium

MAC controller has separate channels or queues for AV data transfer in 100 Mbps and 1000 Mbps modes with single Tx/Rx FIFOs for all selected queues.

2.13 System DMA

DMA is designed to efficiently perform memory to memory, and memory to peripherals transfers, offloading such tasks from the processor, thus reducing interrupt handling load. DMA provides 16 independent channels which can be dynamically assigned to different data-path. Complex scatter/gather transfers can be implemented by programming specific DMA command linked lists.

2.14 Secure CAN subsystem

STA1275 and STA1295 allow isolating critical code from main application by implementing a dedicated subsystem based on ARM® Cortex® M3, along with:

- 256 KB dedicated embedded SRAM
- Interrupt controller
- Timers
- CAN controller, implementing CAN (CAN0) and FD-CAN (CAN1 and CAN2)
- Dedicated GPIOs
- Dedicated Wakeup lines
- Back-up RAM in always on domain
- Local RTC
- Secure OTP, user programmable

All of the above can be completely isolated from the rest of the system. This subsystem can be dedicated to implement secure features, such as boot authentication, as well as interrupt

intensive tasks to offload main CPU. The secure subsystem communicates with the application running on Cortex® A7 using a Hardware Mailbox interrupt based mechanism.

2.15 Crypto accelerator engine

In order to efficiently support security, STA1275 and STA1295 embed a dedicated, flexible hardware accelerator for the following set of cryptographic operations:

- DES, TripleDES
- AES 128, 192, 256:
  Modes of operation: ECB, CBC, CTR, XTS, CCM, GCM, CFB, OFB, CMAC
- SHA1, SHA256, SHA384, SHA512 with HMAC
- Public Key Accelerator for RSA, DH, Elliptic Curve Cryptography
- TRNG, for random number generation, compliant with NIST SP800-90B

These cryptographic acceleration features, along with the embedded secure OTP, the TrustZone aware bus infrastructure, and secure ROM boot, provide a complete set of components to build a secure system, for data confidentiality, integrity, as well as code integrity and rollback protection.

2.16 General purpose ADC

The system is equipped with 10-inputs SAR ADC with a resolution of 10-bits and sampling frequency up to 2.5 MHz. In addition, a second instance of the same SAR ADC implements a continuous voltage monitoring on 6 more channels, to support DC offset detection feature in hardware.

2.17 GPIOs

STA1275 and STA1295 have a total of 160 GPIOs, which can be independently configured either as INPUT or OUTPUT. In order to make the system flexible, these IOs are multiplexed on PINs with other peripherals. Alternate function scheme is described in *Table 10*.

GPIOs are divided into 3 sets:

- 128 application GPIOs:
  Most of system digital IOs are exposed as alternate functions of application GPIOs. This allows maximum flexibility in system definition.
- 16 secure GPIOs (s_GPIO):
  This set of GPIOs can be selectively configured as secure, in order to securely control IO functionality, for secure blocks which expose an interface.
- 16 M3_GPIOs:
  This set of IOs is dedicated to the Cortex® M3 microcontroller and its peripherals.

2.17.1 Application GPIO alternate function mapping

Note: All GPIOs pins are configured by default at reset in GPIO input mode. As an exception to this general rule, the reset default state of GPIO108 to GPIO113 depends on the value latched at reset of REMAP[1:0] (Refer to Table 10 footnote (1)).

Table 10. Application GPIO alternate function mapping

GPIO	ALT A	ALT B	ALT C	DEBUG
GPIO0	SDMMC1_CMD	SDMMC2_DAT2_DIR	SAI4_TX1	ETM_D0
GPIO1	SDMMC1_CLK	SDMMC2_DAT31_DIR	SAI4_TX2	ETM_D1
GPIO2	SDMMC1_DATA_0	SDMMC0_DATA_4	SAI4_TX0	ETM_D2
GPIO3	SDMMC1_DATA_1	SDMMC0_DATA_5	SAI4_BCLK	ETM_D3
GPIO4	SDMMC1_DATA_2	SDMMC0_DATA_6	SAI4_FS	ETM_D4
GPIO5	SDMMC1_DATA_3	SDMMC0_DATA_7	SAI4_RX0	ETM_D5
GPIO6	SQI_FDBSCK	—	SDMMC1_DAT0_DIR	ETM_D6
GPIO7	AUDIO_REFCLK	SAI2_TX	I2S2_TX	ETM_D7
GPIO8	SAI3_BCLK	SDMMC1_CMD	SAI4_RX2	ETM_D8
GPIO9	SAI3_FS	SDMMC1_CLK	SAI4_RX1	ETM_D9
GPIO10	SAI3_RX2	SDMMC1_DATA_0	EFT2_OCMP1	ETM_D10
GPIO11	SAI3_TX1	SDMMC1_DATA_1	EFT2_ICAP1	ETM_D11
GPIO12	SAI3_TX2	SDMMC1_DATA_2	UART2_TX	ETM_D12
GPIO13	SAI3_RX1	SDMMC1_DATA_3	UART2_RX	ETM_CLK
GPIO14	SAI3_TX0	SDMMC2_DAT0_DIR	I2C2_SCL	ETM_CTL
GPIO15	SAI3_RX0	SDMMC1_DAT31_DIR	I2C2_SDA	—
GPIO16	SAI2_BCLK	FSMC_DACK	I2S2_BCLK	ETM_D13
GPIO17	SAI2_FS	FSMC_DREQ	I2S2_FS	ETM_D14
GPIO18	SAI2_RX/TX	SPDIF_RX	I2S2_RX	—
GPIO19	SAI1_BCLK	SPI2_TXD	EFT2_OCMP0	ETM_D15
GPIO20	SAI1_FS	SPI2_RXD	EFT2_OCMP1	—
GPIO21	SAI1_RX	SPI2_SCK	EFT2_EXTCK	—
GPIO22	I2S0_BCLK	SAI4_BCLK	—	—
GPIO23	I2S0_FS	SAI4_FS	—	—
GPIO24	I2S0_TX	SAI4_TX0	—	—
GPIO25	I2S0_RX	SAI4_RX0	—	—
GPIO26	EFT0_ICAP0	EFT0_EXTCK	SPI2_SS	—
GPIO27	EFT0_ICAP1	SDMMC2_CMDDIR	SPI2_TXD	—
GPIO28	EFT0_OCMP0	UART1_TX	SPI2_RXD	—
GPIO29	EFT0_OCMP1	UART1_RX	SPI2_SCK	—
GPIO30	EFT1_ICAP0	EFT1_EXTCK	USB1_DRVVBUS	—
GPIO31	EFT1_ICAP1	SDMMC0_FBCLK	FSMC_DACK	—
GPIO32	EFT1_OCMP1	SDMMC0_PWR	SDMMC1_FBCLK	USB_VCOD1V48
GPIO33	EFT1_OCMP0	SDMMC2_DAT31_DIR	FSMC_DREQ	—

Table 10. Application GPIO alternate function mapping (continued)

GPIO	ALT A	ALT B	ALT C	DEBUG
GPIO34	SPI1_SS	EFT0_EXTCK	I2C1_SCL	ETM_D13
GPIO35	SPI1_TXD	EFT1_EXTCK	I2C1_SDA	ETM_D14
GPIO36	SPI1_RXD	EFT1_OCMP1	UART3_TX	—
GPIO37	SPI1_SCK	EFT1_OCMP0	UART3_RX	ETM_D15
GPIO38	ETH_MDIO	UART1_TX	EFT1_ICAP0	—
GPIO39	ETH_MDC	UART1_RX	EFT1_ICAP1	—
GPIO40	UART1_TX	SDMMC0_DATA_4	SDMMC1_DATA_4	STM_D0
GPIO41	UART1_RX	SDMMC0_DATA_5	SDMMC1_DATA_5	STM_D1
GPIO42	UART2_RX	SDMMC0_DATA_6	SDMMC1_DATA_6	STM_D2
GPIO43	UART2_TX	SDMMC0_DATA_7	SDMMC1_DATA_7	STM_D3
GPIO44	UART3_RX	UART1_CTS	EFT2_ICAP0	—
GPIO45	UART3_TX	UART1_RTS	EFT2_ICAP1	—
GPIO46	I2C1_SDA	EFT0_OCMP0	EFT0_ICAP1	—
GPIO47	I2C1_SCL	EFT0_OCMP1	EFT0_ICAP0	—
GPIO48	EFT2_ICAP0	EFT2_OCMP0	EFT2_EXTCK	—
GPIO49	I2C1_SDA	FSMC_SMADQ_8	SDMMC1_CMDDIR	STM_CTL
GPIO50	I2C1_SCL	FSMC_SMADQ_9	SDMMC1_DAT31_DIR	STM_CLK
GPIO51	—	CLKOUT1	SDMMC1_DAT2_DIR	—
GPIO52	VIP_PIXCLK	—	—	—
GPIO53	VIP_HSYNCH	UART1_TX	CLCD_HSYNC1	—
GPIO54	VIP_VSYNCH	UART1_RX	CLCD_DE1	—
GPIO55	VIP_DAT7	—	—	STM_D0
GPIO56	VIP_DAT6	—	—	STM_D1
GPIO57	VIP_DAT5	—	—	STM_D2
GPIO58	VIP_DAT4	—	—	STM_D3
GPIO59	VIP_DAT3	—	—	STM_CTL
GPIO60	VIP_DAT2	—	—	STM_CLK
GPIO61	VIP_DAT1	—	—	—
GPIO62	VIP_DAT0	—	—	—
GPIO63	CLCD_PIXCLK0	CLKOUT_HCLK	—	—
GPIO64	CLCD_VSYNCH	CLKOUT_PERIPH0	—	—
GPIO65	CLCD_HSYNCH	CLKOUT_PERIPH1	—	—
GPIO66	CLCD_DE	—	—	—
GPIO67	CLCD_COLOR23	SPI1_TXD	UART1_RTS	—
GPIO68	CLCD_COLOR22	SPI1_RXD	UART1_CTS	—

Table 10. Application GPIO alternate function mapping (continued)

GPIO	ALT A	ALT B	ALT C	DEBUG
GPIO69	CLCD_COLOR21	SPI1_SS	UART1_TX	—
GPIO70	CLCD_COLOR20	SPI1_SCK	UART1_RX	—
GPIO71	CLCD_COLOR19	I2C2_SCL	—	—
GPIO72	CLCD_COLOR18	I2C2_SDA	—	ETM_CLK
GPIO73	CLCD_COLOR17	—	—	ETM_CTL
GPIO74	CLCD_COLOR16	—	—	ETM_D0
GPIO75	CLCD_COLOR15	—	—	ETM_D1
GPIO76	CLCD_COLOR14	—	—	ETM_D2
GPIO77	CLCD_COLOR13	—	—	ETM_D3
GPIO78	CLCD_COLOR12	—	—	ETM_D4
GPIO79	CLCD_COLOR11	—	—	ETM_D5
GPIO80	CLCD_COLOR10	—	—	ETM_D6
GPIO81	CLCD_COLOR9	—	—	ETM_D7
GPIO82	CLCD_COLOR8	—	—	ETM_D8
GPIO83	CLCD_COLOR7	—	—	ETM_D9
GPIO84	CLCD_COLOR6	—	—	ETM_D10
GPIO85	CLCD_COLOR5	FSMC_ADVn	—	ETM_D11
GPIO86	CLCD_COLOR4	FSMC_CS0n	—	ETM_D12
GPIO87	CLCD_COLOR3	SPI2_TXD	—	ETM_D13
GPIO88	CLCD_COLOR2	SPI2_RXD	—	ETM_D14
GPIO89	CLCD_COLOR1	SPI2_SS	—	ETM_D15
GPIO90	CLCD_COLOR0	SPI2_SCK	—	—
GPIO91	CLCD_PIXCLK1	WDG_SW_RSTOUT	USB1_DRVVBUS	—
GPIO92	FSMC_SMADQ_7	SDMMC2_CMD	—	ETM_D0
GPIO93	FSMC_SMADQ_6	SDMMC2_CLK	—	ETM_D1
GPIO94	FSMC_SMADQ_5	SDMMC2_DATA_0	—	ETM_D2
GPIO95	FSMC_SMADQ_4	SDMMC2_DATA_1	—	ETM_D3
GPIO96	FSMC_SMADQ_3	SDMMC2_DATA_2	—	ETM_D4
GPIO97	FSMC_SMADQ_2	SDMMC2_DATA_3	—	ETM_D5
GPIO98	FSMC_SMADQ_1	SDMMC2_DATA_4	—	ETM_D6
GPIO99	FSMC_SMADQ_0	SDMMC2_DATA_5	—	ETM_D7
GPIO100	FSMC_WPn	SDMMC2_DATA_6	—	ETM_D8
GPIO101	SQI_CE1n	SPI2_SS	—	ETM_D9
GPIO102	FSMC_BUSYn	SDMMC2_DATA_7	—	ETM_D10
GPIO103	FSMC_OEn	SDMMC2_FBCLK	—	ETM_D11

Table 10. Application GPIO alternate function mapping (continued)

GPIO	ALT A	ALT B	ALT C	DEBUG
GPIO104	FSMC_WEn	I2C2_SDA	—	ETM_D12
GPIO105	FSMC_SMAD17/ALE	I2C2_SCL	—	ETM_CLK
GPIO106	FSMC_SMAD16/CLE	UART2_RX	—	ETM_CTL
GPIO107	FSMC_NAND_CS0n	UART2_TX	—	—
GPIO108(1)	SQI_SIO3	SAI4_BCLK	FSMC_SMADQ_10	—
GPIO109(1)	SQI_SIO2	SAI4_FS	FSMC_SMADQ_11	—
GPIO110(1)	SQI_SIO1	SAI4_TX0	FSMC_SMADQ_12	—
GPIO111(1)	SQI_SIO0	SAI4_TX1	FSMC_SMADQ_13	—
GPIO112(1)	SQI_SCK	SAI4_RX0	FSMC_SMADQ_14	—
GPIO113(1)	SQI_CE0n	SAI4_RX1	FSMC_SMADQ_15	—
GPIO114	I2C2_SDA	SDMMC2_DAT0_DIR	ETH_MDIO	—
GPIO115	I2C2_SCL	SDMMC2_DAT31_DIR	ETH_MDC	—
GPIO116	ETH_TXEN	SPI2_TXD	I2S2_TX	—
GPIO117	ETH_TX[0]	SPI2_RXD	I2S2_RX	—
GPIO118	ETH_TX[1]	SPI2_SS	I2S2_FS	—
GPIO119	ETH_RXDV_CRS	SPI2_SCK	I2S2_BCLK	—
GPIO120	ETH_RX[0]	—	—	—
GPIO121	ETH_RX[1]	—	—	—
GPIO122	ETH_RMII_CLK	ETH_MII_RX_CLK	—	—
GPIO123	ETH_TX[2]	UART2_RX	I2S2_TX	—
GPIO124	ETH_TX[3]	UART2_TX	I2S2_RX	—
GPIO125	ETH_RX[2]	ETH_RX_ER	USB0_DRVVBUS	—
GPIO126	ETH_RX[3]	UART3_RX	I2S2_FS	—
GPIO127	ETH_MII_TX_CLK	UART3_TX	I2S2_BCLK	—

1. The default reset state of GPIO108 to GPIO113 depends on the value latched at reset of REMAP[1:0].

0b00: GPIO input

0b01: GPIO input

0b10: ALT-A (SQI interface for XiP)
GPIO108 ALT-A input PU (SQI_SIO3)
GPIO109 ALT-A input PU (SQI_SIO2)
GPIO110 ALT-A input PU (SQI_SIO1)
GPIO110 ALT-A input PU (SQI_SIO1)
GPIO111 ALT-A input PU (SQI_SIO0)
GPIO112 ALT-A output low (SQI_SCK)
GPIO113 ALT-A output high (SQI_CE0n)

0b11: GPIO input

In case of REMAP[1:0]=0b10, the configuration cannot be changed if not through a hardware reset, with a different REMAP configuration.

2.17.2 Secure GPIO alternate function mapping

Note: All GPIOs pins are configured by default at reset in GPIO input mode.

Table 11. Secure GPIO alternate function mapping

GPIO	ALT A	ALT B	ALT C
S_GPIO0	EFT3_ICAP1	EFT3_OCMP0	CAN1_RX
S_GPIO1	EFT3_ICAP0	EFT3_OCMP1	CAN1_TX
S_GPIO2	EFT4_ICAP0	SPI0_RXD	EFT4_EXTCK
S_GPIO3	EFT4_ICAP1	EFT4_OCMP0	CAN2_RX
S_GPIO4	EFT3_OCMP0	SPI0_TXD	EFT3_EXTCK
S_GPIO5	EFT3_ICAP1	EFT4_OCMP0	EFT3_OCMP1
S_GPIO6	SPI0_TXD	EFT4_ICAP0	EFT4_EXTCK
S_GPIO7	SPI0_RXD	EFT4_OCMP1	CAN2_TX
S_GPIO8	SPI0_SCK	—	—
S_GPIO9	SPI0_SS	—	—
S_GPIO10	I2C0_SDA	EFT4_ICAP1	—
S_GPIO11	I2C0_SCL	EFT4_OCMP1	—
S_GPIO12	UART0_RX	CAN2_TX	—
S_GPIO13	UART0_TX	CAN2_RX	—
S_GPIO14	UART0_CTS	EFT4_ICAP1	—
S_GPIO15	UART0_RTS	EFT4_OCMP1	—

2.17.3 Cortex® M3 GPIO alternate function mapping

Table 12. Cortex® M3 GPIO alternate function mapping

GPIO	ALT A	ALT B	ALT C	BOOTSTRAP
M3_GPIO0_WAKE0	—	—	—	—
M3_GPIO1_WAKE1	—	—	—	—
M3_GPIO2_WAKE2	—	—	—	—
M3_GPIO3_WAKE3	—	—	—	—
M3_GPIO4_WAKE4	—	—	—	—
M3_GPIO5_WAKE5	—	—	—	—
M3_GPIO6_WAKE6	—	—	—	—
M3_GPIO7_WAKE7	—	—	—	—
M3_GPIO8	CAN0_TX	—	—	—
M3_GPIO9	CAN0_RX	—	—	—
M3_GPIO10	UART0_RX	—	—	—

Table 12. Cortex® M3 GPIO alternate function mapping (continued)

GPIO	ALT A	ALT B	ALT C	BOOTSTRAP
M3_GPIO11	UART0_CTS	USB0_DRVVBUS	—	—
M3_GPIO12	I2C0_SDA	—	—	—
M3_GPIO13	I2C0_SCL	—	—	—
M3_GPIO14	UART0_TX	—	—	REMAP0
M3_GPIO15	UART0_RTS	CLKOUT0	—	REMAP1

2.18 Generic interfaces

2.18.1 4x UARTS

- Programmable baud rates up to 3 Mbps
- Hardware flow control
- DMA capable

2.18.2 3x I2C

- Master/slave modes in multi-master environment
- Multiple baud rates supported: 100/400/1000/3400 Kbits/s
- DMA capable

2.18.3 3x SSP/SPI ports supporting

- Serial Peripheral Interface bus standards
- Synchronous Serial Protocol bus standards
- Microwire interface bus standards
- Unidirectional interface
- DMA capable

2.19 Input capture / Output compare

Five EFT (Enhanced Function timers) implement a very flexible input capture and output compare feature set. Each EFT block can provide two input capture and two output compare lines (1 PWM). EFT are based on 16-bit counters with dedicated pre-scaler.

2.20 Watchdog and timers

2.20.1 Cortex® A7

It has the following features:

- 2x MTU timers each providing access to four programmable 32-bit Free-Running decrementing Counters (FRCs)
- 1x Watchdog (WDT) unit that provides a way to recover from software crashes
- 1x RTC counter clocked with 32 kHz oscillator

2.20.2 Cortex® M3

It has the following features:

- 1x MTU timers providing access to four programmable 32-bit Free-Running decrementing Counters (FRCs)
- 1x Watchdog (WDT) unit that provides a way to recover from software crashes

3 Package pinouts and signal description

3.1 STA1275 and STA1295 signal description

Table 13. Debug signals

Name	GPIOs	BALLs	DIR	Power domain	Description
STM_D0	GPIO40	C20	I/O	VIO	TPIU: TPIU data line 0
	GPIO55	C15			
STM_D1	GPIO41	C21	I/O	VIO	TPIU: TPIU data line 1
	GPIO56	C16			
STM_D2	GPIO42	C22	I/O	VIO	TPIU: TPIU data line 2
	GPIO57	A16			
STM_D3	GPIO43	C23	I/O	VIO	TPIU: TPIU data line 3
	GPIO58	B18			
STM_CTL	GPIO49	A13	O	VIO	TPIU: TPIU control line
	GPIO59	A17			
STM_CLK	GPIO50	A14	O	VIO	TPIU: TPIU clock line
	GPIO60	B17			
ETM_CTL	GPIO14	AA23	O	VIO	ETM. ETM control line. This signal indicates whether trace can be stored this cycle, in conjunction with TRACEDATA[0]. This signal does not have to be stored.
	GPIO73	AA17			
	GPIO106	D13			
ETM_CLK	GPIO13	C18	O	VIO	ETM. TRACE clock output. The trace port must be sampled on both edges of this clock. There is no requirement for this to be linked to the core clock.
	GPIO72	Y17			
	GPIO105	B13			
ETM_D0	GPIO0	B21	O	VIO	ETM. TRACEDATA0.
	GPIO74	AB17			
	GPIO92	A10			
ETM_D1	GPIO1	B22	O	VIO	ETM. TRACEDATA1.
	GPIO75	AC17			
	GPIO93	C10			
ETM_D10	GPIO10	A20	O	VIO	ETM. TRACEDATA10.
	GPIO84	Y14			
	GPIO102	D11			

Table 13. Debug signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
ETM_D11	GPIO11	A19	O	VIO	ETM. TRACEDATA11.
	GPIO85	AA14			
	GPIO103	E11			
ETM_D12	GPIO12	A21	O	VIO	ETM. TRACEDATA12.
	GPIO86	AC14			
	GPIO104	D12			
ETM_D13	GPIO16	R22	O	VIO	ETM. TRACEDATA13.
	GPIO34	C6			
	GPIO87	AB14			
ETM_D14	GPIO17	Y23	O	VIO	ETM. TRACEDATA14.
	GPIO35	B4			
	GPIO88	Y13			
ETM_D15	GPIO19	P22	O	VIO	ETM. TRACEDATA15.
	GPIO37	A5			
	GPIO89	AA13			
ETM_D2	GPIO2	D19	O	VIO	ETM. TRACEDATA2.
	GPIO76	Y16			
	GPIO94	B11			
ETM_D3	GPIO3	A22	O	VIO	ETM. TRACEDATA3.
	GPIO77	AA16			
	GPIO95	D10			
ETM_D4	GPIO4	B19	O	VIO	ETM. TRACEDATA4.
	GPIO78	AB16			
	GPIO96	E10			
ETM_D5	GPIO5	B20	O	VIO	ETM. TRACEDATA5.
	GPIO79	AC16			
	GPIO97	A11			
ETM_D6	GPIO6	D14	O	VIO	ETM. TRACEDATA6.
	GPIO80	Y15			
	GPIO98	B12			
ETM_D7	GPIO7	T23	O	VIO	ETM. TRACEDATA7.
	GPIO81	AA15			
	GPIO99	C11			

Table 13. Debug signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
ETM_D8	GPIO8	B23	O	VIO	ETM. TRACEDATA8.
	GPIO82	AB15			
	GPIO100	A12			
ETM_D9	GPIO9	A18	O	VIO	ETM. TRACEDATA9.
	GPIO83	AC15			
	GPIO101	F19			
JTAG_TCK	—	AC22	I	VIO	JTAG. Test clock.
JTAG_TDI	—	AB23	I	VIO	JTAG. Test Data In.
JTAG_TDO	—	AB22	O	VIO	JTAG. Test Data Output.
JTAG_TMS	—	AA22	I	VIO	JTAG. Test Mode Select.
JTAG_TRSTn	—	AA21	I	VIO	JTAG. TRSTn. If JTAG/Debug is used, TRSTn must transit from LOW to HIGH before or at same time as PORn. If JTAG/Debug is not used, TRSTn can be left unconnected.

Table 14. Video input signals

Name	GPIOs	BALLs	DIR	Power domain	Description
VIP_DAT0	GPIO62	B16	I	VIO	Video Input Port. Data 0.
VIP_DAT1	GPIO61	C17	I	VIO	Video Input Port. Data 1.
VIP_DAT2	GPIO60	B17	I	VIO	Video Input Port. Data 2.
VIP_DAT3	GPIO59	A17	I	VIO	Video Input Port. Data 3.
VIP_DAT4	GPIO58	B18	I	VIO	Video Input Port. Data 4.
VIP_DAT5	GPIO57	A16	I	VIO	Video Input Port. Data 5.
VIP_DAT6	GPIO56	C16	I	VIO	Video Input Port. Data 6.
VIP_DAT7	GPIO55	C15	I	VIO	Video Input Port. Data 7.
VIP_HSYNCH	GPIO53	A15	I	VIO	Video Input Port. Horizontal synchronization pulse signal.
VIP_PIXCLK	GPIO52	D15	I	VIO	Video Input Port. Pixel clock.
VIP_VSYNCH	GPIO54	D16	I	VIO	Video Input Port. Vertical synchronization pulse signal.

Table 15. Display signals

Name	GPIOs	BALLs	DIR	Power domain	Description
CLCD_COLOR0	GPIO90	AB13	O	VIO	LCD. Display data line RED[0].
CLCD_COLOR1	GPIO89	AA13	O	VIO	LCD. Display data line RED[1].
CLCD_COLOR10	GPIO80	Y15	O	VIO	LCD. Display data line GREEN[2].
CLCD_COLOR11	GPIO79	AC16	O	VIO	LCD. Display data line GREEN[3].
CLCD_COLOR12	GPIO78	AB16	O	VIO	LCD. Display data line GREEN[4].
CLCD_COLOR13	GPIO77	AA16	O	VIO	LCD. Display data line GREEN[5].
CLCD_COLOR14	GPIO76	Y16	O	VIO	LCD. Display data line GREEN[6].
CLCD_COLOR15	GPIO75	AC17	O	VIO	LCD. Display data line GREEN[7].
CLCD_COLOR16	GPIO74	AB17	O	VIO	LCD. Display data line BLUE[0].
CLCD_COLOR17	GPIO73	AA17	O	VIO	LCD. Display data line BLUE[1].
CLCD_COLOR18	GPIO72	Y17	O	VIO	LCD. Display data line BLUE[2].
CLCD_COLOR19	GPIO71	AC18	O	VIO	LCD. Display data line BLUE[3].
CLCD_COLOR20	GPIO70	AB18	O	VIO	LCD. Display data line BLUE[4].
CLCD_COLOR21	GPIO69	AA18	O	VIO	LCD. Display data line BLUE[5].
CLCD_COLOR22	GPIO68	Y18	O	VIO	LCD. Display data line BLUE[6].
CLCD_COLOR23	GPIO67	AC20	O	VIO	LCD. Display data line BLUE[7].
CLCD_PIXCLK1	GPIO91	AC13	O	VIO	LCD. Display pixel clock1 line.
CLCD_COLOR2	GPIO88	Y13	O	VIO	LCD. Display data line RED[2].
CLCD_COLOR3	GPIO87	AB14	O	VIO	LCD. Display data line RED[3].
CLCD_COLOR4	GPIO86	AC14	O	VIO	LCD. Display data line RED[4].
CLCD_COLOR5	GPIO85	AA14	O	VIO	LCD. Display data line RED[5].
CLCD_COLOR6	GPIO84	Y14	O	VIO	LCD. Display data line RED[6].
CLCD_COLOR7	GPIO83	AC15	O	VIO	LCD. Display data line RED[7].
CLCD_COLOR8	GPIO82	AB15	O	VIO	LCD. Display data line GREEN[0].
CLCD_COLOR9	GPIO81	AA15	O	VIO	LCD. Display data line GREEN[1].
CLCD_DE	GPIO66	AC19	O	VIO	LCD. Display data enable line.
CLCD_HSYNCH	GPIO65	AB19	O	VIO	LCD. Display horizontal synchronization line.
CLCD_PIXCLK0	GPIO63	Y19	O	VIO	LCD. Display pixel clock0 line.
CLCD_VSYNCH	GPIO64	AA19	O	VIO	LCD. Display vertical synchronization line.
CLCD_DE1	GPIO54	D16	O	VIO	LCD. Display data enable line for dual display.
CLCD_HSYNCH1	GPIO53	A15	O	VIO	LCD. Display horizontal synchronization line for dual display.

Table 16. System and power management signals

Name	GPIOs	BALLs	DIR	Power domain	Description
CLKOUT0	M3_GPIO15	A9	O	VIO	Programmable clock output 0
CLKOUT1	GPIO51	C5	O	VIO	Programmable clock output 1
WAKE0	—	—	I	VIO_AON	Wake up signal line 0. An event on this line wakes the system up from Stand-By state.
WAKE1	—	—	I	VIO_AON	Wake up signal line 1. An event on this line wakes the system up from Stand-By state.
WAKE2	—	—	I	VIO_AON	Wake up signal line 2. An event on this line wakes the system up from Stand-By state.
WAKE3	—	—	I	VIO_AON	Wake up signal line 3. An event on this line wakes the system up from Stand-By state.
WAKE4	—	—	I	VIO_AON	Wake up signal line 4. An event on this line wakes the system up from Stand-By state.
WAKE5	—	—	I	VIO_AON	Wake up signal line 5. An event on this line wakes the system up from Stand-By state.
WAKE6	—	—	I	VIO_AON	Wake up signal line 6. An event on this line wakes the system up from Stand-By state.
WAKE7	—	—	I	VIO_AON	Wake up signal line 7. An event on this line wakes the system up from Stand-By state.
JTAGSEL	—	H20	I	VIO	Test Signal. It selects whether the JTAG is used for ATE test or as debug port. Connect it to GND in the application.
M3_CLK32KOUT	—	C19	O	VIO_AON	Output 32 kHz clock
M3_IGNKEY	—	M20	I	VIO_AON	PMU Ignition Key signal. Used by PMU to change the state of the system (Normal, Standby). (Edge sensitive).
M3_LVI	—	U23	I	VIO_AON	PMU Low Voltage Indication. With system in OFF state, LVI when high enable the transition to standby or Normal state. With system in Standby or in Normal it indicates a battery low voltage.
M3_ONOFF	—	T21	I	VIO_AON	PMU ON/OFF. Used by PMU to change the state of the system (Normal, Standby). (Edge sensitive).

Table 16. System and power management signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
M3_PWREN	—	V22	O	VIO_AON	PMU Power Enable. Used by the PMU to enable external voltage regulator, when moving out of Standby state.
M3_VDDOK	—	U22	I	VIO_AON	PMU VDDOK. This signal is used by the PMU to detect if the external power is valid. The PMU moves to Normal state if VDDOK = 1.
SYS_MXTALI	—	P20	I	VIO	Crystal input. 24/26 MHz crystal.
SYS_MXTALO	—	N20	O	VIO	Crystal output.
M3_XTALI	—	D17	I	VIO_AON	Crystal input. 32 kHz RTC clock.
M3_XTALO	—	D18	O	VIO_AON	Crystal output.
SYS_SYSRES	—	AC21	I	VIO	System reset active low.
OTP_FUSE_HV	—	F5	P	VIO	OTP programming voltage. Leave it floating in the application.

Table 17. Analog audio signals

Name	GPIOs	BALLs	DIR	Power domain	Description
ADC0_AIN1_L	—	J22	I	ADC0_AVDD	ADC0 (Audio). Analog input 1 left channel.
ADC0_AIN1_R	—	K22	I	ADC0_AVDD	ADC0 (Audio). Analog input 1 right channel.
ADC0_AIN2_L	—	J21	I	ADC0_AVDD	ADC0 Audio). Analog input 2 left channel.
ADC0_AIN2_R	—	L20	I	ADC0_AVDD	ADC0 (Audio). Analog input 2 right channel.
ADC1_AIN1_N	—	K23	I	ADC1_AVDD	ADC1 (Voice). Analog auxiliary differential input 1 negative.
ADC1_AIN1_P	—	J23	I	ADC1_AVDD	ADC1 (Voice). Analog auxiliary differential input 1 positive.
ADC1_MICIN_N	—	H23	I	ADC1_AVDD	ADC1 (Voice). Analog MIC differential input negative.
ADC1_MICIN_P	—	H22	I	ADC1_AVDD	ADC1 (Voice). Analog MIC differential input positive.
DAC_OUT0L	—	G23	O	DAC I/OAVDD	DAC0. Analog output Channel 0 left.
DAC_OUT0R	—	G22	O	DAC I/OAVDD	DAC0. Analog output channel 0 right.
DAC_OUT1L	—	H21	O	DAC I/OAVDD	DAC1. Analog output channel 1 left.
DAC_OUT1R	—	J20	O	DAC I/OAVDD	DAC1. Analog output channel 1 right.
DAC_OUT2L	—	F22	O	DAC I/OAVDD	DAC2. Analog output channel 2 left.
DAC_OUT2R	—	F23	O	DAC I/OAVDD	DAC2. Analog output channel 2 right.

Table 18. Digital audio signals

Name	GPIOs	BALLs	DIR	Power domain	Description
I2S0_BCLK	GPIO22	AB20	I/O	VIO	I2S0 (MSP0). Bit clock line.
I2S2_BCLK	GPIO16	R22	I/O	VIO	I2S2 (MSP2). Bit clock line.
	GPIO119	E4			
	GPIO127	C2			
SAI1_BCLK	GPIO19	P22	I	VIO	Serial Audio Interface 1. Bit Clock line. Slave only configuration.
SAI2_BCLK	GPIO16	R22	I	VIO	Serial Audio Interface 2. Bit clock line. Slave only configuration.
AUDIO_REFCLK	GPIO7	T23	I/O	VIO	Audio Master Clock. Input: it can be used as master audio clock for MSP peripherals. Output: audio master clock.
I2S0_FS	GPIO23	Y20	I/O	VIO	I2S0 (MSP0). Frame Synchronization line.
I2S2_FS	GPIO17	Y23	I/O	VIO	I2S2 (MSP2). Frame Synchronization line.
	GPIO118	E1			
	GPIO126	D4			
SAI1_FS	GPIO20	R21	I	VIO	Serial Audio Interface 1. Frame synchronization line. Slave only configuration.
SAI2_FS	GPIO17	Y23	I	VIO	Serial Audio Interface 2. Frame synchronization line. Slave only configuration.
I2S0_RX	GPIO25	W21	I	VIO	I2S0 (MSP0). Receive data line.
I2S2_RX	GPIO18	R23	I	VIO	I2S2 (MSP2). Receive data line.
	GPIO117	E3			
	GPIO124	D2			
SAI1_RX	GPIO21	P23	I	VIO	Serial Audio Interface 1. Receive data line.
SAI2_RX/TX	GPIO18	R23	I/O	VIO	Serial Audio Interface 2. Receive/transmit data line.
SPDIF_RX	GPIO18	R23	I	VIO	SPIDIF. Data input line.
I2S0_TX	GPIO24	Y21	O	VIO	I2S0 (MSP0). Transmit data line.
I2S2_TX	GPIO7	T23	O	VIO	I2S2 (MSP2). Transmit data line.
	GPIO116	C4			
	GPIO123	D1			
SAI2_TX	GPIO7	T23	O	VIO	Serial Audio Interface 2. Transmit data line.

Table 18. Digital audio signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
SAI3_BCLK	GPIO8	B23	I/O	VIO	Serial Audio Interface 3. Bit clock.
SAI3_FS	GPIO9	A18	I/O	VIO	Serial Audio Interface 3. Frame synchronization line.
SAI3_TX0	GPIO14	AA23	O	VIO	Serial Audio Interface 3. Transmit data line 0.
SAI3_TX1	GPIO11	A19	O	VIO	Serial Audio Interface 3. Transmit data line 1.
SAI3_TX2	GPIO12	A21	O	VIO	Serial Audio Interface 3. Transmit data line 2.
SAI3_RX0	GPIO15	T22	I	VIO	Serial Audio Interface 3. Receive data line 0.
SAI3_RX1	GPIO13	C18	I	VIO	Serial Audio Interface 3. Receive data line 1.
SAI3_RX2	GPIO10	A20	I	VIO	Serial Audio Interface 3. Receive data line 2.
SAI4_BCLK	GPIO3	A22	I/O	VIO	Serial Audio Interface 4. Bit clock.
	GPIO22	AB20			
	GPIO108	E13			
SAI4_FS	GPIO4	B19	I/O	VIO	Serial Audio Interface 4. Frame synchronization line.
	GPIO23	Y20			
	GPIO109	C12			
SAI4_TX0	GPIO2	D19	O	VIO	Serial Audio Interface 4. Transmit data line 0.
	GPIO24	Y21			
	GPIO110	B15			
SAI4_TX1	GPIO0	B21	O	VIO	Serial Audio Interface 4. Transmit data line 1.
	GPIO111	B14			
SAI4_TX2	GPIO1	B22	O	VIO	Serial Audio Interface 4. Transmit data line 2.
SAI4_RX0	GPIO5	B20	I	VIO	Serial Audio Interface 4. Receive data line 0.
	GPIO25	W21			
	GPIO112	C14			
SAI4_RX1	GPIO9	A18	I	VIO	Serial Audio Interface 4. Receive data line 1.
	GPIO113	C13			
SAI4_RX2	GPIO8	B23	I	VIO	Serial Audio Interface 4. Receive data line 2.

Table 19. Peripherals signals

Name	GPIOs	BALLs	DIR	Power domain	Description
CAN0_RX	M3_GPIO9	C8	I	VIO	CAN0. Receive signal line.
CAN0_TX	M3_GPIO8	B10	O	VIO	CAN0. Transmit signal line.
CAN1_RX	S_GPIO0	D6	I	VIO	CAN1. Receive signal line.
CAN1_TX	S_GPIO1	D5	O	VIO	CAN1. Transmit signal line.

Table 19. Peripherals signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
CAN2_RX	S_GPIO3	E6	I	VIO	CAN2. Receive signal line.
	S_GPIO13	W19			
CAN2_TX	S_GPIO7	A6	O	VIO	CAN2. Transmit signal line.
	S_GPIO12	W22			
I2C0_SCL	S_GPIO11	B7	O	VIO	I2C0. Clock line. It needs an external Pull-up.
	M3_GPIO13	B8			
I2C0_SDA	S_GPIO10	B6	I/O	VIO	I2C0. Data line. It needs an external Pull-up.
	M3_GPIO12	D9			
I2C1_SCL	GPIO34	C6	O	VIO	I2C1. Clock line. It needs an external Pull-up.
	GPIO47	E19			
	GPIO50	A14			
I2C1_SDA	GPIO35	B4	I/O	VIO	I2C1. Data line. It needs an external Pull-up.
	GPIO46	E20			
	GPIO49	A13			
I2C2_SCL	GPIO14	AA23	O	VIO	I2C2. Clock line. It needs an external Pull-up.
	GPIO71	AC18			
	GPIO105	B13			
	GPIO115	F1			
I2C2_SDA	GPIO15	T22	I/O	VIO	I2C2. Data line. It needs an external Pull-up.
	GPIO72	Y17			
	GPIO104	D12			
	GPIO114	E5			
SPI0_SCK	S_GPIO8	A7	I/O	VIO	SPI0. Clock signal line.
SPI0_SS	S_GPIO9	A8	I/O	VIO	SPI0. Frame signal line.
SPI0_RXD	S_GPIO2	F20	I	VIO	SPI0. Receive data line.
	S_GPIO7	A6			
SPI0_TXD	S_GPIO4	D7	O	VIO	SPI0. Transmit data line.
	S_GPIO6	B5			
SPI1_SCK	GPIO37	A5	I/O	VIO	SPI1. Clock signal line.
	GPIO70	AB18			
SPI1_SS	GPIO34	C6	I/O	VIO	SPI1. Frame signal.
	GPIO69	AA18			
SPI1_RXD	GPIO36	C7	I	VIO	SPI1. Receive data line.
	GPIO68	Y18			

Table 19. Peripherals signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
SPI1_TXD	GPIO35	B4	O	VIO	SPI1. Transmit data line.
	GPIO67	AC20			
SPI2_SCK	GPIO21	P23	I/O	VIO	SPI2. Clock signal line.
	GPIO29	C3			
	GPIO90	AB13			
	GPIO119	E4			
SPI2_SS	GPIO26	A4	I/O	VIO	SPI2. Frame signal line.
	GPIO89	AA13			
	GPIO101	F19			
	GPIO118	E1			
SPI2_RXD	GPIO20	R21	I	VIO	SPI2. Receive data line.
	GPIO28	A3			
	GPIO88	Y13			
	GPIO117	E3			
SPI2_TXD	GPIO19	P22	O	VIO	SPI2. Transmit data line.
	GPIO27	A2			
	GPIO87	AB14			
	GPIO116	C4			
UART0_CTS	S_GPIO14	AA20	I	VIO	UART0. Clear to send.
	M3_GPIO11	D8			
UART0_RX	S_GPIO12	W22	I	VIO	UART0. Received serial data.
	M3_GPIO10	C9			
UART0_RTS	S_GPIO15	W20	O	VIO	UART0. Request to send.
	M3_GPIO15	A9			
UART0_TX	S_GPIO13	W19	O	VIO	UART0. Transmitted serial data.
	M3_GPIO14	B9			
UART1_RX	GPIO29	C3	I	VIO	UART1. Received serial data.
	GPIO39	B2			
	GPIO41	C21			
	GPIO54	D16			
	GPIO70	AB18			

Table 19. Peripherals signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
UART1_TX	GPIO28	A3	O	VIO	UART1. Transmitted serial data.
	GPIO38	B1			
	GPIO40	C20			
	GPIO53	A15			
	GPIO69	AA18			
UART1_RTS	GPIO45	F11	O	VIO	UART1. Request to send.
	GPIO67	AC20			
UART1_CTS	GPIO44	F12	I	VIO	UART1. Clear to send.
	GPIO68	Y18			
UART2_RX	GPIO13	C18	I	VIO	UART2. Received serial data.
	GPIO42	C22			
	GPIO106	D13			
	GPIO123	D1			
UART2_TX	GPIO12	A21	O	VIO	UART2. Transmitted serial data.
	GPIO43	C23			
	GPIO107	E12			
	GPIO124	D2			
UART3_RX	GPIO37	A5	I	VIO	UART3. Received serial data.
	GPIO44	F12			
	GPIO126	D4			

Table 20. EFT signals

Name	GPIOs	BALLs	DIR	Power domain	Description
EFT0_EXTCK	GPIO26	A4	I	VIO	EFT0. External Input Clock.
	GPIO34	C6			
EFT0_ICAP0	GPIO26	A4	I	VIO	EFT0. Input Capture 0.
	GPIO47	E19			
EFT0_ICAP1	GPIO27	A2	I	VIO	EFT0. Input Capture 1.
	GPIO46	E20			
EFT0_OCMP0	GPIO28	A3	O	VIO	EFT0. Output compare 0.
	GPIO46	E20			
EFT0_OCMP1	GPIO29	C3	O	VIO	EFT0. Output compare 1.
	GPIO47	E19			

Table 20. EFT signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
EFT1_EXTCK	GPIO30	AB21	I	VIO	EFT1 External Input Clock.
	GPIO35	B4			
EFT1_ICAP0	GPIO30	AB21	I	VIO	EFT1. Input Capture 0.
	GPIO38	B1			
EFT1_ICAP1	GPIO31	F4	I	VIO	EFT1. Input Capture 1.
	GPIO39	B2			
EFT1_OCMP0	GPIO33	Y22	O	VIO	EFT1. Output compare 0.
	GPIO37	A5			
EFT1_OCMP1	GPIO32	D20	O	VIO	EFT1. Output compare 1.
	GPIO36	C7			
EFT2_EXTCK	GPIO21	P23	I	VIO	EFT2. External Input Clock.
	GPIO48	E17			
EFT2_ICAP0	GPIO44	F12	I	VIO	EFT2. Input Capture 0.
	GPIO48	E17			
EFT2_ICAP1	GPIO11	A19	I	VIO	EFT2. Input Capture 1.
	GPIO45	F11			
EFT2_OCMP0	GPIO19	P22	O	VIO	EFT2. Output compare 0.
	GPIO48	E17			
EFT2_OCMP1	GPIO10	A20	O	VIO	EFT2. Output compare 1.
	GPIO20	R21			
EFT3_EXTCK	S_GPIO4	D7	I	VIO	EFT3. External input clock.
EFT3_ICAP0	S_GPIO1	D5	I	VIO	EFT3. Input Capture 0.
EFT3_ICAP1	S_GPIO0	D6	I	VIO	EFT3. Input Capture 1.
	S_GPIO5	G20			
EFT3_OCMP0	S_GPIO0	D6	O	VIO	EFT3. Output compare 0.
	S_GPIO4	D7			
EFT3_OCMP1	S_GPIO1	D5	O	VIO	EFT3. Output compare 1.
	S_GPIO5	G20			
EFT4_EXTCK	S_GPIO2	F20	I	VIO	EFT4. External input clock.
	S_GPIO6	B5			
EFT4_ICAP0	S_GPIO2	F20	I	VIO	EFT4. Input Capture 0.
	S_GPIO6	B5			
EFT4_ICAP1	S_GPIO3	E6	I	VIO	EFT4. Input Capture 1.
	S_GPIO10	B6			
	S_GPIO14	AA20			

Table 20. EFT signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
EFT4_OCMP0	S_GPIO3	E6	O	VIO	EFT4. Output compare 0.
	S_GPIO5	G20			
EFT4_OCMP1	S_GPIO7	A6	O	VIO	EFT4. Output compare 1.
	S_GPIO11	B7			
	S_GPIO15	W20			

Table 21. SD MMC signals

Name	GPIOs	BALLs	DIR	Power domain	Description
SDMMC0_DATA_4	GPIO2	D19	I/O	VIO	SD/MMC0. Data line 4.
	GPIO40	C20			
SDMMC0_DATA_5	GPIO3	A22	I/O	VIO	SD/MMC0. Data line 5.
	GPIO41	C21			
SDMMC0_DATA_6	GPIO4	B19	I/O	VIO	SD/MMC0. Data line 6.
	GPIO42	C22			
SDMMC0_DATA_7	GPIO5	B20	I/O	VIO	SD/MMC0. Data line 7.
	GPIO43	C23			
SDMMC0_FBCLK	GPIO31	F4	I	VIO	SD/MMC0. Feedback clock line.
SDMMC0_PWR	GPIO32	D20	O	VIO	SD/MMC0. Power enable.
SDMMC2_DAT31_DIR	GPIO1	B22	O	VIO	SD/MMC2. Data lines 3:1 direction control.
	GPIO33	Y22			
	GPIO115	F1			
SDMMC2_CMDDIR	GPIO27	A2	O	VIO	SD/MMC2. Command line direction control.
SDMMC2_DAT0_DIR	GPIO14	AA23	O	VIO	SD/MMC2. Data 0 line direction control.
	GPIO114	E5			
SDMMC2_DAT2_DIR	GPIO0	B21	O	VIO	SD/MMC2. Data 2 line direction control.
SDMMC2_CMD	GPIO92	A10	I/O	VIO	SD/MMC2. Command line.
SDMMC2_CLK	GPIO93	C10	O	VIO	SD/MMC2. Clock line.
SDMMC2_DATA_0	GPIO94	B11	I/O	VIO	SD/MMC2. Data line 0.
SDMMC2_DATA_1	GPIO95	D10	I/O	VIO	SD/MMC2. Data line 1.
SDMMC2_DATA_2	GPIO96	E10	I/O	VIO	SD/MMC2. Data line 2.
SDMMC2_DATA_3	GPIO97	A11	I/O	VIO	SD/MMC2. Data line 3.
SDMMC2_DATA_4	GPIO98	B12	I/O	VIO	SD/MMC2. Data line 4.
SDMMC2_DATA_5	GPIO99	C11	I/O	VIO	SD/MMC2. Data line 5.

Table 21. SD MMC signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
SDMMC2_DATA_6	GPIO100	A12	I/O	VIO	SD/MMC2. Data line 6.
SDMMC2_DATA_7	GPIO102	D11	I/O	VIO	SD/MMC2. Data line 7.
SDMMC2_FBCLK	GPIO103	E11	I	VIO	SD/MMC2. Feedback clock line.
SDMMC1_CLK	GPIO1	B22	O	VIO	SD/MMC1. Clock line.
	GPIO9	A18			
SDMMC1_CMD	GPIO0	B21	I/O	VIO	SD/MMC1. Command line.
	GPIO8	B23			
SDMMC1_DATA_0	GPIO2	D19	I/O	VIO	SD/MMC1. Data line 0.
	GPIO10	A20			
SDMMC1_DATA_1	GPIO3	A22	I/O	VIO	SD/MMC1. Data line 1.
	GPIO11	A19			
SDMMC1_DATA_2	GPIO4	B19	I/O	VIO	SD/MMC1. Data line 2.
	GPIO12	A21			
SDMMC1_DATA_3	GPIO5	B20	I/O	VIO	SD/MMC1. Data line 3.
	GPIO13	C18			
SDMMC1_DATA_4	GPIO40	C20	I/O	VIO	SD/MMC1. Data line 4.
SDMMC1_DATA_5	GPIO41	C21	I/O	VIO	SD/MMC1. Data line 5.
SDMMC1_DATA_6	GPIO42	C22	I/O	VIO	SD/MMC1. Data line 6.
SDMMC1_DATA_7	GPIO43	C23	I/O	VIO	SD/MMC1. Data line 7.
SDMMC1_FBCLK	GPIO32	D20	I	VIO	SD/MMC1. Feedback clock line.
SDMMC1_DAT31_DIR	GPIO15	T22	O	VIO	SD/MMC1. Data lines 3:1 direction control.
	GPIO50	A14			
SDMMC1_DAT0_DIR	GPIO6	D14	O	VIO	SD/MMC1. Data 0 line direction control.
SDMMC1_CMDDIR	GPIO49	A13	O	VIO	SD/MMC1. Command line direction control.
SDMMC1_DAT2_DIR	GPIO51	C5	O	VIO	SD/MMC1. Data 2 line direction control.
SDMMC0_DATA_0	—	G3	I/O	VIO	SD/MMC0. Data line 0.
SDMMC0_DATA_1	—	G4	I/O	VIO	SD/MMC0. Data line 1.
SDMMC0_DATA_2	—	G2	I/O	VIO	SD/MMC0. Data line 2.
SDMMC0_DATA_3	—	G1	I/O	VIO	SD/MMC0. Data line 3.
SDMMC0_CLK	—	F3	O	VIO	SD/MMC0. Clock line.
SDMMC0_CMD	—	F2	I/O	VIO	SD/MMC0. Command line.

Table 22. General purpose ADC

Name	GPIOs	BALLs	DIR	Power domain	Description
ADC2_AIN4	—	L18	I	ADC2_AVDD	ADC2 (SAR) CH4.
ADC2_AIN5	—	F18	I	ADC2_AVDD	ADC2 (SAR) CH5.
ADC2_AIN6	—	F21	I	ADC2_AVDD	ADC2 (SAR) CH6.
ADC2_AIN7	—	N23	I	ADC2_AVDD	ADC2 (SAR) CH7.
ADC2_AIN8	—	P21	I	ADC2_AVDD	ADC2 (SAR) CH8.
ADC2_AIN9	—	M19	I	ADC2_AVDD	ADC2 (SAR) CH9.
TSC_XP_AIN0	—	D22	I	ADC2_AVDD	ADC2 (SAR) CH 0/Touch screen panel signal XP.
TSC_XN_AIN1	—	D23	I	ADC2_AVDD	ADC2 (SAR) CH 1/Touch screen panel signal XN.
TSC_YP_AIN2	—	E21	I	ADC2_AVDD	ADC2 (SAR) CH 2/Touch screen panel signal YP.
TSC_YN_AIN3	—	D21	I	ADC2_AVDD	ADC2 (SAR) CH3/Touch screen panel signal YN.
ADC3_AIN0	—	N19	I	ADC2_AVDD	ADC3 (SAR) CH0
ADC3_AIN1	—	G19	I	ADC2_AVDD	ADC3 (SAR) CH1
ADC3_AIN2	—	G21	I	ADC2_AVDD	ADC3 (SAR) CH2
ADC3_AIN3	—	V19	I	ADC2_AVDD	ADC3 (SAR) CH3
ADC3_AIN4	—	N21	I	ADC2_AVDD	ADC3 (SAR) CH4
ADC3_AIN5	—	N22	I	ADC2_AVDD	ADC3 (SAR) CH5

Table 23. USB signals

Name	GPIOs	BALLs	DIR	Power domain	Description
USB1_DRVVBUS	GPIO30	AB21	O	VIO	It can be used to enable the VBUS when USB1 is in host mode.
	GPIO91	AC13			
USB0_DRVVBUS	GPIO125	C1	O	VIO	It can be used to enable the VBUS when USB0 is in host mode.
	M3_GPIO11	D8			
USB_REXT	—	L19	P	VIO	Connect to GND with a 3 kOhm 1% resistor.
USB0_DN	—	M23	I/O	USB0_VDD3V3	USB0. Differential line D-.
USB0_DP	—	M22	I/O	USB0_VDD3V3	USB0. Differential line D+.
USB1_DN	—	L23	I/O	USB1_VDD3V3	USB1. Differential line D-.
USB1_DP	—	L22	I/O	USB1_VDD3V3	USB1. Differential line D+.

Table 24. Ethernet Mac interface

Name	GPIOs	BALLs	DIR	Power domain	Description
ETH_TXEN	GPIO116	C4	O	VIO	RGMII: TX_CTL RMII: TX_EN
ETH_TX[0]	GPIO117	E3	O	VIO	Transmit data line 0
ETH_TX[1]	GPIO118	E1	O	VIO	Transmit data line 1
ETH_TX[2]	GPIO123	D1	O	VIO	Transmit data line 2. Used only in RGMII mode.
ETH_TX[3]	GPIO124	D2	O	VIO	Transmit data line 2. Used only in RGMII mode.
ETH_RXDV_CRS	GPIO119	E4	I	VIO	RMII mode: RX_ CRS/DV RGMII mode: RX_CTL
ETH_RX[0]	GPIO120	B3	I	VIO	Receive data line 0
ETH_RX[1]	GPIO121	E2	I	VIO	Receive data line 1
ETH_RX[2]	GPIO125	C1	I	VIO	Receive data line 2. Used only in RGMII mode.
ETH_RX[3]	GPIO126	D4	I	VIO	Receive data line 3. Used only in RGMII mode.
ETH_MDIO	GPIO38	B1	I/O	VIO	Management interface Data line
	GPIO114	E5			
ETH_MDC	GPIO39	B2	O	VIO	Management interface Clock line
	GPIO115	F1			
ETH_RMII_CLK	GPIO122	D3	I	VIO	RMII mode only: Reference clock
ETH_MII_TX_CLK	GPIO127	C2	O	VIO	RGMII mode only: Transmit clock

Table 25. Power signals

Name	GPIOs	BALLs	DIR	Power domain	Description
VDD	—	F13	P	—	Core and ARM M3 supply
	—	F15		—	
	—	G11		—	
	—	G12		—	
	—	G13		—	
	—	G14		—	
	—	H13		—	
	—	H15		—	
	—	J9		—	
	—	J10		—	
	—	J11		—	
	—	J12		—	
	—	J14		—	
	—	J16		—	
	—	K9		—	
	—	K15		—	
	—	L9		—	
	—	M9		—	
	—	M15		—	
	—	N9		—	
	—	P9		—	
	—	P15		—	
	—	R9		—	
	—	R10		—	
	—	R11		—	
	—	R12		—	
	—	R14		—	
ARM_VDD	—	R16	P	—	ARM A7 supply
	—	R17		—	
	—	T16		—	
	—	T17		—	
	—	T18		—	
	—	T19		—	
	—	U17		—	

Table 25. Power signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
ARM_VDD (Cont'd)	—	U18	P	—	ARM A7 supply
	—	U19		—	
VDD_IO_ON	—	E16	P	—	3.3 V Always_on supply
VDD_ON_VREG	—	E18	P	—	1.2 V (LDO) Always_on output voltage. Connect it to a 2.2nF capacitor to GND.
PLL_VREG3.3V	—	P17	P	—	3.3 V for PLLs voltage regulator (LDOs)
VDD_IO_3V3	—	E7	P	—	3.3 V Digital I/O supply
	—	F6		—	
	—	F7		—	
	—	F8		—	
	—	F9		—	
	—	F10		—	
	—	G8		—	
	—	G9		—	
	—	G10		—	
	—	H9		—	
	—	H10		—	
	—	H11		—	
	—	T13		—	
	—	T14		—	
	—	T15		—	
	—	U13		—	
	—	U14		—	
	—	U15		—	
	—	U16		—	
	—	V13		—	
	—	V14		—	
	—	V15		—	
VDD_IO_1V8	—	H7	P	—	1.8 V or 3.3 V for SDMMC0 (4 bit only) and GPIO31
GND	—	A1	P	—	Digital ground
	—	A23		—	
	—	E8		—	

Table 25. Power signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
GND (Cont'd)	—	E9	P	—	Digital ground
	—	E15		—	
	—	F14		—	
	—	H2		—	
	—	H4		—	
	—	H6		—	
	—	H8		—	
	—	H12		—	
	—	H14		—	
	—	H16		—	
	—	J1		—	
	—	J8		—	
	—	J13		—	
	—	J15		—	
	—	K3		—	
	—	K8		—	
	—	K10		—	
	—	K11		—	
	—	K12		—	
	—	K13		—	
	—	K14		—	
	—	L1		—	
	—	L8		—	
	—	L10		—	
	—	L11		—	
	—	L12		—	
	—	L13		—	
	—	L14		—	
	—	L15		—	
	—	M1		—	
	—	M8		—	
	—	M10		—	
	—	M11		—	
	—	M12		—	

Table 25. Power signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
GND (Cont'd)	—	M13	P	—	Digital ground
	—	M14		—	
	—	N3		—	
	—	N8		—	
	—	N10		—	
	—	N11		—	
	—	N12		—	
	—	N13		—	
	—	N14		—	
	—	N15		—	
	—	P1		—	
	—	P8		—	
	—	P10		—	
	—	P11		—	
	—	P12		—	
	—	P13		—	
	—	P14		—	
	—	R3		—	
	—	R8		—	
	—	R13		—	
	—	R15		—	
	—	T1		—	
	—	T5		—	
	—	T8		—	
	—	T9		—	
	—	T10		—	
	—	T11		—	
	—	T12		—	
	—	U6		—	
	—	V1		—	
	—	V11		—	
	—	V12		—	
	—	W3		—	
	—	Y1		—	

Table 25. Power signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
GND (Cont'd)	—	Y12	P	—	Digital ground
	—	AA4		—	
	—	AA7		—	
	—	AA10		—	
	—	AB12		—	
	—	AC1		—	
	—	AC6		—	
	—	AC8		—	
	—	AC9		—	
	—	AC11		—	
	—	AC23		—	
VDD_2_5V	—	E14	P	—	2.5 V LDO (PLL) output voltage. Connect it to a 4.7 uF capacitor to GND.
VDD_2_5V_XOSC	—	R19	P	—	2.5 V supply for internal oscillator to be shorted with VDD_2_5V.
VDD_2_5V_PLL3_4	—	P16	P	—	2.5 V supply for PLL3 and PLL4 to be shorted with VDD_2_5V.
VDD_2_5V_PLL1_2	—	P18	P	—	2.5 V supply for PLL1 and PLL2 to be shorted with VDD_2_5V.
XOSC_AGND	—		P	—	Analog ground
SOC_AGND	—	W18	P	—	Analog ground
OSC32K_GND	—	F16	P	—	Digital ground
VDDQ	—	H1	P	—	DDR3L I/O power
	—	H3		—	
	—	H5		—	
	—	J7		—	
	—	K4		—	
	—	K7		—	
	—	L7		—	
	—	M7		—	
	—	N4		—	
	—	N7		—	
	—	P7		—	
	—	R7		—	
	—	T4		—	

Table 25. Power signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
VDDQ (Cont'd)	—	T6	P	—	DDR3L I/O power
	—	T7		—	
	—	U1		—	
	—	U7		—	
	—	U8		—	
	—	U9		—	
	—	U10		—	
	—	U11		—	
	—	U12		—	
	—	V10		—	
	—	W12		—	
	—	Y4		—	
	—	Y7		—	
	—	Y10		—	
	—	AA12		—	
	—	AB1		—	
	—	AC2		—	
	—	AC12		—	
VREF	—	M6	P	—	DDR3L reference voltage typically 0.5*VDDQ
	—	V9		—	
PLL_VDD	—	L6	P	—	2.5 V for DDR_PLL to be shorted with DDR_PLL_2V5
	—	N6		—	
	—	V7		—	
DDR_PLL_2V5	—	W15	P	—	2.5 V LDO (PLL) output voltage (Analog power for DDR_PLL). Connect it to a 4.7 uF capacitor to GND.
DDR_PLL_3V3	—	W14	P	—	3.3 V for DDR_PLL LDO
DDR_PLL_DVDD	—	W13	P	—	1.2 V Digital supply for DDR PLL
DDR_PLL_DGND	—	W17	P	—	Digital ground
DDR_PLL_AGND	—	W16	P	—	Analog ground
PLL_VSS	—	K6	P	—	Analog ground
	—	P6		—	
	—	V8		—	

Table 25. Power signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
ADC0_1_AVDD	—	M16	P	—	ADC0 and ADC1 analog 3.3 V supply.
ADC0_1_AGND	—	N16	P	—	ADC0 and ADC1 analog 3.3 V supply ground.
ADC0_1_VCM	—	K19	P	—	ADC0, ADC1 common voltage. Connect 10nF and 10uF capacitors connected to GND.
ADC0_1_VRFN	—	L16	P	—	ADC0 and ADC1 Vref negative. Connect it to GND.
ADC0_1_VRFP	—	K20	P	—	ADC0 and ADC1 Vref positive. Connect 10nF and 10uF capacitors connected to GND.
MIC_BIAS	—	K21	P	—	Bias voltage for microphone. 2.5 V +/- 5% 4mA max.
DAC_IO_AGND	—	H19	P	—	DAC0, DAC1, DAC2 I/O analog 3.3 V supply.
	—	K18		—	
DAC_IO_AVDD	—	G18	P	—	DAC0, DAC1, DAC2 I/O analog 3.3 V supply ground.
	—	J19		—	
DAC_AVDD	—	J18	P	—	DAC0, DAC1, DAC2 analog 3.3 V supply.
DAC_AGND	—	H18	P	—	DAC0, DAC1, DAC2 analog 3.3 V supply ground.
DAC_VCOM	—	E22	P	—	DAC0, DAC1, DAC2 common voltage. Connect 10 nF and 10 uF capacitors to DAC_AGND.
DAC_VHI	—	E23	P	—	DAC0, DAC1, DAC2 analog positive reference. Connect 10 nF and 10 uF capacitors to DAC_AGND.
DAC_VLO	—	K17	P	—	DAC0, DAC1, DAC2 analog negative reference. Connect it to DAC_AGND.
ADC2_3_AVDD	—	G16	P	—	ADC2 (SAR) analog 3.3 V supply.
	—	H17		—	
ADC2_3_AGND	—	G15	P	—	ADC2 (SAR) analog 3.3 V supply ground.
ADC2_VREFN	—	J17	P	—	ADC2 (SAR) Vref negative. Connect it to ADC2_3_AGND.
ADC2_VREFP	—	P19	P	—	ADC2 (SAR) Vref positive.

Table 25. Power signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
ADC3_VREFN	—	G17	P	—	ADC3 (SAR) Vref negative. Connect it to ADC2_3_AGND.
ADC3_VREFP	—	K16	P	—	ADC3 (SAR) Vref positive.
USB0_VDD3V3	—	N17	P	—	USB0 3.3 V supply.
USB0_AGND	—	M18	P	—	USB0 analog supply ground.
USB1_VDD3V3	—	N18	P	—	USB1 3.3 V supply.
USB1_AGND	—	M17	P	—	USB1 3.3 V supply.
USB_VREG_1V1	—	L21	P	—	LDO 1.1 V (USB) output. Connect it to 4.7 uF capacitor to GND.
USB_VREG_1V8	—	M21	P	—	LDO 1.8 V (USB) output. Connect it to 4.7 uF capacitor to GND.
USB_VREG3V3_1V1	—	L17	P	—	LDO 1.1 V (USB) 3.3 V supply.
USB_VREG3V3_1V8	—	R18	P	—	LDO 1.8 V (USB) 3.3 V supply.
COMP0	—	G6	P	—	Compensation cell input. Connect to external 121 kOhm res. 1% to GND.
COMP1	—	G5	P	—	Compensation cell input. Connect to external 121 kOhm res. 1% to GND.
COMP2	—	V17	P	—	Compensation cell input. Connect to external 121 kOhm res. 1% to GND.
GNDBGCOMP1	—	G7	P	—	Analog ground
GNDBGCOMP2	—	V18	P	—	Analog ground
VREG_BYPASS	—	F17	P	—	Test signal. Connect it to GND on the application board.

Table 26. Memory signals

Name	GPIOs	BALLs	DIR	Power domain	Description
FSMC_SMAD16/CLE	GPIO106	D13	O	VIO	FSMC. Address line 16 - NAND CLE.
FSMC_SMAD17/ALE	GPIO105	B13	O	VIO	FSMC. Address line 17 - NAND ALE.
SQI_CE1n	GPIO101	F19	O	VIO	SQI. Chip select 1 (active low).
FSMC_NAND_CS0N	GPIO107	E12	O	VIO	FSMC. NAND chip select. (active low).
SQI_CE0n	GPIO113	C13	O	VIO	SQI. Chip select 0 (active low).

Table 26. Memory signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
FSMC_ADVn	GPIO85	AA14	O	VIO	FSMC Address Valid. When low indicates address valid on SMADQ bus.
FSMC_DACK	GPIO16	R22	O	VIO	FSMC. External DMA transfer request acknowledge.
	GPIO31	F4			
FSMC_DREQ	GPIO17	Y23	I	VIO	FSMC. External DMA transfer request.
	GPIO33	Y22			
SQI_FDBSCK	GPIO6	D14	I	VIO	SQI. Feedback clock. It must be used for clock frequencies above 60 MHz.
FSMC_WPn	GPIO100	A12	O	VIO	FSMC Write protect. (active low).
FSMC_SMADQ_0	GPIO99	C11	I/O	VIO	FSMC. Multiplexed address/data line 0.
FSMC_SMADQ_1	GPIO98	B12	I/O	VIO	FSMC. Multiplexed address/data line 1.
FSMC_SMADQ_4	GPIO95	D10	I/O	VIO	FSMC. Multiplexed address/data line 4.
FSMC_SMADQ_5	GPIO94	B11	I/O	VIO	FSMC. Multiplexed address/data line 5.
FSMC_SMADQ_6	GPIO93	C10	I/O	VIO	FSMC. Multiplexed address/data line 6.
FSMC_SMADQ_7	GPIO92	A10	I/O	VIO	FSMC. Multiplexed address/data line 7.
FSMC_SMADQ_8	GPIO49	A13	I/O	VIO	FSMC. Multiplexed address/data line 8.
FSMC_SMADQ_9	GPIO50	A14	I/O	VIO	FSMC. Multiplexed address/data line 9.
FSMC_SMADQ_10	GPIO108	E13	I/O	VIO	FSMC. Multiplexed address/data line 10.
FSMC_SMADQ_11	GPIO109	C12	I/O	VIO	FSMC. Multiplexed address/data line 11.
FSMC_SMADQ_12	GPIO110	B15	I/O	VIO	FSMC. Multiplexed address/data line 12.
FSMC_SMADQ_13	GPIO111	B14	I/O	VIO	FSMC. Multiplexed address/data line 13.
FSMC_SMADQ_14	GPIO112	C14	I/O	VIO	FSMC. Multiplexed address/data line 14.
FSMC_SMADQ_15	GPIO113	C13	I/O	VIO	FSMC. Multiplexed address/data line 15.
FSMC_SMADQ_2	GPIO97	A11	I/O	VIO	FSMC. Multiplexed address/data line 2.

Table 26. Memory signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
FSMC_SMADQ_3	GPIO96	E10	I/O	VIO	FSMC. Multiplexed address/data line 3.
FSMC_OEn	GPIO103	E11	O	VIO	FSMC. Output enable signal (active low).
SQI_SCK	GPIO112	C14	O	VIO	SQI. Clock line.
SQI_SIO0	GPIO111	B14	I/O	VIO	SQI. Data line 0.
SQI_SIO1	GPIO110	B15	I/O	VIO	SQI. Data line 1.
SQI_SIO2	GPIO109	C12	I/O	VIO	SQI. Data line 2.
SQI_SIO3	GPIO108	E13	I/O	VIO	SQI. Data line 3.
FSMC_BUSYn	GPIO102	D11	I	VIO	FSMC Busy. Busy signal for NAND flash memory (active low). It needs an external PU.
FSMC_ADVn	GPIO85	AA14	O	VIO	FSMC Address Valid. When low indicates address valid on SMADQ bus.
FSMC_WEn	GPIO104	D12	O	VIO	FSMC Write Enable. For SRAM/NOR-Flash and NAND-Flash (active low).
DDR_DQ31	—	Y8	I/O	DDR_VIO	Data line 31
DDR_DQ30	—	AA8	I/O	DDR_VIO	Data line 30
DDR_DQ29	—	W7	I/O	DDR_VIO	Data line 29
DDR_DQ28	—	AB8	I/O	DDR_VIO	Data line 28
DDR_DQ27	—	W6	I/O	DDR_VIO	Data line 27
DDR_DQ26	—	Y6	I/O	DDR_VIO	Data line 26
DDR_DQ25	—	AA6	I/O	DDR_VIO	Data line 25
DDR_DQ24	—	AB6	I/O	DDR_VIO	Data line 24
DDR_DQ23	—	Y11	I/O	DDR_VIO	Data line 23
DDR_DQ22	—	AA11	I/O	DDR_VIO	Data line 22
DDR_DQ21	—	AB11	I/O	DDR_VIO	Data line 21
DDR_DQ20	—	W10	I/O	DDR_VIO	Data line 20
DDR_DQ19	—	W9	I/O	DDR_VIO	Data line 19
DDR_DQ18	—	Y9	I/O	DDR_VIO	Data line 18
DDR_DQ17	—	AA9	I/O	DDR_VIO	Data line 17
DDR_DQ16	—	AB9	I/O	DDR_VIO	Data line 16
DDR_DQ15	—	L3	I/O	DDR_VIO	Data line 15
DDR_DQ14	—	L4	I/O	DDR_VIO	Data line 14
DDR_DQ13	—	L5	I/O	DDR_VIO	Data line 13

Table 26. Memory signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
DDR_DQ12	—	K5	I/O	DDR_VIO	Data line 12
DDR_DQ11	—	J5	I/O	DDR_VIO	Data line 11
DDR_DQ10	—	J2	I/O	DDR_VIO	Data line 10
DDR_DQ9	—	J3	I/O	DDR_VIO	Data line 9
DDR_DQ8	—	J4	I/O	DDR_VIO	Data line 8
DDR_DQ7	—	P4	I/O	DDR_VIO	Data line 7
DDR_DQ6	—	P3	I/O	DDR_VIO	Data line 6
DDR_DQ5	—	P2	I/O	DDR_VIO	Data line 5
DDR_DQ4	—	N5	I/O	DDR_VIO	Data line 4
DDR_DQ3	—	M5	I/O	DDR_VIO	Data line 3
DDR_DQ2	—	M4	I/O	DDR_VIO	Data line 2
DDR_DQ1	—	M3	I/O	DDR_VIO	Data line 1
DDR_DQ0	—	M2	I/O	DDR_VIO	Data line 0
DDR_CKE0	—	U2	O	DDR_VIO	Clock enable rank 0
DDR_CKE1	—	U3	O	DDR_VIO	Clock enable rank 1
DDR_CK	—	W1	O	DDR_VIO	Clock
DDR_CKn	—	W2	O	DDR_VIO	Inverted Clock
DDR_ODT0	—	T2	O	DDR_VIO	Data termination enable rank 0
DDR_ODT1	—	T3	O	DDR_VIO	Data termination enable rank 1
DDR_BA2	—	U4	O	DDR_VIO	Bank address 2
DDR_BA1	—	V3	O	DDR_VIO	Bank address 1
DDR_BA0	—	V2	O	DDR_VIO	Bank address 0
DDR_CS0n	—	R4	O	DDR_VIO	Chip select rank 0
DDR_CS1n	—	R5	O	DDR_VIO	Chip select rank 1
DDR_DM3	—	W8	O	DDR_VIO	Data mask byte 3
DDR_DM2	—	W11	O	DDR_VIO	Data mask byte 2
DDR_DM1	—	L2	O	DDR_VIO	Data mask byte 1
DDR_DM0	—	P5	O	DDR_VIO	Data mask byte 0
DDR_DQS0	—	N1	O	DDR_VIO	Data strobe byte 0
DDR_DQS0n	—	N2	I/O	DDR_VIO	Inverted data strobe byte 0
DDR_DQS1	—	K2	I/O	DDR_VIO	Data strobe byte 1
DDR_DQS1n	—	K1	I/O	DDR_VIO	Inverted data strobe byte 1
DDR_DQS2	—	AC10	I/O	DDR_VIO	Data strobe byte 2
DDR_DQS2n	—	AB10	I/O	DDR_VIO	Inverted data Strobe byte 2

Table 26. Memory signals (continued)

Name	GPIOs	BALLs	DIR	Power domain	Description
DDR_DQS3	—	AC7	I/O	DDR_VIO	Data strobe byte 3
DDR_DQS3n	—	AB7	I/O	DDR_VIO	Inverted data strobe byte 3
DDR_RESETn	—	AC5	O	DDR_VIO	Reset
DDR_RASn	—	R1	O	DDR_VIO	Command signal row address strobe
DDR_CASn	—	R2	O	DDR_VIO	Command signal column address strobe
DDR_WEn	—	R6	O	DDR_VIO	Command signal write enable
DDR_AD15	—	V6	O	DDR_VIO	Address line 15
DDR_AD14	—	Y5	O	DDR_VIO	Address line 14
DDR_AD13	—	W5	O	DDR_VIO	Address line 13
DDR_AD12	—	W4	O	DDR_VIO	Address line 12
DDR_AD11	—	AA5	O	DDR_VIO	Address line 11
DDR_AD10	—	AB4	O	DDR_VIO	Address line 10
DDR_AD9	—	AC4	O	DDR_VIO	Address line 9
DDR_AD8	—	Y3	O	DDR_VIO	Address line 8
DDR_AD7	—	AA3	O	DDR_VIO	Address line 7
DDR_AD6	—	AB3	O	DDR_VIO	Address line 6
DDR_AD5	—	AC3	O	DDR_VIO	Address line 5
DDR_AD4	—	AA2	O	DDR_VIO	Address line 4
DDR_AD3	—	AB2	O	DDR_VIO	Address line 3
DDR_AD2	—	Y2	O	DDR_VIO	Address line 2
DDR_AD1	—	AA1	O	DDR_VIO	Address line 1
DDR_AD0	—	V4	O	DDR_VIO	Address line 0
DDR_DTO_0	—	V5	I	DDR_VIO	Test signal
DDR_DTO_1	—	U5	I	DDR_VIO	Test signal
DDR_ZQ	—	J6	I	DDR_VIO	Calibration reference
DDR_ATO	—	AB5	I	DDR_VIO	Test signal

3.2 STA1275 and STA1295 ball list

Table 27. STA1275 and STA1295 ball list

Ball	Signal	Pull up/down	Driving strength
A1	GND	—	—
A2	GPIO27	PU	4
A3	GPIO28	PU	4
A4	GPIO26	PU	4
A5	GPIO37	PU	4
A6	S_GPIO7	PU	4
A7	S_GPIO8	PU	4
A8	S_GPIO9	PU	4
A9	M3_GPIO15	PU	4
A10	GPIO92	PU	8
A11	GPIO97	PU	8
A12	GPIO100	PU	8
A13	GPIO49	PU	4
A14	GPIO50	PU	4
A15	GPIO53	PU	4
A16	GPIO57	PU	2
A17	GPIO59	PU	2
A18	GPIO9	PU	8
A19	GPIO11	PU	8
A20	GPIO10	PU	8
A21	GPIO12	PU	8
A22	GPIO3	PU	8
A23	GND	—	—
B1	GPIO38	PU	4
B2	GPIO39	PU	4
B3	GPIO120	PU	2
B4	GPIO35	PU	4
B5	S_GPIO6	PU	4
B6	S_GPIO10	PU	4
B7	S_GPIO11	PU	4
B8	M3_GPIO13	PU	4
B9	M3_GPIO14	PU	4
B10	M3_GPIO8	PU	2

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
B11	GPIO94	PU	8
B12	GPIO98	PU	8
B13	GPIO105	PU	4
B14	GPIO111	PU	8
B15	GPIO110	PU	8
B16	GPIO62	PU	2
B17	GPIO60	PU	2
B18	GPIO58	PU	2
B19	GPIO4	PU	8
B20	GPIO5	PU	8
B21	GPIO0	PU	8
B22	GPIO1	PU	8
B23	GPIO8	PU	8
C1	GPIO125	PU	8
C2	GPIO127	PU	8
C3	GPIO29	PU	4
C4	GPIO116	PU	8
C5	GPIO51	PU	4
C6	GPIO34	PU	4
C7	GPIO36	PD	4
C8	M3_GPIO9	PU	2
C9	M3_GPIO10	PU	2
C10	GPIO93	PU	8
C11	GPIO99	PU	8
C12	GPIO109	PU	8
C13	GPIO113	Disabled	8
C14	GPIO112	Disabled	8
C15	GPIO55	PU	2
C16	GPIO56	PU	2
C17	GPIO61	PU	2
C18	GPIO13	PU	8
C19	M3_CLK32KOUT	—	—
C20	GPIO40	PU	8
C21	GPIO41	PU	8
C22	GPIO42	PU	8

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
C23	GPIO43	PU	8
D1	GPIO123	PU	8
D2	GPIO124	PU	8
D3	GPIO122	PU	8
D4	GPIO126	PU	8
D5	S_GPIO1	PU	4
D6	S_GPIO0	PU	4
D7	S_GPIO4	PU	4
D8	M3_GPIO11	PU	2
D9	M3_GPIO12	PU	4
D10	GPIO95	PU	8
D11	GPIO102	PU	8
D12	GPIO104	PU	4
D13	GPIO106	PU	4
D14	GPIO6	PU	8
D15	GPIO52	PU	2
D16	GPIO54	PU	2
D17	M3_XTALI	—	—
D18	M3_XTALO	—	—
D19	GPIO2	PU	8
D20	GPIO32	PU	4
D21	TSC_YN_AIN3	—	—
D22	TSC_XP_AIN0	—	—
D23	TSC_XN_AIN1	—	—
E1	GPIO118	PU	8
E2	GPIO121	PU	2
E3	GPIO117	PU	8
E4	GPIO119	PU	8
E5	GPIO114	PU	4
E6	S_GPIO3	PU	4
E7	VDD_IO_3V3	—	—
E8	GND	—	—
E9	GND	—	—
E10	GPIO96	PU	8
E11	GPIO103	PU	8

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
E12	GPIO107	PU	4
E13	GPIO108	PU	8
E14	VDD_2_5V	—	—
E15	GND	—	—
E16	VDD_IO_ON	—	—
E17	GPIO48	PU	4
E18	VDD_ON_VREG	—	—
E19	GPIO47	PU	4
E20	GPIO46	PU	4
E21	TSC_YP_AIN2	—	—
E22	DAC_VCOM	—	—
E23	DAC_VHI	—	—
F1	GPIO115	PU	4
F2	SDMMC0_CMD	—	—
F3	SDMMC0_CLK	—	—
F4	GPIO31	PU	8
F5	OTP_FUSE_HV	—	—
F6	VDD_IO_3V3	—	—
F7	VDD_IO_3V3	—	—
F8	VDD_IO_3V3	—	—
F9	VDD_IO_3V3	—	—
F10	VDD_IO_3V3	—	—
F11	GPIO45	PU	4
F12	GPIO44	PU	2
F13	VDD	—	—
F14	GND	—	—
F15	VDD	—	—
F16	OSC32K_GND	—	—
F17	VREG_BYPASS	—	—
F18	ADC2_AIN5	—	—
F19	GPIO101	PU	4
F20	S_GPIO2	PU	2
F21	ADC2_AIN6	—	—
F22	DAC_OUT2L	—	—
F23	DAC_OUT2R	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
G1	SDMMC0_DATA_3	—	—
G2	SDMMC0_DATA_2	—	—
G3	SDMMC0_DATA_0	—	—
G4	SDMMC0_DATA_1	—	—
G5	COMP1	—	—
G6	COMP0	—	—
G7	GNDBGCOMP1	—	—
G8	VDD_IO_3V3	—	—
G9	VDD_IO_3V3	—	—
G10	VDD_IO_3V3	—	—
G11	VDD	—	—
G12	VDD	—	—
G13	VDD	—	—
G14	VDD	—	—
G15	ADC2_3_AGND	—	—
G16	ADC2_3_AVDD	—	—
G17	ADC3_VREFN	—	—
G18	DAC_IO_AVDD	—	—
G19	ADC3_AIN1	—	—
G20	S_GPIO5	PU	4
G21	ADC3_AIN2	—	—
G22	DAC_OUT0R	—	—
G23	DAC_OUT0L	—	—
H1	VDDQ	—	—
H2	GND	—	—
H3	VDDQ	—	—
H4	GND	—	—
H5	VDDQ	—	—
H6	GND	—	—
H7	VDD_IO_1V8	—	—
H8	GND	—	—
H9	VDD_IO_3V3	—	—
H10	VDD_IO_3V3	—	—
H11	VDD_IO_3V3	—	—
H12	GND	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
H13	VDD	—	—
H14	GND	—	—
H15	VDD	—	—
H16	GND	—	—
H17	ADC2_3_AVDD	—	—
H18	DAC_AGND	—	—
H19	DAC_IO_AGND	—	—
H20	JTAGSEL	—	—
H21	DAC_OUT1L	—	—
H22	ADC1_MICIN_P	—	—
H23	ADC1_MICIN_N	—	—
J1	GND	—	—
J2	DDR_DQ10	—	—
J3	DDR_DQ9	—	—
J4	DDR_DQ8	—	—
J5	DDR_DQ11	—	—
J6	DDR_ZQ	—	—
J7	VDDQ	—	—
J8	GND	—	—
J9	VDD	—	—
J10	VDD	—	—
J11	VDD	—	—
J12	VDD	—	—
J13	GND	—	—
J14	VDD	—	—
J15	GND	—	—
J16	VDD	—	—
J17	ADC2_VREFN	—	—
J18	DAC_AVDD	—	—
J19	DAC_IO_AVDD	—	—
J20	DAC_OUT1R	—	—
J21	ADC0_AIN2_L	—	—
J22	ADC0_AIN1_L	—	—
J23	ADC1_AIN1_P	—	—
K1	DDR_DQS1n	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
K2	DDR_DQS1	—	—
K3	GND	—	—
K4	VDDQ	—	—
K5	DDR_DQ12	—	—
K6	PLL_VSS	—	—
K7	VDDQ	—	—
K8	GND	—	—
K9	VDD	—	—
K10	GND	—	—
K11	GND	—	—
K12	GND	—	—
K13	GND	—	—
K14	GND	—	—
K15	VDD	—	—
K16	ADC3_VREFP	—	—
K17	DAC_VLO	—	—
K18	DAC_IO_AGND	—	—
K19	ADC0_1_VCM	—	—
K20	ADC0_1_VRFP	—	—
K21	MIC_BIAS	—	—
K22	ADC0_AIN1_R	—	—
K23	ADC1_AIN1_N	—	—
L1	GND	—	—
L2	DDR_DM1	—	—
L3	DDR_DQ15	—	—
L4	DDR_DQ14	—	—
L5	DDR_DQ13	—	—
L6	PLL_VDD	—	—
L7	VDDQ	—	—
L8	GND	—	—
L9	VDD	—	—
L10	GND	—	—
L11	GND	—	—
L12	GND	—	—
L13	GND	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
L14	GND	—	—
L15	GND	—	—
L16	ADC0_1_VRFN	—	—
L17	USB_VREG3V3_1V1	—	—
L18	ADC2_AIN4	—	—
L19	USB_REXT	—	—
L20	ADC0_AIN2_R	—	—
L21	USB_VREG_1V1	—	—
L22	USB1_DP	—	—
L23	USB1_DN	—	—
M1	GND	—	—
M2	DDR_DQ0	—	—
M3	DDR_DQ1	—	—
M4	DDR_DQ2	—	—
M5	DDR_DQ3	—	—
M6	VREF	—	—
M7	VDDQ	—	—
M8	GND	—	—
M9	VDD	—	—
M10	GND	—	—
M11	GND	—	—
M12	GND	—	—
M13	GND	—	—
M14	GND	—	—
M15	VDD	—	—
M16	ADC0_1_AVDD	—	—
M17	USB1_AGND	—	—
M18	USB0_AGND	—	—
M19	ADC2_AIN9	—	—
M20	M3_IGNKEY	—	—
M21	USB_VREG_1V8	—	—
M22	USB0_DP	—	—
M23	USB0_DN	—	—
N1	DDR_DQS0	—	—
N2	DDR_DQS0n	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
N3	GND	—	—
N4	VDDQ	—	—
N5	DDR_DQ4	—	—
N6	PLL_VDD	—	—
N7	VDDQ	—	—
N8	GND	—	—
N9	VDD	—	—
N10	GND	—	—
N11	GND	—	—
N12	GND	—	—
N13	GND	—	—
N14	GND	—	—
N15	GND	—	—
N16	ADC0_1_AGND	—	—
N17	USB0_VDD3V3	—	—
N18	USB1_VDD3V3	—	—
N19	ADC3_AIN0	—	—
N20	SYS_MXTALO	—	—
N21	ADC3_AIN4	—	—
N22	ADC3_AIN5	—	—
N23	ADC2_AIN7	—	—
P1	GND	—	—
P2	DDR_DQ5	—	—
P3	DDR_DQ6	—	—
P4	DDR_DQ7	—	—
P5	DDR_DM0	—	—
P6	PLL_VSS	—	—
P7	VDDQ	—	—
P8	GND	—	—
P9	VDD	—	—
P10	GND	—	—
P11	GND	—	—
P12	GND	—	—
P13	GND	—	—
P14	GND	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
P15	VDD	—	—
P16	VDD_2_5V_PLL3_4	—	—
P17	PLL_VREG3.3V	—	—
P18	VDD_2_5V_PLL1_2	—	—
P19	ADC2_VREFP	—	—
P20	SYS_MXTALI	—	—
P21	ADC2_AIN8	—	—
P22	GPIO19	PU	4
P23	GPIO21	PU	4
R1	DDR_RASn	—	—
R2	DDR_CASn	—	—
R3	GND	—	—
R4	DDR_CS0n	—	—
R5	DDR_CS1n	—	—
R6	DDR_WEn	—	—
R7	VDDQ	—	—
R8	GND	—	—
R9	VDD	—	—
R10	VDD	—	—
R11	VDD	—	—
R12	VDD	—	—
R13	GND	—	—
R14	VDD	—	—
R15	GND	—	—
R16	ARM_VDD	—	—
R17	ARM_VDD	—	—
R18	USB_VREG3V3_1V8	—	—
R19	VDD_2_5V_XOSC	—	—
R20	M3_GPIO7_WAKE7	PD	2
R21	GPIO20	PU	4
R22	GPIO16	PU	4
R23	GPIO18	PU	4
T1	GND	—	—
T2	DDR_ODT0	—	—
T3	DDR_ODT1	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
T4	VDDQ	—	—
T5	GND	—	—
T6	VDDQ	—	—
T7	VDDQ	—	—
T8	GND	—	—
T9	GND	—	—
T10	GND	—	—
T11	GND	—	—
T12	GND	—	—
T13	VDD_IO_3V3	—	—
T14	VDD_IO_3V3	—	—
T15	VDD_IO_3V3	—	—
T16	ARM_VDD	—	—
T17	ARM_VDD	—	—
T18	ARM_VDD	—	—
T19	ARM_VDD	—	—
T20	M3_GPIO3_WAKE3	PD	2
T21	M3_ONOFF	—	—
T22	GPIO15	PU	4
T23	GPIO7	PU	4
U1	VDDQ	—	—
U2	DDR_CKE0	—	—
U3	DDR_CKE1	—	—
U4	DDR_BA2	—	—
U5	DDR_DTO_1	—	—
U6	GND	—	—
U7	VDDQ	—	—
U8	VDDQ	—	—
U9	VDDQ	—	—
U10	VDDQ	—	—
U11	VDDQ	—	—
U12	VDDQ	—	—
U13	VDD_IO_3V3	—	—
U14	VDD_IO_3V3	—	—
U15	VDD_IO_3V3	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
U16	VDD_IO_3V3	—	—
U17	ARM_VDD	—	—
U18	ARM_VDD	—	—
U19	ARM_VDD	—	—
U20	M3_GPIO0_WAKE0	PD	2
U21	M3_GPIO1_WAKE1	PD	2
U22	M3_VDDOK	—	—
U23	M3_LVI	—	—
V1	GND	—	—
V2	DDR_BA0	—	—
V3	DDR_BA1	—	—
V4	DDR_AD0	—	—
V5	DDR_DTO_0	—	—
V6	DDR_AD15	—	—
V7	PLL_VDD	—	—
V8	PLL_VSS	—	—
V9	VREF	—	—
V10	VDDQ	—	—
V11	GND	—	—
V12	GND	—	—
V13	VDD_IO_3V3	—	—
V14	VDD_IO_3V3	—	—
V15	VDD_IO_3V3	—	—
V16	XOSC_GND	—	—
V17	COMP2	—	—
V18	GNDBGCOMP2	—	—
V19	ADC3_AIN3	—	—
V20	M3_GPIO2_WAKE2	PD	2
V21	M3_GPIO4_WAKE4	PD	2
V22	M3_PWREN	—	—
V23	M3_GPIO6_WAKE6	PD	2
W1	DDR_CK	—	—
W2	DDR_CKn	—	—
W3	GND	—	—
W4	DDR_AD12	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
W5	DDR_AD13	—	—
W6	DDR_DQ27	—	—
W7	DDR_DQ29	—	—
W8	DDR_DM3	—	—
W9	DDR_DQ19	—	—
W10	DDR_DQ20	—	—
W11	DDR_DM2	—	—
W12	VDDQ	—	—
W13	DDR_PLL_DVDD	—	—
W14	DDR_PLL_3V3	—	—
W15	DDR_PLL_2V5	—	—
W16	DDR_PLL_AGND	—	—
W17	DDR_PLL_DGND	—	—
W18	SOC_AGND	—	—
W19	S_GPIO13	PU	4
W20	S_GPIO15	PU	4
W21	GPIO25	PU	2
W22	S_GPIO12	PU	4
W23	M3_GPIO5_WAKE5	PD	2
Y1	GND	—	—
Y2	DDR_AD2	—	—
Y3	DDR_AD8	—	—
Y4	VDDQ	—	—
Y5	DDR_AD14	—	—
Y6	DDR_DQ26	—	—
Y7	VDDQ	—	—
Y8	DDR_DQ31	—	—
Y9	DDR_DQ18	—	—
Y10	VDDQ	—	—
Y11	DDR_DQ23	—	—
Y12	GND	—	—
Y13	GPIO88	PU	8
Y14	GPIO84	PU	8
Y15	GPIO80	PU	8
Y16	GPIO76	PU	8

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
Y17	GPIO72	PU	8
Y18	GPIO68	PU	8
Y19	GPIO63	PU	8
Y20	GPIO23	PU	4
Y21	GPIO24	PU	4
Y22	GPIO33	PU	4
Y23	GPIO17	PU	4
AA1	DDR_AD1	—	—
AA2	DDR_AD4	—	—
AA3	DDR_AD7	—	—
AA4	GND	—	—
AA5	DDR_AD11	—	—
AA6	DDR_DQ25	—	—
AA7	GND	—	—
AA8	DDR_DQ30	—	—
AA9	DDR_DQ17	—	—
AA10	GND	—	—
AA11	DDR_DQ22	—	—
AA12	VDDQ	—	—
AA13	GPIO89	PU	8
AA14	GPIO85	PU	8
AA15	GPIO81	PU	8
AA16	GPIO77	PU	8
AA17	GPIO73	PU	8
AA18	GPIO69	PU	8
AA19	GPIO64	PU	8
AA20	S_GPIO14	PU	2
AA21	JTAG_TRSTn	—	—
AA22	JTAG_TMS	—	—
AA23	GPIO14	PU	4
AB1	VDDQ	—	—
AB2	DDR_AD3	—	—
AB3	DDR_AD6	—	—
AB4	DDR_AD10	—	—
AB5	DDR_ATO	—	—

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
AB6	DDR_DQ24	—	—
AB7	DDR_DQS3n	—	—
AB8	DDR_DQ28	—	—
AB9	DDR_DQ16	—	—
AB10	DDR_DQS2n	—	—
AB11	DDR_DQ21	—	—
AB12	GND	—	—
AB13	GPIO90	PU	8
AB14	GPIO87	PU	8
AB15	GPIO82	PU	8
AB16	GPIO78	PU	8
AB17	GPIO74	PU	8
AB18	GPIO70	PU	8
AB19	GPIO65	PU	8
AB20	GPIO22	PU	4
AB21	GPIO30	PU	4
AB22	JTAG_TDO	—	—
AB23	JTAG_TDI	—	—
AC1	GND	—	—
AC2	VDDQ	—	—
AC3	DDR_AD5	—	—
AC4	DDR_AD9	—	—
AC5	DDR_RESETn	—	—
AC6	GND	—	—
AC7	DDR_DQS3	—	—
AC8	GND	—	—
AC9	GND	—	—
AC10	DDR_DQS2	—	—
AC11	GND	—	—
AC12	VDDQ	—	—
AC13	GPIO91	PU	8
AC14	GPIO86	PU	8
AC15	GPIO83	PU	8
AC16	GPIO79	PU	8
AC17	GPIO75	PU	8

Table 27. STA1275 and STA1295 ball list (continued)

Ball	Signal	Pull up/down	Driving strength
AC18	GPIO71	PU	8
AC19	GPIO66	PU	8
AC20	GPIO67	PU	8
AC21	SYS_SYSRES	—	—
AC22	JTAG_TCK	—	—
AC23	GND	—	—

3.3 STA1275 and STA1295 ballout

Table 28. STA1275 and STA1295 ballout (part 1/2)

	1	2	3	4	5	6	7	8	9	10	11	12
A	GND	GPIO 27	GPIO 28	GPIO 26	GPIO 37	S_GP IO7	S_GP IO8	S_GP IO9	M3_GP IO15	GPIO 92	GPIO 97	GPIO 100
B	GPIO 38	GPIO 39	GPIO 120	GPIO 35	S_GP IO6	S_GP IO10	S_GP IO11	M3_GP IO13	M3_GP IO14	M3_GP IO8	GPIO 94	GPIO 98
C	GPIO 125	GPIO 127	GPIO 29	GPIO 116	GPIO 51	GPIO 34	GPIO 36	M3_GP IO9	M3_GP IO10	GPIO 93	GPIO 99	GPIO 109
D	GPIO 123	GPIO 124	GPIO 122	GPIO 126	S_GP IO1	S_GP IO0	S_GP IO4	M3_GP IO11	M3_GP IO12	GPIO 95	GPIO 102	GPIO 104
E	GPIO 118	GPIO 121	GPIO 117	GPIO 119	GPIO 114	S_GP IO3	VDD_ IO_3V3	GND	GND	GPIO 96	GPIO 103	GPIO 107
F	GPIO 115	SDMM C0_ CMD	SDMM C0_ CLK	GPIO 31	OTP_ FUSE_ HV	VDD_ IO_3V3	VDD_ IO_3V3	VDD_ IO_3V3	VDD_ IO_3V3	VDD_ IO_3V3	GPIO 45	GPIO 44
G	SDMM C0_ DATA_ 3	SDMM C0_ DATA_ 2	SDMM C0_ DATA_ 0	SDMM C0_ DATA_ 1	COMP 1	COMP 0	GNDB GCOM P1	VDD_ IO_3V3	VDD_ IO_3V3	VDD_ IO_3V3	VDD	VDD
H	VDDQ	GND	VDDQ	GND	VDDQ	GND	VDD_ IO_1V8	GND	VDD_ IO_3V3	VDD_ IO_3V3	VDD_ IO_3V3	GND
J	GND	DDR_ DQ10	DDR_ DQ9	DDR_ DQ8	DDR_ DQ11	DDR_ ZQ	VDDQ	GND	VDD	VDD	VDD	VDD
K	DDR_ DQS1n	DDR_ DQS1	GND	VDDQ	DDR_ DQ12	PLL_ VSS	VDDQ	GND	VDD	GND	GND	GND
L	GND	DDR_ DM1	DDR_ DQ15	DDR_ DQ14	DDR_ DQ13	PLL_ VDD	VDDQ	GND	VDD	GND	GND	GND
M	GND	DDR_ DQ0	DDR_ DQ1	DDR_ DQ2	DDR_ DQ3	VREF	VDDQ	GND	VDD	GND	GND	GND
N	DDR_ DQS0	DDR_ DQS0n	GND	VDDQ	DDR_ DQ4	PLL_ VDD	VDDQ	GND	VDD	GND	GND	GND

Table 28. STA1275 and STA1295 ballout (part 1/2) (continued)

	1	2	3	4	5	6	7	8	9	10	11	12
P	GND	DDR_ DQ5	DDR_ DQ6	DDR_ DQ7	DDR_ DM0	PLL_ VSS	VDDQ	GND	VDD	GND	GND	GND
R	DDR_ RASn	DDR_ CASn	GND	DDR_ CS0n	DDR_ CS1n	DDR_ WEn	VDDQ	GND	VDD	VDD	VDD	VDD
T	GND	DDR_ ODT0	DDR_ ODT1	VDDQ	GND	VDDQ	VDDQ	GND	GND	GND	GND	GND
U	VDDQ	DDR_ CKE0	DDR_ CKE1	DDR_ BA2	DDR_ DTO_1	GND	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ
V	GND	DDR_ BA0	DDR_ BA1	DDR_ AD0	DDR_ DTO_0	DDR_ AD15	PLL_ VDD	PLL_ VSS	VREF	VDDQ	GND	GND
W	DDR_ CK	DDR_ CKn	GND	DDR_ AD12	DDR_ AD13	DDR_ DQ27	DDR_ DQ29	DDR_ DM3	DDR_ DQ19	DDR_ DQ20	DDR_ DM2	VDDQ
Y	GND	DDR_ AD2	DDR_ AD8	VDDQ	DDR_ AD14	DDR_ DQ26	VDDQ	DDR_ DQ31	DDR_ DQ18	VDDQ	DDR_ DQ23	GND
AA	DDR_ AD1	DDR_ AD4	DDR_ AD7	GND	DDR_ AD11	DDR_ DQ25	GND	DDR_ DQ30	DDR_ DQ17	GND	DDR_ DQ22	VDDQ
AB	VDDQ	DDR_ AD3	DDR_ AD6	DDR_ AD10	DDR_ ATO	DDR_ DQ24	DDR_ DQS3n	DDR_ DQ28	DDR_ DQ16	DDR_ DQS2n	DDR_ DQ21	GND
AC	GND	VDDQ	DDR_ AD5	DDR_ AD9	DDR_ RESET n	GND	DDR_ DQS3	GND	GND	DDR_ DQS2	GND	VDDQ

Table 29. STA1275 and STA1295 ballout (part 2/2)

	13	14	15	16	17	18	19	20	21	22	23
A	GPIO49	GPIO50	GPIO53	GPIO57	GPIO59	GPIO9	GPIO11	GPIO10	GPIO12	GPIO3	GND
B	GPIO 105	GPIO 111	GPIO 110	GPIO62	GPIO60	GPIO58	GPIO4	GPIO5	GPIO0	GPIO1	GPIO8
C	GPIO 113	GPIO 112	GPIO55	GPIO56	GPIO61	GPIO13	M3_ CLK32K OUT	GPIO40	GPIO41	GPIO42	GPIO43
D	GPIO 106	GPIO6	GPIO52	GPIO54	M3_ XTALI	M3_ XTALO	GPIO2	GPIO32	TSC_ YN_ AIN3	TSC_ XP_ AIN0	TSC_ XN_ AIN1
E	GPIO 108	VDD_2_ 5V	GND	VDD_IO _ON	GPIO48	VDD_ ON_ VREG	GPIO47	GPIO46	TSC_ YP_ AIN2	DAC_ VCOM	DAC_ VHI
F	VDD	GND	VDD	OSC 32K_ GND	VREG_ BY PASS	ADC2_ AIN5	GPIO 101	S_GPIO 2	ADC2_ AIN6	DAC_ OUT2L	DAC_ OUT2R
G	VDD	VDD	ADC2_3 _AGND	ADC2_3 _AVDD	ADC3_ VREFN	DAC_IO _AVDD	ADC3_ AIN1	S_GPIO 5	ADC3_ AIN2	DAC_ OUT0R	DAC_ OUT0L

Table 29. STA1275 and STA1295 ballout (part 2/2) (continued)

	13	14	15	16	17	18	19	20	21	22	23
H	VDD	GND	VDD	GND	ADC2_3_AVDD	DAC_AGND	DAC_IO_AGND	JTAG SEL	DAC_OUT1L	ADC1_MICIN_P	ADC1_MICIN_N
J	GND	VDD	GND	VDD	ADC2_VREFN	DAC_AVDD	DAC_IO_AVDD	DAC_OUT1R	ADC0_AIN2_L	ADC0_AIN1_L	ADC1_AIN1_P
K	GND	GND	VDD	ADC3_VREFP	DAC_VLO	DAC_IO_AGND	ADC0_1_VCM	ADC0_1_VRFP	MIC_BIAS	ADC0_AIN1_R	ADC1_AIN1_N
L	GND	GND	GND	ADC0_1_VRFN	USB_VREG3V3_1V1	ADC2_AIN4	USB_REXT	ADC0_AIN2_R	USB_VREG_1V1	USB1_DP	USB1_DN
M	GND	GND	VDD	ADC0_1_AVDD	USB1_AGND	USB0_AGND	ADC2_AIN9	M3_IGNKEY	USB_VREG_1V8	USB0_DP	USB0_DN
N	GND	GND	GND	ADC0_1_AGND	USB0_VDD3V3	USB1_VDD3V3	ADC3_AIN0	SYS_MXTALO	ADC3_AIN4	ADC3_AIN5	ADC2_AIN7
P	GND	GND	VDD	VDD_2_5V_PLL3_4	PLL_VREG3.3V	VDD_2_5V_PLL1_2	ADC2_VREFP	SYS_MXTALI	ADC2_AIN8	GPIO19	GPIO21
R	GND	VDD	GND	ARM_VDD	ARM_VDD	USB_VREG3V3_1V8	VDD_2_5V_XOSC	M3_GPIO7_WAKE7	GPIO20	GPIO16	GPIO18
T	VDD_IO_3V3	VDD_IO_3V3	VDD_IO_3V3	ARM_VDD	ARM_VDD	ARM_VDD	ARM_VDD	M3_GPIO3_WAKE3	M3_ONOFF	GPIO15	GPIO7
U	VDD_IO_3V3	VDD_IO_3V3	VDD_IO_3V3	VDD_IO_3V3	ARM_VDD	ARM_VDD	ARM_VDD	M3_GPIO0_WAKE0	M3_GPIO1_WAKE1	M3_VDDOK	M3_LVI
V	VDD_IO_3V3	VDD_IO_3V3	VDD_IO_3V3	XOSC_GND	COMP2	GNDBGCOMP2	ADC3_AIN3	M3_GPIO2_WAKE2	M3_GPIO4_WAKE4	M3_PWREN	M3_GPIO6_WAKE6
W	DDR_PLL_DVDD	DDR_PLL_3V3	DDR_PLL_2V5	DDR_PLL_AGND	DDR_PLL_DGND	SOC_AGND	S_GPIO13	S_GPIO15	GPIO25	S_GPIO12	M3_GPIO5_WAKE5
Y	GPIO88	GPIO84	GPIO80	GPIO76	GPIO72	GPIO68	GPIO63	GPIO23	GPIO24	GPIO33	GPIO17
AA	GPIO89	GPIO85	GPIO81	GPIO77	GPIO73	GPIO69	GPIO64	S_GPIO14	JTAG_TRSTn	JTAG_TMS	GPIO14
AB	GPIO90	GPIO87	GPIO82	GPIO78	GPIO74	GPIO70	GPIO65	GPIO22	GPIO30	JTAG_TDO	JTAG_TDI
AC	GPIO91	GPIO86	GPIO83	GPIO79	GPIO75	GPIO71	GPIO66	GPIO67	SYS_SYSRES	JTAG_TCK	GND

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at TA = 25°C and TA = 85°C.

The 'Limit Values' data is explained and identified with a letter as listed below, and reported in the ‘Note’ field of the following tables where applicable:

- <SR>: System requirements, which means conditions that must be provided to ensure normal device operation.
- <P>: Data tested in production.
- <C>: Data based on engineering characterization, not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (± 3).
- <V>: Data based on design validation performed on three sample devices, not tested in production.
- <S>: Data based on design guidelines and simulation, not tested in production.Typical curves.

4.3 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

Table 30. Absolute maximum ratings

Symbol		Parameter	Limit values		Unit
			Min.	Max.	
VDD	SR	Power supply pins for the internal logic of switchable domain	- 0.3	+ 1.50	V
VDD_IO_ON	SR	Power supply pins for the IO buffers of the always ON section	- 0.3	+ 3.90	V
VDD_IO_3V3	SR	Power supply pins for the 3.3 V IO buffers in switchable domain	- 0.3	+ 3.90	V
VDD_IO_1V8	SR	Power supply pins for the 1.8 V IO buffers in switchable domain	- 0.3	+ 3.90	V
ARM_VDD	SR	Power supply pins for the Cortex® A7 CPU	- 0.3	+ 1.50	V
ADC2_3_AVDD	SR	Analog power supply for SAR ADC	- 0.3	+ 3.90	V

Table 30. Absolute maximum ratings (continued)

Symbol		Parameter	Limit values		Unit
			Min.	Max.	
ADC2_VREFP	SR	Positive reference voltage for SAR ADC	- 0.3	+ 3.90	V
DAC_AVDD	SR	Analog voltage supply for DAC	- 0.3	+ 3.90	V
DAC_IO_AVDD	SR	Power supply of IO buffer in DAC/Stereo/Microphone σΔ ADC section	- 0.3	+ 3.90	V
ADC0_1_VDD	SR	Analog power supply for Stereo/Microphone SDADC	- 0.3	+ 3.90	V
USB_VREG3V3_1V1	SR	Voltage supply for 3V3TO1V1 regulator used within USB subsystem	- 0.3	+ 3.90	V
USB_VREG3V3_1V8	SR	Voltage supply for 3V3TO1V8 regulator used within USB subsystem	- 0.3	+ 3.90	V
USB0_VDD3V3	SR	Voltage supply for Host USB (USB0)	- 0.3	+ 3.90	V
USB1_VDD3V3	SR	Voltage supply for dual role USB (USB)	- 0.3	+ 3.90	V
PLL_VREG3.3V	SR	Voltage supply for 3V3TO2V5 regulator used by PLL and 24 MHz OSC	- 0.3	+ 1.50	V
VDDQ	SR	Power rail of DDR IOs	- 0.3	+ 2.50	V
DDR_PLL_3V3	SR	3.3 V for DDR_PLL LDO	- 0.3	+ 3.90	V
DDR_PLL_DVDD	SR	1.2 V digital supply for DDR PLL	- 0.3	+ 1.50	V
V_{INPUT}	SR	Voltage applied to any pin of the VDD_IO_3V3 domain	GND - 0.3	VDD_IO_3V3 + 0.3	V
		Voltage applied to any pin of the VDD_IO_1V8 domain		VDD_IO_1V8 + 0.3	
		Voltage applied to any pin of the VDD_IO_ON domain		VDD_IO_ON + 0.3	
		Voltage applied to any pin of the VDDQ domain		VDDQ + 0.3	
		Voltage applied to any ΣΔ ADC pin	ADC0_1_AGND - 0.3	ADC0_1_AVDD + 0.3	
		Voltage applied to any SAR ADC pin	ADC2_3_AGND - 0.3	ADC2_3_AVDD + 0.3	
		Voltage applied to any USB pin	See note(1)		

1. Voltage, current, and impedance on USB*_DP and USB*_DN pins should strictly be compliant with the USB 2.0 standard, including the following Engineering Change Notice (ECN) issued by the USB Implementers Forum: 5V Short Circuit Withstand Requirement Change ECN.

Warning: **Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

4.4 Electrical sensitivity

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.4.1 Electrostatic discharge (ESD)

Table 31. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Max value(1)	Unit
VESD0 (HBM)	Electrostatic discharge voltage (Human body model)	Conforming to AEC-Q100-002	H2	2000	V
VESD (CDM)	Electrostatic discharge voltage (Charged device model)	Conforming to AEC-Q100-011	C4	500	
				750 (for corners)	

1. Data is based on qualification results, not tested in production.

Note: All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.4.2 Static latch-up (LU)

Table 32. Latch-up results

Symbol	Ratings	Conditions	Class
LU	Static latch-up class	Conforming to JESD 78	II level A

4.5 Thermal characteristics

Devices are available in both Consumer Grade and Automotive Grade Qualification (AEC-Q100 Grade 3).

Table 33. Thermal characteristics

Symbol		Parameter	Limit values		Unit
			Min	Max	
T_{oper}	SR	Operative ambient temperature	-40	+85	°C
T_j	SR	Operative junction temperature	-40	+125	°C
T_{st}	SR	Storage temperature	-55	+125	°C
Θ_{j-a}	S	Thermal resistance junction to ambient(1)	—	19.6	°C/W
Ψ_{j-b}	S	Thermal resistance junction to board(1)	—	11.8	°C/W

Table 33. Thermal characteristics (continued)

Symbol		Parameter	Limit values		Unit
			Min	Max	
$\Psi_{j\text{-}c}$	S	Thermal resistance junction to case(1)	—	1	°C/W
$\Theta_{j\text{-}a}$	S	Thermal resistance junction to ambient(2)	—	18.5	°C/W
$\Psi_{j\text{-}b}$	S	Thermal resistance junction to board(2)	—	11	°C/W
$\Psi_{j\text{-}c}$	S	Thermal resistance junction to case(2)	—	1	°C/W
$\Theta_{j\text{-}a}$	S	Thermal resistance junction to ambient(3)	—	17.2	°C/W
$\Psi_{j\text{-}b}$	S	Thermal resistance junction to board(3)	—	10.3	°C/W
$\Psi_{j\text{-}c}$	S	Thermal resistance junction to case(3)	—	1	°C/W

1. LFBGA 19x19 package, thermal simulation with 2s2p board as per Jedec standard JESD51-7; T_{amb} = 85 °C.
2. LFBGA 19x19 package, thermal simulation with 4 layer application board; T_{amb} = 85 °C.
3. LFBGA 19x19 package, thermal simulation with 6 layer application board; T_{amb} = 85 °C.

Table 34. Frequency limits

Symbol		Parameter	Test condition	Limit values			Notes	Unit
				Min.	Typ.	Max.		
$F_{CLK\text{-}A7}$(1)	P	Operating frequency Cortex® A7 CP. ECO version (-E).	VDD = 1.14 V TC = 85 °C	—	600(2)	650	—	MHz
$F_{CLK\text{-}M3}$(1)	P	Operating Cortex-M3 CPU frequency		—	—	208	—	
F_{VIP}(1)	P	Operating frequency for VIP		—	—	240	—	
F_{SSP}(1)	P	Operating frequency for SSP in master mode		—	—	52	—	
F_{SAI}(1)	P	Operating frequency for SAI		—	—	12	—	
F_{SQI}(1)	P	Operating frequency for SQI		—	—	125	—	
F_{DDR3}(1)	P	Operating frequency for DDR3L		—	—	660	—	
F_{LCD}(1)	P	Operating frequency for single display LCD		—	—	156	Edge shift mode	
F_{LCD}(1)	P	Operating frequency for dual display LCD		—	—	38	—	
F_{SDMMC0}(1)	P	Operating frequency for SDMMC0		—	96(3)	104(3)	1.8 V SDIO mode	
F_{SDMMC1}(1)	P	Operating frequency for SDMMC1/2		—	48(3)	52(3)	—	

Table 34. Frequency limits (continued)

Symbol		Parameter	Test condition	Limit values			Notes	Unit
				Min.	Typ.	Max.		
F_{ETM}	P	Operating frequency for ETM	VDD = 1.14 V TC = 85 °C	—	—	70	—	MHz
$F_{Graphics}$	P	Operating frequency for Graphics		—	—	445	—	
F_{STM}	P	Operating frequency for STM		—	—	70	—	
F_{JTAG}(1)	P	Operating frequency for JTAG		—	—	20	—	

1. Values programmable through configurable PLL. Refer to SRC chapter for details.
2. The value of 600 MHz allows coupling with the maximum interconnect frequency of 200 MHz.
3. The value indicated as typical is the relevant one in some of the use cases where the IP itself can run up to the frequency value indicated as maximum, but standard external components/cards cannot; typical setting is recommended as a consequence.

Table 35: Accordo5 - STA1295 - current consumption provides an indication of power consumption on each power supply rail for different use cases. All measurements are taken on standard process samples, in typical conditions (midpoint of supply voltage range and 25°C junction temperature).

Cases 1 and 2 are relevant as low power consumption modes, typically operated on battery supply.

Current consumption on VDD_IO_ON power rail is listed were relevant (which means in the low power use cases, when battery operated). In the other use cases it can be considered not relevant (< 0.1 mA).

A power consumption measurement campaign should be repeated by customer using their actual application, that will surely differ from ST software demo applications in the way software is implemented and optimized.

Table 35. Accordo5 - STA1295 - current consumption

Use case	I_VDD (mA)	I_ARM_VDD (mA)	I_VDDIO_3V3 (mA)	I_VDDQ (mA)	I_AVDD (mA)	I_USB (mA)	I_VDD_IO_ON (uA)	TOTAL POWER (mW)
Deep standby(1)	0	0	0	0	0	0	0.016	0.053
Deep standby(2)	0	0	0	0	0	0	0.021	0.07
Idle	125	15	17.9	66	30	1	—	319.569
Smartphone mirroring application(3)	707	163	133	164	26	19	—	1852.8
Video decoding application(4)	628	60	74	135	40	18	—	1443.45
Cortex-A7 CPUs 50%	556	146	73	93	40	13	—	1383.75

Table 35. Accordo5 - STA1295 - current consumption (continued)

Use case	I_VDD (mA)	I_ARM_VDD (mA)	I_VDDIO_3V3 (mA)	I_VDDQ (mA)	I_AVDD (mA)	I_USB (mA)	I_VDD_IO_ON (uA)	TOTAL POWER (mW)
Cortex-A7 CPUs 100%	557	253	73	93	40	13	—	1513.35
Video play from USB (WVGA LCD) + graphic animation	700	80	82	180	25	19	—	1594.8

1. PMU only, with RTC disabled
2. PMU only, with RTC enabled.
3. Smartphone is plugged to evaluation board via USB; Smartphone mirroring software is activated and MP3 is played from smartphone.
4. Video is being read from USB key connected to USB0, video decoding at 720p is run and LCD is used (1280x800 HD - 10 inch display).

4.6 Recommended DC operation conditions

The table below lists the functional recommended operating DC parameters for STA1275 and STA1295.

Table 36. Recommended DC operation conditions

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
V_{DD}	SR	Digital supply voltage	1.14	1.2	1.26	V
$V_{DD\_IO\_ON}$	SR	I/O supply voltage (I/Os in always ON domain)	3.0	3.3	3.6	V
$V_{DD\_IO\_3V3}$	SR	I/O supply voltage (I/Os is switchable domain)	3.0	3.3	3.6	V
$V_{DD\_IO\_1V8}$	SR	I/O supply voltage (I/Os is switchable domain)	1.65	1.8	1.95	V
V_{ARM_VDD}	SR	Digital supply voltage for Cortex® A7 CPU	1.14	1.2	1.26	V
$V_{ADC2\_3\_AVDD}$	SR	Analog supply voltage for SAR ADC	3.0	3.3	3.6	V
V_{DAC_AVDD}	SR	Analog supply voltage for DAC	3.0	3.3	3.6	V
$V_{DAC\_IO\_AVDD}$	SR	IO supply voltage for in DAC/SDADC IO ring section	3.0	3.3	3.6	V
$V_{ADC0\_1\_AVDD}$	SR	Voltage power supply for ADC0 and ADC1	3.0	3.3	3.6	V
$V_{USB\_VREG\_3V3\_1V1}$	SR	Voltage supply for 3V3TO1V1 USB regulator	3.0	3.3	3.6	V
$V_{DD\_USB\_VREG3V3\_1V8}$	SR	Voltage supply for 3V3TO1V8 USB regulator(1)	3.0	3.3	3.6	V
$V_{DD\_USB0\_VDD3V3}$	SR	3.3V dedicated power supply to USB0 PHY(1)	3.0	3.3	3.6	V
$V_{DD\_USB1\_VDD3V3}$	SR	3.3V dedicated power supply to USB0 PHY(1)	3.0	3.3	3.6	V
$V_{DD\_PLL\_VREG3V3}$	SR	Voltage power supply for SOC PLL	3.0	3.3	3.6	V
V_{DDQ}	SR	I/O supply voltage for DDR3L IOs	1.28	1.35	1.42	V
V_{DDR_VREF}	SR	Voltage reference for DDR3L IOs	$V_{DDQ}/2$			V
$V_{DDR\_PLL\_3V3}$	SR	3.3V supply voltage for DDR3L PLL	3.0	3.3	3.6	V
$V_{DDR\_PLL\_DVDD}$	SR	Digital supply voltage for DDR3L PLL	1.14	1.2	1.26	V

1. $V_{DD\_USB0\_VDD3V3}$, $V_{DD\_USB1\_VDD3V3}$ and $V_{DD\_USB\_VREG3V3\_1V8}$ are internally shorted.

4.7 DC characteristics

IOs in Accordo5 fall into three categories:

- Logical CMOS function operating at 3.3 V
- Logical CMOS function operating at 1.8 V
- DDR3L (specific functionality operating according to standards)

The table below lists the functional operating DC characteristics for the first (non-standard) IO categories.

Table 37. Digital DC characteristics at 3.3 V

Symbol		Parameter	Test condition	Limit values			Unit	Notes
				Min.	Typ.	Max.		
V_{IL}	P	Logical input low level voltage	V_{DDIO} = 3.3 V	-0.3	—	0.8	V	(1)
V_{IH}	P	Logical input high level voltage	V_{DDIO} = 3.3 V	2.0	—	V_{DDIO} + 0.3	V	(1)
V_{HYST}	S	Schmitt-trigger hysteresis	—	250	—	—	mV	(2)
V_{TH+}	S	Schmitt-trigger high threshold	—	1.49	—	—	V	(3)
V_{TL-}	S	Schmitt-trigger low threshold	—	—	—	1.39	V	(3)
R_{PU}	P	Equivalent pull-up	—	32	50	60	kΩ	—
R_{PD}	P	Equivalent pull-down	—	32	50	60	kΩ	—
V_{OL}	P	Low level output voltage	I_{OL} = 4 mA / 8 mA	—	—	0.4	V	(4)
V_{OH}	P	High level output voltage	I_{OH} = 4 mA / 8 mA	V_{DDIO} - 0.4	—		V	(4)
I_{IH}	S	High level input current	—	—	—	< 1	µA	(5)
I_{IL}	S	Low level input current	—	—	—	< 1	µA	(5)
C_{IN}	S	Input Pin Capacitance	—	—	—	1.5	pF	—

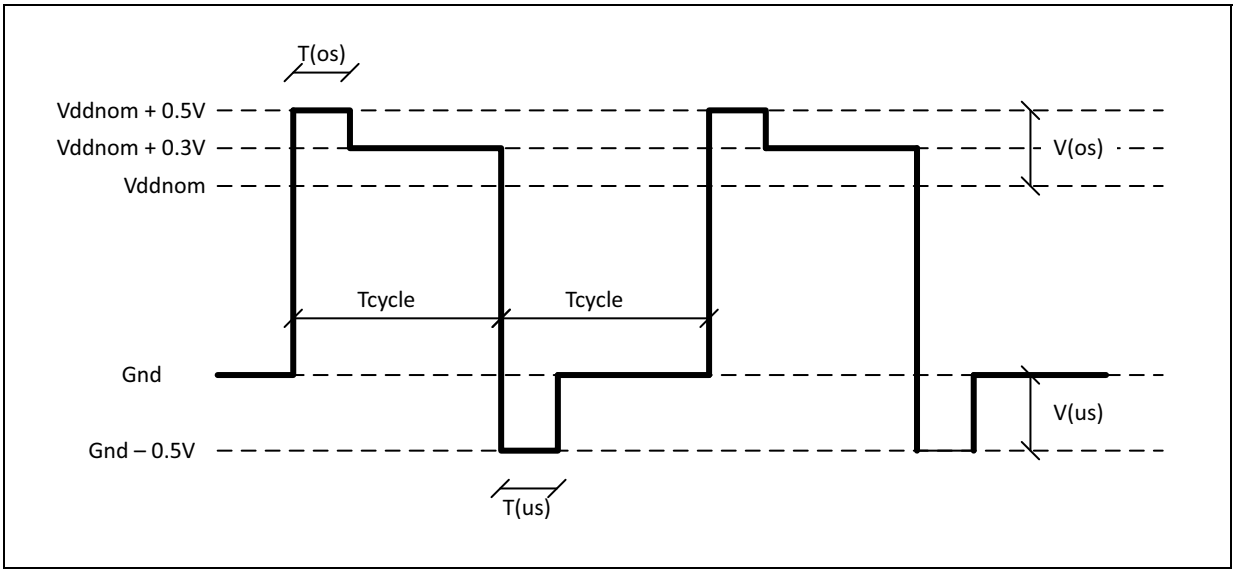
1. Excludes oscillator inputs SXTALI and MXTALI. Refer to oscillator electrical specifications.
2. Apply to all digital inputs unless specified otherwise.
3. Values for V_{TH+} and V_{TL-} are referred to different PVTs
4. I_{OH}/I_{OL} is the maximum source/sink current drive that guarantees the V_{OH}/V_{OL} level, depending on the IO buffer drive capability level (4 or 8 mA, not programmable).
5. Pull-up or pull-down disabled.

Table 38. Digital DC characteristics at 1.8 V

Symbol		Parameter	Test condition	Limit values			Unit
				Min.	Typ.	Max.	
V_{IL}	P	Logical input low level voltage	$V_{DD\_IO\_1V8}$ = 1.8 V	-0.3	—	0.35 × $V_{DD\_IO\_1V8}$	V
V_{IH}	P	Logical input high level voltage	$V_{DD\_IO\_1V8}$ = 1.8 V	0.65 × VDD_IO_1V8	—	$V_{DD\_IO\_1V8}$ + 0.3	V
V_{HYST}	S	Schmitt-trigger hysteresis	—	150	—	—	mV
V_{TH+}	S	Schmitt-trigger high threshold	—	—	—	—	—
V_{TL-}	S	Schmitt-trigger low threshold	—	—	—	—	—
R_{PU}	P	Equivalent pull-up	—	—	50	—	kΩ
R_{PD}	P	Equivalent pull-down	—	—	—	—	—
V_{OL}	P	Low level output voltage	IOL = 4 mA	—	—	0.4	V
V_{OH}	P	High level output voltage	IOL = 4 mA	$V_{DD\_IO\_1V8}$ - 0.4	—	—	V
I_{IH}	S	High level input current	—	—	—	< 1	uA
I_{IL}	S	Low level input current	—	—	—	< 1	uA
C_{IN}	S	Input Pin Capacitance	—	—	—	1.5	pf

The following is a representation of allowed signal levels, overshoot and undershoot conditions:

Figure 3. Signal overshoot and undershoot limits



The maximum signal level allowed is Vddnom + 0.3 V.

Signal overshoots up to V(os) (that is 0.5 V above Vddnom level) are allowed, for a time T(os) that must be shorter than the smaller between 2nsec and 1/3 of the signal's Tcycle (that is 2nsec for "slow" signals, 1/3 of the cycle time for “fast” signals).

Signal undershoots up to V(us) (that is 0.5 V below Gnd level) are allowed, for a time T(us) that must be shorter than the smaller between 2nsec and 1/3 of the signal's Tcycle (that is 2nsec for "slow" signals, 1/3 of the cycle time for "fast" signals).

4.8 AC characteristics

4.8.1 Oscillator electrical specifications

This device contains two oscillators:

- a 32.768 kHz oscillator
- a 24-26 MHz oscillator

Each requires a specific crystal, with parameters that must be as close as possible to the following recommended values.

Clock from external source can also be applied on input pins.

4.8.2 32.768 kHz oscillator specifications

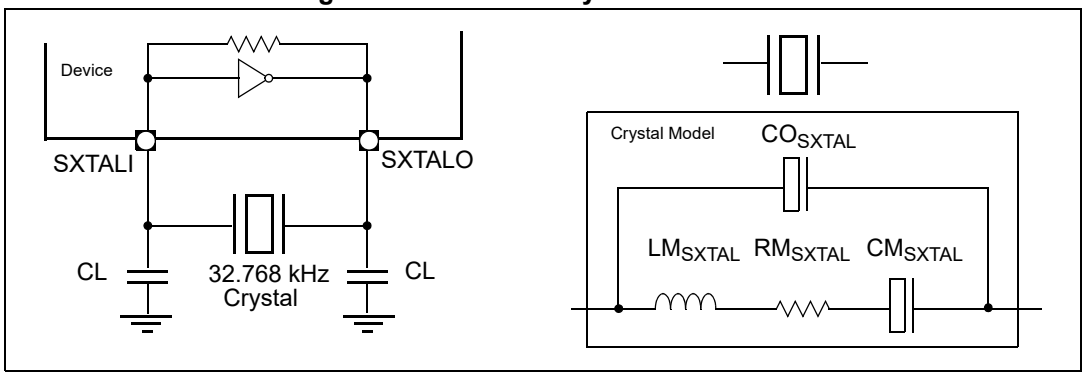
The internal oscillator amplifier specifications are shown in the table below:

Table 39. Oscillator amplifier specifications

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
T_{SXTAL}	V	Startup time		$15 \times L_m/R_m$	1.5	s
$T_{duty\ cycle}$(Zi & NZi)	V	Duty cycle	40	50	60	%
—	V	Amplitude of oscillation at M3_SXTALO	1.6		2.6	V
P_{SXTAL}	S	Power consumption during stable oscillation	—	10	—	µA
$GM_{0\text{-}SXTAL}$	P	Transconductance	28	—	56	µA/V
R_{neg}	S	Negative resistance	350		500	kΩ
Fs	S	Frequency stability			25	PPM

The 32.768 kHz oscillator is connected between M3_SXTALI (oscillator amplifier input) and M3_SXTALO (oscillator amplifier output). It also requires two external capacitors of CL pF, as shown in *Figure 4*.

Figure 4. 32.768 kHz crystal connection



The specifications of a typical external crystal are shown in the table below.

Table 40. Typical crystal recommended specifications

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
F_{SXTAL}	SR	Crystal frequency	—	32.768	—	kHz
L_{MSXTAL}	—	Motion inductance	—	11.8	—	mH
CM_{SXTAL}	—	Motional capacitance	—	2.0	—	fF
RM_{SXTAL}	—	Motional resistance	—	50	—	kΩ
CO_{SXTAL}	—	Shunt capacitance	—	3.5	—	pF
CL_{SXTAL}	—	Load capacitance(1)	—	22	—	pF

1. Total capacitance, including board and package parasitics.

There are two ways to drive the 32.768 kHz crystal pins from an external clock source:

- Bypass mode (for test). Enable the bypass mode (bit XCOSC32K_BYPASS= 1b in PMU_CTRL register). Apply external single ended clock at M3_SXTALI. Input clock should be of CMOS level (Low = GND, High = VDDIO_ON).
- Force Through Mode. Apply external single ended clock at M3_SXTALI. Input clock should be of CMOS level (Low = GND, High = VDDIO_ON). Clock is available after OSC startup time. The node M3_SXTALO must not be tied high as this may cause large current to enter amplifier and damage it permanently.

4.8.3 24-26 MHz oscillator specifications

The internal oscillator amplifier specifications are shown in the table below.

Table 41. Oscillator amplifier specifications

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
T_{MXTAL}	V	Startup time			3.4	ms
$T_{duty\ cycle}$(Zi & NZi)	V	Duty cycle	40%	50%	60%	%
—	V	Amplitude of oscillation at MXTALO	0.4		1.6	V
P_{SXTAL}	S	Power consumption during stable oscillation	—	—	8	µA
$GM_{0\text{-}MXTAL}$	P	Transconductance	8.5		15.8	mA/V
R_{neg}	S	Negative resistance	175		285	Ω
F	S	Frequency stability			25	PPM

The 24 to 26 MHz oscillator is connected between MXTALI (oscillator amplifier input) and MXTALO (oscillator amplifier output). It also requires two external load capacitors of CL pF, as shown in *Figure 5*.

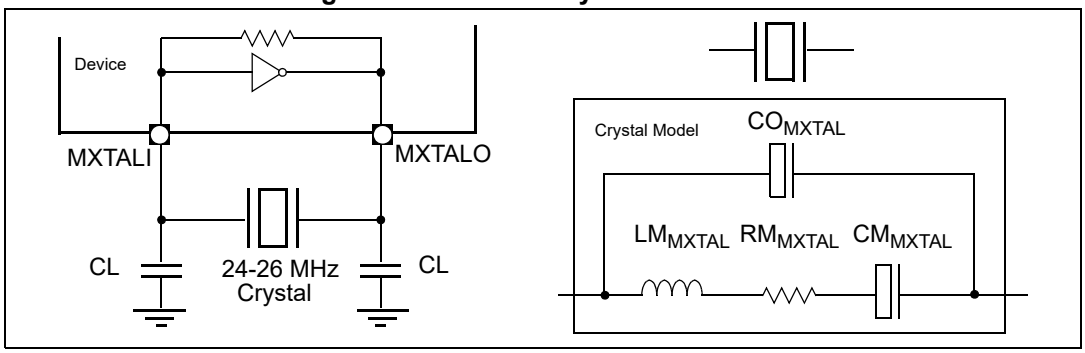
The specifications of a typical external crystal are shown in the table below.

Table 42. Typical crystal recommended specifications

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
F_{MXTAL}	SR	Crystal frequency		24		MHz
LM_{MXTAL}, 24 MHz XTAL			—	4.0		mH
CM_{MXTAL}, 24 MHz XTAL			—	10.1	—	fF
RM_{MXTAL}		Motional resistance	—	20	—	Ω
CO_{MXTAL}		Shunt capacitance	—	—	4.0	pF
CL_{MXTAL}		Load capacitance(1)	—	—	30	pF

1. Total capacitance, including package and board parasitics.

Figure 5. 24-26 MHz crystal connection



To drive the 24/26 MHz crystal pins from an external clock source, use Force Through Mode: Bias MXTALO at 1.25 V. Apply external single ended square clock at MXTALI. Input clock should be of CMOS level (Low = GND, High = 2.5 V). Clock is available after OSC startup time.

4.9 Sound subsystem

4.9.1 ADC1: Microphone ΣΔ ADC electrical characteristics

Table 43. MICADC electrical characteristics

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
$V_{ASupply}$	SR	Analog supply	3.0	3.3	3.6	V
V_{in}	S	Differential analog input		5.6		V_{p-p}
				2.0		V_{rms}
V_{in}	SR	Single ended analog input		2.8		V_{p-p}
				1.0		V_{rms}
V_{com}	P	DC coupled input common mode	1.5	1.65	1.8	V
		AC coupled input common mode	0	1.65	3.3	
SNR	V	Differential mode signal to noise ratio (A-weighted, Output rate 48 kHz, BW = 20 kHz)	86			dB
SNR	V	Differential mode signal to noise ratio (Unweighted, Output rate 48 kHz, BW = 3.2 kHz)	88			dB
SNR	V	Single ended mode signal to noise ratio (A-weighted, Output rate 48 kHz, BW = 20 kHz)	80			dB
SNR	V	Single ended mode Signal to Noise ratio (Unweighted, Output rate 48 kHz, BW = 3.2 kHz)	81			dB
THD + N	V	Differential mode Total harmonic distortion + Noise	-80	-85		dB
THD + N	V	Single ended mode Total harmonic distortion + Noise	-74	-79		dB
V_{MIC_BIAS}	P	MIC_BIAS		2.5(1)		V

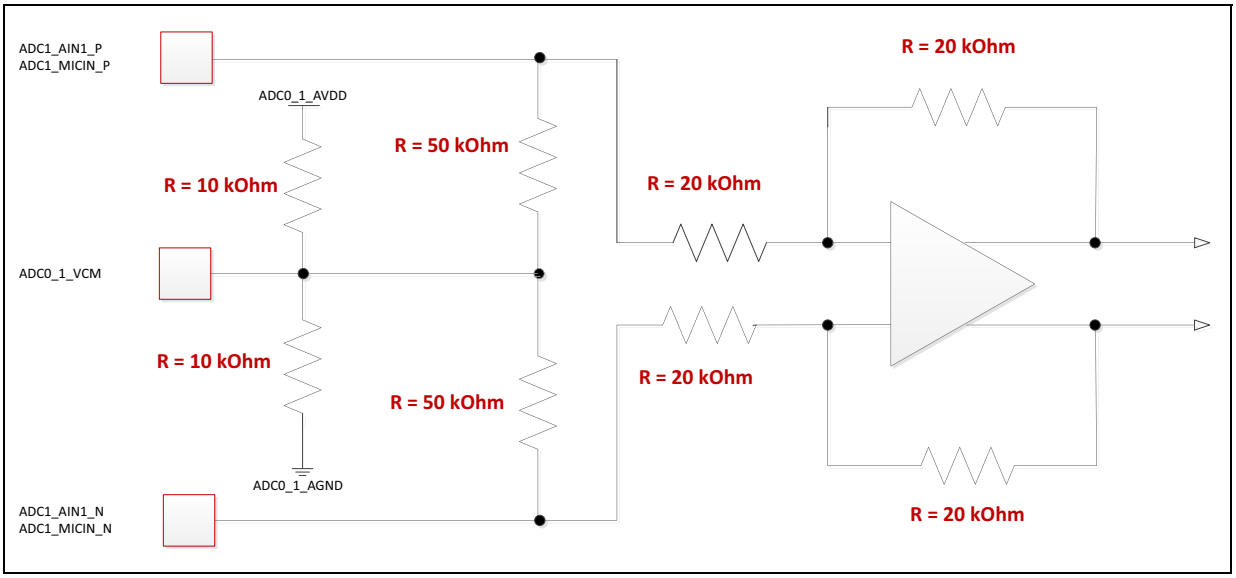
Table 43. MICADC electrical characteristics (continued)

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
I_{MIC_BIAS}	V	Current through MIC_BIAS			2	mA
$I_{DD\_AMICADC}$	C	Analog current consumption		6.5		mA

1. Max variation due to process mismatch +/- 5%

The equivalent circuit representative of the MIC ADC input is depicted in *Figure 6*.

Figure 6. MICADC input equivalent circuit



4.9.2 ADC0: Audio ΣΔ ADC electrical characteristics

Table 44. ΣΔ Audio ADC electrical characteristics

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
$V_{ASupply}$	SR	Analog supply	3.0	3.3	3.6	V
V_{in}	SR	Single ended analog input		2.8(1)		V_{p-p}
				1.0(1)		V_{rms}
V_{com}	P	DC coupled input common mode	1.5	1.65	1.8	V
		AC coupled input common mode	0	1.65	3.3	
SNR	V	Signal to noise ratio (A-weighted, 1 kHz, 0 dBFs, BW = 20 kHz)	91	94		dB
THD + N	V	Total harmonic distortion + noise	-80	-87		dB
I_{DD_ASDADC}	C	Analog current consumption		12.5		mA

1. Max possible tolerable variation +/-5%

Figure 7. Audio ADC input equivalent circuit

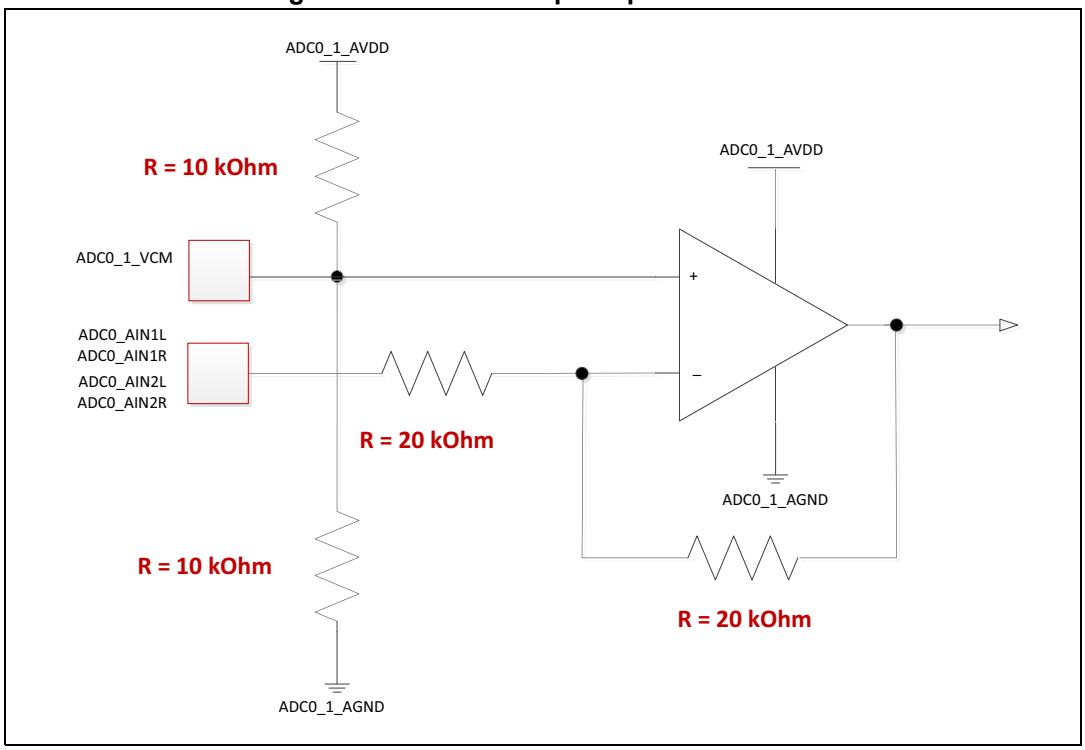
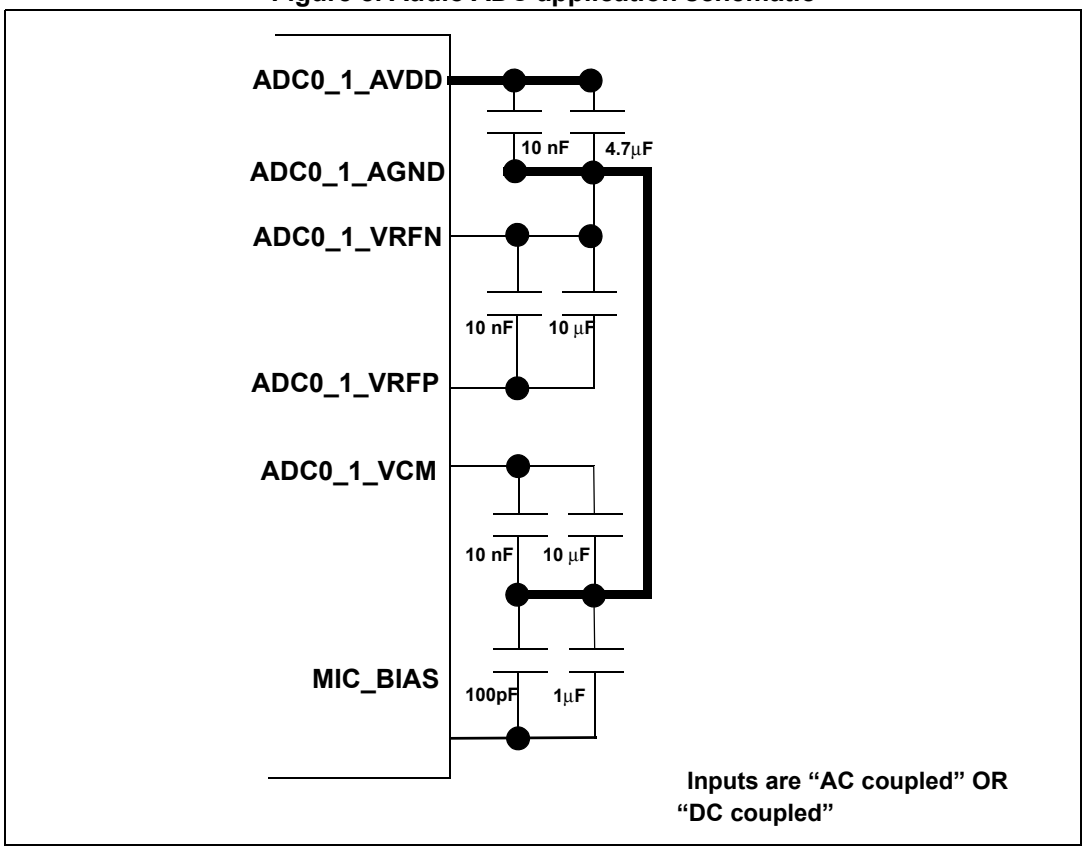


Figure 8. Audio ADC application schematic



4.9.3 DAC electrical characteristics

Table 45. DAC electrical characteristics

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
$V_{ASupply}$	SR	Analog supply	3.0	3.3	3.6	V
V_{rms}(1)	V	Analog RMS output	741	780	819	mV_{rms}
V_{rms}(2)	V	Analog RMS output	693	730	766	mV_{rms}
V_{com}	P	—	—	1.45(3)	—	V
C_{max}	SR	Maximum output load	—	—	10	pF
R_{min}	SR	Minimum output resistance	10K	—	—	Ohm
SNR	V	Signal to Noise ratio (A-weighted, BW = 20 kHz, 1 kHz, -60 dBFs)	98	103	—	dB
THD + N	V	Total harmonic distortion + Noise (A-weighted, BW = 20 kHz, 1 kHz, 0dbFS)	-82	-90	—	dB
PSRR	V	Power supply rejection ratio	57	—	78	dB
Rs	C	Series resistance at output	40	50	60	Ohm
I_{DD_ADAC}	C	Analog current consumption of single DAC	—	—	8	mA

1. No external load resistance.
2. External load resistance: 500 Ohm series on 10 kOhm next stage (10/10.5 partition).
3. Max variation due to process mismatch +/- 5%.

Figure 9. DAC output equivalent circuit

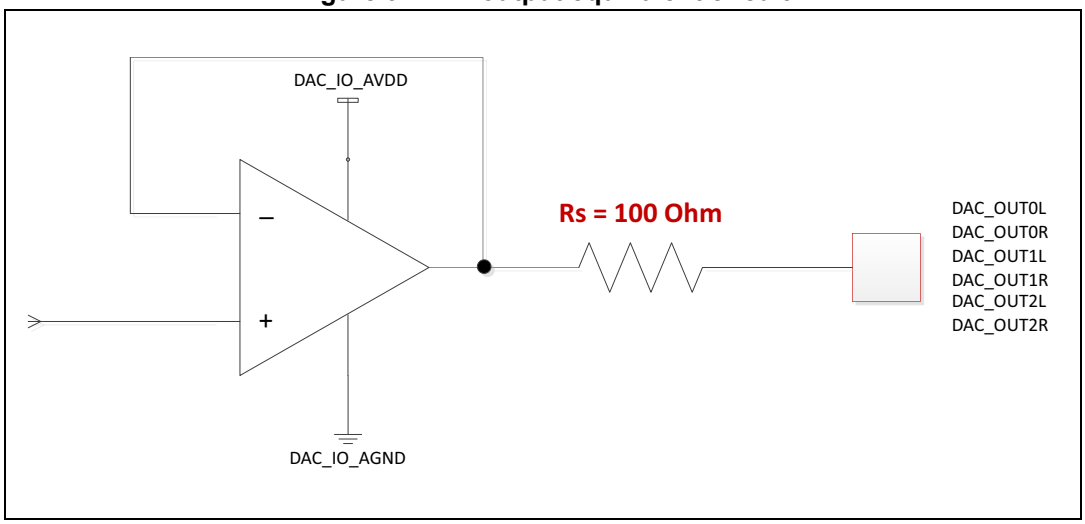


Figure 10. DAC VCOM equivalent circuit

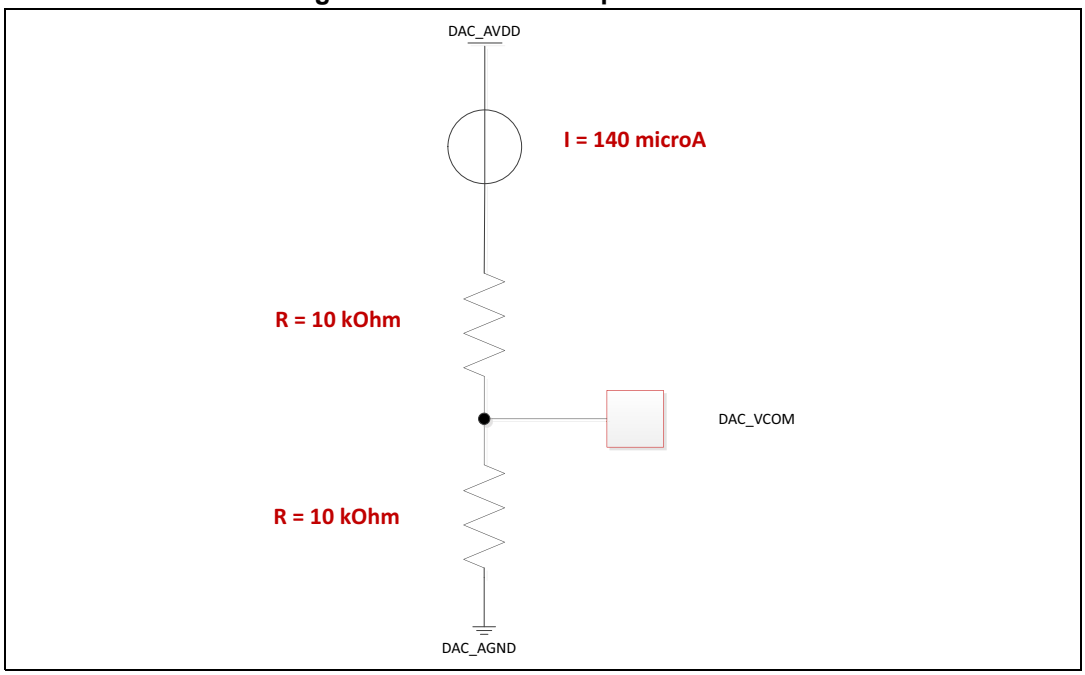
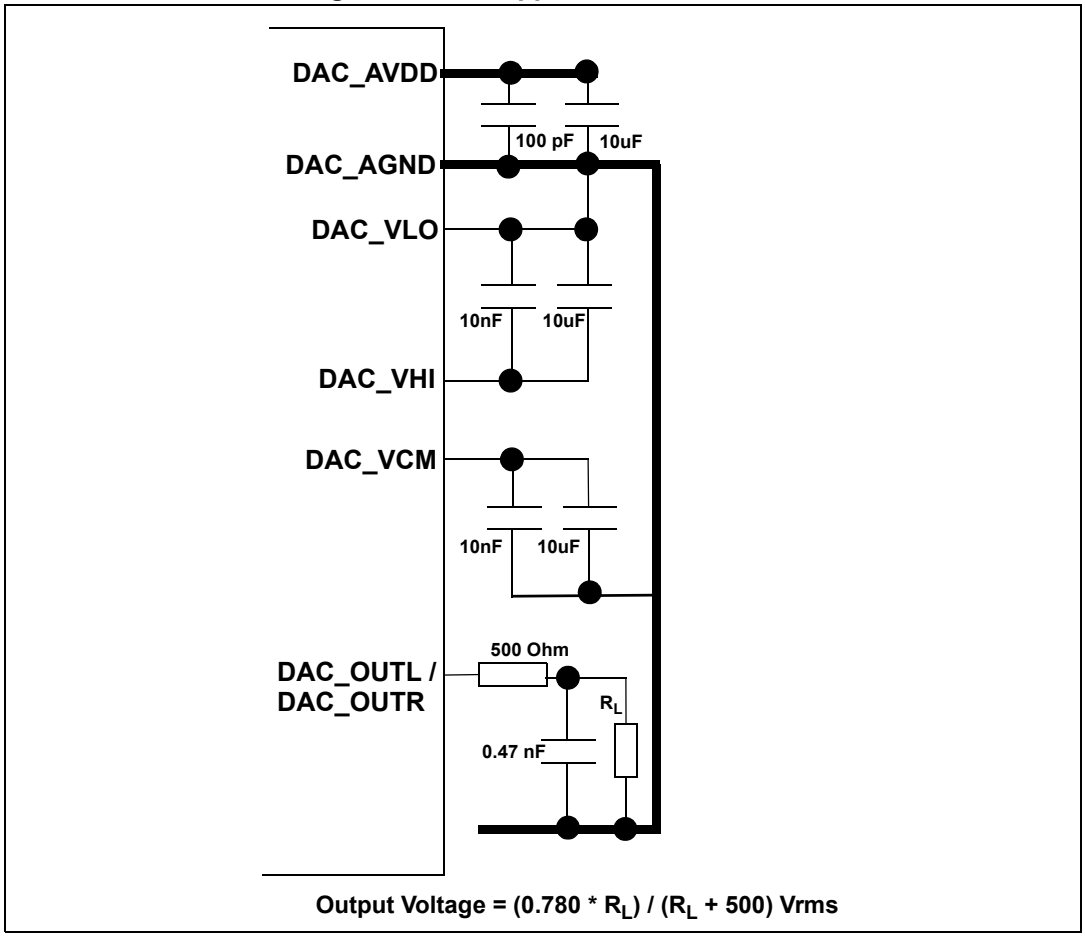


Figure 11. DAC application schematic



4.10 ADC2 and ADC3: SAR ADCs electrical characteristics

The SAR ADC is a successive approximation 10 bit Analog-to-Digital converter. Its characteristics are reported in the table below.

Table 46. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Min.	Typ.	Max.	Unit
V_{REFE}	SR	External reference voltage[2]	—	3.0	3.3	3.6	V
R_{REFE}	S	External reference input impedance	—	75	—	—	kΩ
V_{REFI}	V	Internal reference voltage	—	1.95	2.0	2.05	V
t_{START}	S	Start-up time	From Enable to first EOC	—	—	10	µs
f_{CK}	SR	ADC clock frequency (depends on system configuration)	—	4	—	13	MHz
f_s	SR	Sampling + conversion cycle	—	—	14	—	cycle
INL	P	Integral non linearity	—	-2	—	2	LSB
DNL	P	Differential non linearity[3]	—	-1	—	1	LSB
OFS	P	Offset error	—	-5	—	5	LSB
GNE	P	Gain error	—	-2	—	2	LSB
TUE	P	Total unadjusted error	Without current injection	-6	—	6	LSB
I_{INJ}	V	Max positive/negative injection[4]	—	–3	—	3	mA
SNR	V	Signal-to-noise ratio	—	58	—	—	dB
THD	V	Total harmonic distortion	—	63	—	—	dB
SINAD	V	Signal-to-noise and distortion	—	58	—	—	dB
ENOB	V	Effective number of bits	—	9.4	—	—	bits
I_{SAM}	S	Average sampling current drawn from input source	—	—	5	—	µA/Msps

1. V_{DD} = 3.3 V, T_J = -40 to +125 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}.
2. VREFP ≤ VDDA + 25 mV.
3. No missing codes.
4. Maximum current injection without ADC performance degradation.

Figure 12. ADC input equivalent circuit

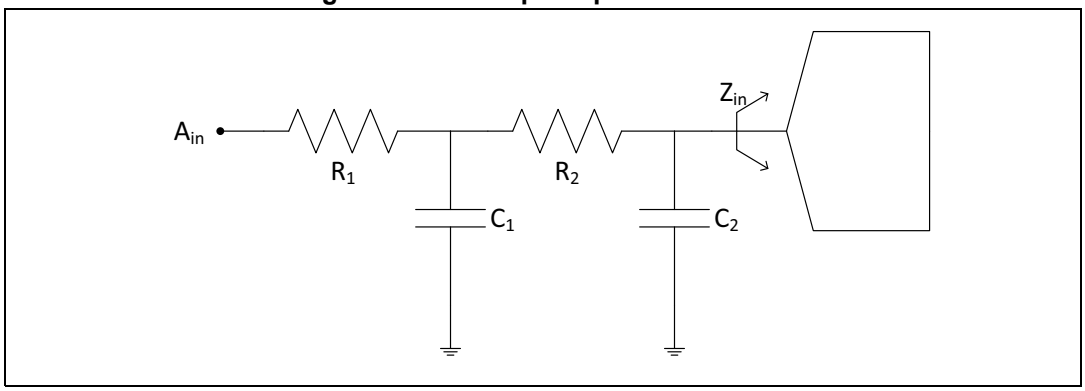


Table 47. ADC input equivalent circuit parameters values

	Min.	Typ.	Max.	Unit
R1	1.5 K	2 K	2.5 K	Ohm
C1	4p	5p	6p	Farad
R2	1.1 K	1.5 K	1.9 K	Ohm
C2	1p	1.4p	2p	Farad
Zin	—	1M	—	Ohm

4.11 Touch Screen Controller (TSC) electrical characteristics

The following table lists the electrical characteristics of the TSC.

Table 48. Touch screen controller

Symbol		Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDTSC}	SR	Full scale voltage input span(1)		3.0	3.3	3.6	V
C_{IN}	S	Total input capacitance(2)				13	pF
I_{LEAK}	S	Input leakage		-2		+2	µA
t_{SETTLE}	S	Panel settling time(3)		0.01		100	ms
t_{TOUCH}	S	Touch detect delay(3)		0.01		50	ms
R_{ON-P}	P	Y+, X+ drivers on resistance	I_{OH} = -30 mA			12	Ω
R_{ON-N}	P	Y-, X- drivers on resistance	I_{OL} = +30 mA			13	Ω
I_{PANEL}	P	Panel driver current capability				30	mA
V_{TOUCH}	P	Touch detect comparator threshold(4)	V_{DDTSC} = 3.0 V	2.1			V
V_{TOHYS}	S	Touch detect comparator hysteresis		300			mV

1. It is the same as ADC voltage reference range.
2. Equivalent to Cp1 + Cp2 + Cs in ADC section.
3. Controlled by the Touch Screen Configuration Register (TSCCONFIG).
4. Measured as VIH on X+ input.

4.12 Regulator specifications

4.12.1 Always-on LDO (3V3TO1V2 low power regulator)

Table 49. 3V3TO1V2 low power regulator

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
$V_{ASupply}$	SR	Analog supply	3.0	3.3	3.6	V
$V_{out(@100\mu A)}$	P	Output voltage @ $I_{load = max}$	1.14	1.2	1.26	V
C_{load}	SR	Total off chip capacitance value(1)	—	—	2.2	nF
PSRR	S	Power supply rejection at DC @ Full load	—	-50	-40	dB
PSRR	S	Power supply rejection at 1 MHz @ Full load	—	-50	-40	dB
T_{start}	S	Start up time from power down to active	—	—	500	µs

1. This is mandatory for proper device functionality.

4.12.2 VDDIO_ON main voltage detector

Table 50. VDDIO_ON supply LVD

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
V_{uthres}	P	Upper voltage threshold (Value @ 27C, 0 sigma) Sigma: 12 mV	2.78	—	2.92	V
V_{lthres}	P	lower voltage threshold (Value @ 27C, 0 sigma) Sigma: 12 mV	2.69	—	2.83	V
V_{hyst}	S	Hysteresis	—	90	—	mV

4.12.3 PLL LDO (3V3TO2V5 low power regulator)

Table 51. 3V3TO2V5 regulator

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
$V_{ASupply}$	SR	Analog supply	3.0	3.3	3.6	V
V_{out}	P	Output voltage @ $I_{load = max}$	2.375	2.5	2.63	V
C_{load}	SR	Total off chip capacitance values (1)	—	4.7	—	µF
		ESR of each external capacitor in frequency range of 100 kHz - 100 MHz	10 m	—	150 m	Ω
PSRR_DC	S	Power supply rejection at DC @ NO load	—	—	-23	dB

Table 51. 3V3TO2V5 regulator (continued)

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
PSRR	S	Power supply rejection at 2 MHZ @ NO load	—	—	-12	dB
T_{start}	S	Start up time from power down to active after input supply stabilizes (Supply rise time of 1 µs)	—	—	300	µs

1. This is mandatory for proper device functionality.

4.12.4 USB 1V8 LDO (3V3TO1V8 low power regulator)

Table 52. 3V3TO1V8 regulator

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
$V_{ASupply}$	SR	Analog supply(1)	3.0	3.3	3.6	V
V_{out}	P	Output voltage @ $I_{load = max}$	1.71	—	1.87	V
C_{load}	SR	Total off chip capacitance value(2)	—	4.7	—	µF
		ESR of each external capacitor in frequency range of 100 kHz - 100 MHz	10 m	—	150 m	Ω
PSRR_DC	S	Power supply rejection at DC @ NO load	—	—	-40	dB
PSRR	S	Power supply rejection at 2 MHz @ NO load	—	—	-11	dB
T_{start}	S	Start up time from power down to active after input supply stabilizes (Supply rise time of 1 µs)	—	—	300	µs

1. USB_VREG3V3_1V8, USB0_VDD3V3 and USB1_VDD3V3 are internally shorted in the device IO ring.
2. This is mandatory for proper device functionality.

4.12.5 USB 1V1 LDO (3V3TO1V1 low power regulator)

Table 53. 3V3TO1V1 regulator

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
$V_{ASupply}$	SR	Analog supply	3.0	3.3	3.6	V
V_{out}	P	Output voltage @ $I_{load = max}$	1.0	1.1	—	V
C_{load}	SR	Total off chip capacitance value(1)	—	4.7	—	µF
PSRR_DC	S	Power supply rejection at DC @ Full load	—	—	-30	dB
PSRR	S	Power supply rejection at 1 MHz @ Full load	—	—	-28	dB
T_{start}	S	Start up time from power down to active after input supply stabilizes (Supply rise time of 1 µs)	—	—	300	µs

1. Mandatory for proper device functionality

4.13 Temperature sensor

Table 54. Temperature sensor

Symbol		Parameter	Limit values			Unit
			Min.	Typ.	Max.	
T_{sens}	C	Sensitivity	—	—	1	°C
T_{acc}	C	Accuracy	+/-4	—	+/-6	°C
T_{max}	S	Start-up time for analog core after PDN signal is asserted(1)	—	—	0.5	ms

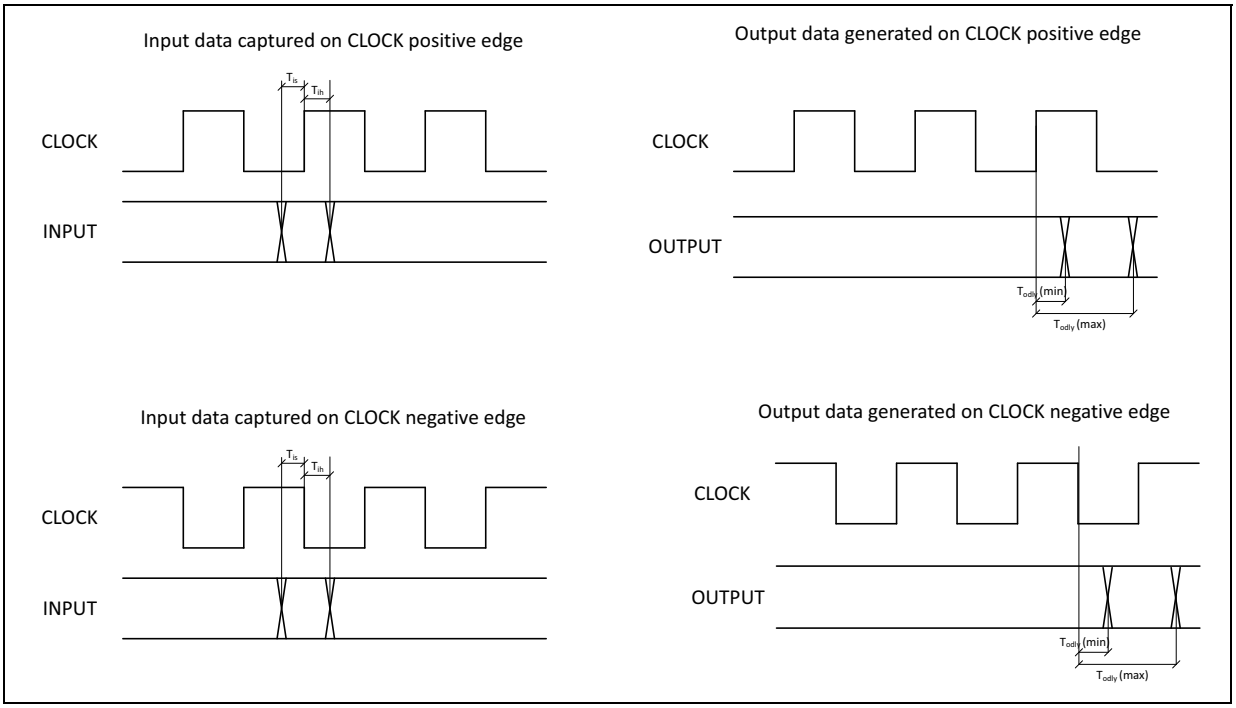
1. Corresponds to bit 31 of Thermal sensor control register

4.14 Interface timing characteristics

The values for interface timings provided in the paragraphs belonging to this section refer to the following diagrams valid respectively for:

- Input data sampled on the rising edge of the clock
- Input data sampled on the falling edge of the clock
- Output data generated on the rising edge of the clock
- Output data generated on the falling edge of the clock

Figure 13. Timing diagrams



4.14.1 SDMMC0 interface timing

The following tables provide the timings for SDMMC0 interface.

Launching and capturing clock edges are as per standard. This means: in Default Speed mode, launching occurs on falling clock edges and capturing occurs on rising clock edges. In High Speed mode and SDR50 mode, launching and capturing both occur on rising clock edges.

Timings are provided taking the active edge at SoC side as reference.

Table 55. Normal Speed (JEDEC); Default Speed (SD); UHS- I SDR12 (SD)

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	26	MHz	25 pF	IP can run up to 26 MHz. For SD modes, setting of 24 MHz is recommended to meet typical external component limitations (25 MHz).
	CLK period	38.4	—	ns	25 pF	—
	CLK duty cycle	40	60	%	—	
Input	TIS	3	—	ns	—	7 ns in case internal clocking mode is used (no feedback clock).
	TIH	1	—	ns	—	—
Output	Todly	0	5.5	ns	25 pF	Output hold time is taken care of by capturing on opposite clock edge.

Table 56. High Speed SDR (JEDEC); High Speed (SD); UHS- I SDR25 (SD)

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	52	MHz	25 pF	IP can run up to 52 MHz. For SD modes, setting of 48 MHz is recommended to meet typical external component limitations (50 MHz).
	CLK period	19.2	—	ns	25 pF	—
	CLK duty cycle	40	60	%	—	
Input	TIS	2	—	ns	—	
	TIH	1	—	ns	—	
Output	Todly	1	5.5	ns	25 pF	

Table 57. HS200 (JEDEC); UHS- I UHS50: SDR50 (SD)

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	104	MHz	25 pF	IP can run up to 104 MHz. Setting of 96 MHz is recommended to meet typical external component limitations (100 MHz).
	CLK period	9.6	—	ns	25 pF	—
	CLK duty cycle	40	60	%	—	
Input	TIS	2	—	ns	—	
	TIH	1	—	ns	—	
Output	Todly	1	5.2	ns	25 pF	

4.14.2 SDMMC1/2 interface timing

The following tables provide the timings for SDMMC1/2 interface.

Launching and capturing clock edges are as per standard. This means: in Default Speed mode, launching occurs on falling clock edges and capturing occurs on rising clock edges. In High Speed mode, launching and capturing both occur on rising clock edges.

Timings are provided taking the active edge at SoC side as reference.

Table 58. Normal Speed (JEDEC); Default Speed (SD); UHS- I SDR12 (SD)

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	26	MHz	33 pF	IP can run up to 26 MHz. For SD modes, setting of 24 MHz is recommended to meet typical external component limitations (25 MHz).
	CLK period	38.4	—	ns	33 pF	—
	CLK duty cycle	40	60	%	—	
Input	TIS	2	—	ns	—	6 ns in case internal clocking mode is used (no feedback clock)
	TIH	2.5	—	ns	—	—
Output	Todly	0	13.7	ns	33 pF	

Table 59. High Speed SDR (JEDEC); High Speed (SD); UHS- I SDR25 (SD)

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	52	MHz	33 pF	IP can run up to 52 MHz. Setting of 48 MHz is recommended to meet typical external component limitations (50 MHz).
	CLK period	19.2	—	ns	33 pF	—
	CLK duty cycle	30	70	%	—	
Input	TIS	2	—	ns	—	
	TIH	2.5	—	ns	—	
Output	Todly	2.2	13	ns	33 pF	

4.14.3 SQIO interface timing

The following table provides the timings for SQIO interface.

Launching occurs on falling clock edge, capturing occurs on rising clock edge.

Timings are provided taking the active edge at SoC side as reference.

Table 60. SQIO

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	125	MHz	25 pF	—
	CLK period	8	—	ns	25 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	0	—	ns	—	
	TIH	2	—	ns	—	
Output	Todly	-1	1	ns	25 pF	

4.14.4 LCD interface timing

The following tables provide the timings for LCD interface.

The launching edge is programmable: the edge should be chosen in such a way that capturing occurs on the clock edge opposite to the launching edge.

Timings are provided taking the active edge at SoC side as reference.

Table 61. LCD - Single display

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	Display CLK freq	—	156	MHz	25 pF	—
	Display CLK period	6.41	—	ns	25 pF	
	Display CLK duty cycle	40	60	%	—	
	Pixel CLK freq	—	156	MHz	25 pF	
	Pixel CLK period	6.41	—	ns	25 pF	
	Pixel CLK duty cycle	40	60	%	—	
Output	Todly	-0.72	1	ns	25 pF	

Table 62. LCD - Dual display with edge shift (valid for each display output)

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	Display CLK freq	—	44.55	MHz	25 pF	—
	Display CLK period	22.45	—	ns	25 pF	
	Display CLK duty cycle	40	60	%	—	
	Pixel CLK freq	—	89.1	MHz	25 pF	
	Pixel CLK period	11.22	—	ns	25 pF	
	Pixel CLK duty cycle	40	60	%	—	
Output	Todly	-2.5	3.5	ns	25 pF	

4.14.5 VIP interface timing

The following table provides the timings for VIP interface.

The capturing edge is programmable and should be chosen to be the one opposite to the launching edge of external device.

Timings are provided taking the active edge at SoC side as reference.

Table 63. VIP timing

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	60	MHz	—	—
	CLK period	16.7	—	ns	—	
	CLK duty cycle	40	60	%	—	
Input	TIS	2	—	ns	—	
	TIH	0.5	—	ns	—	

4.14.6 SPI interface timing

The following tables provide the timings for SSP interface.

The clock and data alignment is configurable depending on the frame format that is selected; data is assumed to always be captured on the clock edge opposite to the launching edge.

Timings are provided taking the active edges (capture edge for inputs and launching edge for outputs) at SoC side as reference.

Table 64. SSP - SPI (master)

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	52	MHz	25 pF	—
	CLK period	19.2	—	ns	25 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	7	—	ns	—	
	TIH	2	—	ns	—	
Output	Todly	-2	4		25 pF	

Table 65. SSP- SPI (slave)

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	12	MHz	25 pF	—
	CLK period	83.3	—	ns	25 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	4	—	ns	—	
	TIH	—	—	ns	—	
Output	Todly	0	13	ns	25 pF	

4.14.7 Ethernet interface timing

The following tables provide the timings for the Ethernet interface.

In RGMII mode 1Gbit/sec speed, operation is double-data-rate.

In all other modes, the active clock edge (data launch and data capture) is the rising clock edge.

Timings are provided taking the active edges at SoC side as reference.

Table 66. RGMII mode - 1Gbit/sec operation

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	125	MHz	10 pF	—
	CLK period	8	—	ns	10 pF	
	CLK duty cycle	45	55	%	—	
Input	TIS	1	—	ns	—	
	TIH	1	—	ns	—	
Output	Todly	-0.5	0.5	ns	10 pF	Data is launched in double data rate (on both of the clock edges)

Table 67. RGMII mode - 100Mbit/sec operation

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	25	MHz	10 pF	—
	CLK period	40	—	ns	10 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	1	—	ns	—	
	TIH	1	—	ns	—	
Output	Todly	-0.5	0.5	ns	10 pF	

Table 68. RGMII mode - 10Mbit/sec operation

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	2.5	MHz	10 pF	—
	CLK period	400	—	ns	10 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	1	—	ns	—	
	TIH	1	—	ns	—	
Output	Todly	-0.5	0.5	ns	10 pF	

Table 69. RGMII mode

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	50	MHz	10 pF	—
	CLK period	20	—	ns	10 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	2	—	ns	—	
	TIH	2	—	ns	—	
Output	Todly	2	10	ns	10 pF	

4.14.8 MSP (I2S) interface timing

The following tables provide the timings for MSP interface.

Opposite edge data capture protocol should be used for both master and slave modes.

All timings are given with regards to the active clock edge (capturing edge for input and launching edge for output).

Table 70. MSP2 - Master

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	12.5	MHz	25 pF	—
	CLK period	80	—	ns	25 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	18	—	ns	—	
	TIH	0	—	ns	—	
Output	Todly	-0.5	2	ns	25 pF	

Table 71. MSP0 - Master

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	12.5	MHz	25 pF	—
	CLK period	80	—	ns	25 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	12	—	ns	—	
	TIH	0	—	ns	—	
Output	Todly	-0.5	2	ns	25 pF	

Table 72. MSP2 - Slave

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	12.5	MHz	25 pF	—
	CLK period	80	—	ns	25 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	7	—	ns	—	
	TIH	4	—	ns	—	
Output	Todly	0	12	ns	25 pF	

Table 73. MSP0 - Slave

Type	Symbol	Min	Max	Unit	Load	Notes
Clock	CLK freq	—	12.5	MHz	25 pF	—
	CLK period	80	—	ns	25 pF	
	CLK duty cycle	40	60	%	—	
Input	TIS	4	—	ns	—	
	TIH	4	—	ns	—	
Output	Todly	0	11	ns	25 pF	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK is an ST trademark.

5.1 LFBGA529 package information

Figure 14. LFBGA529 package outline

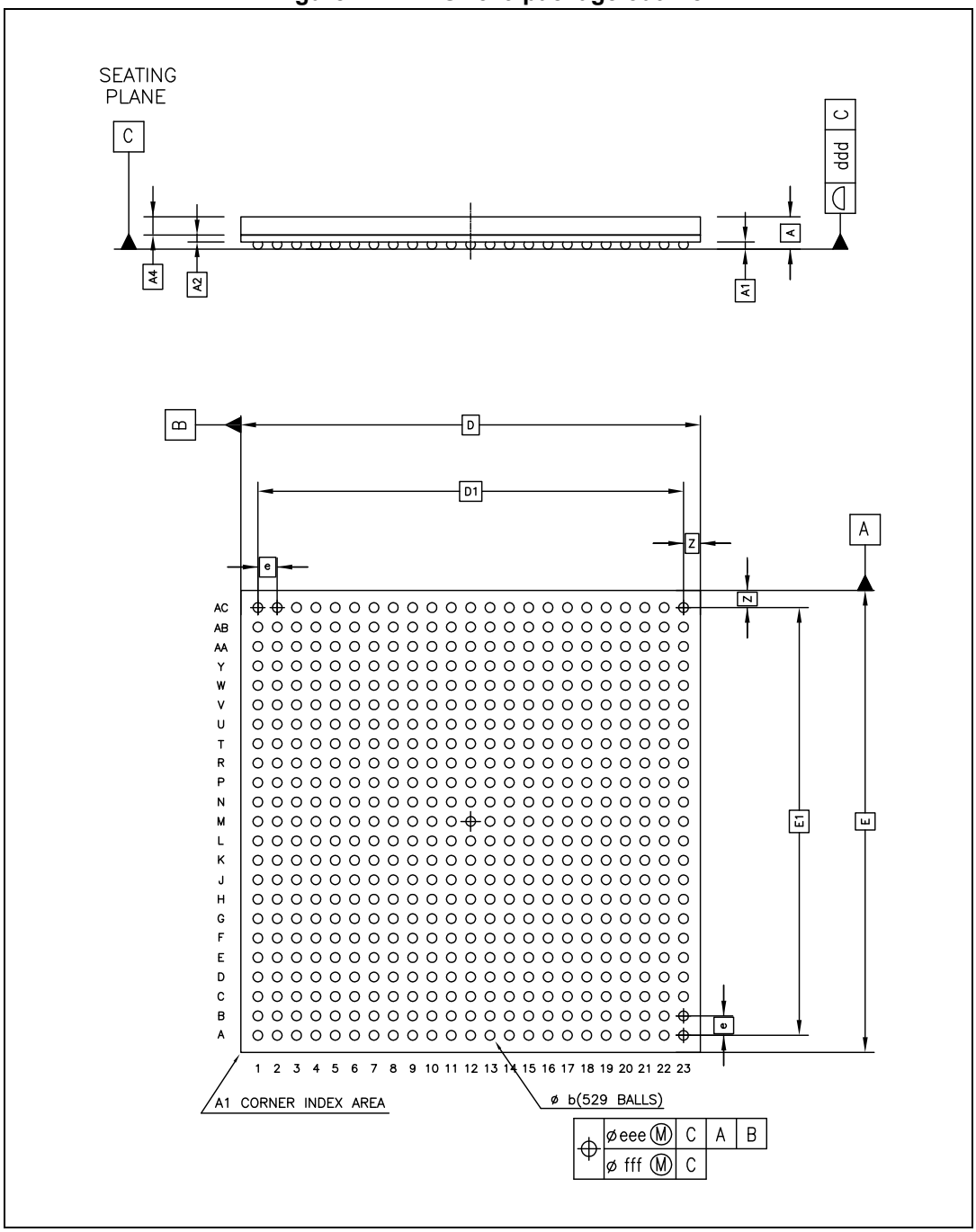


Table 74. LFBGA529 package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A[2]	—	—	1.70	—	—	0.0669
A1	0.25	—	—	0.0098	—	—
A2	—	0.28	—	—	0.0110	—
A4	—	—	0.80	—	—	0.0315
b[3]	0.35	0.40	0.48	0.0138	0.0157	0.0189
D	18.85	19.00	19.15	0.7421	0.7480	0.7539
D1	—	17.60	—	—	0.6929	—
E	18.85	19.00	19.15	0.7421	0.7480	0.7539
E1	—	17.60	—	—	0.6929	—
e	—	0.80	—	—	0.0315	—
Z	—	0.70	—	—	0.0276	—
ddd	—	—	0.10	—	—	0.0039
eee[4]	—	—	0.15	—	—	0.0059
fff[5]	—	—	0.08	—	—	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. FPBGA stands for Fine Pitch Plastic Ball Grid Array:
   Low Profile: the total profile height (Dim A) is measured from the seating plane to the top of the component:
   1.20 mm < A ≤ 1.70 mm / fine pitch: e < 1.00 mm pitch.
   The maximum total package height is calculated by the following methodology:
   Amax = A1 Typ + A2 Typ + A4 Typ + $\sqrt{(A1^2 + A2^2 + A4^2}$ tolerance values).
3. The typical ball diameter before mounting is 0.40 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

6 Ordering information

Part numbers / sales codes are composed as follows:

- STA
- Root
- Freq
- Sec
- Grade
- Pack

Table 75. Order codes description

[Root] Root code	[Freq] Cortex® A7 frequency	[Sec] Security	[Grade] Qualification grade	[Pack] Packing
1275 (single core Cortex® A7, 16bit DDR3)	**E** = Eco (650 MHz)	**L** = Locked(1)	**A** = Automotive	[empty] = Tray
1295 (dual core Cortex® A7, 32bit DDR3)		**O** = Open(2)		**TR** = Tape&Reel
		U = Unsecure(3)		
Part number example: STA1295EOA				
1295	**E** = Eco (650 MHz)	**O** = Open	**A** = Automotive	[empty] = Tray

1. JTAG locked, secure boot enabled.
2. JTAG open, secure boot disabled.
3. JTAG locked, secure boot disabled.

Note: Contact your ST sales office to ask for the availability of a particular commercial product. Features (for instance, single/dual core, security open/locked) which are not included in the commercial product, cannot be used.
ST cannot be called to take any liability for features used outside the commercial product.

7 Revision history

Table 76. Document revision history

Date	Revision	Changes
07-June-2018	1	Initial release.
20-Sep-2018	2	Minor format updates in *Section : Features* Added *Chapter 4: Electrical characteristics* Removed STA1295 from title of *Chapter 5: Package information*
09-May-2019	3	Added STA1275 in the whole document. *Section : Features*: – Updated package picture. – *Core and infrastructure*: updated 1st bullet. – *Operating conditions*: added Junction temperature range. *Chapter 1: Description* – Updated 1st bullet. – *Figure 1: Accordo5 block diagram*: renamed this title. *Chapter 2: System description* *Section 2.1: Application processor*: updated. *Section 2.2.2: DDR controller*: updated. – *Figure 2: Accordo5 sound subsystem application example*: updated figure and title. *Chapter 4: Electrical characteristics* *Section 4.3: Absolute maximum ratings* – *Table 30: Absolute maximum ratings*: updated Min. and Max. columns. *Section 4.5: Thermal characteristics*: – Replaced sentence ‘The number ... for power” by “Table 35 ... junction temperature. – Deleted from “Cases 3 and 4” to “worst corner”. – Deleted Table 35: Current consumption (mA). – Added *Table 35: Accordo5 - STA1295 - current consumption*. *Chapter 6: Ordering information*: – *Table 75: Order codes description*: updated table and added footnotes.

Table 76. Document revision history

Date	Revision	Changes
27-Aug-2020	4	Removed “ST restricted” Watermark throughout the document. Cover page – Updated title – Added “LFBGA529” under the figure – Updated the frequency to 660MHz in the memory organization section *Section 2.2.2: DDR controller* Updated frequency to 660 MHz *Section 2.2.3: SQI NOR interface* Updated frequency to 125 MHz *Section 2.11.1: Audio interfaces*: – updated bullet starting with “2x Voice ADC” – Removed “mic pre amp” and “ADC is shared among voice and TEL IN lines with embedded multiplexer” *Section 2.17.1: Application GPIO alternate function mapping*: Added note under section title *Table 10: Application GPIO alternate function mapping*: Added table footnote to GPIO108-113 *Section 2.17.2: Secure GPIO alternate function mapping*: Added note under section title *Table 23: USB signals*: – USB0_DN and USB0_DP: Power domain updated to USB0_VDD3V3 – USB1_DN and USB1_DP: Power domain updated to USB1_VDD3V3 *Table 30: Absolute maximum ratings*: V_{INPUT}: Updated maximum value to V_{VDD_IOx} + 0.3 *Table 37: Digital DC characteristics at 3.3 V*: Added table footnote related to V_{TH+} and V_{TL-} And other minor editing updates.
29-Apr-2021	5	Following are the changes in this version of the document: Updated the document header from STA1275, STA1295 to STA1295, STA1275 throughout the document. *Table 30: Absolute maximum ratings*: Updated V_{INPUT} *Section 6: Ordering information*: Added note “Contact your ST sales office to ask....”

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