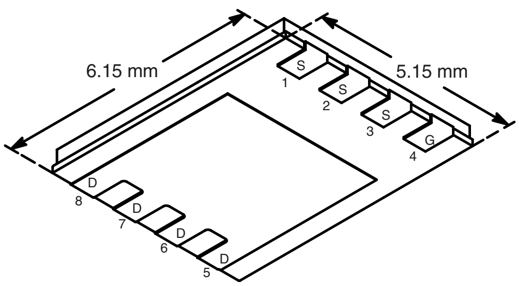
N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
100	0.0306 at V_{GS} = 10 V	28.4	15.5 nC
	0.0327 at V_{GS} = 7.5 V	27.5	

PowerPAK SO-8



Bottom View

Ordering Information: SiR432DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

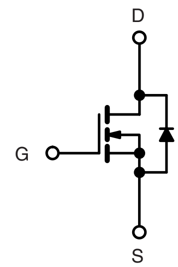
FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Primary Side Switch



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	28.4	A
	T_C = 70 °C		22.7	
	T_A = 25 °C		8.6[b, c]	
	T_A = 70 °C		6.9[b, c]	
Pulsed Drain Current		I_{DM}	40	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	40[g]	
	T_A = 25 °C		4.2[b, c]	
Avalanche Current	L = 0.1 mH	I_{AS}	17	
Single-Pulse Avalanche Energy		E_{AS}	14.5	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	54	W
	T_C = 70 °C		34.7	
	T_A = 25 °C		5.0[b, c]	
	T_A = 70 °C		3.2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 10 s	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.8	2.3	

Notes:
a. Based on T_C = 25 °C.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under Steady State conditions is 65 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		100		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 8.6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	2		4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ 5 V, V_{GS} = 10 V	40			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 8.6 A		0.0255	0.0306	Ω
		V_{GS} = 7.5 V, I_D = 8.3 A		0.0272	0.0327	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 8.6 A		38		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		1170		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			45		
Total Gate Charge	Q_g	V_{DS} = 50 V, V_{GS} = 10 V, I_D = 8.6 A		21	32	nC
		V_{DS} = 50 V, V_{GS} = 7.5 V, I_D = 8.6 A		15.5	24	
Gate-Source Charge	Q_{gs}			5.9		
Gate-Drain Charge	Q_{gd}			5.4		
Gate Resistance	R_g	f = 1 MHz	0.2	0.9	1.8	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 7.2 Ω $I_D \cong$ 6.9 A, V_{GEN} = 10 V, R_g = 1 Ω		12	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, R_L = 7.2 Ω $I_D \cong$ 6.9 A, V_{GEN} = 7.5 V, R_g = 1 Ω		14	21	
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			18	27	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			40	A
Pulse Diode Forward Current[a]	I_{SM}				40	
Body Diode Voltage	V_{SD}	I_S = 6.9 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 6.9 A, dI/dt = 100 A/µs, T_J = 25 °C		43	65	ns
Body Diode Reverse Recovery Charge	Q_{rr}			80	120	nC
Reverse Recovery Fall Time	t_a			33		ns
Reverse Recovery Rise Time	t_b			10		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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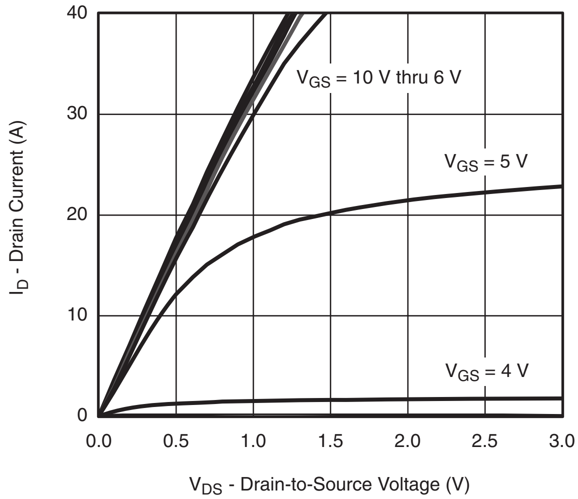
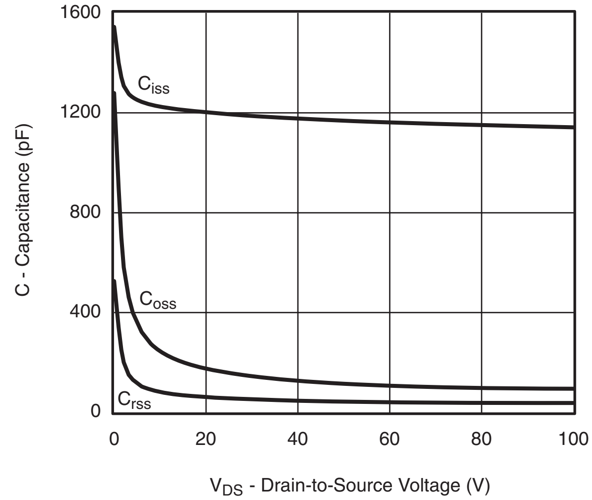
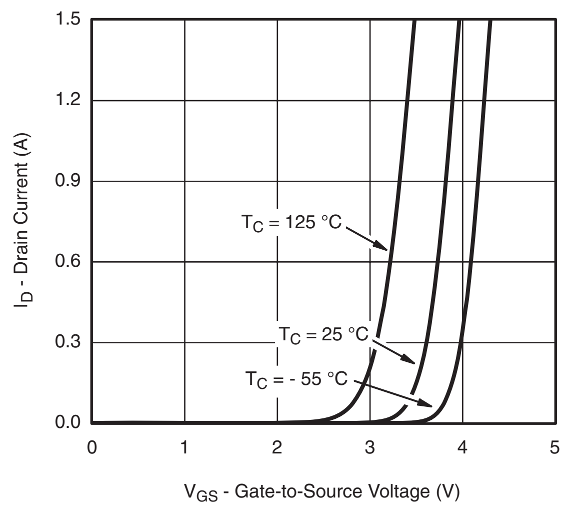
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



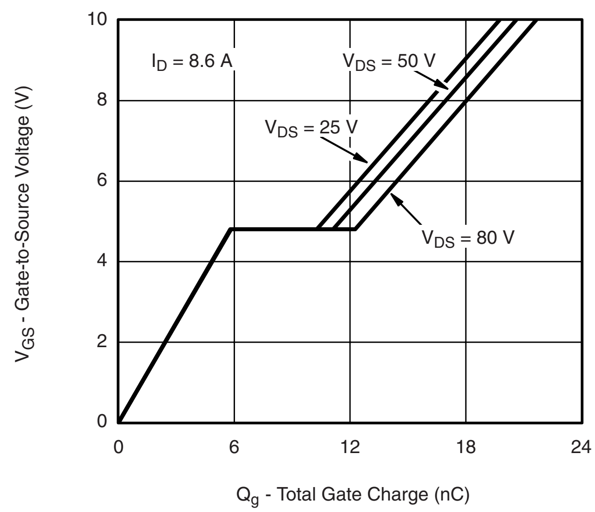
Output Characteristics



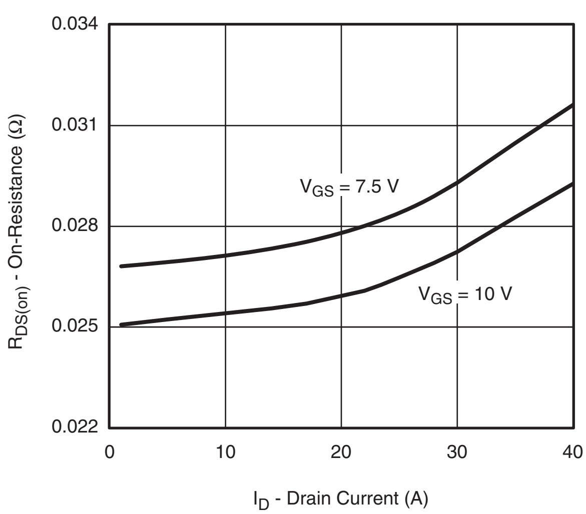
Transfer Characteristics



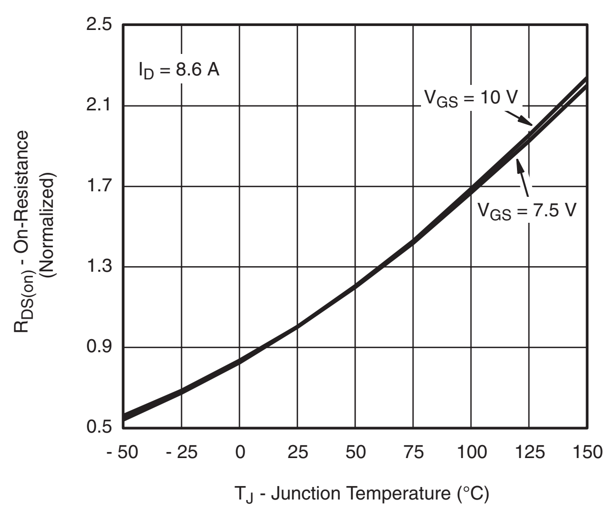
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

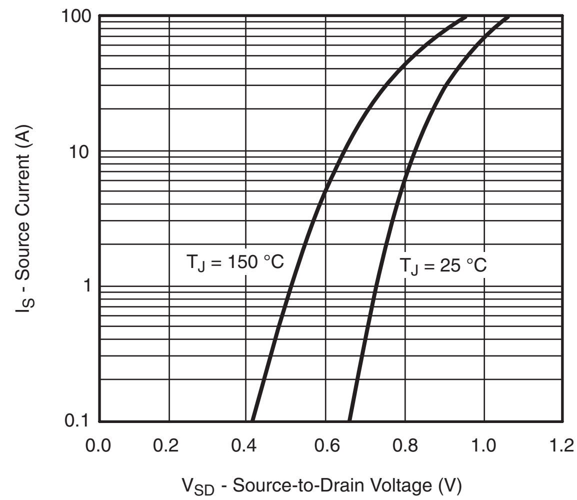


Gate Charge

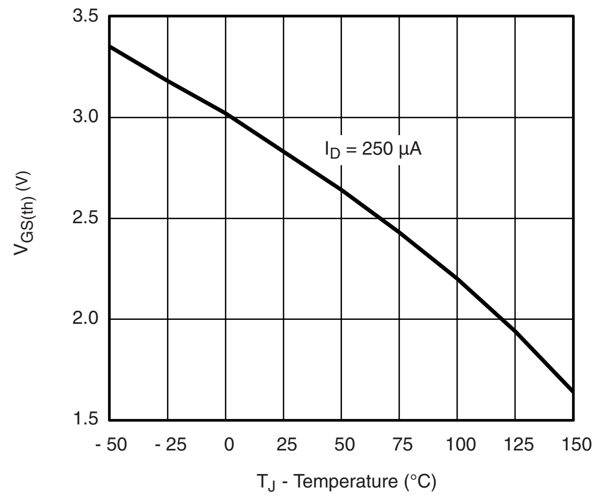


On-Resistance vs. Junction Temperature

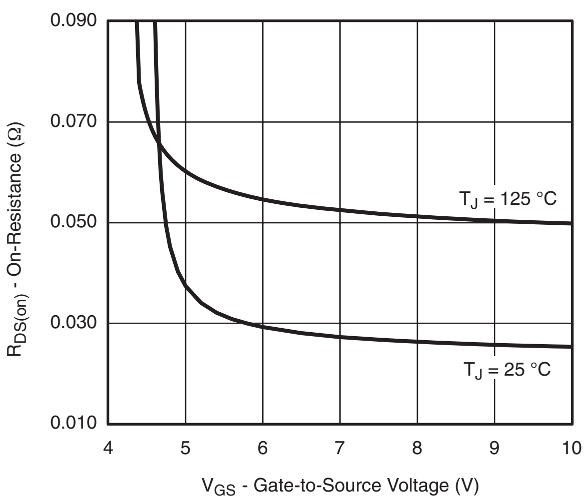
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



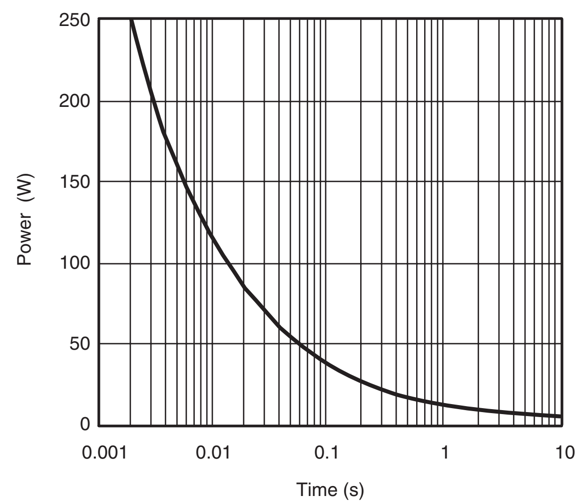
Source-Drain Diode Forward Voltage



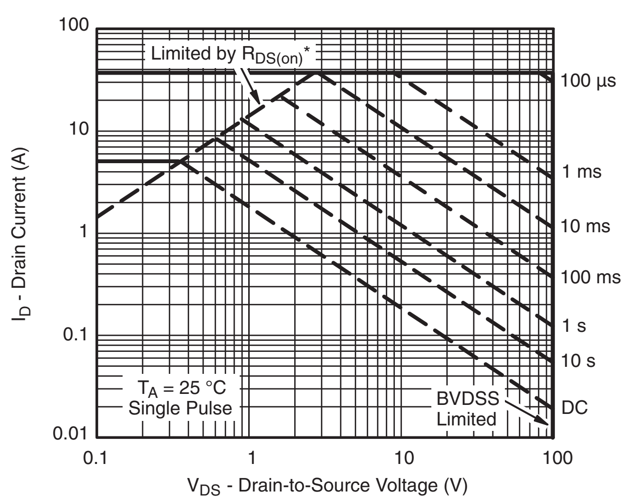
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



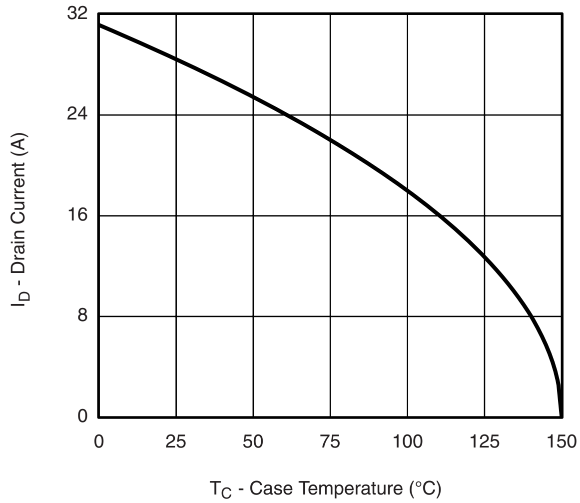
Single Pulse Power, Junction-to-Ambient



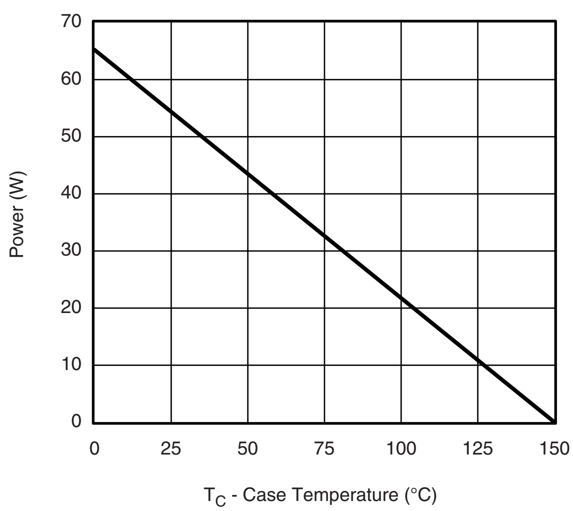
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

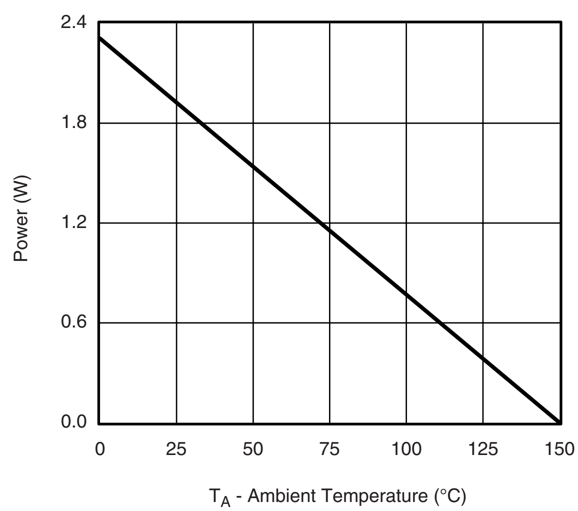
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



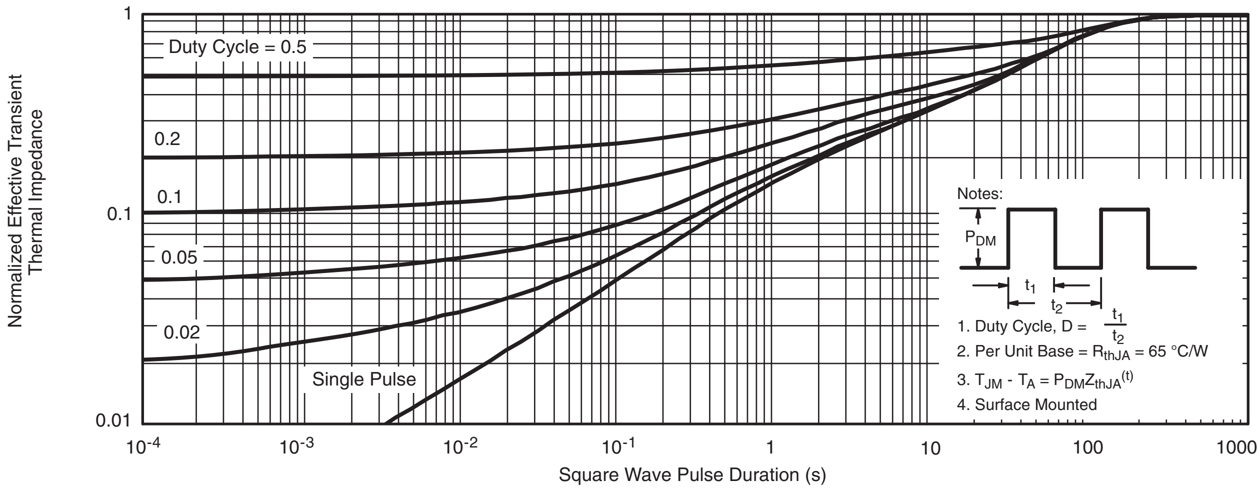
Power Derating



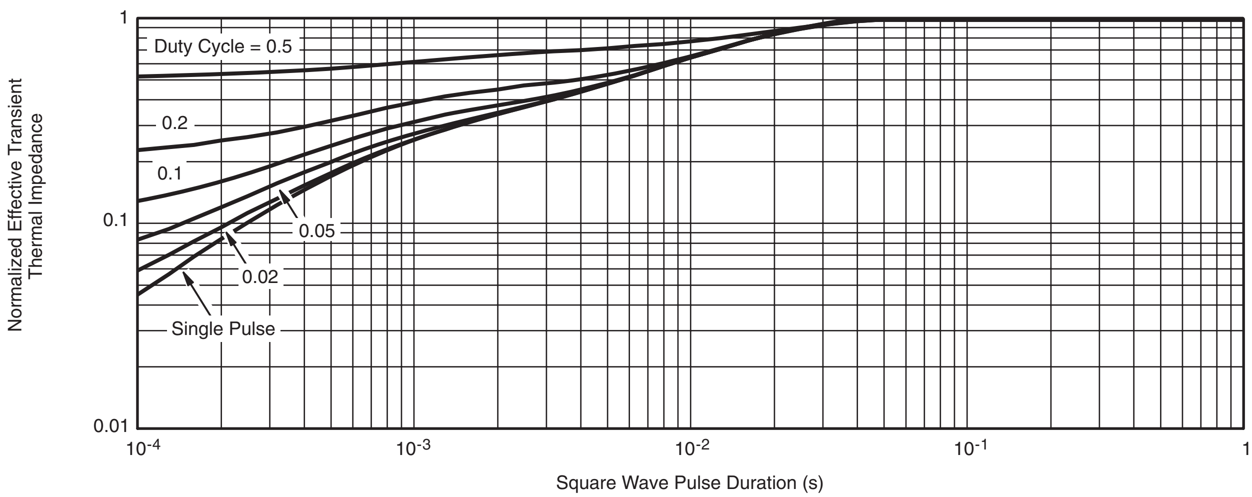
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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