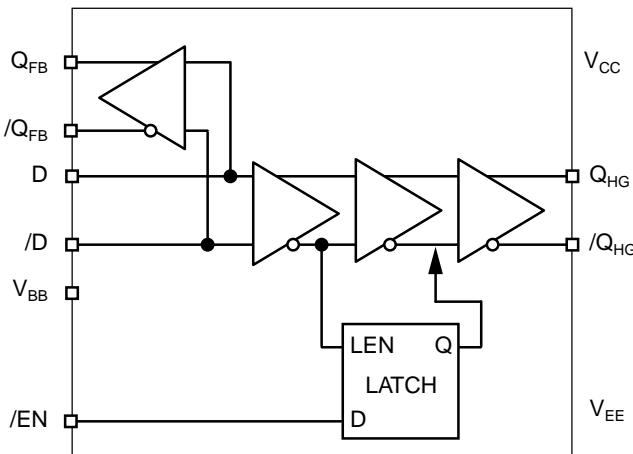


- **3.3V and 5V  $\pm 10\%$  power supply options**
- **Guaranteed AC parameters over temperature:**
  - $f_{MAX} = 800\text{MHz}$
  - $< 200\text{ps}$  differential propagation delay (D to  $Q_{FB}$ )
  - $< 730\text{ps}$  differential propagation delay (D to  $Q_{HG}$ )
  - $< 250\text{ps}$   $t_r / t_f$
- **Low gain feedback path  $Q_{FB} = +10\text{V/V}$**
- **Output enable**
- **$V_{BB}$  reference output voltage**
- **Wide temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$**
- **Available in 10-pin (3x3mm) MSOP**

The SY100EL16VO is a differential receiver amplifier optimized for crystal oscillator applications. The device includes an additional low gain ( $+10\text{V/V}$ ) output stage ( $Q_{FB}$ ) ideal for feedback applications common in crystal oscillator gain blocks. The SY100EL16VO is fully differential, with a bandwidth  $> 800\text{MHz}$  over temperature and voltage. For applications that require output disable control, an Enable pin (/EN) will force the differential output into a fixed logic state. The SY100EL16VO also includes a  $V_{BB}$  reference voltage for single-ended or AC-coupled applications.

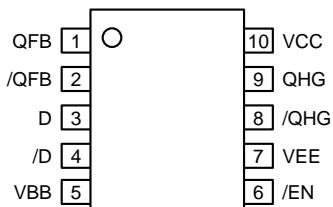
The SY100EL16VO PECL logic is 100k ECL compatible. Operation is guaranteed over the  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range and 3.3V to 5V nominal supply voltage range.

/EN	QHG Out	/QHG Out
0	Data	/Data
1	Logic Low	Logic High



Pin	Function
$Q_{FB}, /Q_{FB}$	Differential clock outputs for feedback path: Nominal DC gain +10.
D, /D	PECL, LVPECL, ECL, LVECL differential inputs: Internal $75\text{k}\Omega$ pull-down resistor.
$V_{BB}$	$V_{CC} - 1.32\text{V}$ reference voltage for single-ended inputs: It provides the switching reference for the input differential amplifier. When unused, it can be left open. For single-ended PECL applications connect $V_{BB}$ to /D input, and bypass with a $0.01\mu\text{F}$ capacitor to $V_{CC}$ .
/EN	Enable: PECL compatible input control with internal $75\text{k}\Omega$ pull-down resistor. It controls the high-gain output ( $Q_{HG}$ ). When HIGH, $Q_{HG}$ is low and $/Q_{HG}$ is high. /EN is synchronous so that the outputs will only be enabled/disabled when they are in the LOW state.
$V_{EE}$	Negative power supply: For ECL/LVECL operation, connect to negative supply. For PECL/ LVPECL operation, connect to GND.
$Q_{HG}, /Q_{HG}$	Differential high-gain outputs: Nominal DC gain is greater than +200.
$V_{CC}$	Positive power supply: For ECL/LVECL operation, connect to $V_{CC} = 0\text{V}$ . For PECL/ LVPECL operation, connect to either 3.3V or 5.0V. Bypass with $0.1\mu\text{F} // 0.01\mu\text{F}$ low ESR capacitors.

## Ordering Information<sup>(1)</sup>



**10-Pin MSOP (K10-1)**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100EL16VOKC	K10-1	Commercial	X16VO	Sn-Pb
SY100EL16VOKCTR <sup>(2)</sup>	K10-1	Commercial	X16VO	Sn-Pb
SY100EL16VOKI	K10-1	Industrial	X16VO	Sn-Pb
SY100EL16VOKITR <sup>(2)</sup>	K10-1	Industrial	X16VO	Sn-Pb
SY100EL16VOKG <sup>(3)</sup>	K10-1	Industiral	X16VO with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EL16VOKGTR <sup>(2, 3)</sup>	K10-1	Industrial	X16VO with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EL16VOKG <sup>(3)</sup>	K10-1	Industiral	X16VO with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY100EL16VOKGTR <sup>(2, 3)</sup>	K10-1	Industrial	X16VO with Pb-Free bar-line indicator	NiPdAu Pb-Free

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Symbol	Rating	Value	Unit
$V_{CC} - V_{EE}$	Power Supply Voltage	+6.0	V
$V_{IN}$	PECL Input Voltage	0 to $V_{CC} + 0.5$	V
$V_{OUT}$	Voltage Applied to Output at High State ( $V_{EE} = 0V$ )	-0.5 to +5.5	V
$I_{OUT}$	Output Current -Continuous -Surge	50 100	mA
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{store}$	Storage Temperature Range	-65 to +150	°C
$\theta_{JA}$	Package Thermal Resistance (Junction-to-Ambient) -Still-Air -500lfpm	113 96	°C/W
$\theta_{JC}$	Package Thermal Resistance (Junction-to-Case)	42	°C/W

**Note:**

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Symbol	Parameter	$T_A = -40^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$V_{CC}$	Power Supply Voltage (PECL) (LVPECL)	4.5 3.0	5.0 3.3	5.5 3.8	4.5 3.0	5.0 3.3	5.5 3.8	4.5 3.0	5.0 3.3	5.5 3.8	V	$V_{EE} = \text{GND}$
	(ECL) (LVECL)	-5.5 -3.8	-5.0 -3.3	-4.5 -3.0	-5.5 -3.8	-5.0 -3.3	-4.5 -3.0	-5.5 -3.8	-5.0 -3.3	-4.5 -3.0	V	$V_{CC} = \text{GND}$
$I_{CC}$	Power Supply Current	—	—	46	—	—	46	—	—	46	mA	$V_{CC} = 5.5\text{V}$
$V_{BB}$	Reference Voltage	$V_{CC}-1.26$	$V_{CC}-1.32$	$V_{CC}-1.38$	$V_{CC}-1.26$	$V_{CC}-1.32$	$V_{CC}-1.38$	$V_{CC}-1.26$	$V_{CC}-1.32$	$V_{CC}-1.38$	V	
$I_{IH}$	Input HIGH Current	—	—	150	—	—	150	—	—	150	$\mu\text{A}$	$V_{IN} = V_{IH}(\text{Max})$
$I_{IL}$	Input LOW Current	0.5	—	—	0.5	—	—	0.5	—	—	$\mu\text{A}$	$V_{IN} = V_{IL}(\text{Min})$
$C_{IN}$	Input Capacitance	—	—	—	—	0.75	—	—	—	—	pF	



$V_{CC} = 3.0$  to  $5.5V$ ;  $V_{EE} = GND$ ;  $V_{EE} = -3.0$  to  $-5.5V$ ;  $V_{CC} = GND$

Symbol	Parameter	$T_A = -40^\circ C$			$T_A = +25^\circ C$			$T_A = +85^\circ C$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$f_{MAX}$	Maximum Frequency	800	—	—	800	—	—	800	—	—	MHz	
$t_{PD}$	Propagation Delay to $Q_{FB}$ , $/Q_{FB}$ (Diff.) (Single)	—	—	200	—	—	200	—	—	200	ps	
	to $Q_{HG}$ , $/Q_{HG}$ (Diff.) (Single)	—	—	230	—	—	230	—	—	230	ps	
$t_S$	Set-Up Time <sup>(1)</sup>	150	—	—	150	—	—	150	—	—	ps	Enable Pin
$t_H$	Hold Time <sup>(1)</sup>	150	—	—	150	—	—	150	—	—	ps	Enable Pin
$t_{JITTER}$	Cycle-to-Cycle Jitter	—	0.2	—	—	0.2	—	—	0.2	—	ps	RMS
$t_{SKEW}$	Duty Cycle Skew <sup>(2)</sup>	—	5	20	—	5	20	—	5	20	ps	
$V_{PP}$	Minimum Input Swing <sup>(3)</sup>	150	—	—	150	—	—	150	—	—	mV	
$t_r$ $t_f$	Output Rise/Fall Times (20% to 80%)	—	—	250	—	—	250	—	—	250	ps	

#### Notes:

1. See "Timing Waveform."
2. Duty cycle skew is the difference between  $t_{PLH}$  and  $t_{PHL}$  propagation delay through the device.
3. The device has a DC gain of 10 for  $Q$ ,  $/Q$  outputs, and DC gain of 200 or higher for  $Q_{HG}$ ,  $/Q_{HG}$ . See "Timing Waveform" minimum input swing.

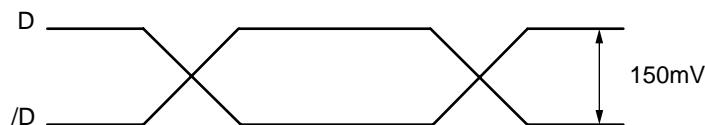


Figure 1. Minimum Input Swing

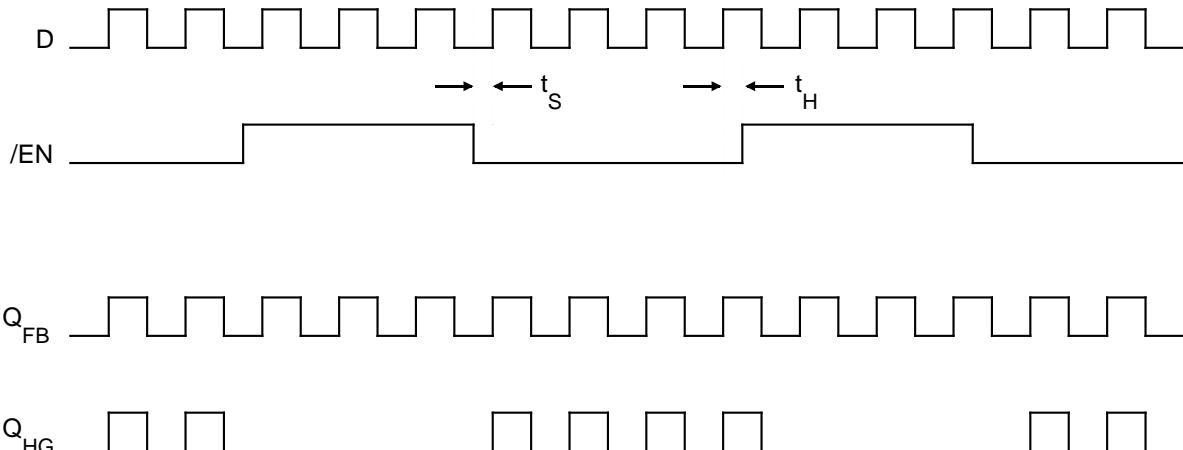


Figure 2. Set-Up and Hold Timing

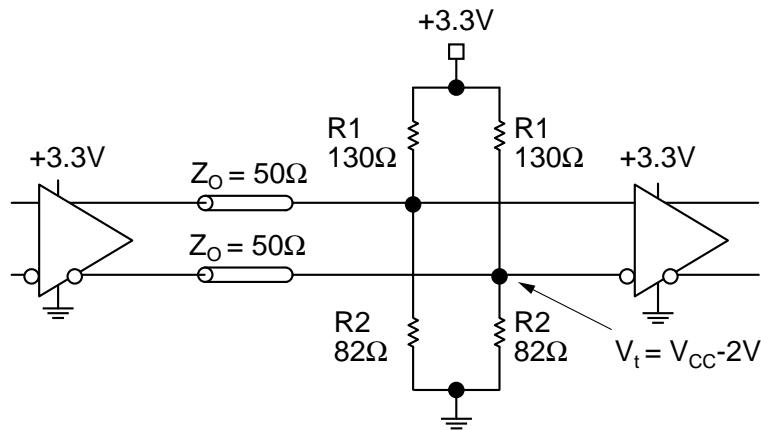


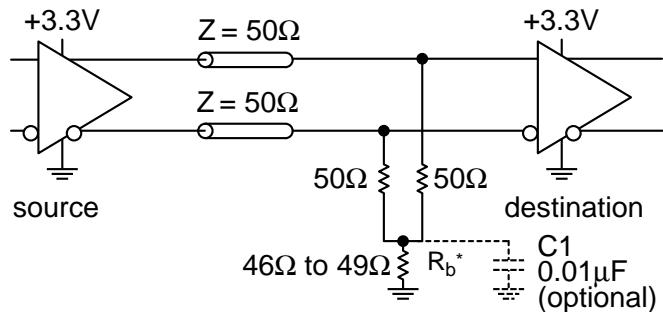
Figure 3. Parallel Termination-Thevenin Equivalent

**Notes:**

1. For +5V systems:

$$R1 = 82\Omega$$

$$R2 = 130\Omega$$

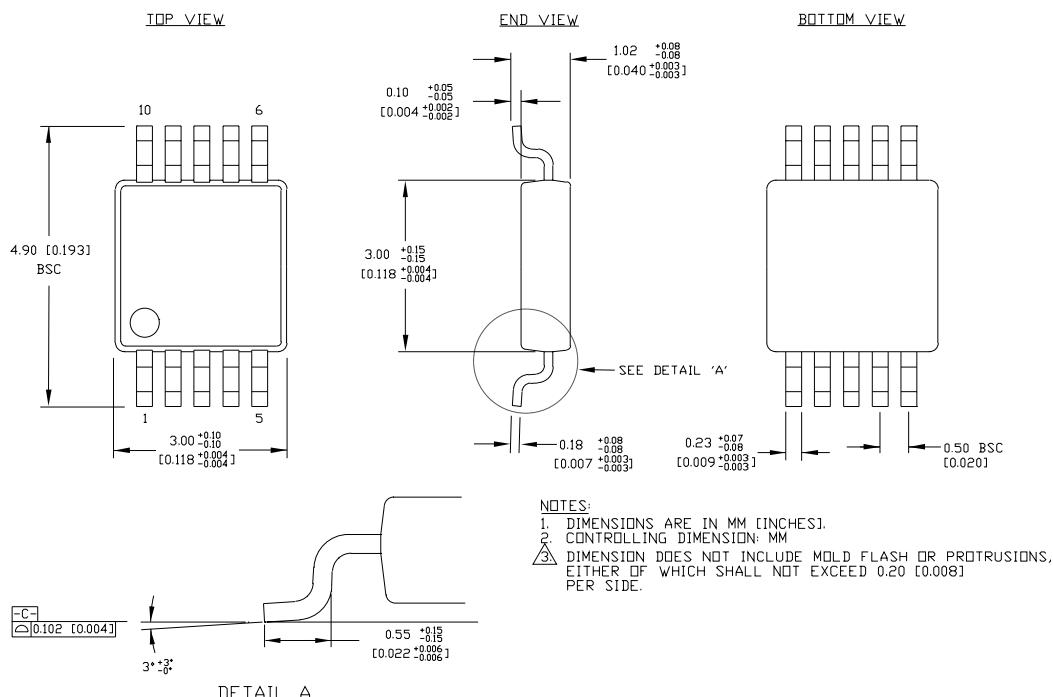


\* For +5V,  $R_b = 110\Omega$   
 For +3.3V,  $R_b = 46\Omega$  to  $49\Omega$

Figure 4. Three-Resistor "Y-Termination"

**Notes:**

1. Power-saving alternative to 4-resistor, Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3.  $R_b$  resistor sets the DC bias voltage, equal to  $V_t$ . For +5V,  $R_b = 100\Omega$



Rev. 00

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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