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Structure	Silicon Monolithic Bipolar IC
Appearance	SIL-12 Pin Plastic Package (Power Type with Fin attached)
Application	Hi-Fi and Car Stereo
Function	BTL 23W Audio Power Amplifier

A	Absolute Maximum Ratings				
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	° C	1
2	Operating Ambient Temperature	Topr	-30 ~ +75	° C	1
3	Supply Voltage	Vcc	26	V	
4	Supply Current	Icc	4.0	A	
5	Power Dissipation	P_D	62.5	W	
6	Surge Voltage	V_{surge}	50	V	

Note: 1) The temperature of all items shall be Ta=25°C except storage temperature and operating ambient temperature.

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B Electrical Characteristics (Unless otherwise specified, the ambient temperature is 25°C ± 2°C)

No	Item	Symbol	Test Circuit	Conditions	Limits min	Limits typ	Limits max	Unit	Note
1	Quiescent Circuit Current	I_{CQ}	1	V_{CC}=15V, V_{in}=0V	-	45	75	mA	
	Power Amplifier (V_{CC}=15V, R_L=4Ω, freq.=1kHz)								
2	Output Noise Voltage	V_N	1	f=15Hz ~ 30kHz, 12dB/oct, R_g=10kΩ	-	0.6	1.0	mV	
3	Voltage Gain	G_V	1	V_{in}=5mV	48.5	50.5	52.5	dB	
4	Total Harmonic Distortion	THD	1	V_{in}=5mV	-	0.15	0.5	%	
5	Maximum Power Output	P_O	1	THD=10%	20	23	-	W	
6	Output Offset Voltage	V_{OS}	1	R_g=0Ω	-	-	150	mV	
	Headphone Amplifier (V_{CC}=15V, R_L=33Ω, freq.=1kHz)								
7	Output Noise Voltage	V_{N-H}	1	f=15Hz ~ 30kHz, 12dB/oct, R_g=10kΩ	-	0.1	0.7	mV	
8	Voltage Gain	G_{V-H}	1	V_{in}=10mV Power Amplifier mute	17.5	19.5	21.5	dB	
9	Maximum Output Power	P_{O-H}	1	THD=1% Power Amplifier mute	10	-	-	mW	

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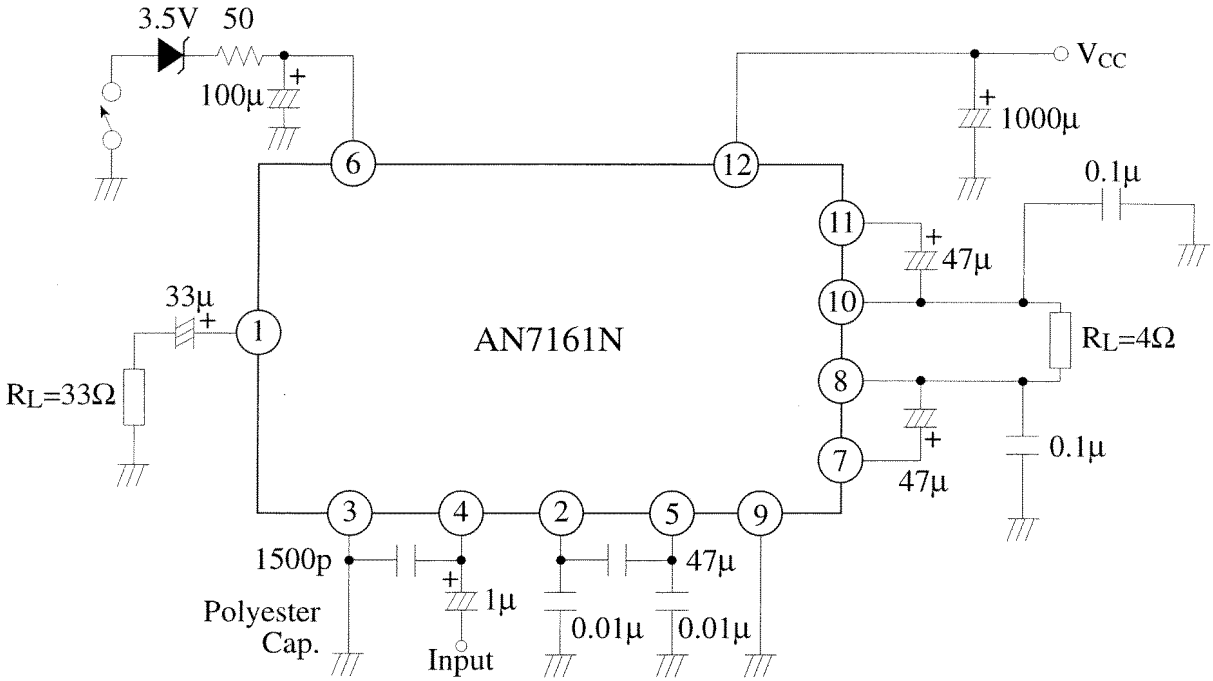
(Description of test circuit and test method)

Test Circuit 1



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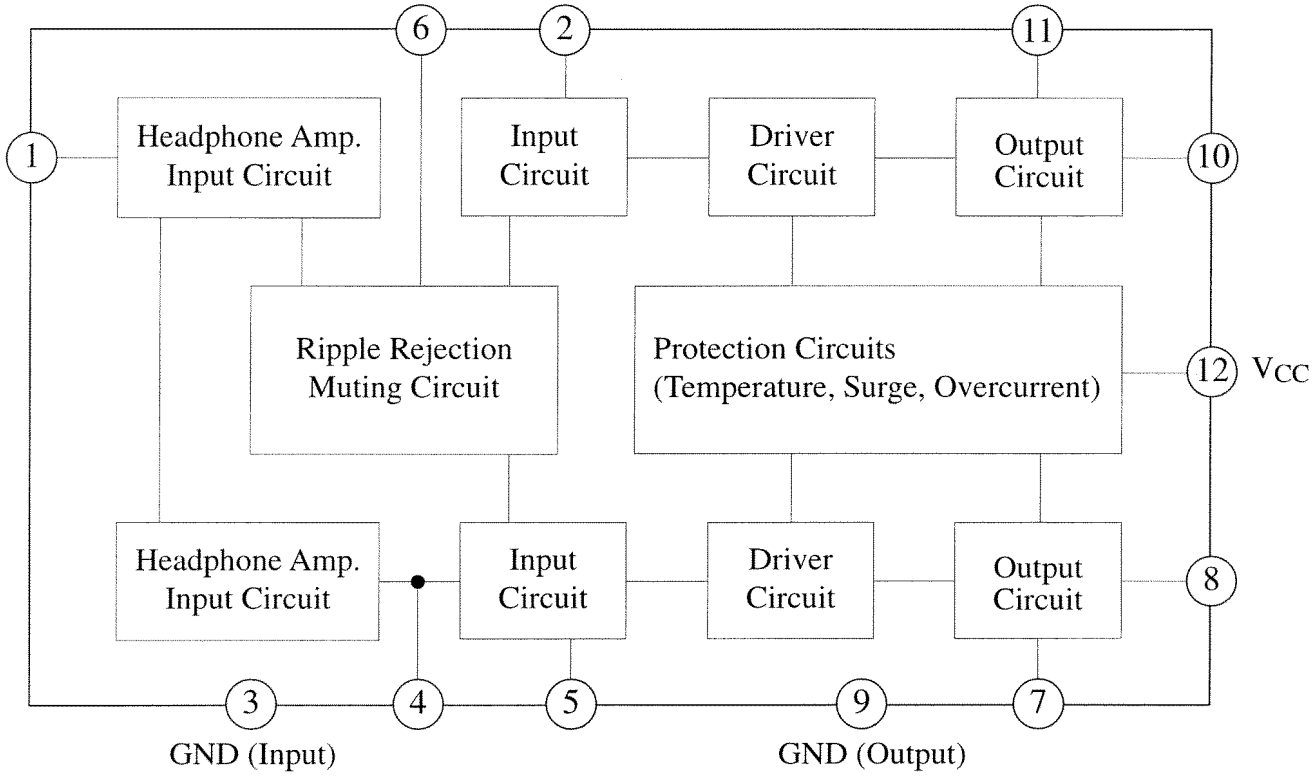
Circuit Function Block Diagram



Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Output (Headphone)	7	Bootstrap Channel 1
2	Negative Feedback Channel 2	8	Output Channel 1
3	GND (Input)	9	GND (Output)
4	Input	10	Output Channel 2
5	Negative Feedback Channel 1	11	Bootstrap Channel 2
6	Ripple Filter	12	V_{CC}

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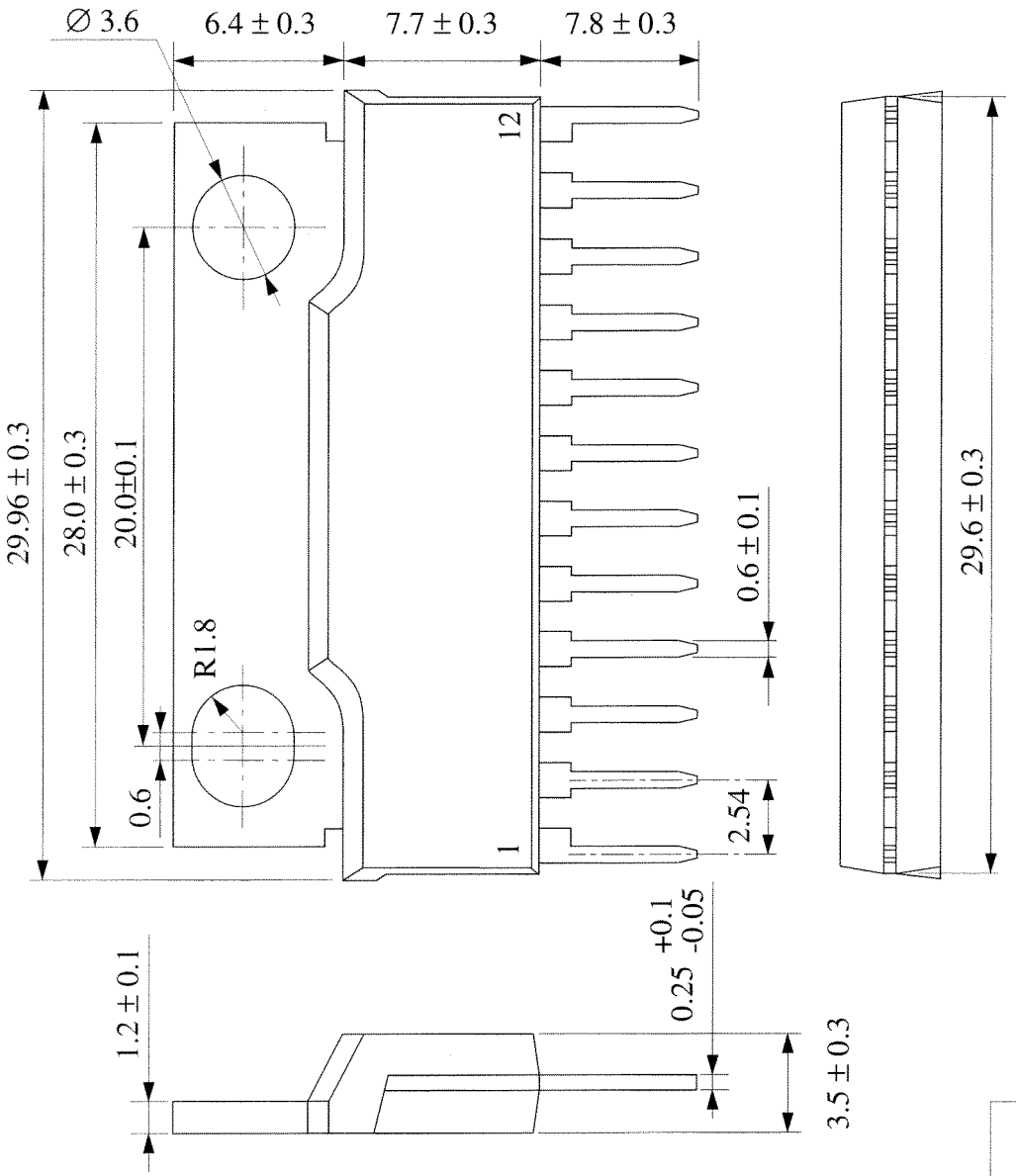
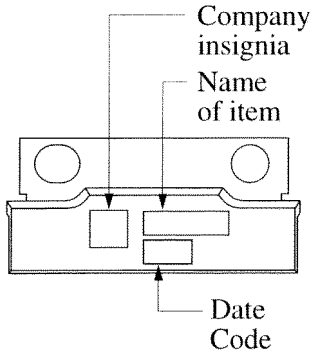
Package Name	FP-12S

Unit : mm





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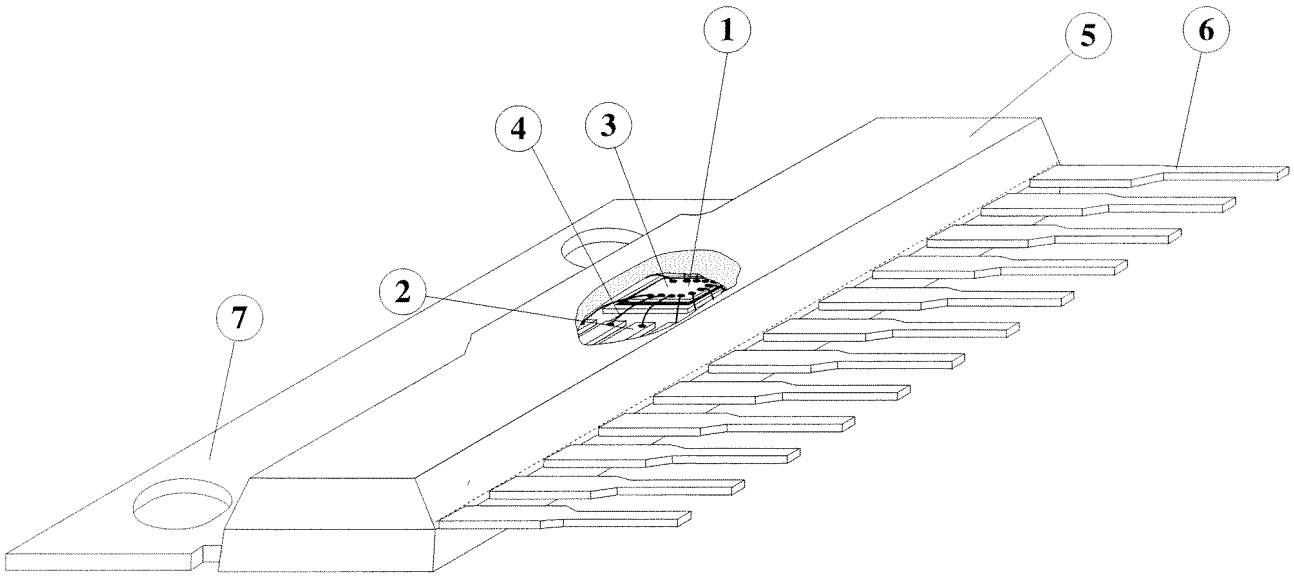
(Structure Description)

Chip surface passivation	SiN, [PSG,] Others ( )	1
Lead frame material	Fe group, [Cu group,] Others ( )	2, 6
Inner lead surface process	[Ag plating,] Au plating, Others ( )	2
Outer lead surface process	Solder plating, [Solder dip,] Others ( )	6
Chip mounting method	Ag paste, Au-Si alloy, [Solder,] Others ( )	3
Wire bonding method	[Thermalsonic bonding,] Others ( )	4
Wire material, Diameter	[Au,] Diameter 50 µm Others ( )	4
Mold material	[Epoxy,] Others ( )	5
Molding method	[Transfer mold,] Multiplunger mold, Others ( )	5
Fin material	[Cu Group] Others ( )	7

Package FP-12S



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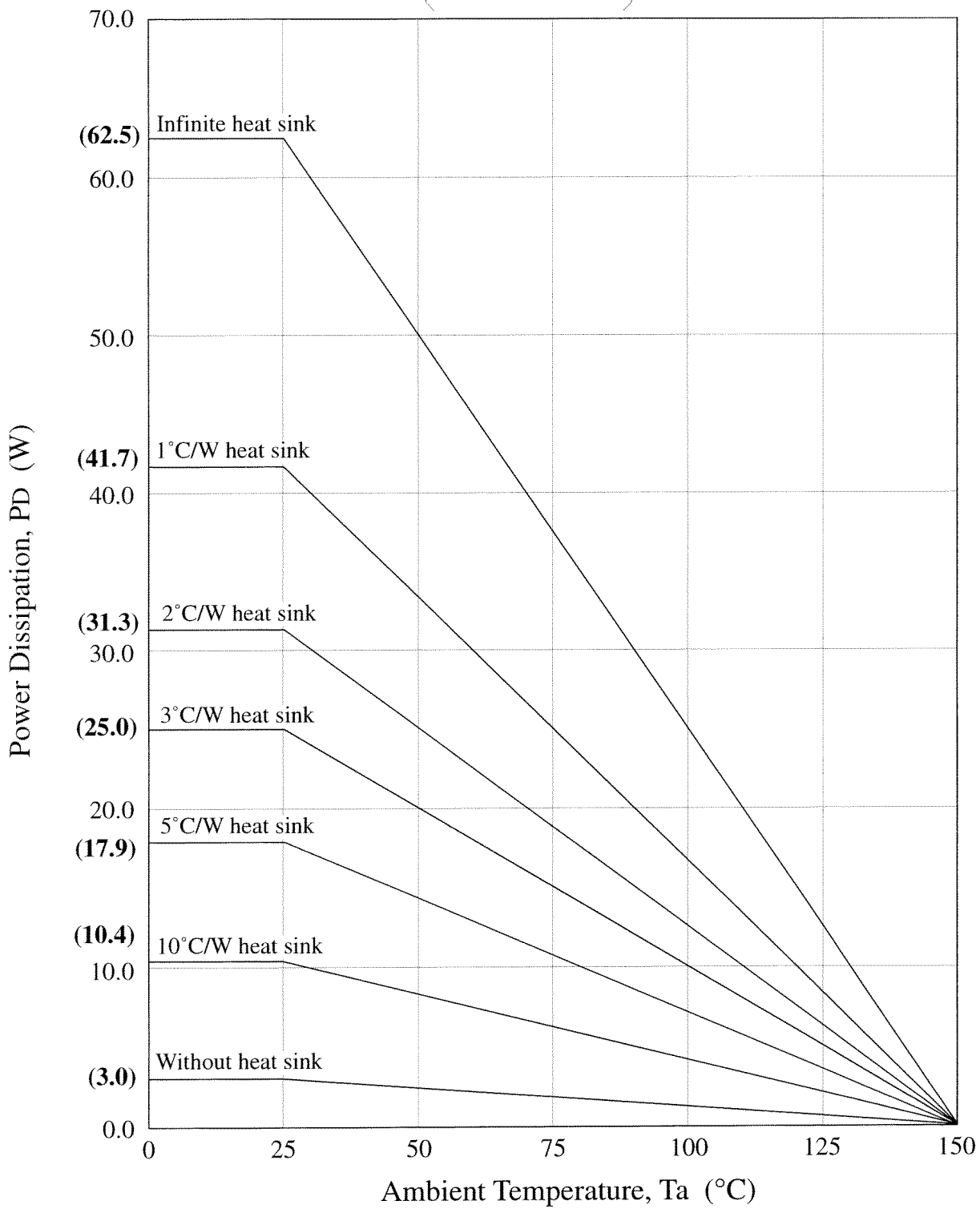
FP-12S Package Power Dissipation

P_D - Ta

$R_{th(j-c)}$ = 2°C/W
$R_{th(j-a)}$ = 42°C/W



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