1.35V DDR3L SDRAM UDIMM

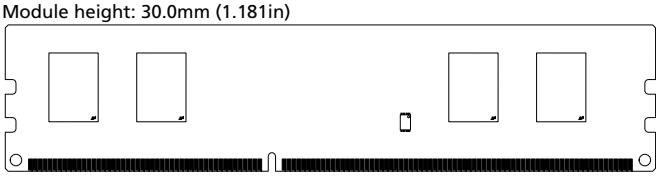
MT4KTF25664AZ – 2GB

Features

- DDR3L functionality and operations supported as defined in the component data sheet
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC3-14900 or PC3-12800
- 2GB (256 Meg x 64)
- $V_{DD} = V_{DDQ}$ = 1.35V (1.238–1.45V)
- $V_{DD} = V_{DDQ}$ = 1.5V (1.425–1.575V)
- Backward-compatible to $V_{DD} = V_{DDQ}$ = 1.5V ±0.075V
- V_{DDSPD} = 3.0–3.6V
- Reset pin for improved system stability
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single-rank
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Adjustable data-output drive strength
- Serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 240-Pin UDIMM (R/C C1)

Module height: 30.0mm (1.181in)



Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
• Package	
– 240-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 1.07ns @ CL = 13 (DDR3-1866)	-1G9
– 1.25ns @ CL = 11 (DDR3-1600)	-1G6

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)								^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 13	CL = 11	CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G9	PC3-14900	1866	1600	1333	1333	1066	1066	800	667	13.125	13.125	47.125
-1G6	PC3-12800	–	1600	1333	1333	1066	1066	800	667	13.125	13.125	48.125
-1G4	PC3-10600	–	–	1333	1333	1066	1066	800	667	13.125	13.125	49.125
-1G1	PC3-8500	–	–	–	–	1066	1066	800	667	13.125	13.125	50.625
-1G0	PC3-8500	–	–	–	–	1066	–	800	667	15	15	52.5
-80B	PC3-6400	–	–	–	–	–	–	800	667	15	15	52.5

Table 2: Addressing

Parameter	2GB
Refresh count	8K
Row address	32K A[14:0]
Device bank address	8 BA[2:0]
Device configuration	4Gb (256 Meg x 16)
Column address	1K A[9:0]
Module rank address	1 S0#

Table 3: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT41K256M16,[1] 4Gb 1.35V DDR3L SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT4KTF25664AZ-1G9__	2GB	256 Meg x 64	14.9 GB/s	1.07ns/1866 MT/s	13-13-13
MT4KTF25664AZ-1G6__	2GB	256 Meg x 64	12.8 GB/s	1.25ns/1600 MT/s	11-11-11

Notes:
1. Data sheets for the base device parts can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT4KTF25664AZ-1G9P1.

Pin Assignments

Table 4: Pin Assignments

240-Pin DDR3 UDIMM Front								240-Pin DDR3 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}	122	DQ4	152	DM3	182	V_{DD}	212	DM5
3	DQ0	33	DQS3#	63	CK1	93	DQS5#	123	DQ5	153	NC	183	V_{DD}	213	NC
4	DQ1	34	DQS3	64	CK1#	94	DQS5	124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}	125	DM0	155	DQ30	185	CK0#	215	DQ46
6	DQS0#	36	DQ26	66	V_{DD}	96	DQ42	126	NC	156	DQ31	186	V_{DD}	216	DQ47
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43	127	V_{SS}	157	V_{SS}	187	NC	217	V_{SS}
8	V_{SS}	38	V_{SS}	68	NC	98	V_{SS}	128	DQ6	158	NF	188	A0	218	DQ52
9	DQ2	39	NF	69	V_{DD}	99	DQ48	129	DQ7	159	NF	189	V_{DD}	219	DQ53
10	DQ3	40	NF	70	A10	100	DQ49	130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}	131	DQ12	161	NF	191	V_{DD}	221	DM6
12	DQ8	42	NF	72	V_{DD}	102	DQS6#	132	DQ13	162	NF	192	RAS#	222	NC
13	DQ9	43	NF	73	WE#	103	DQS6	133	V_{SS}	163	V_{SS}	193	S0#	223	V_{SS}
14	V_{SS}	44	V_{SS}	74	CAS#	104	V_{SS}	134	DM1	164	NF	194	V_{DD}	224	DQ54
15	DQS1#	45	NF	75	V_{DD}	105	DQ50	135	NC	165	NF	195	ODT0	225	DQ55
16	DQS1	46	NF	76	NF	106	DQ51	136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
17	V_{SS}	47	V_{SS}	77	NF	107	V_{SS}	137	DQ14	167	NC	197	V_{DD}	227	DQ60
18	DQ10	48	NC	78	V_{DD}	108	DQ56	138	DQ15	168	RESET#	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQ57	139	V_{SS}	169	NF	199	V_{SS}	229	V_{SS}
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}	140	DQ20	170	V_{DD}	200	DQ36	230	DM7
21	DQ16	51	V_{DD}	81	DQ32	111	DQS7#	141	DQ21	171	NF	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V_{SS}	172	A14	202	V_{SS}	232	V_{SS}
23	V_{SS}	53	NC	83	V_{SS}	113	V_{SS}	143	DM2	173	V_{DD}	203	DM4	233	DQ62
24	DQS2#	54	V_{DD}	84	DQS4#	114	DQ58	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}	146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V_{SS}	178	A6	208	V_{SS}	238	SDA
29	V_{SS}	59	A4	89	V_{SS}	119	SA2	149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}	150	DQ29	180	A3	210	DQ45	240	V_{TT}

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command.
CKx, CKx#	Input	**Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx, DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I^2C bus.
TDQSx, TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V. The component V_{DD} and V_{DDQ} are connected to the module V_{DD}.
V_{DDSPD}	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address $V_{DD}/2$.
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address $V_{DD}/2$.
NC	–	**No connect:** These pins are not connected on the module.
NF	–	**No function:** These pins are connected within the module, but provide no functionality.

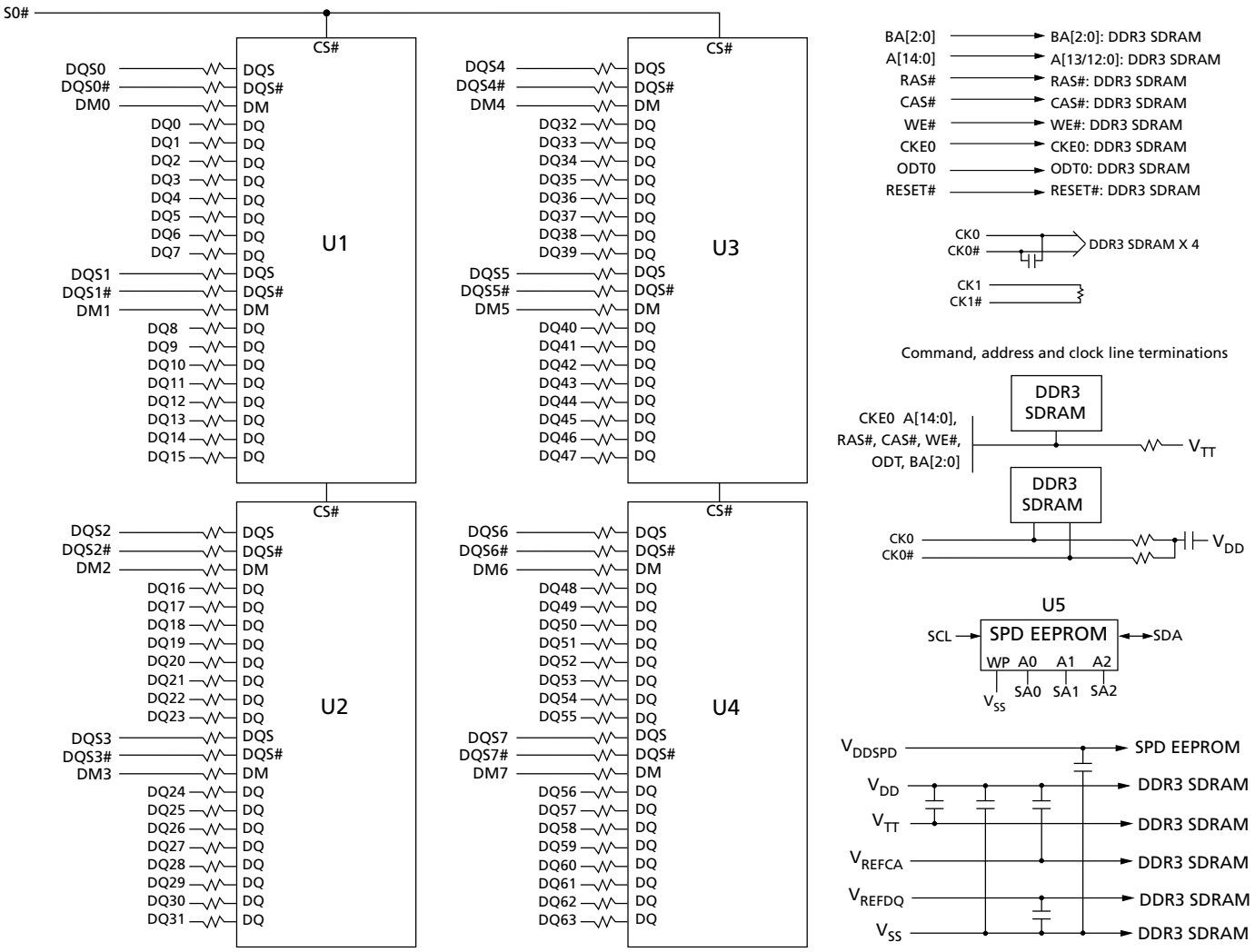
DQ Map

Table 6: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	2	9	U2	0	18	27
	1	1	4		1	17	22
	2	3	10		2	19	28
	3	5	123		3	21	141
	4	6	128		4	22	146
	5	4	122		5	20	140
	6	7	129		6	23	147
	7	0	3		7	16	21
	8	8	12		8	24	30
	9	15	138		9	31	156
	10	9	13		10	25	31
	11	11	19		11	27	37
	12	12	131		12	28	149
	13	14	137		13	30	155
	14	13	132		14	29	150
	15	10	18		15	26	36
U3	0	34	87	U4	0	50	105
	1	33	82		1	49	100
	2	35	88		2	51	106
	3	37	201		3	53	219
	4	38	206		4	54	224
	5	36	200		5	52	218
	6	39	207		6	55	225
	7	32	81		7	48	99
	8	40	90		8	56	108
	9	47	216		9	63	234
	10	41	91		10	57	109
	11	43	97		11	59	115
	12	44	209		12	60	227
	13	46	215		13	62	233
	14	45	210		14	61	228
	15	42	96		15	58	114

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V

Table 8: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.283	1.35	1.45	V	
			1.425	1.5	1.575	V	1
I_{VTT}	Termination reference current from V_{TT}		–600	–	600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	2
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, S#, CKE, ODT, CK, CK#	–8	0	8	µA	
		DM	–2	0	2		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–5	0	5	µA	
I_{VREF}	V_{REF} supply leakage current; V_{REFDQ} = V_{DD}/2 or V_{REFCA} = V_{DD}/2 (All other pins not under test = 0V.)		–4	0	4	µA	
T_A	Module ambient operating temperature	Commercial	0	–	70	°C	3, 4
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	95	°C	3, 4, 5

Notes:
1. Module is backward-compatible with 1.5V operation. Refer to device specification for details and operation guidance.
2. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
3. T_A and T_C are simultaneous requirements.
4. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
5. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available at micron.com. Module speed grades correlate with component speed grades, as shown below.

Table 9: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-2G1	-093
-1G9	-107
-1G6	-125
-1G4	-15E
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 10: DDR3 I_{DD} Specifications and Conditions – 2GB (Die Revision P)

Values are for the MT41K256M16 DDR3L SDRAM only and are computed from values specified in the 1.35V 4Gb (256 Meg x 16) component data sheet

Parameter	Symbol	1866	1600	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}	128	128	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	184	180	mA
Precharge power-down current: Slow exit	I_{DD2P0}	48	48	mA
Precharge power-down current: Fast exit	I_{DD2P1}	48	48	mA
Precharge quiet standby current	I_{DD2Q}	60	60	mA
Precharge standby current	I_{DD2N}	68	68	mA
Precharge standby ODT current	I_{DD2NT}	92	92	mA
Active power-down current	I_{DD3P}	68	68	mA
Active standby current	I_{DD3N}	92	88	mA
Burst read operating current	I_{DD4R}	416	368	mA
Burst write operating current	I_{DD4W}	468	424	mA
Refresh current	I_{DD5B}	624	624	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	60	60	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	92	92	mA
All banks interleaved read current	I_{DD7}	588	528	mA
Reset current	I_{DD8}	56	56	mA

Serial Presence-Detect EEPROM

For the latest SPD data, refer to Micron's SPD page: micron.com/spd.

Table 11: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{DDSPD}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.45	V_{DDSPD} x 0.3	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 1.0	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	–	±2.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	–	±2.0	µA

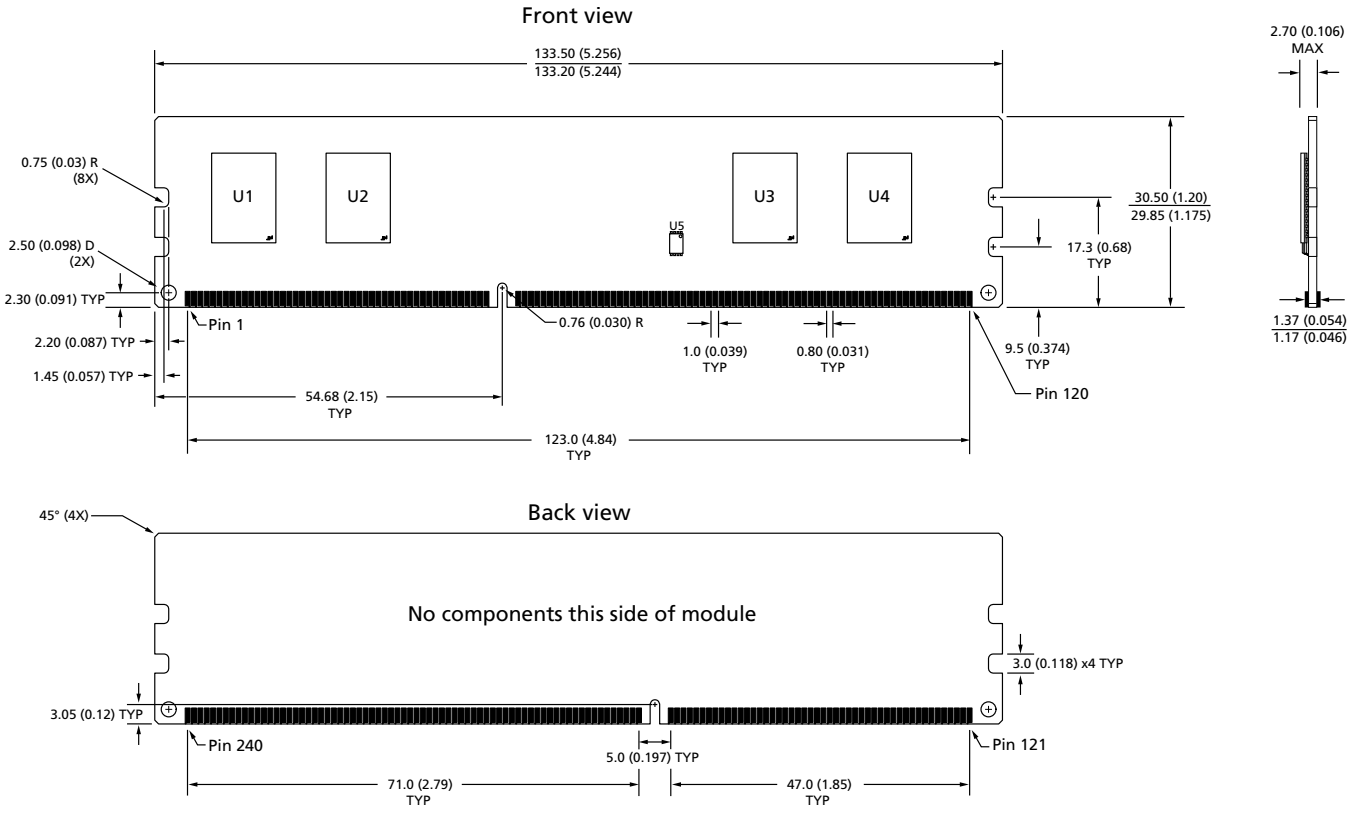
Table 12: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	^{f}SCL	10	400	kHz	
Clock pulse width HIGH time	^{t}HIGH	0.6	–	µs	
Clock pulse width LOW time	^{t}LOW	1.3	–	µs	
SDA rise time	^{t}R	20	300	µs	1
SDA fall time	^{t}F	20	300	ns	1
Data-in setup time	^{t}SU:DAT	100	–	ns	
Data-in hold time	^{t}HD:DI	0	–	µs	
Data-out hold time	^{t}HD:DAT	200	900	ns	
Data out access time from SCL LOW	^{t}AA:DAT	0.2	0.9	µs	2
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Start condition hold time	^{t}HD:STA	0.6	–	µs	
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
WRITE time	^{t}W	–	10	ms	

Notes:
1. Guaranteed by design and characterization, not necessarily tested.
2. To avoid spurious start and stop conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.
3. For a restart condition, or following a WRITE cycle.

Module Dimensions

Figure 3: 240-Pin DDR3 UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.
3. Tolerance on all dimensions ±0.15mm unless otherwise specified.

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