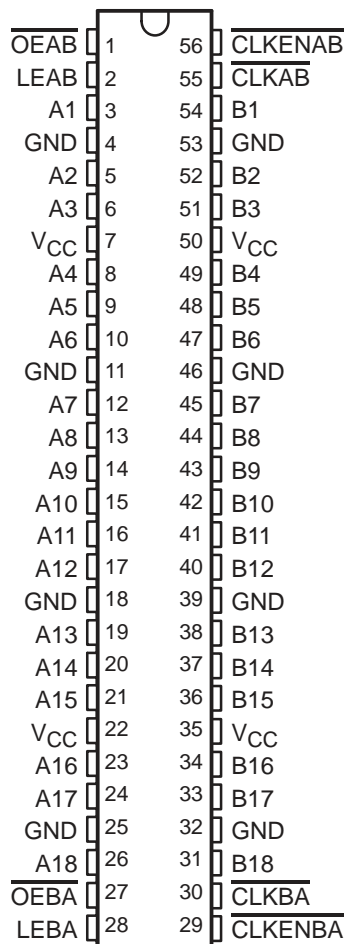- **Members of the Texas Instruments *Widebus*™ Family**

- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**

- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**

- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**

- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**

- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16600 . . . WD PACKAGE
SN74ABT16600 . . . DGG OR DL PACKAGE
(TOP VIEW)

$\overline{\text{OEAB}}$	1		56	$\overline{\text{CLKENAB}}$
LEAB	2		55	$\overline{\text{CLKAB}}$
A1	3		54	B1
GND	4		53	GND
A2	5		52	B2
A3	6		51	B3
V_{CC}	7		50	V_{CC}
A4	8		49	B4
A5	9		48	B5
A6	10		47	B6
GND	11		46	GND
A7	12		45	B7
A8	13		44	B8
A9	14		43	B9
A10	15		42	B10
A11	16		41	B11
A12	17		40	B12
GND	18		39	GND
A13	19		38	B13
A14	20		37	B14
A15	21		36	B15
V_{CC}	22		35	V_{CC}
A16	23		34	B16
A17	24		33	B17
GND	25		32	GND
A18	26		31	B18
$\overline{\text{OEBA}}$	27		30	$\overline{\text{CLKBA}}$
LEBA	28		29	$\overline{\text{CLKENBA}}$

description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes.

Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. The clock can be controlled by the clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CLKAB}}$. Output enable $\overline{\text{OEAB}}$ is active low. When $\overline{\text{OEAB}}$ is low, the outputs are active. When $\overline{\text{OEAB}}$ is high, the outputs are in the high-impedance state.

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description (continued)

Data flow for B to A is similar to that of A to B, but uses $\overline{\text{OEBA}}$, LEBA, $\overline{\text{CLKBA}}$, and $\overline{\text{CLKENBA}}$.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16600 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16600 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE[†]

INPUTS					OUTPUT
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	$\overline{\text{CLKAB}}$	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0[‡]
H	L	L	X	X	B_0[‡]
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B_0[‡]
L	L	L	L	X	B_0[§]

[†] A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, $\overline{\text{CLKBA}}$, and $\overline{\text{CLKENBA}}$.
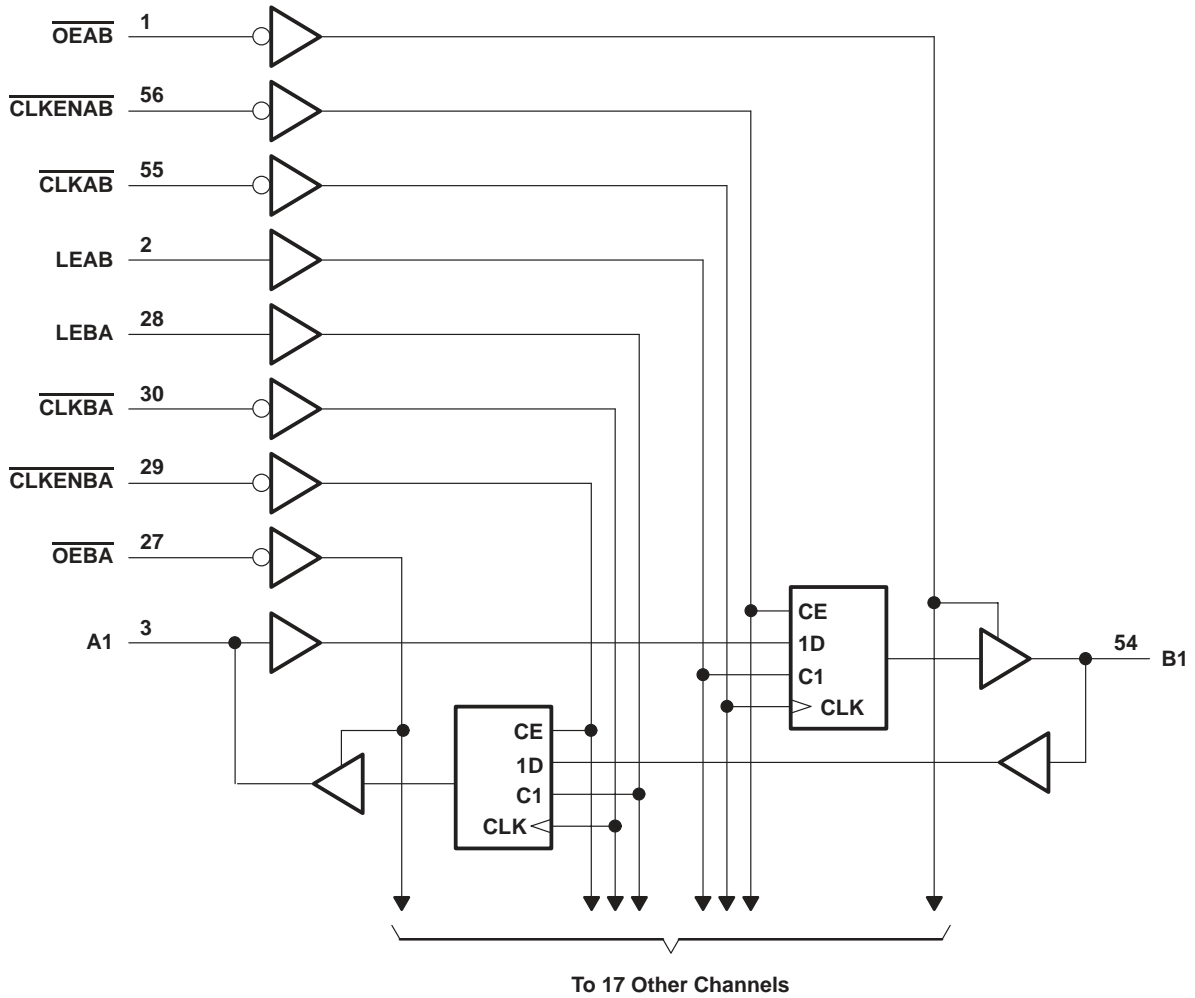
[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was low before LEAB went low

logic diagram (positive logic)

To 17 Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) .... –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O .... –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT16600 .... 96 mA
　　　　　　　　　　　　　　　　　　　　　　　　SN74ABT16600 .... 128 mA
Input clamp current, I_{IK} (V_I < 0) .... –18 mA
Output clamp current, I_{OK} (V_O < 0) .... –50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 81°C/W
　　　　　　　　　　　　　　　　　　　　　　　　　　DL package .... 74°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
　　　　2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABT16600 MIN	SN54ABT16600 MAX	SN74ABT16600 MIN	SN74ABT16600 MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$ MIN	TYP†	MAX	SN54ABT16600 MIN	MAX	SN74ABT16600 MIN	MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -3$ mA	2.5			2.5		2.5		V
		$V_{CC} = 5$ V,	$I_{OH} = -3$ mA	3			3		3		
		$V_{CC} = 4.5$ V	$I_{OH} = -24$ mA	2			2				
			$I_{OH} = -32$ mA	2*					2		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA			0.55		0.55			V
			$I_{OL} = 64$ mA			0.55*				0.55	
V_{hys}					100						mV
I_I	Control inputs	$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND			±1		±1		±1	µA
	A or B ports					±20		±20		±20	
I_{off}		$V_{CC} = 0$,	V_I or $V_O \leq 4.5$ V			±100				±100	µA
I_{CEX}		$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O‡		$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−50	−100	−180	−50	−180	−50	−180	mA
I_{OZH}§		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			10		10		10	µA
I_{OZL}§		$V_{CC} = 5.5$ V,	$V_O = 0.5$ V			−10		−10		−10	µA
I_{CC}	A or B ports	$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			3		3		3	mA
			Outputs low			36		36		36	
			Outputs disabled			3		3		3	
ΔI_{CC}¶		$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				50		50		50	µA
C_i	Control inputs	$V_I = 2.5$ V or 0.5 V			3						pF
C_{io}	A or B ports	$V_O = 2.5$ V or 0.5 V			9						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT16600		SN74ABT16600		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	150	0	150	MHz
t_w	Pulse duration	LEAB or LEBA high	2.5		2.5		ns
		$\overline{CLKAB}$ or $\overline{CLKBA}$ high or low	3		3		
t_{su}	Setup time	A before $\overline{CLKAB}\downarrow$ or B before $\overline{CLKBA}\downarrow$	3		3		ns
		A before LEAB$\downarrow$ or B before LEBA$\downarrow$	2.5		2.5		
		$\overline{CLKEN}$ before CLK$\downarrow$	2.5		2.5		
t_h	Hold time	A after $\overline{CLKAB}\downarrow$ or B after $\overline{CLKBA}\downarrow$	0		0		ns
		A after LEAB$\downarrow$ or B after LEBA$\downarrow$	2		2		
		$\overline{CLKEN}$ after CLK$\downarrow$	1		1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT16600		SN74ABT16600		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			150			150		150		MHz
t_{PLH}	A or B	B or A	1.5	2.5	3.6	1.5	4.2	1.5	4	ns
t_{PHL}			1.5	3.2	4.5	1.5	5.1	1.5	4.9	
t_{PLH}	LEAB or LEBA	B or A	2	3.2	4.5	2	5.6	2	5	ns
t_{PHL}			2	3.4	4.5	2	5.4	2	5	
t_{PLH}	$\overline{CLKAB}$ or $\overline{CLKBA}$	B or A	2	3.5	4.7	2	5.4	2	5.3	ns
t_{PHL}			2	3.5	4.3	2	5.2	2	5	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	1.5	3.4	4.6	1.5	5.3	1.5	5.1	ns
t_{PZL}			2	3.8	4.7	2	5.6	2	5.4	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.5	5.4	2	6.6	2	6.2	ns
t_{PLZ}			1.5	3.4	4.7	1.5	5.8	1.5	5.4	

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PARAMETER MEASUREMENT INFORMATION
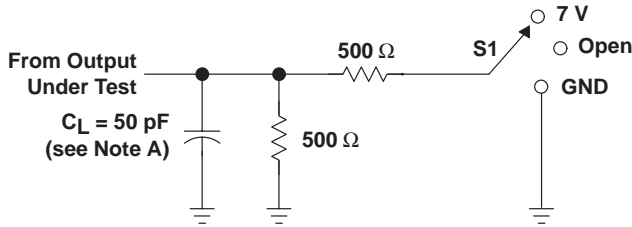
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
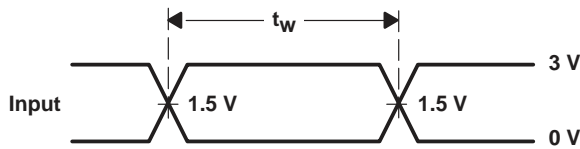
**VOLTAGE WAVEFORMS
PULSE DURATION**
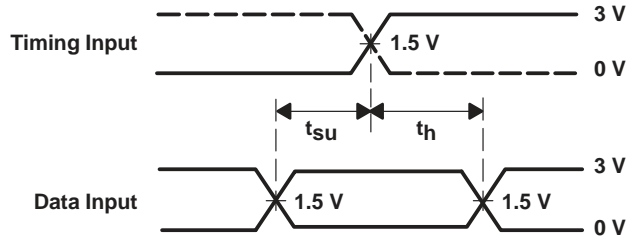
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
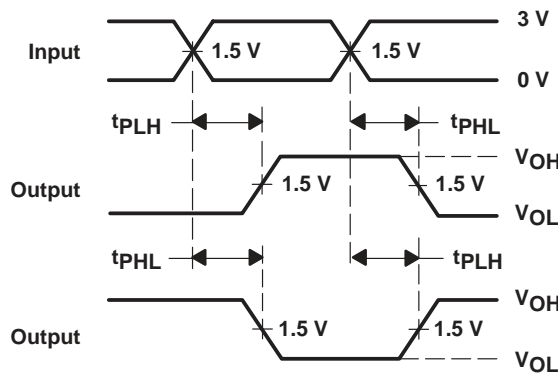
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**
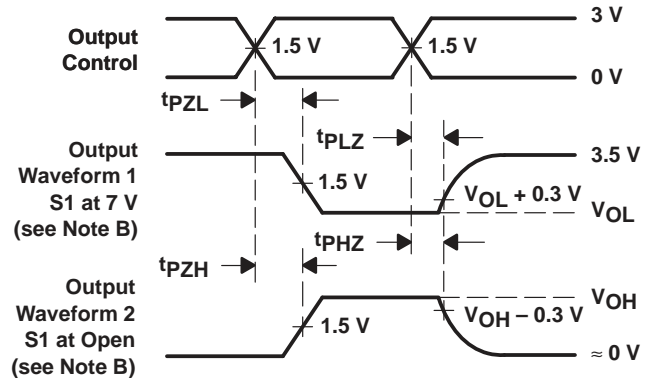
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω, $t_r \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT16600DL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		
SN74ABT16600DLG4	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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