MAX14955

Single-Lane PCIe Gen III Redriver with Equalization and Extended Temperature Operation

General Description

The MAX14955 dual equalizer/redriver improves PCI Express® (PCIe) signal integrity by providing programmable input equalization. This feature reduces deterministic jitter and redrives circuitry to reestablish deemphasis, which compensates for circuit-board loss at high frequencies. The device permits optimal placement of key PCIe components and allows for longer runs of stripline, microstrip, or cable.

The device contains two identical channels capable of equalizing PCIe Gen III (8GT/s), Gen II (5GT/s), and Gen I (2.5GT/s) signals and features electrical idle and receiver detection.

The MAX14955 is available in a small, 40-pin, 5.0mm x 5.0mm TQFN package with flow-through traces for optimal layout and minimal space requirements. The device is specified over the -40°C to +85°C extending operating temperature range.

Applications

- Industrial/Embedded PCs
- Computer on Modules
- Carrier Boards
- Test Equipment
- Rack Server Industrial PCs
- Medical Equipment

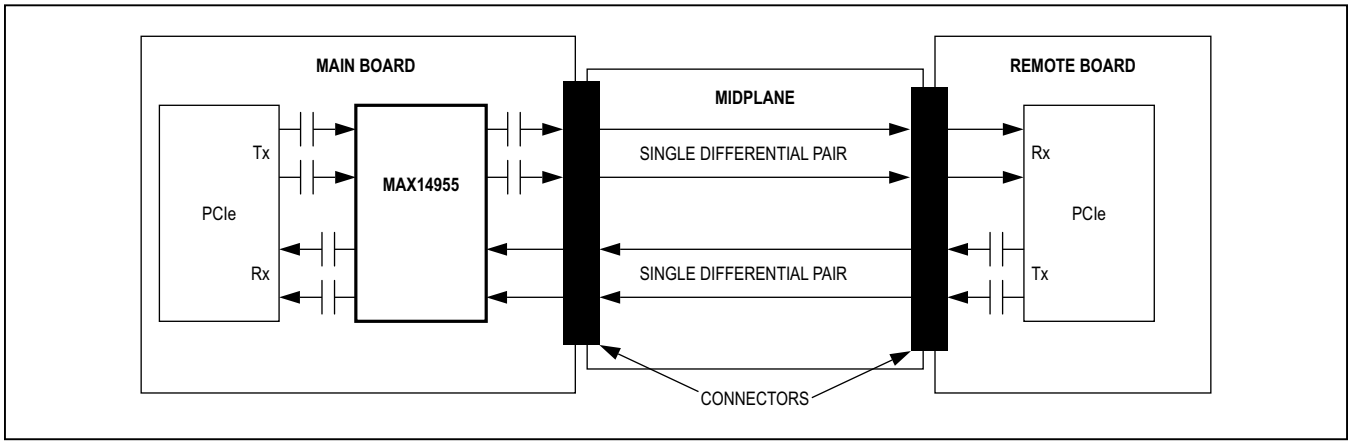
Benefits and Features

- Fully Integrated for Ease of Use and Design Flexibility
  - Optimized for PCIe Gen III (8.0GT/s), Gen II (5.0GT/s), Gen I (2.5 GT/s) Compatible
  - Four Levels of Input Equalization up to 16dB
  - Eight Levels of Output Deemphasis up to 9dB
- High Level of Performance to Overcome Noise in Lossy Channels
  - Random Jitter: 0.5ps$_{RMS}$ (typ)
  - Deterministic Jitter: 7ps$_{P-P}$ (typ)
  - Equalization Permits Placement Up to 30in FR4
- Robust Solution for Harsh Environments
  - Industrial Temperature Rated: -40°C to +85°C
  - ±4kV Human Body Model (HBM) Protection on All Pins
  - Housed in a Flow-Through (5mm x 5mm) TQFN Package for Resistance to Vibration/Shocks

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX14955.related**.*

Typical Operating Circuit



PCI Express is a registered service mark of PCI-SIG Corporation.

19-6640; Rev 0; 3/13

maxim integrated™

Absolute Maximum Ratings

(Voltages referenced to GND.)
V_{CC} ..... -0.3V to +4.0V
All Other Pins (Note 1) ..... -0.3V to (V_{CC} + 0.3V)
Continuous Current IN_P, IN_M, OUT_P, OUT_M ..... ±30mA
Peak Current IN_P, IN_M, OUT_P, OUT_M (pulsed for 1µs, 1% duty cycle) ..... ±100mA

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 35.7mW/°C above +70°C) 2857mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: All I/O pins are clamped by internal diodes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 2°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = +3.0V to +3.6V, C_{CL} = 200nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Power-Supply Range	V_{CC}			3.0	3.3	3.6	V
Supply Current	I_{CC}	EN = V_{CC}	OEQ_2 = OEQ_1 = OEQ_0 = GND		102	135	mA
			OEQ_2 = OEQ_1 = GND, OEQ_0 = V_{CC}		106	140	
			OEQ_2 = OEQ_0 = GND, OEQ_1 = V_{CC}		107	140	
			OEQ_2 = GND, OEQ_1 = OEQ_0 = V_{CC}		125	160	
			OEQ_2 = V_{CC}, OEQ_1 = OEQ_0 = GND		106	140	
			OEQ_2 = OEQ_0 = V_{CC}, OEQ_1 = GND		132	170	
			OEQ_2 = OEQ_1 = V_{CC}, OEQ_0 = GND		140	180	
			OEQ_2 = OEQ_1 = OEQ_0 = V_{CC}		165	210	

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 200nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Standby Current	I_{STBY}	EN = GND	OEQ_2 = OEQ_1 = OEQ_0 = GND		57	80	mA
			OEQ_2 = OEQ_1 = GND, OEQ_0 = V_{CC}		61	85	
			OEQ_2 = OEQ_0 = GND, OEQ_1 = V_{CC}		62	85	
			OEQ_2 = GND, OEQ_1 = OEQ_0 = V_{CC}		75	100	
			OEQ_2 = V_{CC}, OEQ_1 = OEQ_0 = GND		62	80	
			OEQ_2 = OEQ_0 = V_{CC}, OEQ_1 = GND		85	110	
			OEQ_2 = OEQ_1 = V_{CC}, OEQ_0 = GND		92	120	
			OEQ_2 = OEQ_1 = OEQ_0 = V_{CC}		120	150	
Differential Input Impedance	$Z_{RX-DIFF-DC}$	DC		80	100	120	Ω
Differential Output Impedance	$Z_{TX-DIFF-DC}$	DC		80	100	120	Ω
Common-Mode Resistance to GND, Input Termination Not Powered	$Z_{RX-HIGH-IMP-DC}$	-150mV ≤ V_{IN_CM} ≤ +200mV		50			kΩ
Common-Mode Resistance to GND, Input Termination Powered	Z_{RX-DC}			20	25	30	Ω
Output Short-Circuit Current	$I_{TX-SHORT}$	Single-ended (Note 4)		90			mA
Common-Mode Delta, Between Active and Idle States	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$					100	mV
DC Output Offset, During Active State	$V_{TX-ACTIVE-DIFF-DC}$	$\lvert(V_{OUT\_P} - V_{OUT\_M})\rvert$				65	mV
DC Output Offset, During Electrical Idle	$V_{TX-IDLE-DIFF-DC}$	$\lvert(V_{OUT\_P} - V_{OUT\_M})\rvert$				65	mV

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 200nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE (Note 4)						
Input Return Loss, Differential	$RL_{RX-DIFF}$	f = 0.05GHz to 1.25GHz	9			dB
		f = 1.25GHz to 2.5GHz	8			dB
		f = 2.5GHz to 4GHz	5			dB
Input Return Loss, Common Mode	RL_{RX-CM}	f = 0.05GHz to 2.5GHz	6			dB
		f = 2.5GHz to 4GHz	4			dB
Output Return Loss, Differential	$RL_{TX-DIFF}$	f = 0.05GHz to 1.25GHz	10			dB
		f = 1.25GHz to 2.5GHz	8			dB
		f = 2.5GHz to 4GHz	4			dB
Output Return Loss, Common Mode	RL_{TX-CM}	f = 0.05GHz to 2.5GHz	6			dB
		f = 2.5GHz to 4GHz	4			dB
Redriver-Operation Differential Input-Signal Range	$V_{RX-DIFF-PP}$		100		1200	mV_{P-P}
Full-Swing Differential Output Voltage (No Deemphasis)	$V_{TX-DIFF-PP}$	2 x $\lvert(V_{OUT\_P} - V_{OUT\_M})\rvert$, OEQ_2 = OEQ_1 = OEQ_0 = GND	800	1000	1400	mV_{P-P}
Output Deemphasis Ratio, 0dB	$V_{TX-DE-RATIO-0dB}$	OEQ_2 = OEQ_1 = OEQ_0 = GND, Figure 1		0		dB
Output Deemphasis Ratio, 3.5dB	$V_{TX-DE-RATIO-3.5dB}$	OEQ_2 = OEQ_1 = GND, OEQ_0 = V_{CC}, Figure 1		3.5		dB
Output Deemphasis Ratio, 6dB	$V_{TX-DE-RATIO-6dB}$	OEQ_2 = OEQ_0 = GND, OEQ_1 = V_{CC}, Figure 1		6		dB
Output Deemphasis Ratio, 6dB with Higher Amplitude	$V_{TX-DE-HA-RATIO-6dB}$	OEQ_2 = GND, OEQ_1 = OEQ_0 = V_{CC}, Figure 1		6		dB
Output Deemphasis Ratio, 3.5dB with Preshoot	$V_{TX-DE-PS-RATIO-3.5dB}$	OEQ_2 = V_{CC}, OEQ_1 = OEQ_0 = GND, Figure 1		3.5		dB
Output Deemphasis Ratio, 6dB with Preshoot	$V_{TX-DE-PS-RATIO-6dB}$	OEQ_2 = OEQ_0 = V_{CC}, OEQ_1 = GND, Figure 1		6		dB
Output Deemphasis Ratio, 9dB with Preshoot	$V_{TX-DE-PS-RATIO-9dB}$	OEQ_2 = OEQ_1 = V_{CC}, OEQ_0 = GND, Figure 1		9		dB
Output Deemphasis Ratio, 9dB with Preshoot and Higher Amplitude	$V_{TX-DE-PS-HA-RATIO-9dB}$	OEQ_2 = OEQ_1 = OEQ_0 = V_{CC}, Figure 1		9		dB
Input Equalization, 5dB	$V_{RX-EQ-5dB}$	INEQ_1 = INEQ_0 = GND (Note 5)		5		dB

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 200nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Equalization, 8dB	$V_{RX-EQ-8dB}$	INEQ_1 = GND, INEQ_0 = V_{CC} (Note 5)		8		dB
Input Equalization, 12dB	$V_{RX-EQ-12dB}$	INEQ_1 = V_{CC}, INEQ_0 = GND (Note 5)		12		dB
Input Equalization, 16dB	$V_{RX-EQ-16dB}$	INEQ_1 = INEQ_0 = V_{CC} (Note 5)		16		dB
Output Common-Mode Voltage	$V_{TX-CM-AC-PP}$	MAX(V_{OUT_P} + V_{OUT_M})/2 - MIN(V_{OUT_P} + V_{OUT_M})/2			100	mV_{P-P}
Propagation Delay	t_{PD}		120	160	240	ps
Rise/Fall Time	$t_{TX-RISE-FALL}$	(Note 6)	20			ps
Rise/Fall Time Mismatch	$t_{TX-RF-MISMATCH}$	(Note 6)			20	ps
Deterministic Jitter	$t_{TX-DJ-DD}$	K28.5 pattern, AC-coupled, R_L = 50Ω, no deemphasis, no preshoot, data rate = 8GT/s		7	23.5	ps_{P-P}
Random Jitter	$t_{TX-RJ-DD}$	D10.2 pattern, no deemphasis, no preshoot, data rate = 8GT/s		0.5	1.5	ps_{RMS}
Electrical Idle Entry Delay	$t_{TX-IDLE-SET-TO-IDLE}$	From input to output, D10.2 pattern, data rate = 1GT/s		5		ns
Electrical Idle Exit Delay	$t_{TX-IDLE-TO-DIFF-DATA}$	From input to output, D10.2 pattern, data rate = 1GT/s		5		ns
Electrical Idle Detect Threshold	$V_{TX-IDLE-THRESH}$	D10.2 pattern, data rate = 1GT/s (Note 3)	50	112	190	mV_{P-P}
		D10.2 pattern, data rate = 1GT/s to 8GT/s		112		
Output Voltage During Electrical Idle (AC)	$V_{TX-IDLE-DIFF-AC-P}$	|(V_{OUT_P} - V_{OUT_M})|			20	mV_{P-P}
Receiver-Detect Pulse Amplitude	$V_{TX-RCV-DETECT}$	Voltage change in positive direction		600		mV
Receiver-Detect Pulse Width				100		ns
Receiver-Detect Retry Period				200		ns
CONTROL LOGIC						
Input-Logic Level Low	V_{IL}				0.6	V
Input-Logic Level High	V_{IH}		1.4			V
Input-Logic Hysteresis	V_{HYST}			0.1		V
Input Pulldown Resistance	R_{PD}		200	375		kΩ
ESD PROTECTION						
ESD Voltage		Human Body Model (HBM)		±4		kV

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, C_{CL} = 200nF coupling capacitor on each output, R_L = 50Ω on each output, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 3)

Note 3: All devices are 100% production tested at T_A = +85°C. Specifications over operating temperature range are guaranteed by design.
Note 4: Guaranteed by design, unless otherwise noted.
Note 5: Equivalent to same amount of deemphasis driving the input.
Note 6: Rise and fall times are measured using 20% and 80% levels.

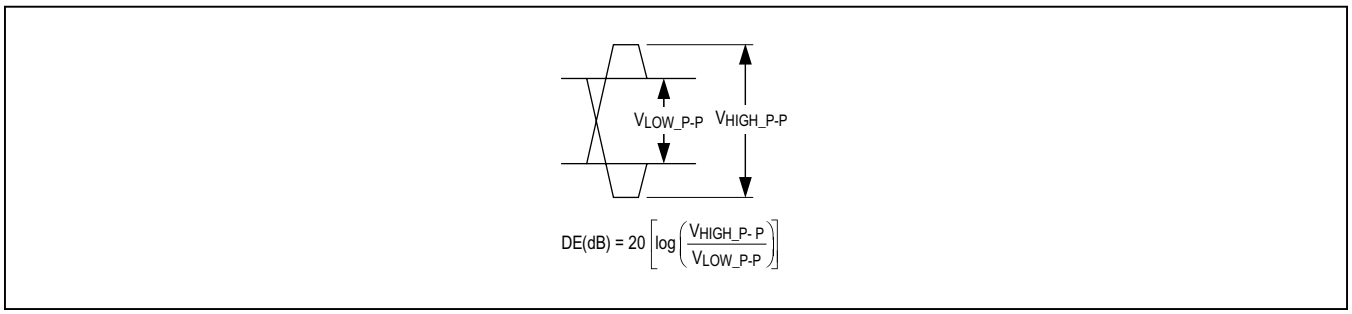
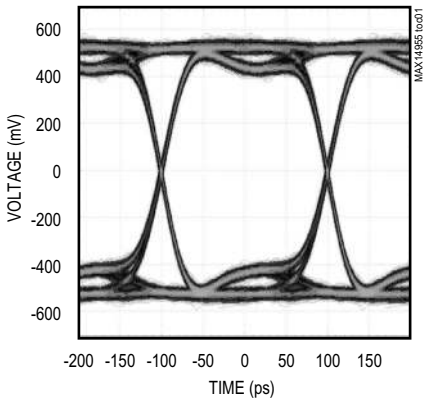


Figure 1. Illustration of Output Deemphasis

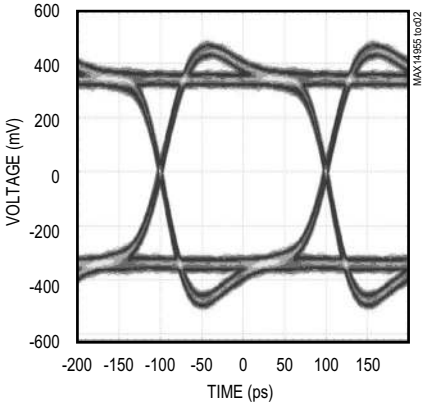
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

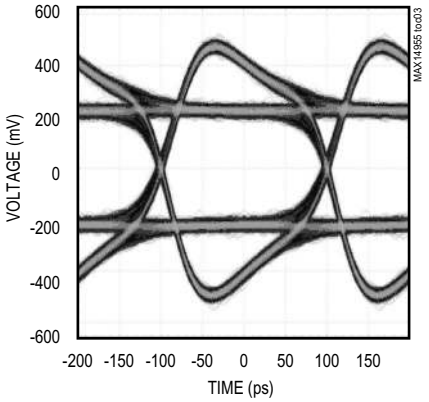
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 0, OEQ2 = 0, DATA RATE = 5GT/s



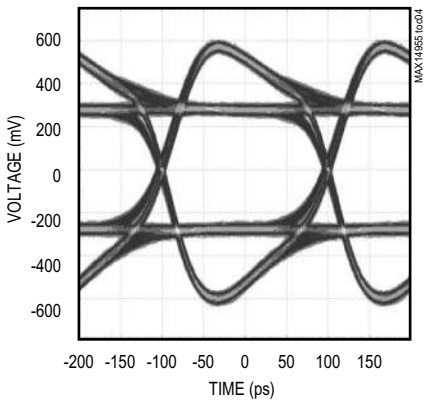
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 0, OEQ2 = 0, DATA RATE = 5GT/s



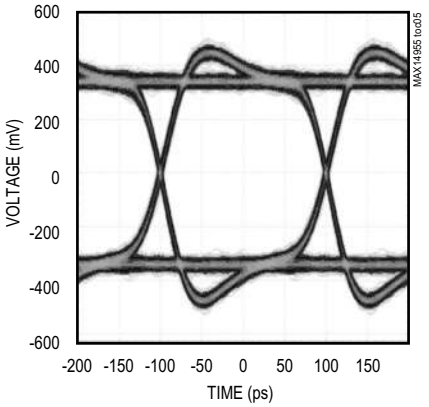
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 1, OEQ2 = 0, DATA RATE = 5GT/s



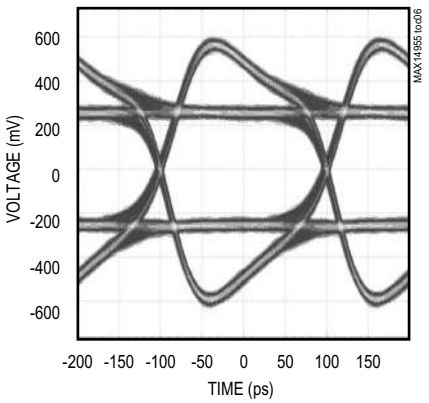
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 1, OEQ2 = 0, DATA RATE = 5GT/s



INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 0, OEQ2 = 1, DATA RATE = 5GT/s



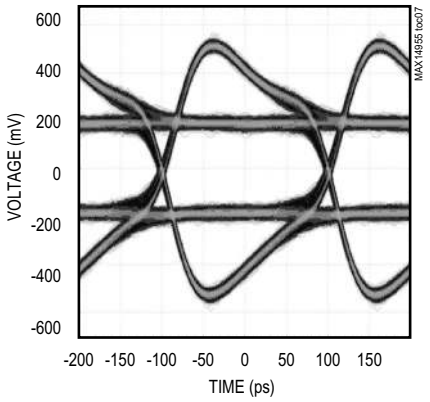
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 0, OEQ2 = 1, DATA RATE = 5GT/s



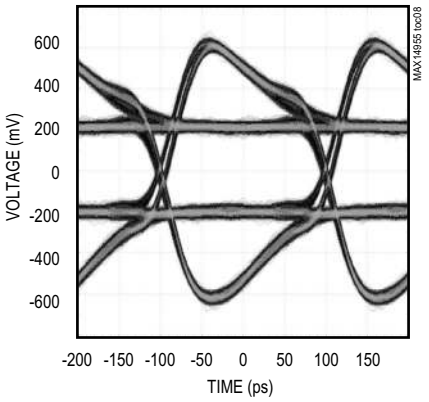
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

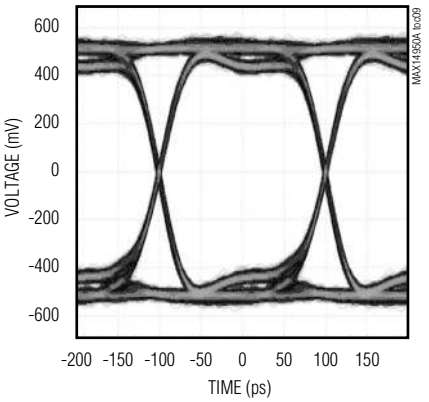
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 1, OEQ2 = 1, DATA RATE = 5GT/s



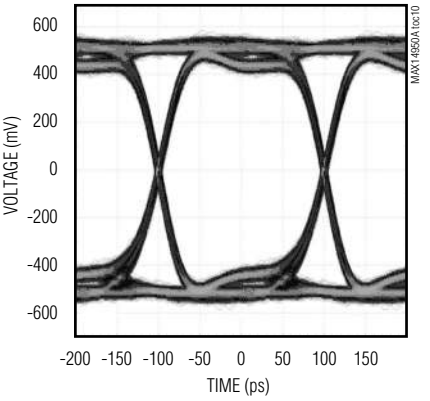
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 1, OEQ2 = 1, DATA RATE = 5GT/s



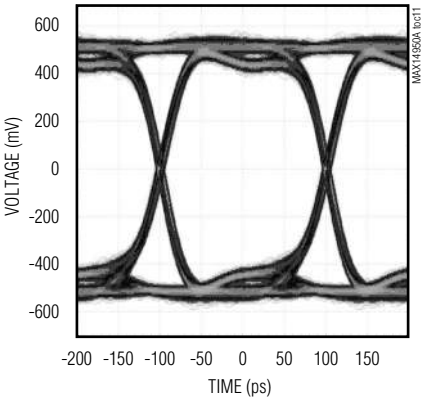
INEQ0 = 1, INEQ1 = 0, V_{IN} = 500mV$_{P-P}$, OEQ0 = OEQ1 = OEQ2 = 0, 6in MICROSTRIP ON INPUT, DATA RATE = 5GT/s



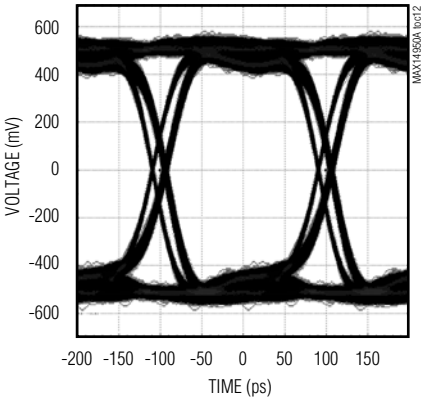
INEQ0 = 1, INEQ1 = 0, V_{IN} = 500mV$_{P-P}$, OEQ0 = OEQ1 = OEQ2 = 0, 12in MICROSTRIP ON INPUT, DATA RATE = 5GT/s



INEQ0 = 0, INEQ1 = 1, V_{IN} = 500mV$_{P-P}$, OEQ0 = OEQ1 = OEQ2 = 0, 18in MICROSTRIP ON INPUT, DATA RATE = 5GT/s



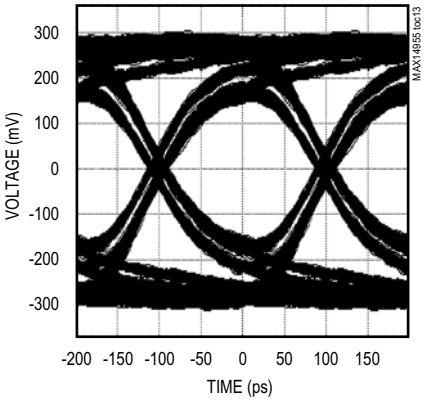
INEQ0 = 1, INEQ1 = 1, V_{IN} = 500mV$_{P-P}$, OEQ0 = OEQ1 = OEQ2 = 0, 24in MICROSTRIP ON INPUT, DATA RATE = 5GT/s



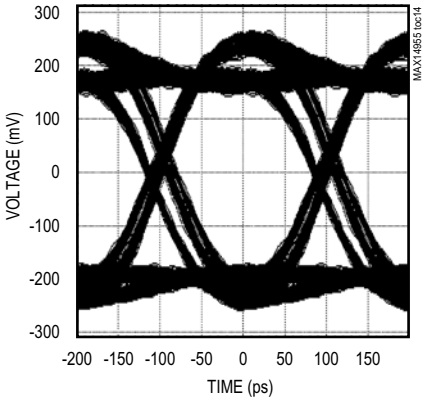
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

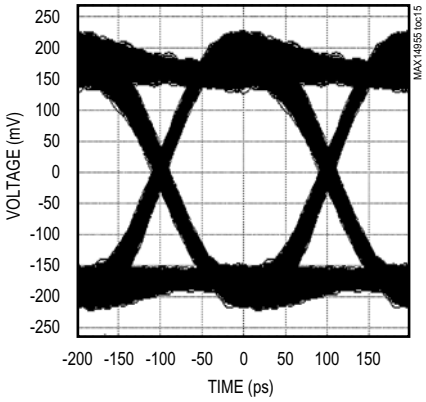
DATA RATE = 5Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



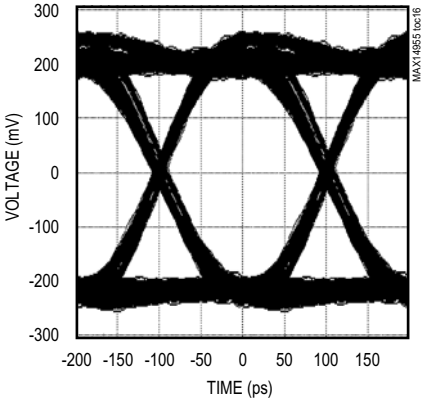
DATA RATE = 5Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



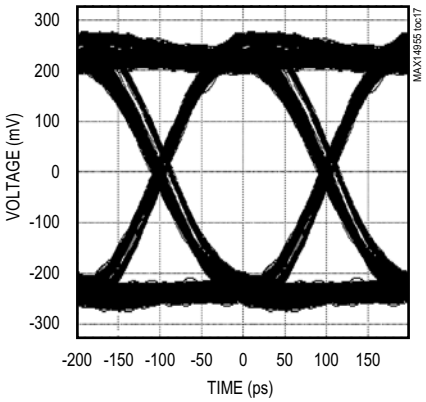
DATA RATE = 5Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



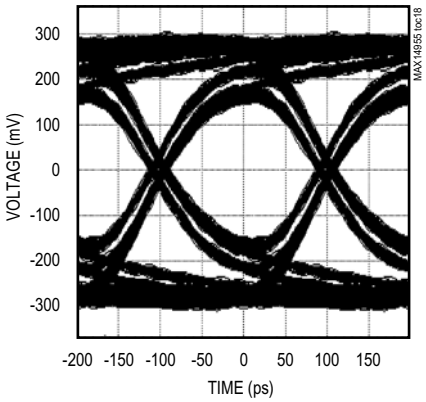
DATA RATE = 5Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



DATA RATE = 5Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



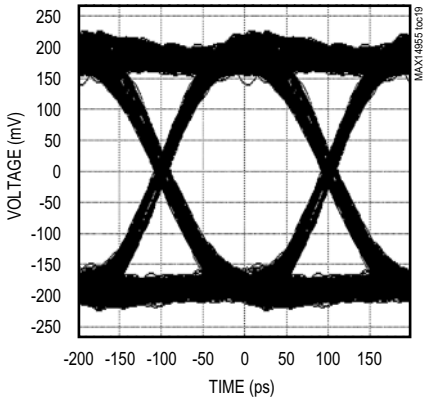
DATA RATE = 5Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



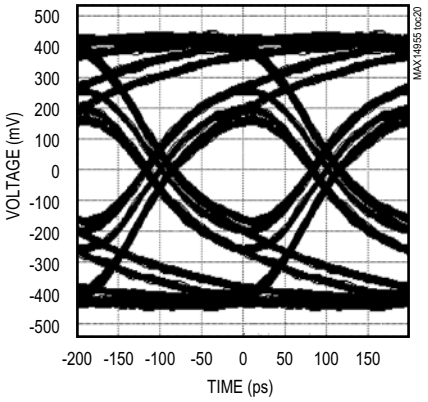
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

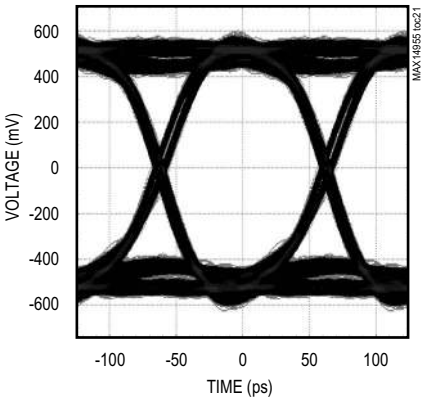
DATA RATE = 5Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



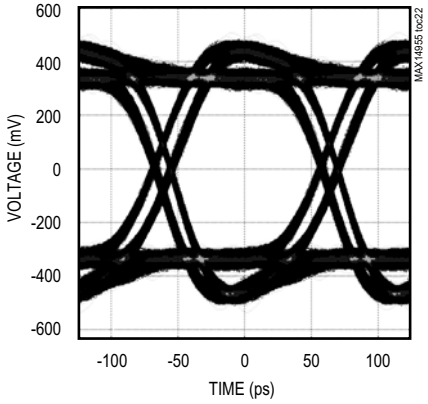
DATA RATE = 5Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



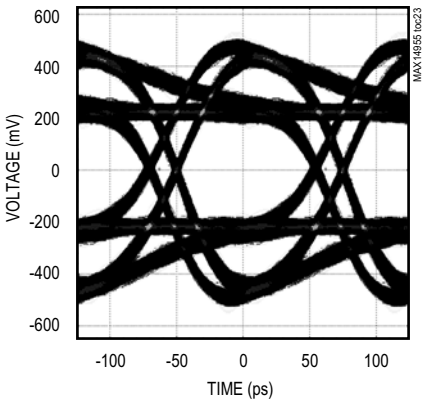
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 0, OEQ2 = 0, DATA RATE = 8GT/s



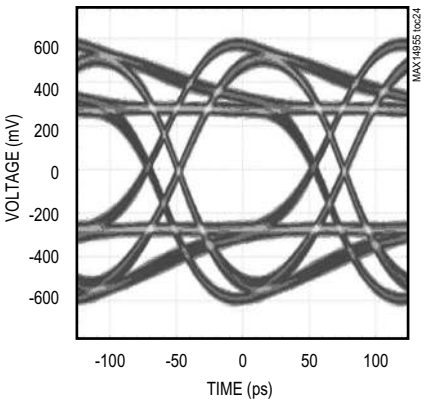
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 0, OEQ2 = 0, DATA RATE = 8GT/s



INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 1, OEQ2 = 0, DATA RATE = 8GT/s



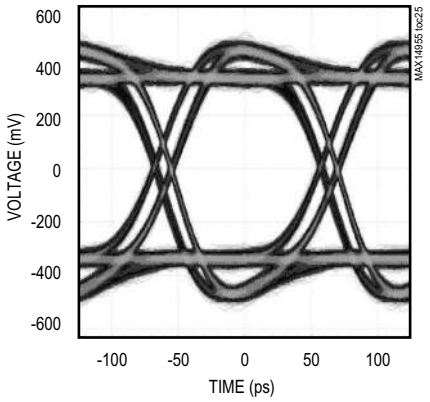
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 1, OEQ2 = 0, DATA RATE = 8GT/s



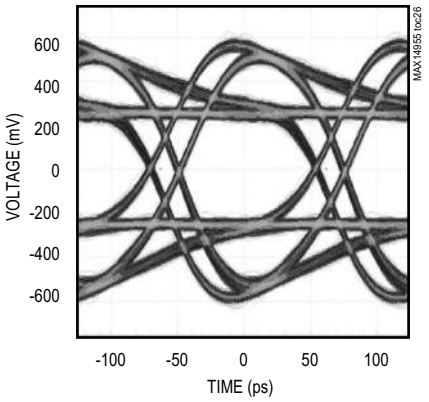
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

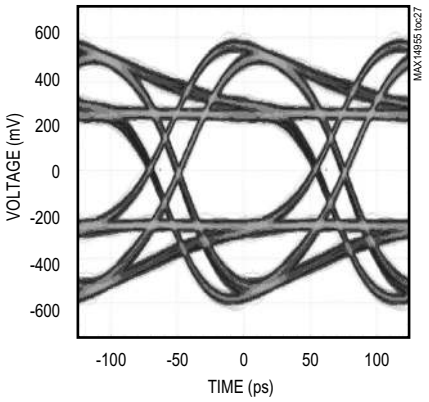
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 0, OEQ2 = 1, DATA RATE = 8GT/s



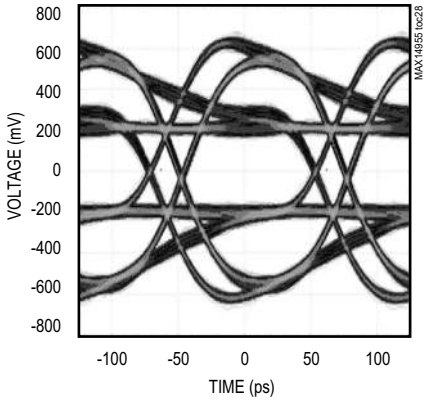
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 0, OEQ2 = 1, DATA RATE = 8GT/s



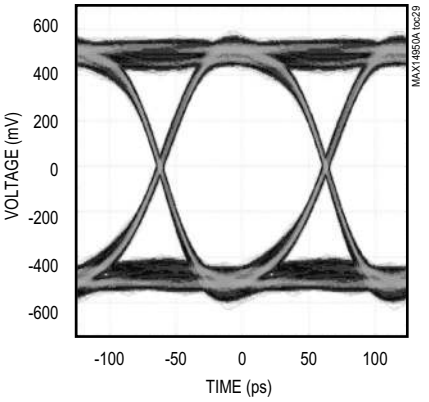
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 0, OEQ1 = 1, OEQ2 = 1, DATA RATE = 8GT/s



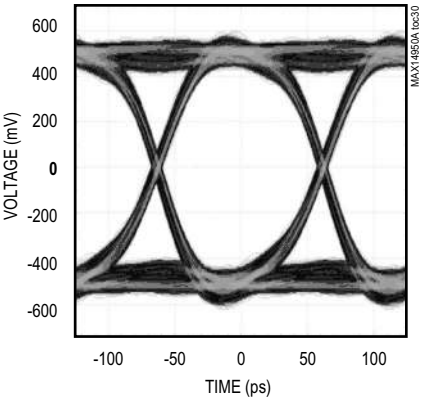
INEQ0 = INEQ1 = 0, V_{IN} = 200mV$_{P-P}$, OEQ0 = 1, OEQ1 = 1, OEQ2 = 1, DATA RATE = 8GT/s



INEQ0 = 0, INEQ1 = 0, V_{IN} = 500mV$_{P-P}$, OEQ0 = OEQ1 = OEQ2 = 0, 6in MICROSTRIP ON INPUT, DATA RATE = 8GT/s



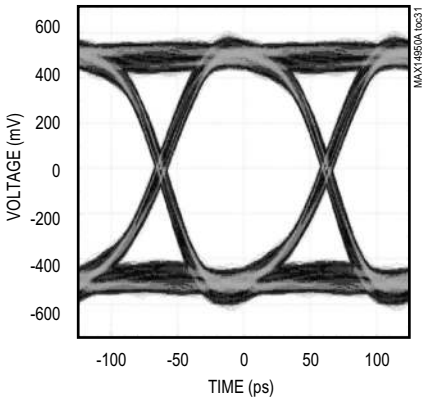
INEQ0 = 1, INEQ1 = 0, V_{IN} = 500mV$_{P-P}$, OEQ0 = OEQ1 = OEQ2 = 0, 12in MICROSTRIP ON INPUT, DATA RATE = 8GT/s



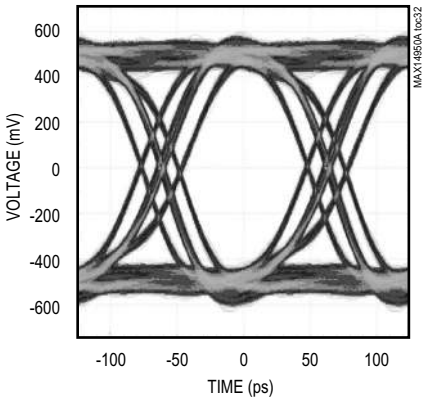
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

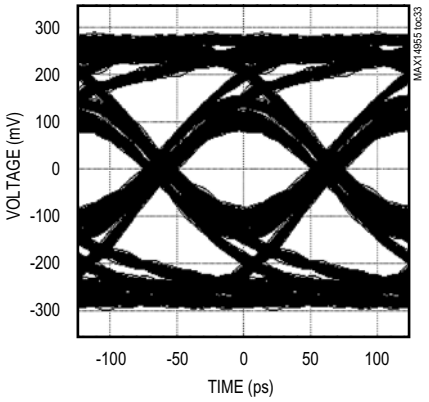
INEQ0 = 0, INEQ1 = 1, V_{IN} = 500mV$_{P-P}$, OEQ0 = OEQ1 = OEQ2 = 0, 18in MICROSTRIP ON INPUT, DATA RATE = 8GT/s



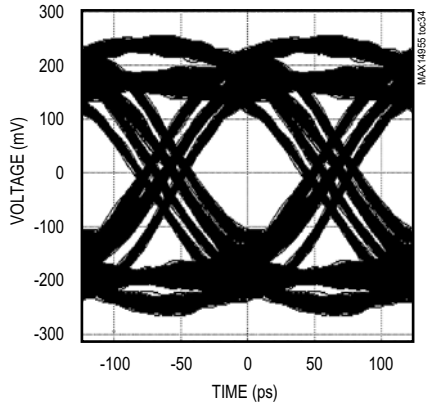
INEQ0 = 1, INEQ1 = 1, V_{IN} = 500mV$_{P-P}$, OEQ0 = OEQ1 = OEQ2 = 0, 24in MICROSTRIP ON INPUT, DATA RATE = 8GT/s



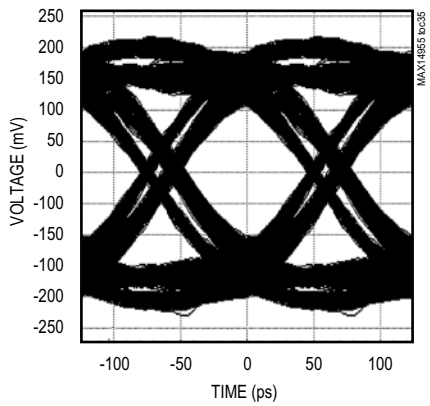
DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_0 = INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



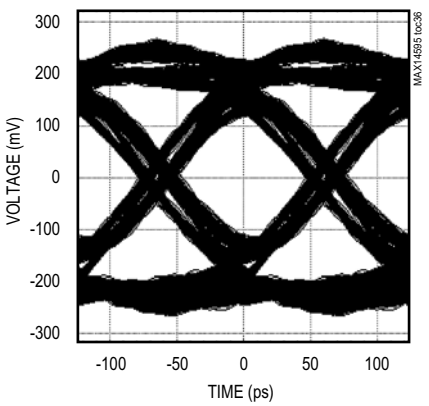
DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_0 = INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_0 = INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



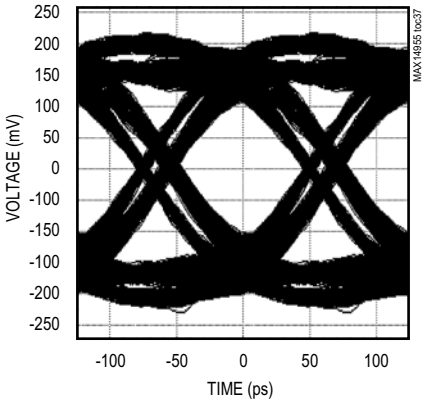
DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_0 = INEQ_1 = 0, V_{IN} = 200mV$_{P-P}$



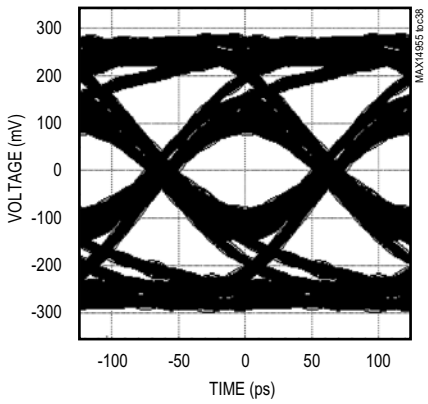
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

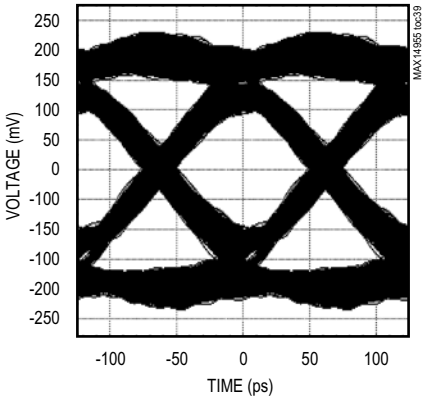
DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_0 = INEQ_1 = 0, V_{IN} = 200mV_{P-P}



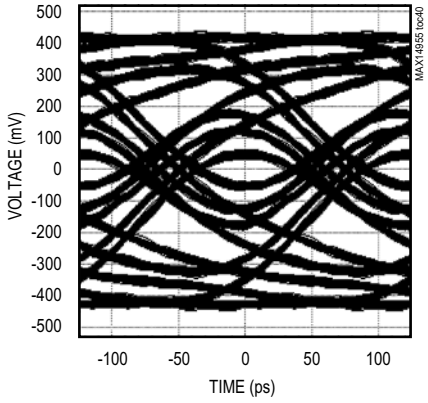
DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_0 = INEQ_1 = 0, V_{IN} = 200mV_{P-P}



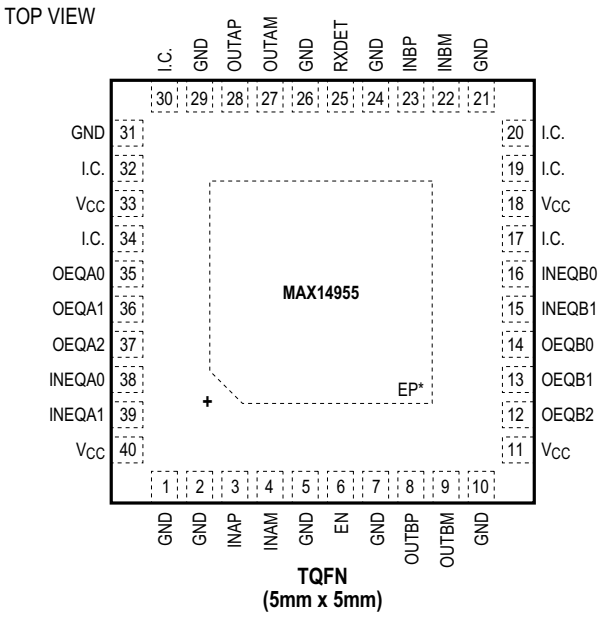
DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_0 = INEQ_1 = 0, V_{IN} = 200mV_{P-P}



DATA RATE = 8Gbps, OUTPUT AFTER 19in STRIPLINE, INEQ_0 = INEQ_1 = 0, V_{IN} = 200mV_{P-P}



Pin Configuration



*EXPOSED PAD. CONNECT TO GND.

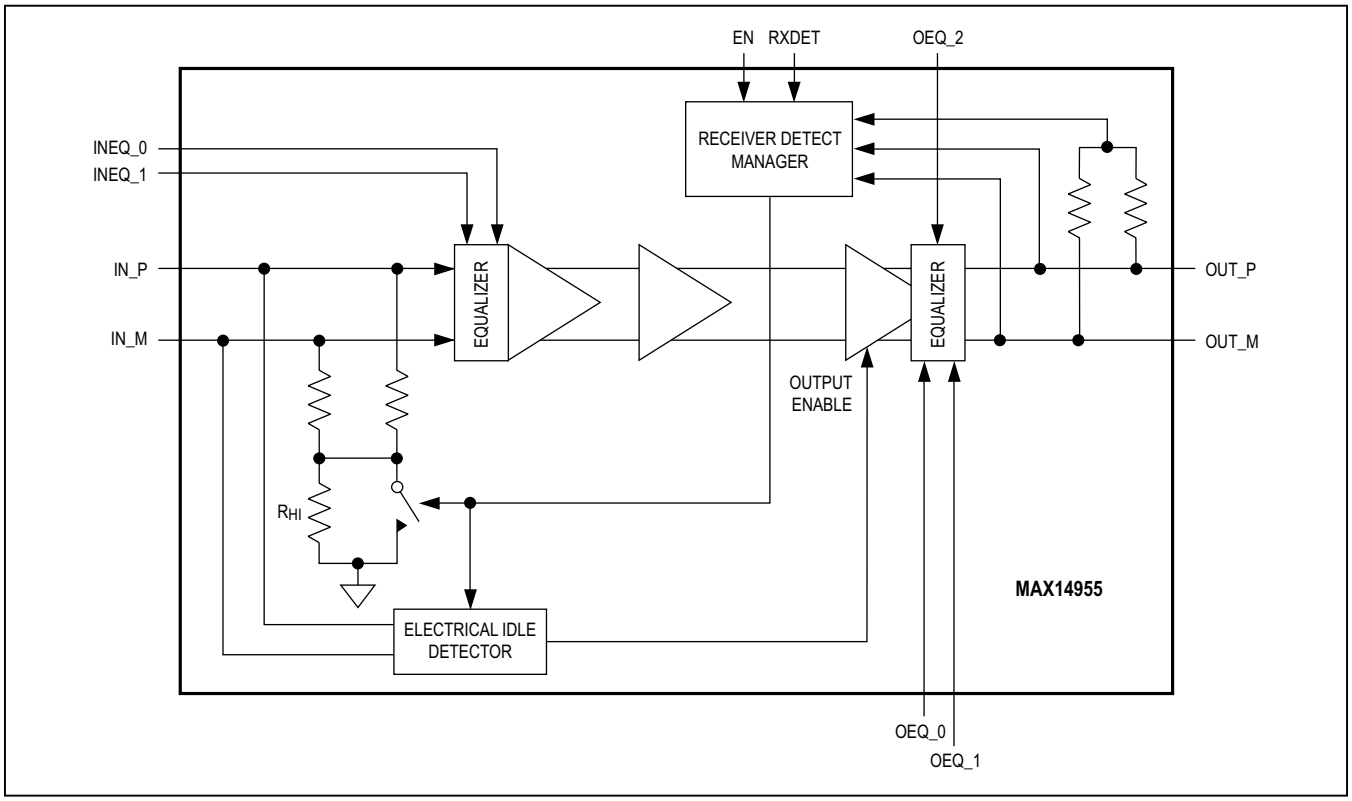
Pin Description

PIN	NAME	FUNCTION
1, 2, 5, 7, 10, 21, 24, 26, 29, 31	GND	Ground
3	INAP	Noninverting Input, Channel A
4	INAM	Inverting Input, Channel A
6	EN	Enable Input. Drive EN low for standby mode. Drive EN high for normal mode. EN has a 375kΩ (typ) internal pulldown resistor.
8	OUTBP	Noninverting Output, Channel B
9	OUTBM	Inverting Output, Channel B
11, 18, 33, 40	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 0.1µF and 0.01µF capacitors in parallel as close as possible to the device.
12	OEQB2	Output Deemphasis Control MSB, Channel B. OEQB2 has a 375kΩ (typ) internal pulldown resistor.
13	OEQB1	Output Deemphasis Bit 1, Channel B. OEQB1 has a 375kΩ (typ) internal pulldown resistor.

Pin Description (continued)

PIN	NAME	FUNCTION
14	OEQB0	Output Deemphasis Control LSB, Channel B. OEQB0 has a 375kΩ (typ) internal pulldown resistor.
15	INEQB1	Input Equalization Control MSB, Channel B. INEQB1 has a 375kΩ (typ) internal pulldown resistor.
16	INEQB0	Input Equalization Control LSB, Channel B. INEQB0 has a 375kΩ (typ) internal pulldown resistor.
17, 19, 20, 30, 32, 24	I.C.	Internally Connected. Leave I.C. unconnected.
22	INBM	Inverting Input, Channel B
23	INBP	Noninverting Input, Channel B
25	RXDET	Receiver Detection Control Bit. Toggle RXDET to initiate receiver detection. RXDET has a 375kΩ (typ) internal pulldown resistor.
27	OUTAM	Inverting Output, Channel A
28	OUTAP	Noninverting Output, Channel A
35	OEQA0	Output Deemphasis Control LSB, Channel A. OEQA0 has a 375kΩ (typ) internal pulldown resistor.
36	OEQA1	Output Deemphasis Control Bit 1, Channel A. OEQA1 has a 375kΩ (typ) internal pulldown resistor.
37	OEQA2	Output Deemphasis Control MSB, Channel A. OEQA2 has a 375kΩ (typ) internal pulldown resistor.
38	INEQA0	Input Equalization Control LSB, Channel A. INEQA0 has a 375kΩ (typ) internal pulldown resistor.
39	INEQA1	Input Equalization Control MSB, Channel A. INEQA1 has a 375kΩ (typ) internal pulldown resistor.
—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance and ground conductivity to the device. Do not use EP as the only GND connection.

Functional Diagram



Detailed Description

The MAX14955 dual equalizer/redriver supports Gen III (8GT/s), Gen II (5GT/s), and Gen I (2.5GT/s) PCIe data rates. The device contains two identical drivers with idle/receive detect on each lane and equalization/deemphasis/preshoot to compensate for circuit board loss. Programmable input equalization circuitry reduces deterministic jitter, improving signal integrity. The device features programmable output deemphasis/preshoot, permitting optimal placement of key PCIe components and longer runs of stripline, microstrip, or cable.

Programmable Input Equalization

Programmable input equalization for channel A is controlled by two bits: INEQA1 and INEQA0 and for channel B is controlled by two bits: INEQB1 and INEQB0 (Table 1.)

Programmable Output Deemphasis

Programmable output deemphasis/preshoot for channel A is controlled by the three bits: OEQA2, OEQA1, OEQA0 and channel B is controlled by the three bits: OEQB2, OEQB1, OEQB0 (Table 2.)

Receiver Detection

The device features receiver detection on each channel. Upon initial power-up, if EN is high, receiver detection initializes. Receiver detection can also be initiated on a rising or falling edge of the RXDET input when EN is high. During this time, the part remains in low-power standby mode and the outputs are squelched, despite the logic-high state of EN. Until a channel has detected a receiver, the receiver detection repeats indefinitely on each channel. If a channel detects a receiver, the other channel is limited to a few retries. Upon receiver detection, input common-mode termination and electrical idle detection are enabled (Table 3.)

Table 1. Input Equalization

INEQ_1	INEQ_0	INPUT EQUALIZATION (dB)
0	0	5
0	1	8
1	0	12
1	1	16

Table 2. Output Deemphasis/Preshoot

OEQ_2	OEQ_1	OEQ_0	OUTPUT DEEMPHASIS RATIO (dB)	PEAK-TO-PEAK SWING	PRESHOOT
0	0	0	0	1.0V	No
0	0	1	3.5	1.0V	No
0	1	0	6	1.0V	No
0	1	1	6	1.2V	No
1	0	0	3.5	1.0V	Yes
1	0	1	6	1.0V	Yes
1	1	0	9	0.9V	Yes
1	1	1	9	1.0V	Yes

Table 3. Receiver Detection Input Function

RXDET	EN	DESCRIPTION
X	0	Receiver detection is inactive.
X	1	Following a rising edge of EN signal, indefinite retry until a receiver is detected for at least one channel. Retries stop a few times after any channel is detected.
Rising/falling edge	1	Initiate receiver detection.

X = Don't care.

Electrical Idle Detection

The device features electrical idle detection to prevent unwanted noise from being redriven at the output. When the device detects the differential input has fallen below the electrical idle low threshold, it squelches the output. For differential input signals that are above the electrical idle high threshold, the device turns on the output and redrives the signal.

Applications Information

Layout

Circuit board layout and design can significantly affect the performance of the device. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on data signals. Power-supply decoupling capacitors must be placed as close as possible to V_{CC}. Always connect V_{CC} to a power plane. It is recommended to run receive and transmit on different layers to minimize crosstalk.

Exposed-Pad Package

The exposed-pad, 40-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the device must be soldered to the circuit board ground plane for proper thermal performance. For more information on exposed-pad packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply GND then V_{CC} before applying signals, especially if the signal is not current limited.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14955ETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	**21-0140**	**90-0002**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/13	Initial release	—

