TPS6283810, Tiny 6-pin 3-A Step-Down Converter in 1.2-mm x 0.8-mm WCSP

1 Features

- DCS-Control™ Topology
- 1-V Fixed Output Voltage, with 1% Accuracy
- 26mΩ and 26mΩ Internal Power MOSFETs
- 2.4-V to 5.5-V Input Voltage Range
- 4-µA Operating Quiescent Current
- 3.5-MHz Switching Frequency
- Power Save Mode for Light Load Efficiency
- Active Output Discharge
- Power Good Output
- Thermal Shutdown Protection
- Hiccup Short-Circuit Protection
- Available in 0.8 x 1.2 x 0.5-mm 6-Pin WCSP
- Create a Custom Design Using the TPS6283810 With the WEBENCH® Power Designer

2 Applications

- Consumer Wireless Modules
- Wearable Products
- Smart Phones
- Optical Modules

3 Description

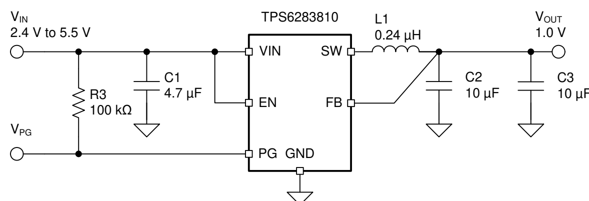
The device is a high-frequency synchronous step-down converter optimized for small solution size and high efficiency. With an input voltage range of 2.4 V to 5.5 V, common battery technologies are supported. At medium to heavy loads, the converter operates in PWM mode and automatically enters Power Save Mode operation at light load to maintain high efficiency over the entire load current range. The 3.5-MHz switching frequency allows the device to use small external components. Together with its DCS-control architecture, excellent load transient performance and output voltage regulation accuracy are achieved. Other features like over current protection, thermal shutdown protection, active output discharge and power good are built-in. The device is available in a 6-pin WCSP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6283810	YFP (6)	1.2mm x 0.8mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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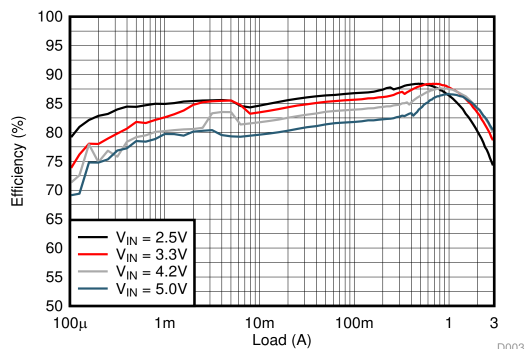
Efficiency



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2018	*	Initial release

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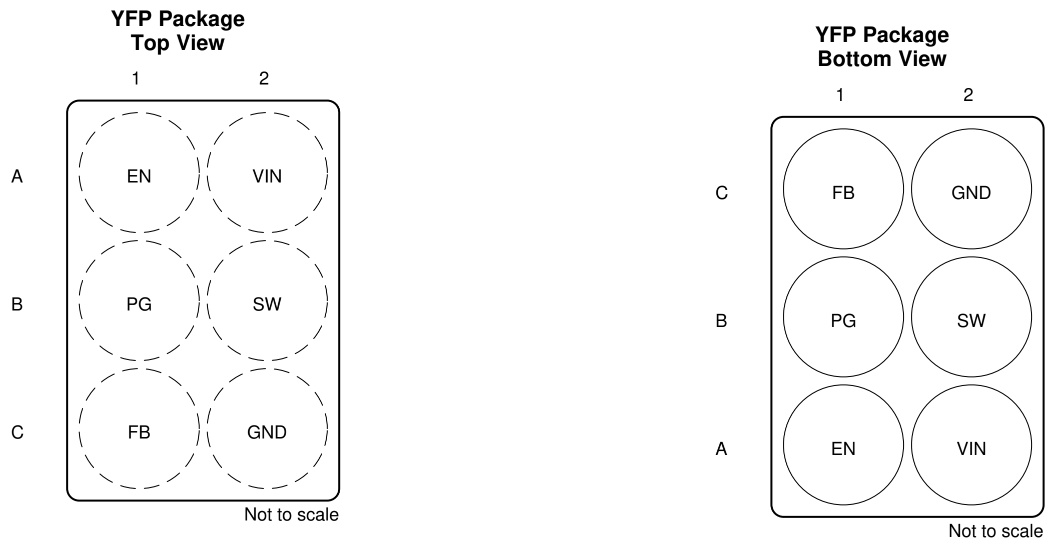
5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	A1	I	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
PG	B1	O	Power good open drain output pin. The pull-up resistor can be connected to voltages up to 5.5 V. If unused, leave it floating.
FB	C1	I	Feedback pin. For the fixed output voltage versions, this pin must be connected to the output.
GND	C2		Ground pin.
SW	B2	PWR	Switch pin of the power stage.
VIN	A2	PWR	Input voltage pin.

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6 Specifications

6.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
Voltage at Pins[2]	VIN, FB, EN, PG	–0.3	6	V
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (DC, in current limit)	-1.0	V_{IN} + 0.3	
	SW (AC, less than 10ns)[3]	-2.5	10	
Temperature	Operating Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.4		5.5	V
V_{OUT}	Output voltage range	0.6		4	V
I_{OUT}	Output current range[1]	0		3	A
I_{SINK_PG}	Sink current at PG pin			1	mA
V_{PG}	Pull-up resistor voltage			5.5	V
T_J	Operating junction temperature	–40		125	°C

(1) Lifetime is reduced when operating continuously at I_{OUT} = 3 A and the junction temperature ≥ 105 °C.

6.4 Thermal Information

THERMAL METRIC[1]		TPS6283810 YFP (6-PINS), JEDEC	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 ELECTRICAL CHARACTERISTICS

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching		4	10	µA
I_{SD}	Shutdown current	EN = Low, T_J = -40°C to 85°C		0.05	0.5	µA

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ELECTRICAL CHARACTERISTICS (continued)

T_J = -40 °C to 125 °C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25 °C and V_{IN} = 5 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Under voltage lock out hysteresis	V_{IN} rising		160		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level threshold voltage		1.0			V
V_{IL}	Low-level threshold voltage				0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	0.1	µA
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		1.25		ms
V_{PG}	Power good lower threshold	V_{PG} rising, V_{FB} referenced to V_{OUT} nominal	94	96	98	%
		V_{PG} falling, V_{FB} referenced to V_{OUT} nominal	90	92	94	%
	Power good upper threshold	V_{PG} rising, V_{FB} referenced to V_{OUT} nominal	103	105	107	%
		V_{PG} falling, V_{FB} referenced to V_{OUT} nominal	108	110	112	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01	0.1	µA
OUTPUT						
V_{OUT}	Output voltage accuracy	TPS6283810, PWM mode	0.990	1.0	1.010	V
R_{FB}	Internal resistor divider connected to FB pin			7.5		MΩ
I_{DIS}	Output discharge current	V_{SW} = 0.4V; EN = LOW	75	400		mA
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			26		mΩ
I_{LIM}	High-side FET switch current limit		3.6	4.3	5.0	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 1.0 V		3.5		MHz

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6.6 Typical Characteristics

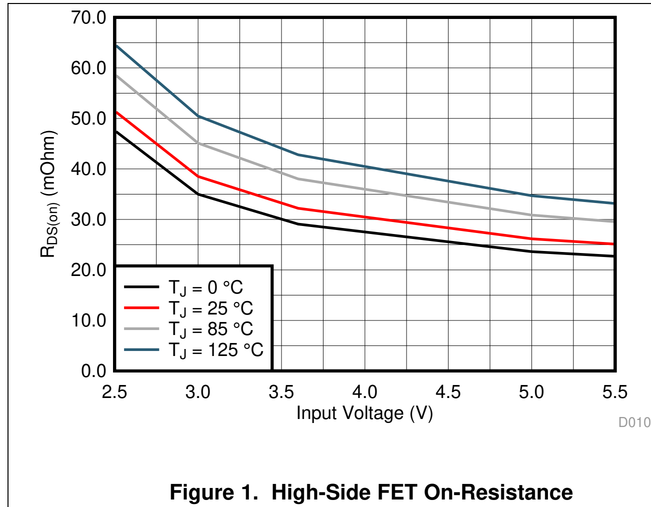

Figure 1. High-Side FET On-Resistance

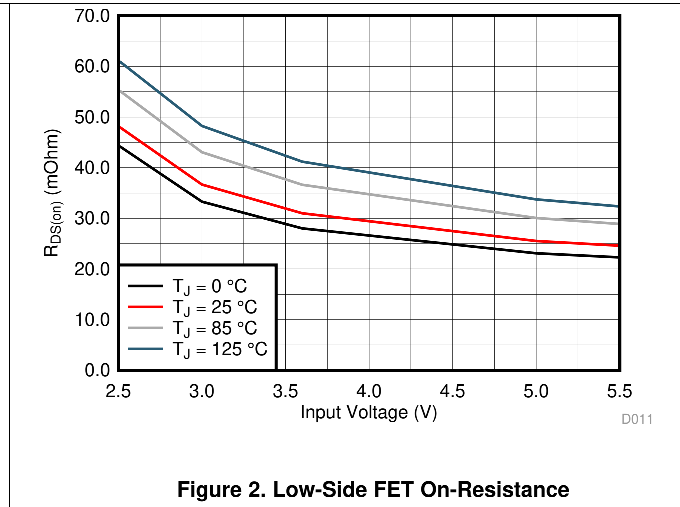

Figure 2. Low-Side FET On-Resistance

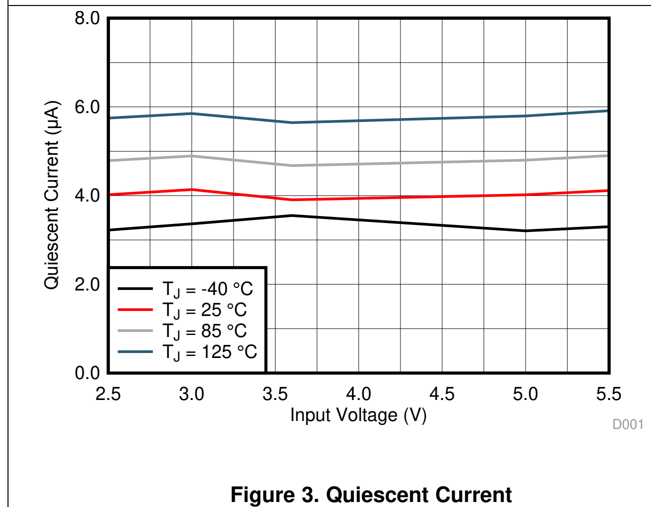

Figure 3. Quiescent Current

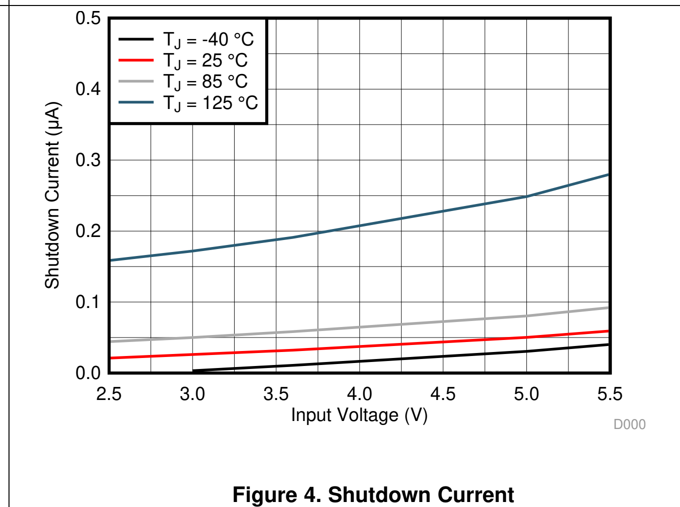

Figure 4. Shutdown Current

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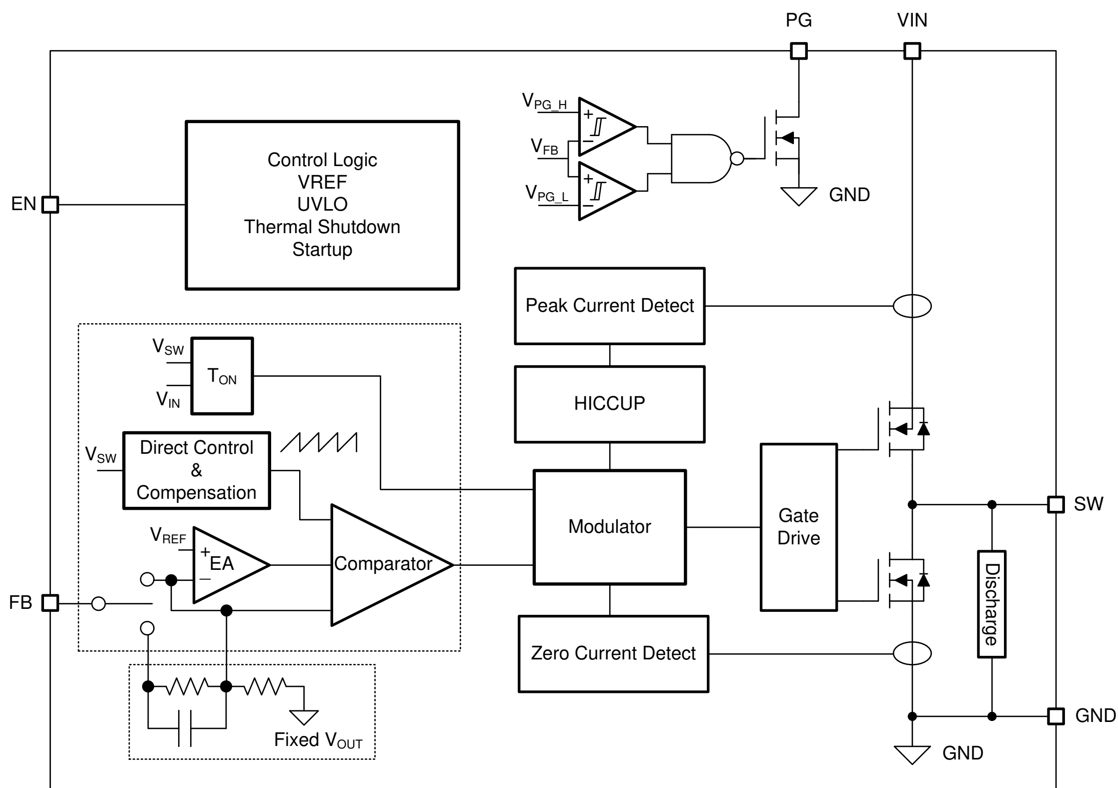
7 Detailed Description

7.1 Overview

The synchronous step-down converter adopts a DCS-Control (Direct Control with Seamless transition into Power Save Mode) topology. This is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control schemes.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its nominal switching frequency of 3.5 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC current consumption to achieve high efficiency over the entire load current range. Because DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to Power Save Mode is seamless and without effects on the output voltage. The devices offer both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

As the load current decreases, the device enters Power Save Mode (PSM) operation. The power save mode occurs when the inductor current becomes discontinuous. PSM is based on a fixed on-time architecture and the switching frequency in PSM is reduced, as related in Equation 1.

Feature Description (continued)

$$t_{ON} = 250ns \times \frac{V_{OUT}}{V_{IN}}$$

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (1)$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

When the device operates close to 100% duty cycle mode, the device can't enter Power Save Mode regardless of the load current if the input voltage decreases to typically 10% above the output voltage. The device maintains output regulation in PWM mode.

7.3.2 100% Duty Cycle Low Dropout Operation

The devices offer low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain output regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L)$$

where

- $V_{IN,MIN}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR) (2)

7.3.3 Soft Start

After enabling the device, there is a 250-µs delay before switching starts. Then, an internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during the startup time of 1 ms. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The device is able to start into a pre-biased output capacitor. It starts with the applied bias voltage and ramps the output voltage to its nominal value.

7.3.4 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET remains off, while the inductor current flows through its body diode and quickly ramps down.

When this switch current limits is triggered 32 times, the device stops switching. The device then automatically starts a new start-up after a typical delay time of 128 µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

7.3.5 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO}.

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Feature Description (continued)

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops the power stage switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically by switching the power stage again.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic High. Accordingly, shutdown mode is forced if the EN pin is pulled Low with a shutdown current of typically 50 nA. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal switch smoothly discharges the output through the SW pin in shutdown mode. Do not leave the EN pin floating.

The typical threshold value of the EN pin is 0.89 V for rising input signal, and 0.62 V for falling input signal.

7.4.2 Power Good

The device has a power good output. The PG pin goes high impedance once the FB pin voltage is above 96% and less than 105% of the nominal voltage, and is driven low once the voltage falls below typically 92% or higher than 110% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

The PG rising edge has a 100-µs blanking time and the PG falling edge has a deglitch delay of 20 µs.

Table 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable	EN = High, V_{FB} ≥ 96% of Nominal Value	√	
	EN = High, V_{FB} ≤ 92% of Nominal Value		√
	EN = High, V_{FB} ≤ 105% of Nominal Value	√	
	EN = High, V_{FB} ≥ 110% of Nominal Value		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 0.7\ V$	√	

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

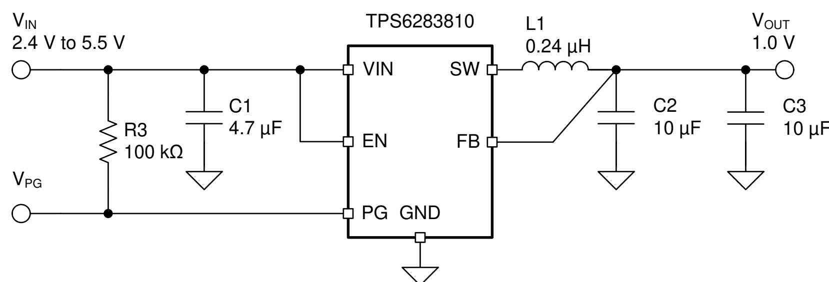

Figure 5. Typical Application of Fixed Output

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4 V to 5.5 V
Output voltage	1.0 V
Maximum peak output current	3 A

Table 3 lists the components used for the example.

Table 3. List of Components of Figure 5

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	4.7 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, JMK107BB7475MA	Taiyo Yuden
C2, C3	10 µF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106MA73D	Murata
L1	0.24 µH, Power Inductor, size 0603, DFE160810S-R24M (DFE18SANR24MG0)	Murata
R3	100 kΩ, Chip resistor, 1/16 W, 1%, size 0603	Std

(1) See Third-party Products disclaimer.

Table 4. List of Components of Figure 5, Smallest Solution

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1, C2, C3	10 µF, Ceramic capacitor, 6.3 V, X5R, size 0402, GRM155R60J106ME47	Murata
L1	0.24 µH, Power Inductor, size 0603, DFE160810S-R24M (DFE18SANR24MG0)	Murata
R3	100 kΩ, Chip resistor, 1/16 W, size 0402	Std

(1) See Third-party Products disclaimer.

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, Table 5 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

Table 5. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH] (1)	NOMINAL C_{OUT} [µF] (2)			
	10	2 x 10 or 1 x 22	47	100
0.24	+	+ (3)	+	
0.33	+	+	+	
0.47				

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) This LC combination is the standard value and recommended for most applications.

8.2.2.3 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 3 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}$$

where

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value (3)

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size should also be taken into account when selecting an appropriate inductor. Table 6 lists recommended inductors.

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Table 6. List of Recommended Inductors(1)

Inductance [µH]	Current Rating [A]	Dimensions [L x W x H mm]	DC Resistance [mΩ]	Part Number
0.24	4.9	1.6 x 0.8 x 1.0	30	Murata, DFE160810S-R24M (DFE18SANR24MG0)
0.24	6.5	2.0 x 1.2 x 1.0	25	Murata, DFE201210U-R24M
0.24	4.9	1.6 x 0.8 x 0.8	22	Cyntec, HTEH16080H-R24MSR
0.25	9.7	4.0 x 4.0 x 1.2	7.64	Coilcraft, XFL4012-251ME
0.24	3.5	2.0 x 1.6 x 0.6	35	Wurth Electronics, 74479977124
0.24	3.5	2.0 x 1.6 x 0.6	35	Sunlord, MPM201606SR24M

(1) See Third-party Products disclaimer.

8.2.2.4 Capacitor Selection

The input capacitor is the low-impedance energy source for the converters which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, 4.7 µF is sufficient, though a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended typical output capacitor value is 2 x 10 µF or 1 x 22 µF; this capacitance can vary over a wide range as outline in the output filter selection table.

8.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 1.0 V, T_A = 25 ºC, BOM = Table 3, unless otherwise noted.

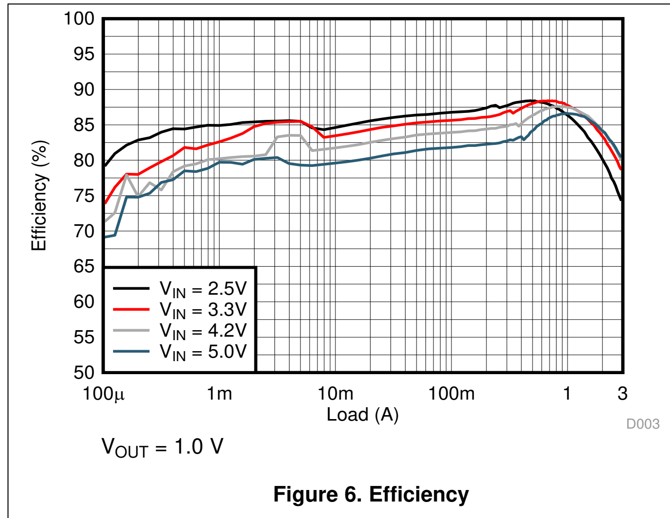

Figure 6. Efficiency

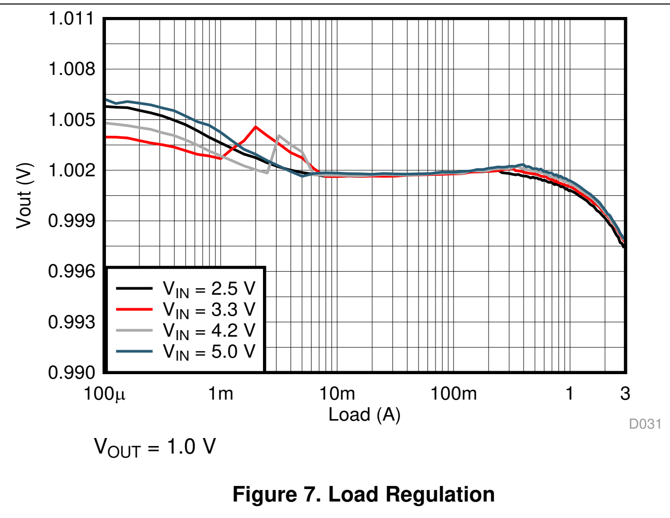

Figure 7. Load Regulation

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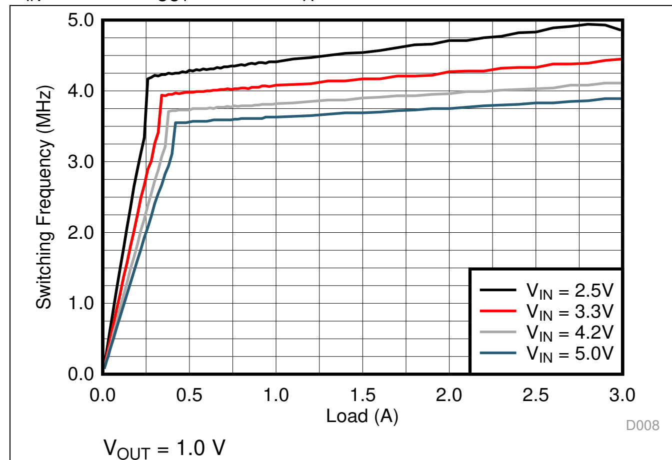
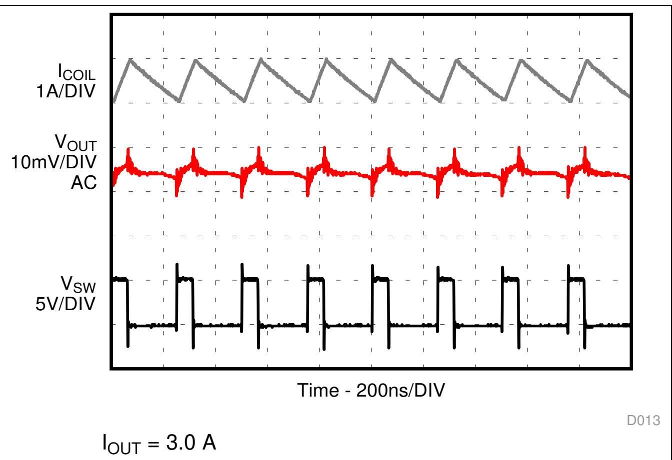
V_{IN} = 5.0 V, V_{OUT} = 1.0 V, T_A = 25 ºC, BOM = Table 3, unless otherwise noted.



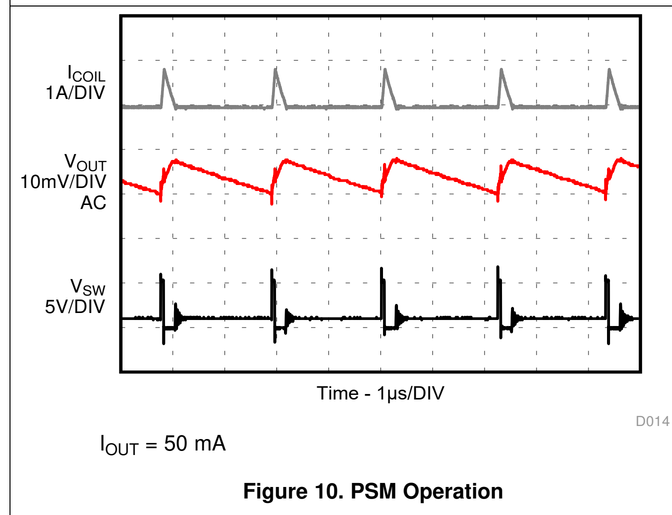
V_{OUT} = 1.0 V

Figure 8. Switching Frequency



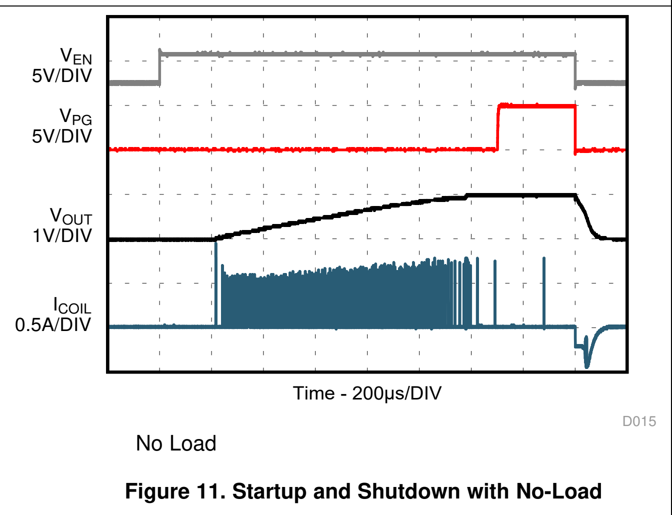
I_{OUT} = 3.0 A

Figure 9. PWM Operation



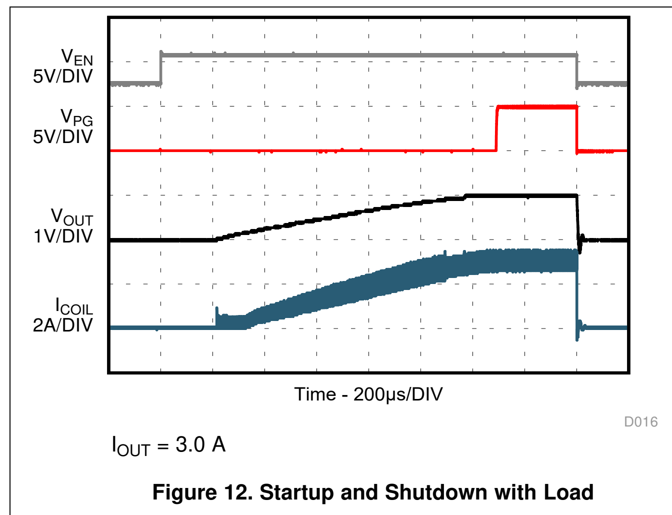
I_{OUT} = 50 mA

Figure 10. PSM Operation



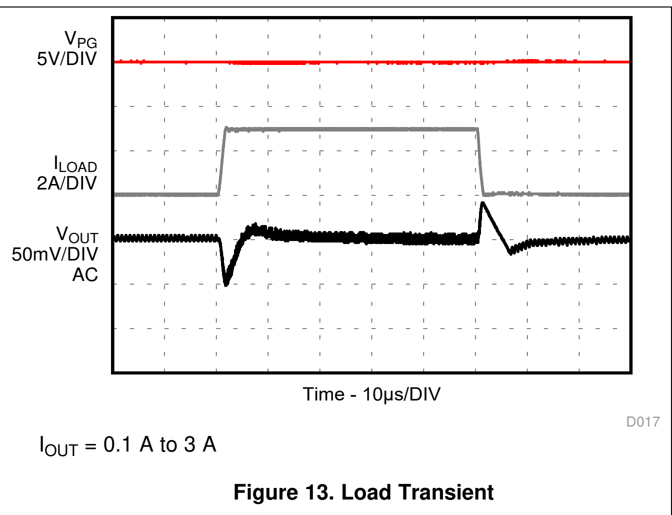
No Load

Figure 11. Startup and Shutdown with No-Load



I_{OUT} = 3.0 A

Figure 12. Startup and Shutdown with Load



I_{OUT} = 0.1 A to 3 A

Figure 13. Load Transient

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V_{IN} = 5.0 V, V_{OUT} = 1.0 V, T_A = 25 ºC, BOM = Table 3, unless otherwise noted.

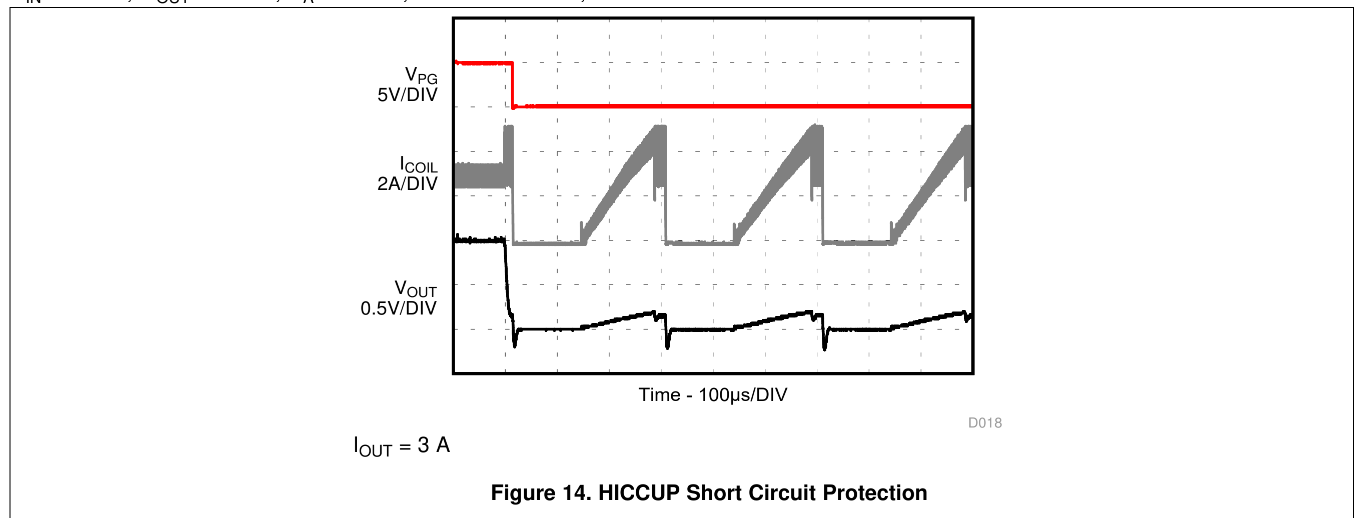

Figure 14. HICCUP Short Circuit Protection

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

10 Layout

10.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See and Figure 15 for the recommended PCB layout.

- The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
- The sense traces connected to FB is a signal trace. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors should be made at the output capacitor.
- Refer to and Figure 15 for an example of component placement, routing and thermal design.

10.2 Layout Example

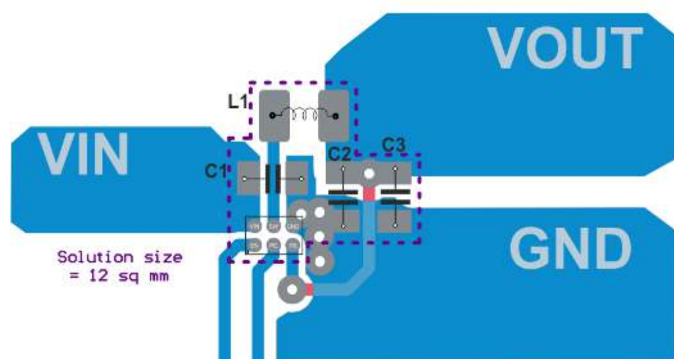

Figure 15. PCB Layout of Fixed Output Voltage Application

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the *Thermal Characteristics Application Notes*, SZZA017 and SPRA953.

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Development Support

11.2.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2.2 Related Documentation

For related documentation, see the following:

- *Thermal Characteristics Application Note*, SZZA017
- *Thermal Characteristics Application Note*, SPRA953

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YFP0006-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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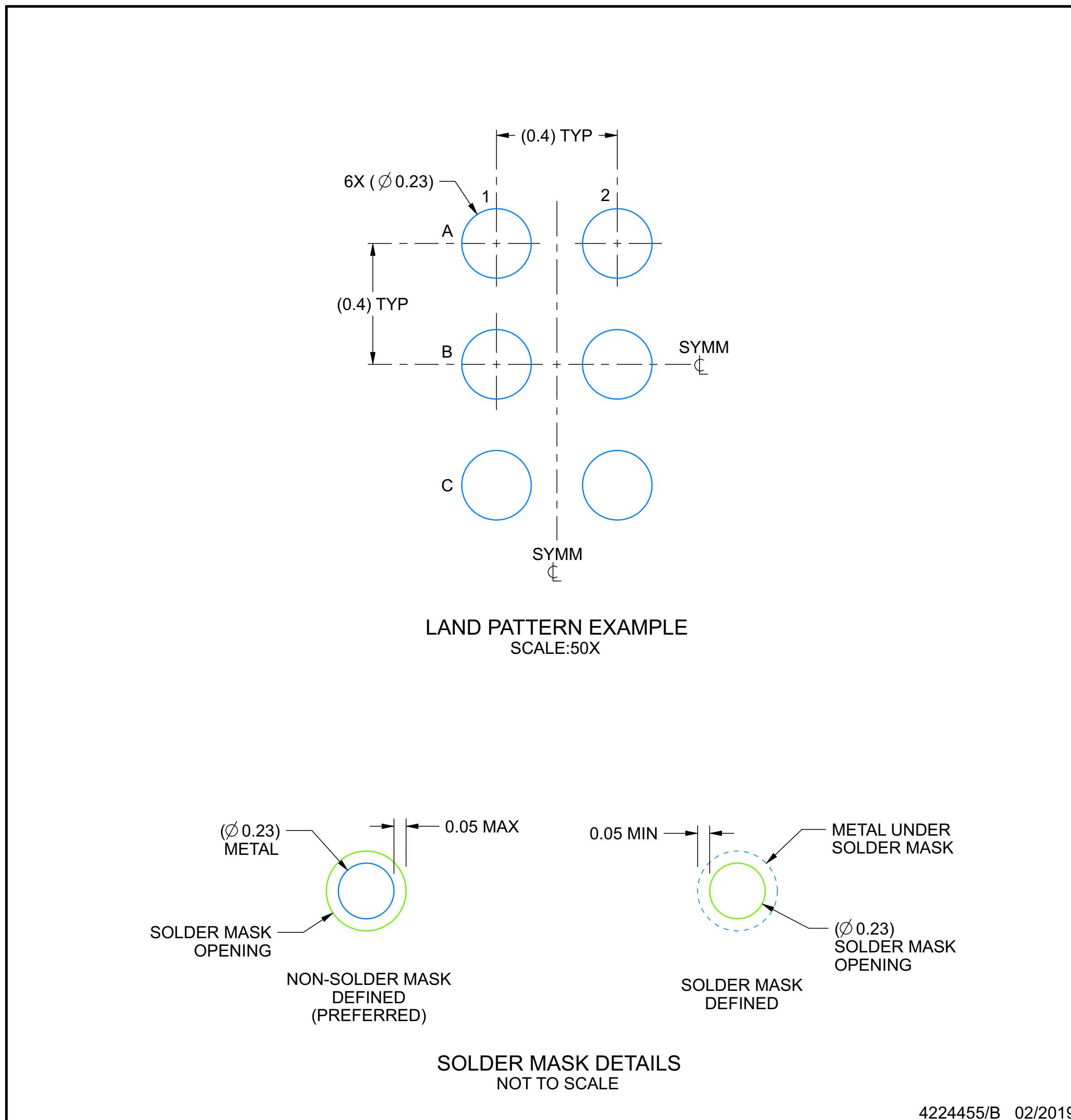
EXAMPLE BOARD LAYOUT

YFP0006-C01 DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

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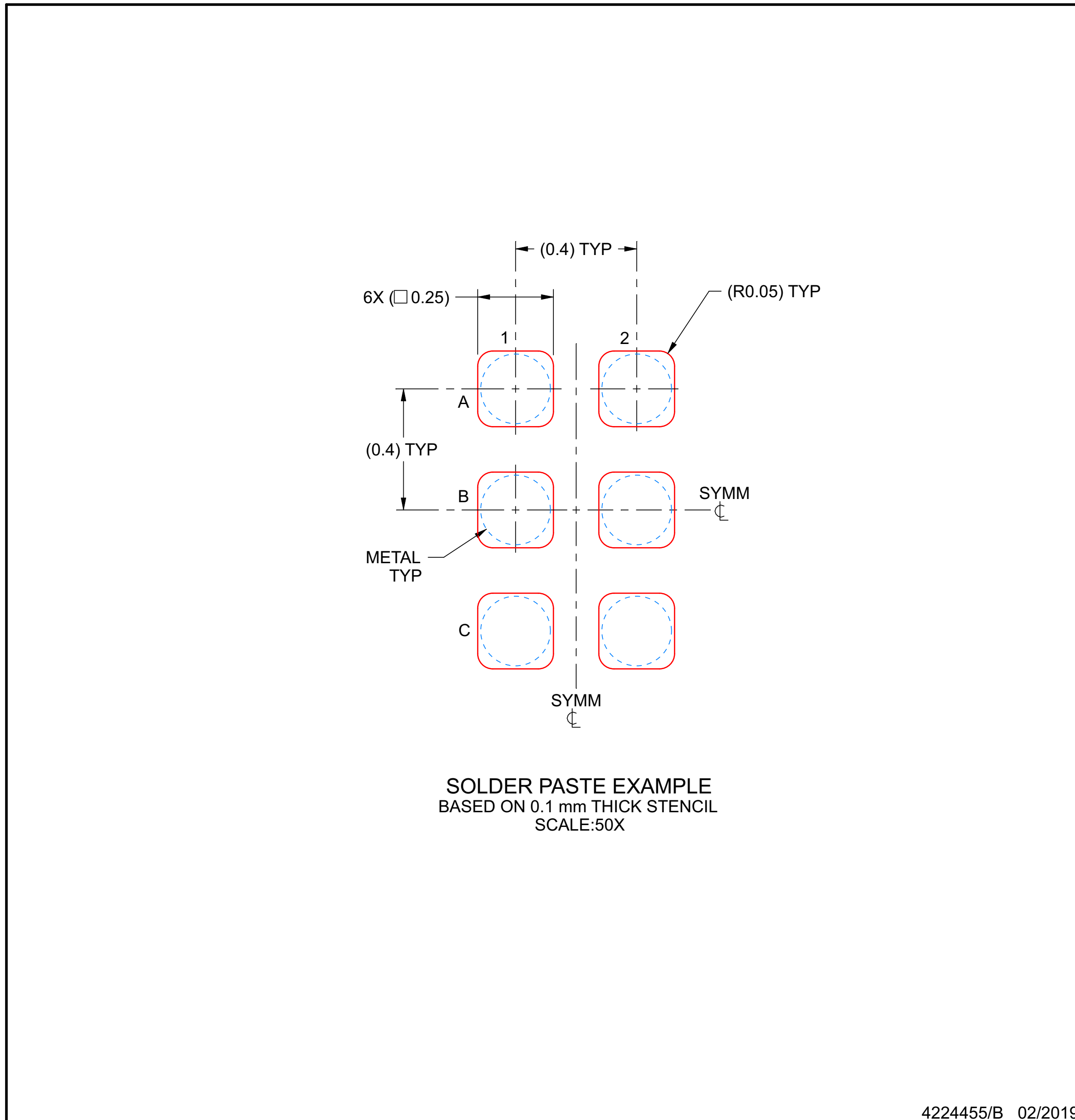
EXAMPLE STENCIL DESIGN

YFP0006-C01 DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS6283810YFPR	ACTIVE	DSBGA	YFP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1DU	Samples
TPS6283810YFPT	ACTIVE	DSBGA	YFP	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1DU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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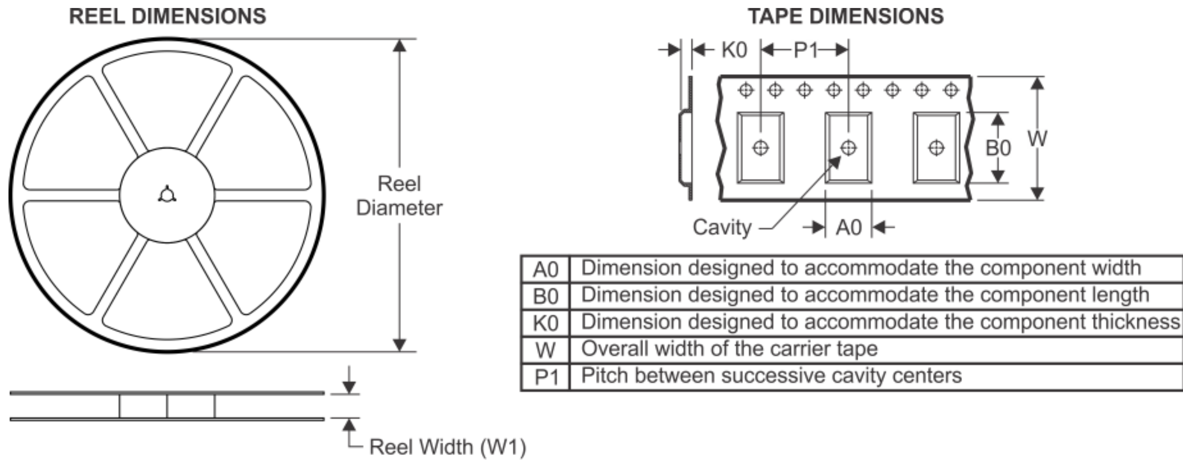
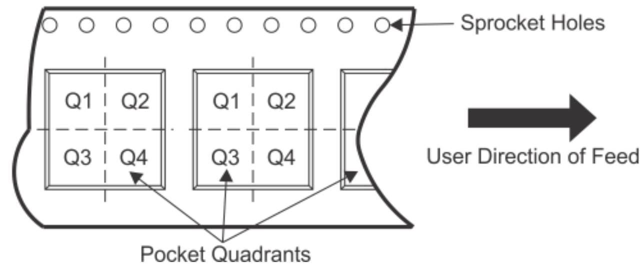
TAPE AND REEL INFORMATION



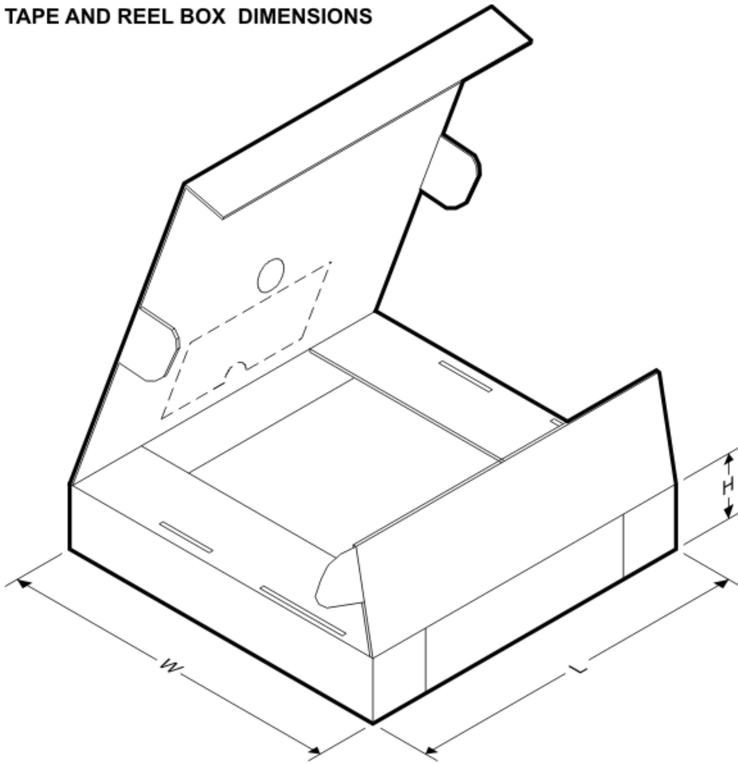
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6283810YFPR	DSBGA	YFP	6	3000	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1
TPS6283810YFPT	DSBGA	YFP	6	250	180.0	8.4	0.9	1.3	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

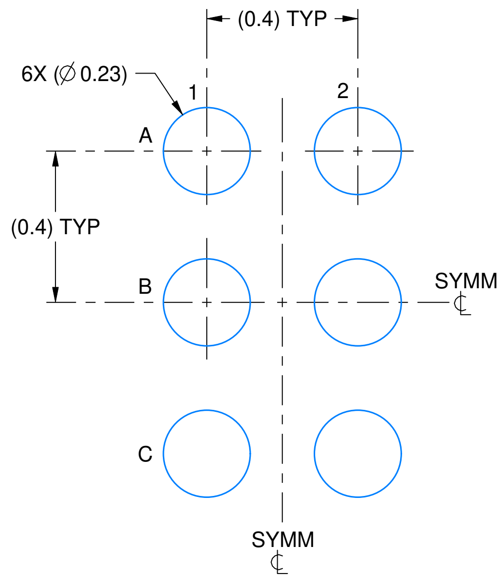


*All dimensions are nominal

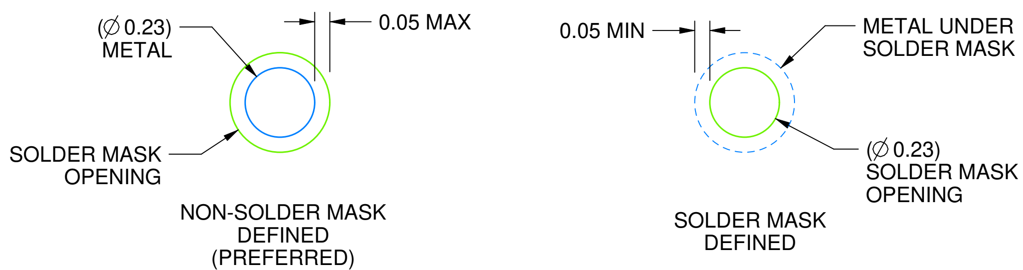
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6283810YFPR	DSBGA	YFP	6	3000	182.0	182.0	20.0
TPS6283810YFPT	DSBGA	YFP	6	250	182.0	182.0	20.0

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

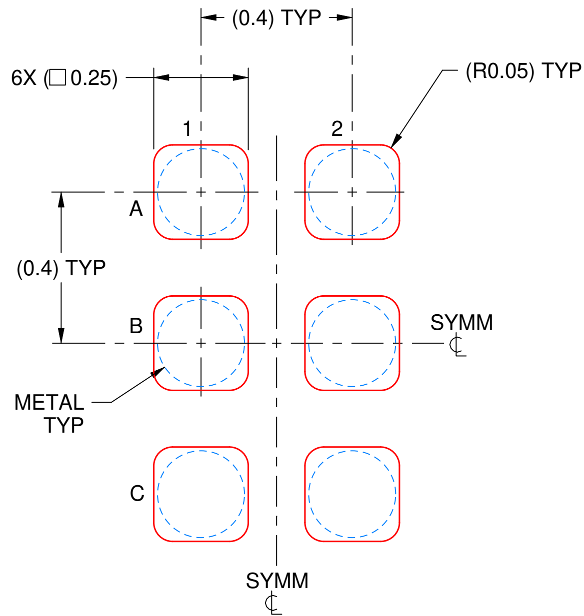


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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