ISL1539A

Dual Port VDSL2 Line Driver

FN6916
Rev 0.00
September 23, 2009

The ISL1539A provides 4 internal wideband op amps intended to be used as two pairs of differential line drivers. The ISL1539A's high bandwidth, 240MHz, and ultra low distortion, -89dBc @ 1MHz, $2V_{P-P}$, support the demanding MTPR requirements of emerging VDSL2 line driver designs. Less demanding requirements can be met at very low quiescent powers using the supply current adjustment features.

Each of the 4 internal op amps is a wideband current feedback amplifier offering very high slew rate intrinsic to that design using low quiescent current levels. Each of the two pair of amplifiers (ports) can also be power optimized to the application using two external quiescent control logic pins. Full power is nominally 27.2mA/port with options of medium power cutback to 23mA/port, a low power condition at 13.5mA/port, and an off state at <0.5mA/port. Added quiescent power flexibility is provided through an external I_{ADJ} pin. Grounding the pin gives the nominal currents listed above while inserting a resistor from this pin to ground can be used to scale each of the settings downward.

High power push/pull line driver applications as illustrated in the example below are best supported using a low headroom, high output current device. On ±12V supplies, the ISL1539A offers a 1.1V headroom with >360mA peak output current. Driving differentially this gives >$41.8V_{P-P}$ swing to as low as 58Ω differential load. High SFDR operation is also supported for supplies as low as ±7.5V. Intended to be used as differential pairs, this two port device includes special circuitry to minimize common mode loop peaking while also reducing the common mode output noise spectrum. That circuitry links the two sides of each port, precluding their application as individual amplifiers.

Features

- 360mA Output Drive Capability
- $41.8V_{P-P}$ Differential Output Drive into 100Ω
- -89dBc THD @ 1MHz $2V_{P-P}$
- -65dBc MTPR (VDSL 8b Profile)
- High Slew Rate of 3000V/µs Differential
- Bandwidth (240MHz @ A_{V-DIFF} = 10)
- Supply Current Control Pins
- Port Separation
  - 78dB @ 500kHz
  - 70dB @ 1MHz
  - 60dB @ 4MHz
- Pb-Free (RoHS Compliant)

Applications* (see page 21)

- 8MHz and 17MHz VDSL2 Profiles
- ADSL2+

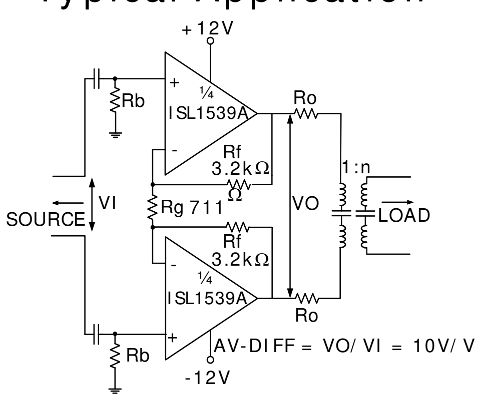
Related Literature (see Device Info page)

- AN1325 "Choosing and Using Bypass Capacitors"
- TB426 "Characterization of the Output Protection Circuitry of the EL1528 DSL Driver for Lightning Surges"

TABLE 1. ALTERNATE SOLUTIONS

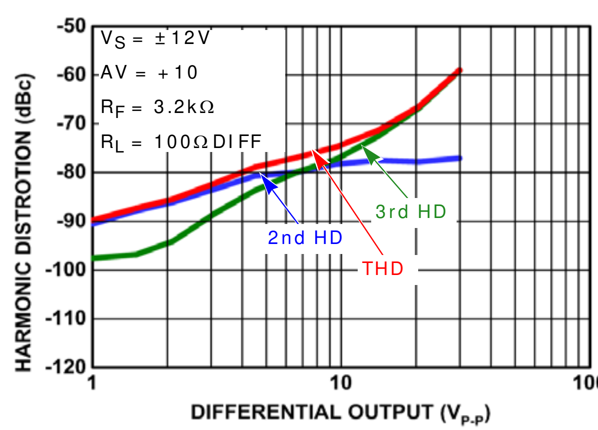
PART #	NOMINAL ±V_{CC} (V)	BANDWIDTH (MHz)	APPLICATIONS
ISL1557	±6	200	VDSL
ISL1534	±12	40	ADSL2+
ISL1536	±12	50	ADSL2+

Typical Application

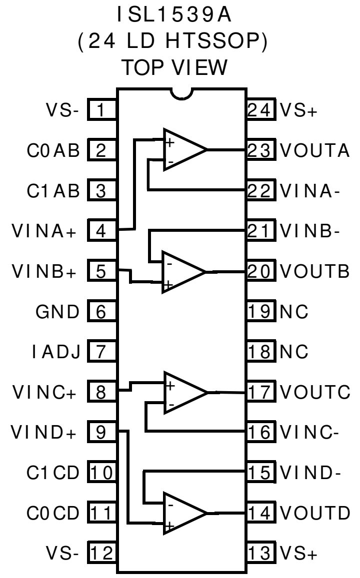


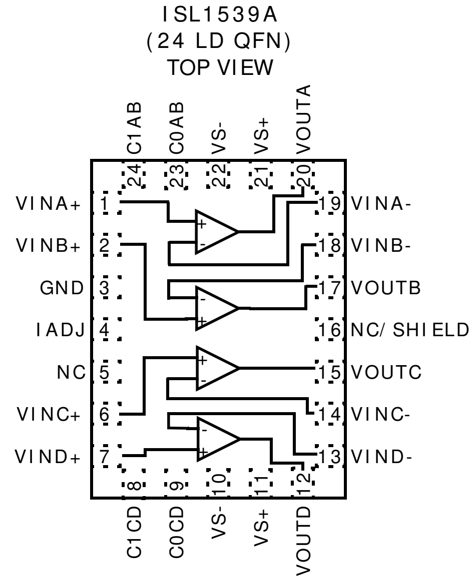
TYPICAL DIFFERENTIAL I/O LINE DRIVER
(1 OF 2 PORTS)

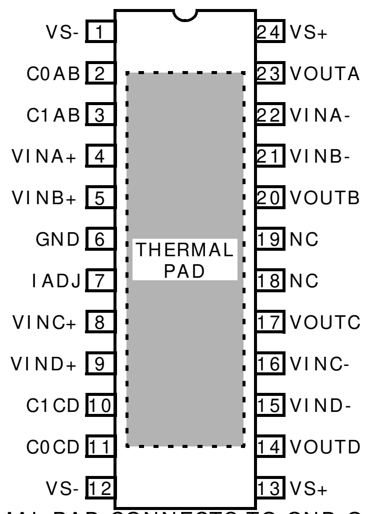
4MHz Harmonic Distortion



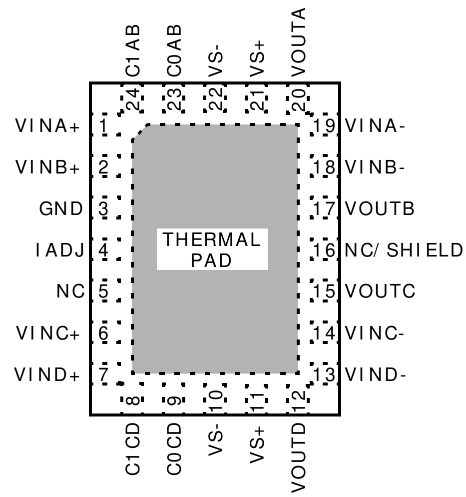
Pin Configurations







THERMAL PAD CONNECTS TO GND OR $-V_S$



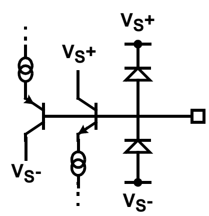
THERMAL PAD CONNECTS TO GND OR $-V_S$

Pin Descriptions

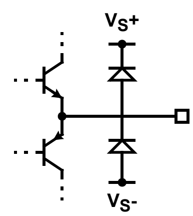
ISL1539AIR (24 Ld QFN)	ISL1539AIV (24 Ld HTSSOP)	PIN NAME	FUNCTION	CIRCUIT
1	4	VINA+	Amplifier A non-inverting input	(Refer to Circuit 1)
2	5	VINB+	Amplifier B non-inverting input	(Refer to Circuit 1)
3	6	GND	Ground connection	
4	7	IADJ	Supply current control pin for both DSL Port #1 and #2	(Refer to Figure 46)
5	18, 19	NC	Not connected	
6	8	VINC+	Amplifier C non-inverting input	(Refer to Circuit 1)
7	9	VIND+	Amplifier D non-inverting input	(Refer to Circuit 1)
8	10	C1CD	DSL Port #2 current control pin	(Refer to Figure 46)
9	11	C0CD	DSL Port #2 current control pin	(Refer to Figure 46)
10, 22	1, 12	VS-	Negative supply	
11, 21	13, 24	VS+	Positive supply	
12	14	VOUTD	Amplifier D output	(Refer to Circuit 2)

Pin Descriptions (Continued)

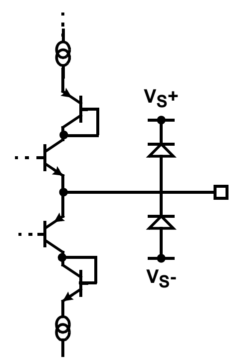
ISL1539AIR (24 Ld QFN)	ISL1539AIV (24 Ld HTSSOP)	PIN NAME	FUNCTION	CIRCUIT
13	15	VIND-	Amplifier D Inverting Input	(Refer to Circuit 3)
14	16	VINC-	Amplifier C Inverting Input	(Refer to Circuit 3)
15	17	VOUTC	Amplifier C output	(Refer to Circuit 2)
16	18, 19	NC/SHIELD	Not Connected	
17	20	VOUTB	Amplifier B output	(Refer to Circuit 2)
18	21	VINB-	Amplifier B Inverting Input	(Refer to Circuit 3)
19	22	VINA-	Amplifier A Inverting Input	(Refer to Circuit 3)
20	23	VOUTA	Amplifier A output	(Refer to Circuit 2)
23	2	C0AB	DSL Port #1 current control pin	(Refer to Figure 46)
24	3	C1AB	DSL Port #1 current control pin	(Refer to Figure 46)
-	-	THERMAL PAD	Connects to GND or -V_S	



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

PART NUMBER	PART MARKING	OPERATING AMBIENT TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL1539AIRZ (Note 2)	1539A IRZ	-40 to +85	24 Ld QFN	L24.4x5B
ISL1539AIRZ-T13 (Notes 1, 2)	1539A IRZ	-40 to +85	24 Ld QFN	L24.4x5B
COMING SOON ISL1539AIVEZ (Note 2)	1539A IVEZ	-40 to +85	24 Ld HTSSOP	MDP0048
COMING SOON ISL1539AIVEZ-T13 (Notes 1, 2)	1539A IVEZ	-40 to +85	24 Ld HTSSOP	MDP0048

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL1539A. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

V_S+ to V_S- Supply Voltage . . . . -0.3V to +26.4V
V_S+ Voltage to GND . . . . -0.3V to +26.4V
V_S- Voltage to GND . . . . -26.4V to +0.3V
Driver V_{IN}+ Voltage . . . . V_S- to V_S+
C_0, C_1 Voltage to GND . . . . -0.3V to +6V
I_{ADJ} Voltage to GND . . . . -1V to +4V
ESD Rating
Machine Model 200V
Human Body Model (Per MIL-STD-883 Method 3015.7). . 3kV
Charge Device Model 1.5kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN Package (Notes 4, 5)	39	4.5
24 Ld HTSSOP Package (Notes 4, 5)	TBD	TBD

Maximum Junction Temperature (Plastic Package). . . +150°C
Current into any Input 8mA
Continuous Output Current for Long Term Reliability 50mA
Power Dissipation. . . . . See Figure 42
Storage Temperature Range . . . . -40°C to +150°C
Pb-Free Reflow Profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Temperature Range . . . .-40°C to +85°C
Junction Temperature Range . . . .-40°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. QFN and HTSSOP exposed pad soldered to PCB per JESD51-5. See Tech Brief TB379 for details.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = ±12V, R_L= 100Ω differential, I_{ADJ} = C_0 = C_1 = 0V, A_V = 10V/V, R_F = 3.2kΩ, T_A = +25°C. Amplifier pairs tested separately unless otherwise indicated.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Small Signal Bandwidth	V_O < $2V_{P-P-DIFF}$, A_V = 10		240		MHz
		V_O < $2V_{P-P-DIFF}$ (Note 6)		120		MHz
	-3dB Large Signal Bandwidth	V_O = $10V_{P-P-DIFF}$		100		MHz
SR	20% to 80%	V_O = $32V_{P-P-DIFF}$	2000	3000		V/µs
200kHz Harmonic Distortion	2nd Harmonic	V_{OUT} = $10V_{P-P-DIFF}$		-93		dBc
	3rd Harmonic	V_{OUT} = $10V_{P-P-DIFF}$		-90		dBc
	THD	V_{OUT} = $10V_{P-P-DIFF}$		-88		dBc
1MHz Harmonic Distortion	2nd Harmonic	V_{OUT} = $2V_{P-P-DIFF}$		-91		dBc
	3rd Harmonic	V_{OUT} = $2V_{P-P-DIFF}$		-109		dBc
	THD	V_{OUT} = $2V_{P-P-DIFF}$		-91		dBc
8MHz Harmonic Distortion	2nd Harmonic	V_{OUT} = $2V_{P-P-DIFF}$		-87		dBc
	3rd Harmonic	V_{OUT} = $2V_{P-P-DIFF}$		-95		dBc
	THD	V_{OUT} = $2V_{P-P-DIFF}$		-86		dBc
MTPR	Multi-Tone Power Ratio	26kHz to 8MHz, 4kHz Tone Spacing, P_{LINE} = 19dBm, VDSL2+ 8b (Note 6)		-70		dBc
200kHz Harmonic Distortion	2nd Harmonic	V_{OUT} = $10V_{P-P-DIFF}$ (Note 6)		-93		dBc
	3rd Harmonic	V_{OUT} = $10V_{P-P-DIFF}$ (Note 6)		-90		dBc
	THD	V_{OUT} = $10V_{P-P-DIFF}$ (Note 6)		-88		dBc

Electrical Specifications $V_S = \pm 12V$, $R_L = 100\Omega$ differential, $I_{ADJ} = C_0 = C_1 = 0V$, $A_V = 10V/V$, $R_F = 3.2k\Omega$, $T_A = +25°C$. Amplifier pairs tested separately unless otherwise indicated. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
4MHz Harmonic Distortion	2nd Harmonic	$V_{OUT} = 10V_{P-P-DIFF}$ (Note 6)		-72		dBc
	3rd Harmonic	$V_{OUT} = 10V_{P-P-DIFF}$ (Note 6)		-70		dBc
	THD	$V_{OUT} = 10V_{P-P-DIFF}$ (Note 6)		-68		dBc
8MHz Harmonic Distortion	2nd Harmonic	$V_{OUT} = 2V_{P-P-DIFF}$ (Note 6)		-83		dBc
	3rd Harmonic	$V_{OUT} = 2V_{P-P-DIFF}$ (Note 6)		-78		dBc
	THD	$V_{OUT} = 2V_{P-P-DIFF}$ (Note 6)		-76		dBc
e_N	Non-Inverting Input Voltage Noise at each of the 4 Inputs	f = 1MHZ		4.0		$nV/\sqrt{Hz}$
$+i_N$	Non-Inverting Input Current Noise at each of the 4 Inputs	f = 1MHZ		2.7		$pA/\sqrt{Hz}$
$-i_N$	Inverting Input Current Noise at each of the 4 Inputs	f = 1MHZ		23		$pA/\sqrt{Hz}$
e_{N-CM}	Common Mode Output Noise at each Port Pair	f = 1MHZ		90		$nV/\sqrt{Hz}$
POWER CONTROL FEATURES						
V_{IH}	Logic High Voltage	C_0 and C_1 inputs	2.0			V
V_{IL}	Logic Low Voltage	C_0 and C_1 inputs			0.8	V
I_{IH0}, I_{IH1}	Logic High Current for C_0, C_1	$C_0 = 3.3V$, $C_1 = 3.3V$	-5	1	+5	µA
I_{IL0}, I_{IL1}	Logic Low Current for C_0 or C_1	$C_0 = 0V$, $C_1 = 0V$	-17	-13	-10	µA
I_{ADJ}	Input Resistance			500		Ω
SUPPLY CHARACTERISTICS						
	Maximum Operating Supply Voltage			±12.6		V
	Minimum Operating Supply Voltage			±7.5		V
I_{GND}	GND Pin Current per Port	All outputs at 0V (Note 7)	0.2	0.4	0.5	mA
I_{S+} (Full Power)	Positive Supply Current per Port	All outputs at 0V, $C_0 = C_1 = 0V$, No Load	21	27.2	31.5	mA
I_{S+} (Medium)	Positive Supply Current per Port	All outputs at 0V, $C_0 = 3.3V$, $C_1 = 0V$, No Load	17.8	23	26.7	mA
I_{S+} (Low)	Positive Supply Current per Port	All outputs at 0V, $C_0 = 0V$, $C_1 = 3.3V$, No Load	10.4	13.5	15.6	mA
I_{S+} (Power-down)	Positive Supply Current per Port	All outputs at 0V, $C_0 = C_1 = 3.3V$, No Load	0.2	0.4	0.5	mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output Swing	R_{L-DIFF} = No Load	±10.7	±10.9		V
	Lightly Loaded Positive Swing	$R_{L-DIFF} = 100\Omega$	+10.3	+10.5		V
	Lightly Loaded Negative Swing	$R_{L-DIFF} = 100\Omega$		-10.4	-10.2	V
	Heavy Loaded Positive Swing	$R_{L-DIFF} = 60\Omega$	+9.4	+9.8		V
	Heavy Loaded Negative Swing	$R_{L-DIFF} = 60\Omega$		-9.7	-9.3	V
I_{OL}	Linear Output Current	$R_L = 25\Omega$, f = 100kHz, THD = -60dBc		±360		mA

Electrical Specifications

V_S = ±12V, R_L= 100Ω differential, I_{ADJ} = C_0 = C_1 = 0V, A_V = 10V/V, R_F = 3.2kΩ, T_A = +25°C. Amplifier pairs tested separately unless otherwise indicated. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_{OUT}	Peak Output Current	V_{OUT} = ±1V, R_L = 1Ω		±600		mA
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage		-8	+3.5	+8	mV
ΔV_{OS}	Input V_{OS} Mismatch Between Amplifiers for Each Port		-2	0	+2	mV
$V_{OS, DRIFT}$	Input V_{OS} Drift	-25°C to +125°C T_J		±15		µV/°C
I_{B+}	Non-Inverting Input Bias Current		-8		+8	µA
ΔI_{B+}	Non-Inverting I_{B+} Mismatch Between Amplifiers for Each Port		-2		+2	µA
$I_{B+, DRIFT}$	Non-Inverting I_{B+} Drift	-25°C to +125°C T_J		±12		nA/°C
I_{B-}	Inverting Input Bias Current		-75		+75	µA
ΔI_{B-}	Inverting I_{B-} Mismatch Between Amplifiers for Each Port		-35		+35	µA
$I_{B-, DRIFT}$	Inverting I_{B-} Drift	-25°C to +125°C T_J		±25		nA/°C
CMIR	Common Mode Input Range at each of the 4 Non-Inverting Input Pins			±7.5		V
CMRR	Common Mode Rejections for each Port. V_{CM} = -5V to +5V	V_{CM} to Differential Mode Output (Input Referred)		80		dB
		V_{CM} to Commonl Mode Output (Output Referred)		43		dB
PSRR	Power Supply Rejections for each Port to Differential Output (Input Referred)	$+V_S$ = +7.5V to +12V, $-V_S$ = -12V		97		dB
		$-V_S$ = -7.5V to -12V, $+V_S$ = +12V		92		dB
	Power Supply Rejections for each Port to Common Mode Output (Output Referred)	$+V_S$ = +7.5V to +12V, $-V_S$ = -12V		51		dB
		$-V_S$ = -7.5V to -12V, $+V_S$ = +12V		45		dB

NOTES:

6. Active Termination Test Circuit. Low Power Mode (see Figure 45).
7. The $-V_S$ supply current is the $+V_S$ supply current minus the ground current, except power down condition.

Typical Performance Curves

V_{CC} = ±12V, R_F = 3.2kΩ, G_D = 10V/V (differential), R_{LOAD} = 100Ω, $T_A \approx$ +25°C, C0 = C1 = I_{ADJ} = 0V (full power), unless otherwise noted.

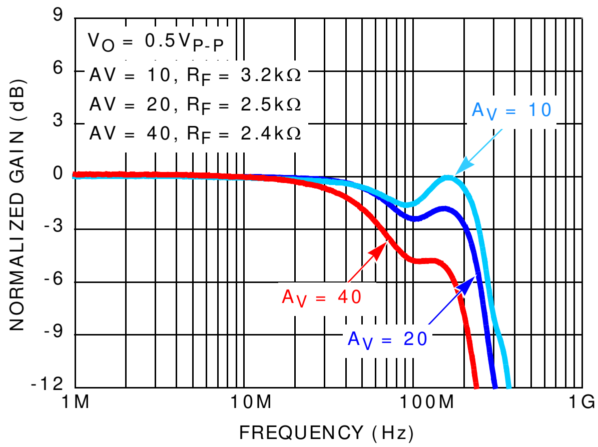


FIGURE 1. SMALL SIGNAL FREQUENCY RESPONSE vs GAIN

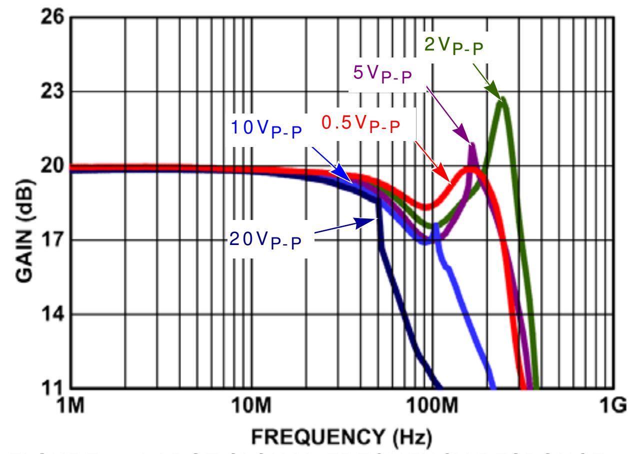


FIGURE 2. LARGE SIGNAL FREQUENCY RESPONSE

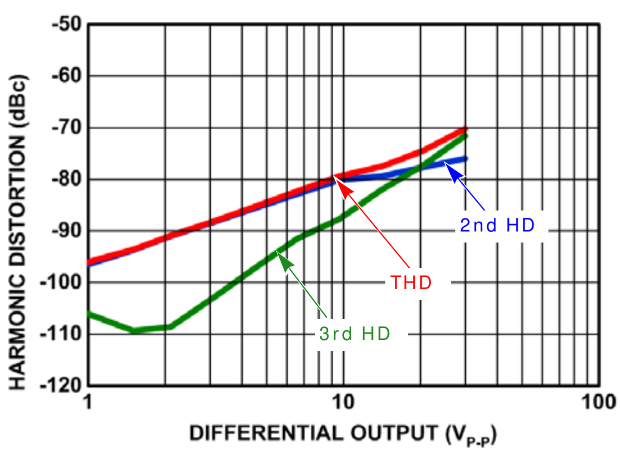


FIGURE 3. 1MHz HARMONIC DISTORTION vs OUTPUT SWING

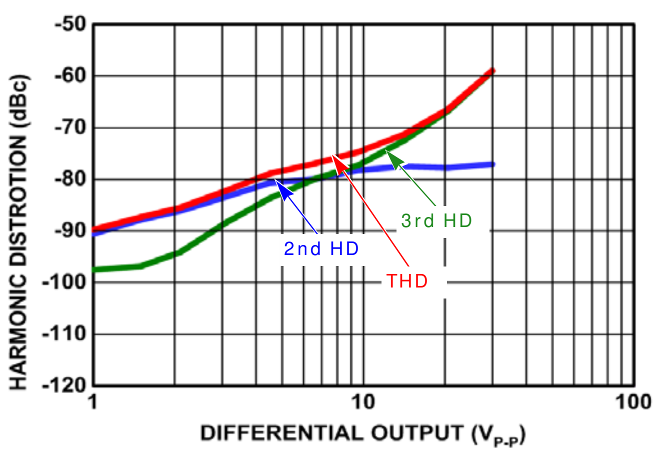


FIGURE 4. 4MHz HARMONIC DISTORTION vs OUTPUT SWING

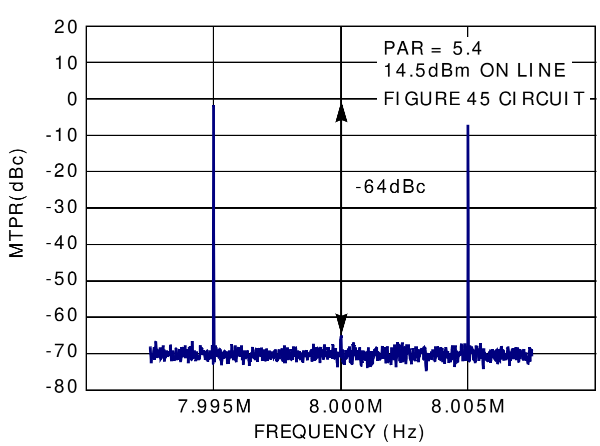


FIGURE 5. 17MHz DMT PROFILE

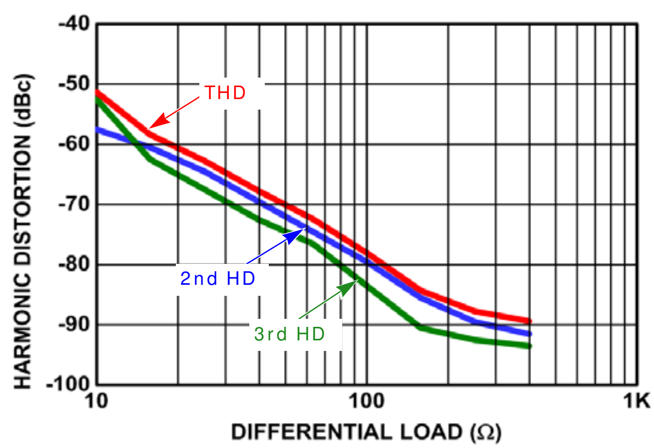


FIGURE 6. 4MHz HARMONIC DISTORTION vs LOAD

Typical Performance Curves

V_{CC} = ±12V, R_F = 3.2kΩ, G_D = 10V/V (differential), R_{LOAD} = 100Ω, T_A ≈ +25°C, C0 = 3.3V, C1 = I_{ADJ} = 0V (medium power), unless otherwise noted.

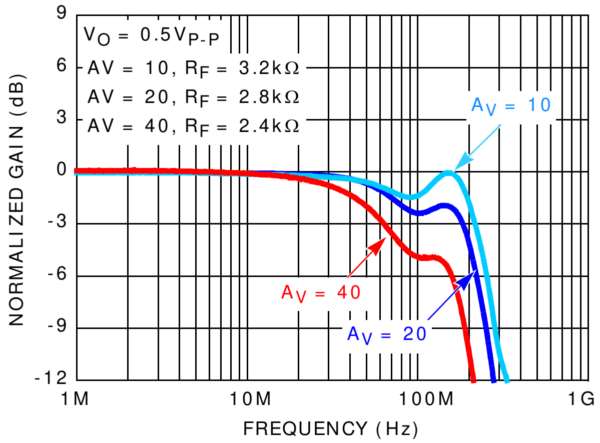


FIGURE 7. SMALL SIGNAL FREQUENCY RESPONSE vs GAIN

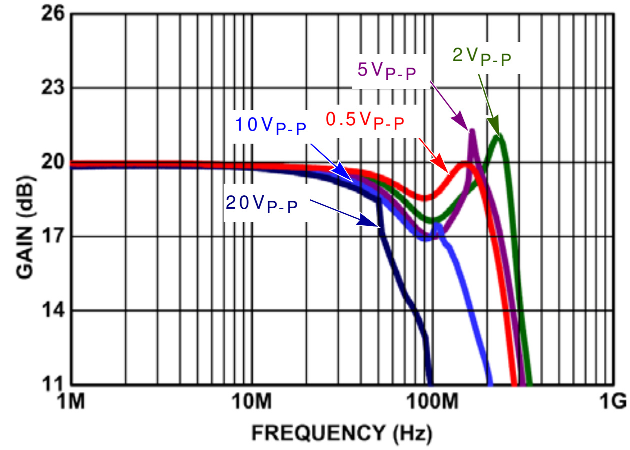


FIGURE 8. LARGE SIGNAL FREQUENCY RESPONSE

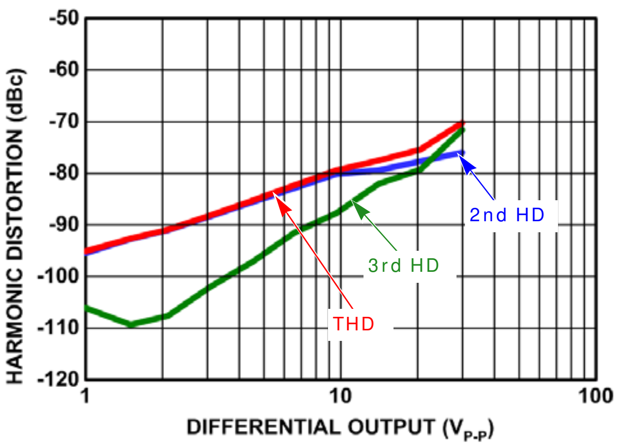


FIGURE 9. 1MHz HARMONIC DISTORTION vs OUTPUT SWING

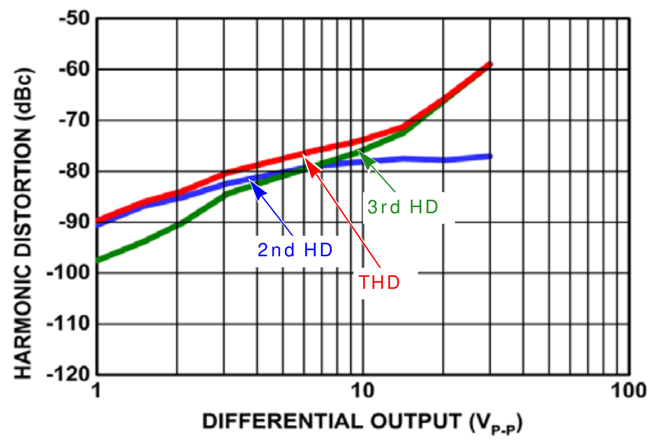


FIGURE 10. 4MHz HARMONIC DISTORTION vs OUTPUT SWING

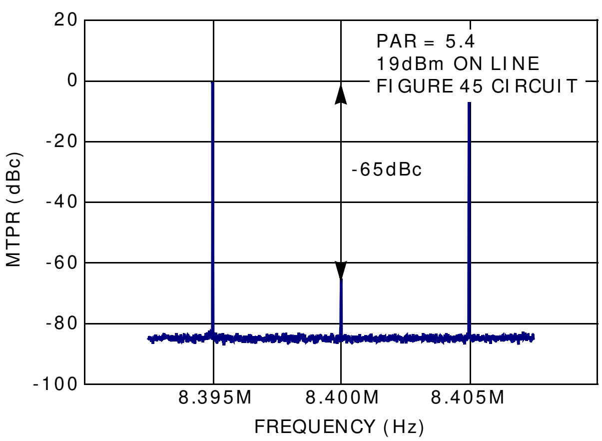


FIGURE 11. VDSL2+ 8MHz DMT PROFILE

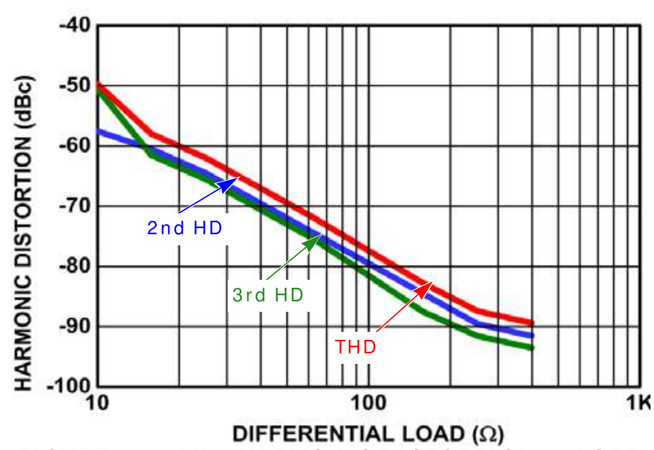


FIGURE 12. 4MHz HARMONIC DISTORTION vs LOAD

Typical Performance Curves

V_{CC} = ±12V, R_F = 3.2kΩ, G_D = 10V/V (differential), R_{LOAD} = 100Ω, $T_A \approx +25°C$, C1 = 3.3V, C0 = I_{ADJ} = 0V (low power), unless otherwise noted.

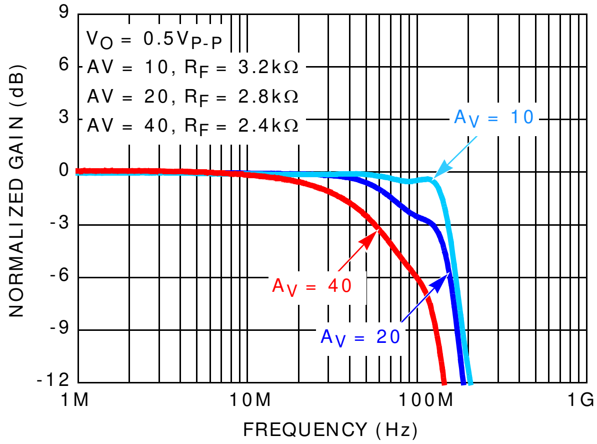


FIGURE 13. SMALL SIGNAL FREQUENCY RESPONSE vs GAIN

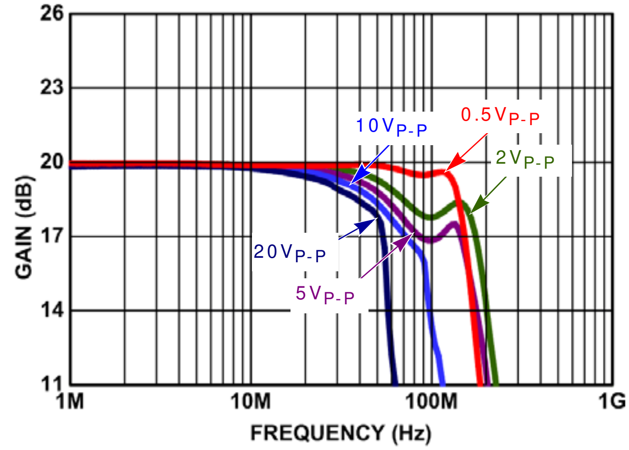


FIGURE 14. LARGE SIGNAL FREQUENCY RESPONSE

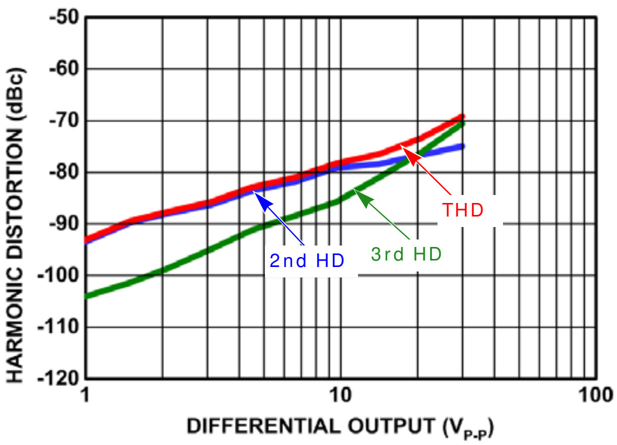


FIGURE 15. 1MHz HARMONIC DISTORTION vs OUTPUT SWING

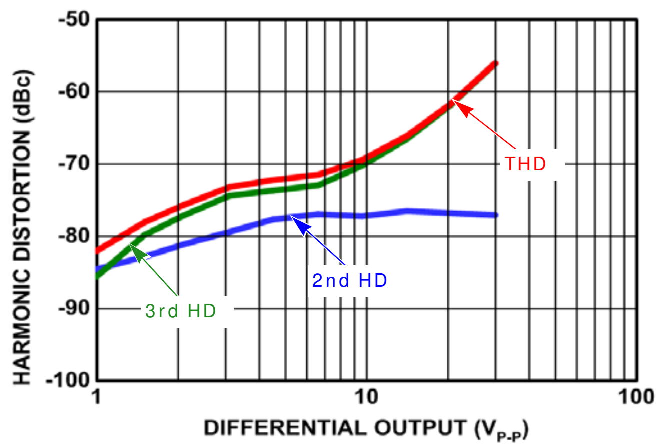


FIGURE 16. 4MHz HARMONIC DISTORTION vs OUTPUT SWING

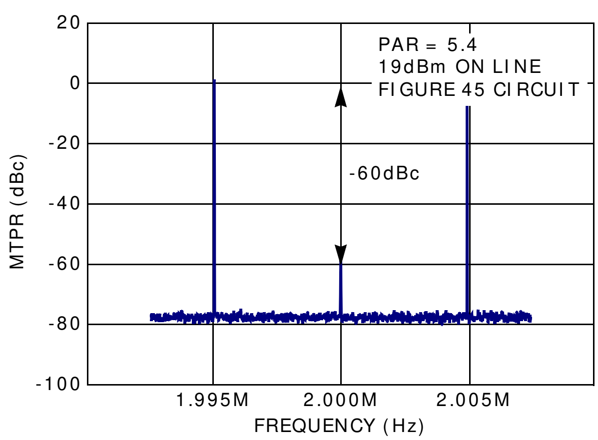


FIGURE 17. ADSL2+ DMT

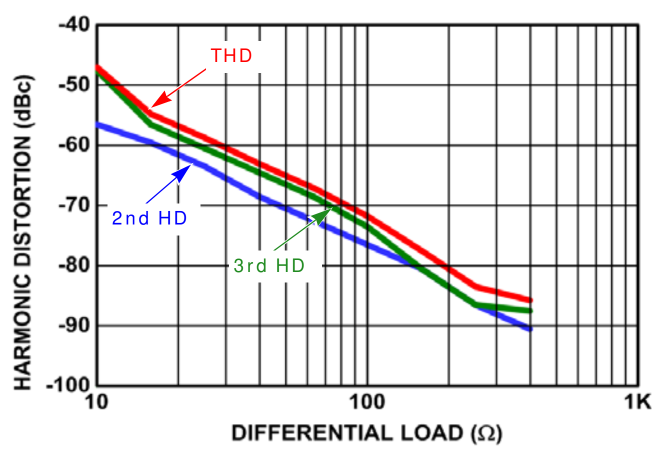


FIGURE 18. 4MHz HARMONIC DISTORTION vs LOAD

Typical Performance Curves

V_{CC} = ±12V, R_F = 3.2kΩ, G_D = 10V/V (differential), R_{LOAD} = 100Ω, $T_A \approx +25°C$, C0 = C1= I_{ADJ} = 0V (full power), unless otherwise noted.

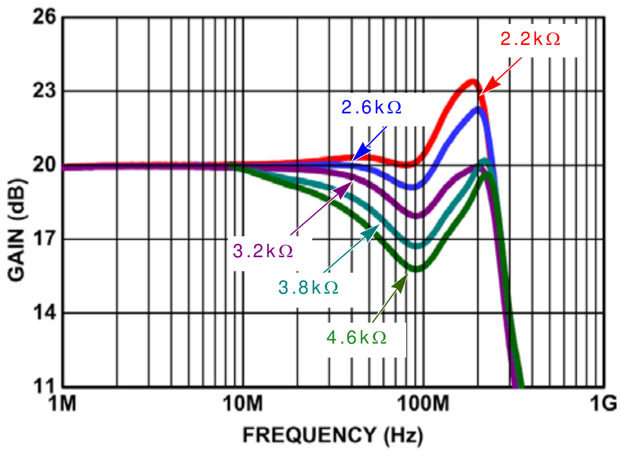


FIGURE 19. SMALL SIGNAL FREQUENCY RESPONSE vs RF

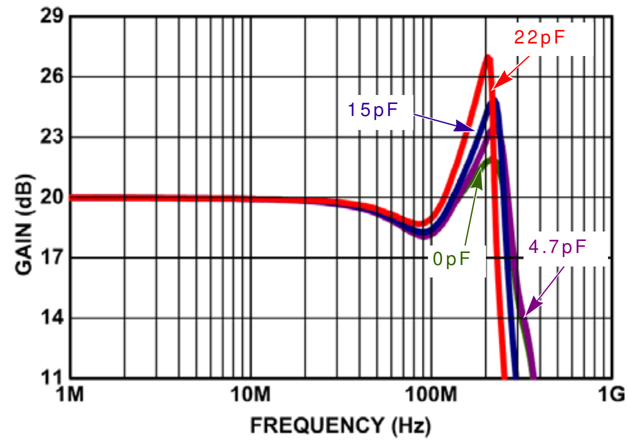


FIGURE 20. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LOAD}

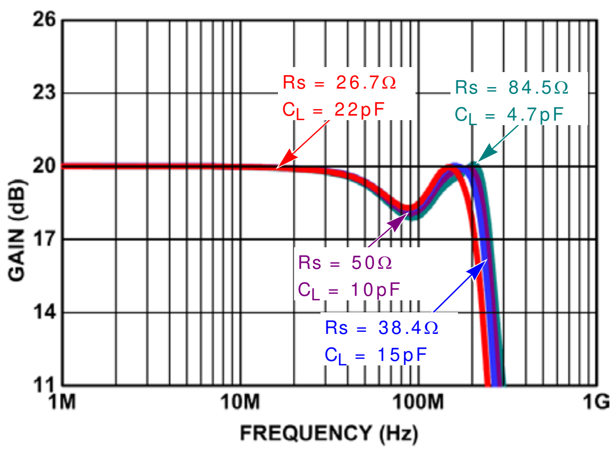


FIGURE 21. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LOAD} WITH Rs

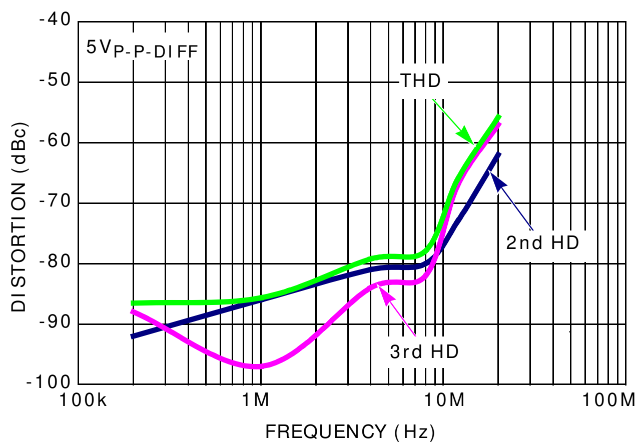


FIGURE 22. DISTORTION vs FREQUENCY

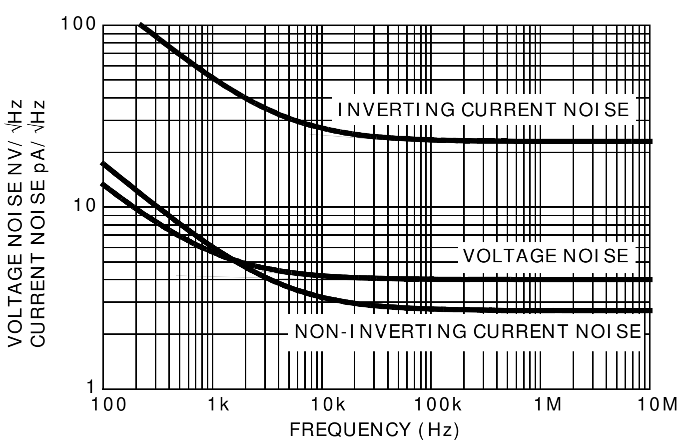


FIGURE 23. INPUT VOLTAGE AND CURRENT NOISE DENSITY

Typical Performance Curves

V_{CC} = ±12V, R_F = 3.2kΩ, G_D = 10V/V (differential), R_{LOAD} = 100Ω, T_A ≈ +25°C, C0 = 3.3V, C1 = I_{ADJ} = 0V (medium power), unless otherwise noted.

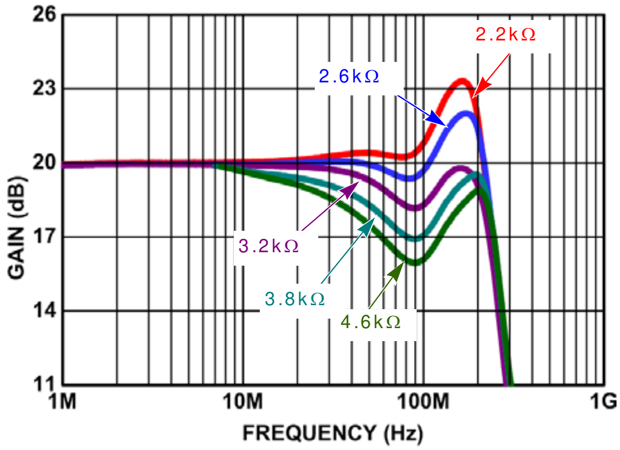


FIGURE 24. SMALL SIGNAL FREQUENCY RESPONSE vs RF

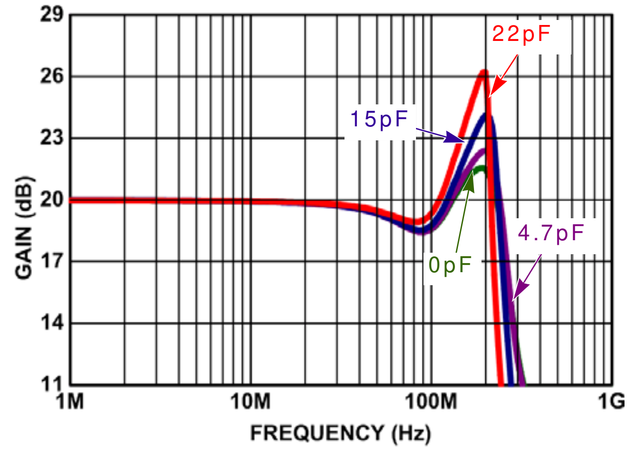


FIGURE 25. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LOAD}

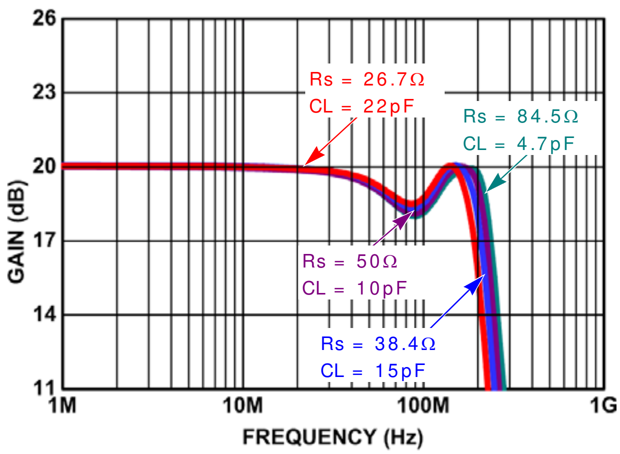


FIGURE 26. SMALL SIGNAL FREQUENCY RESPONSE vs CLOAD WITH Rs

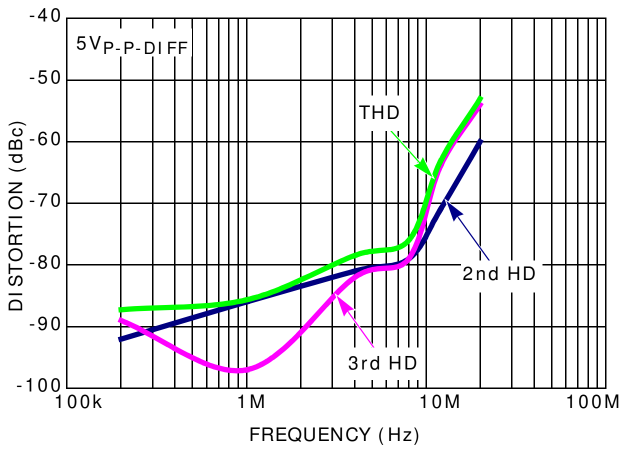


FIGURE 27. DISTORTION vs FREQUENCY

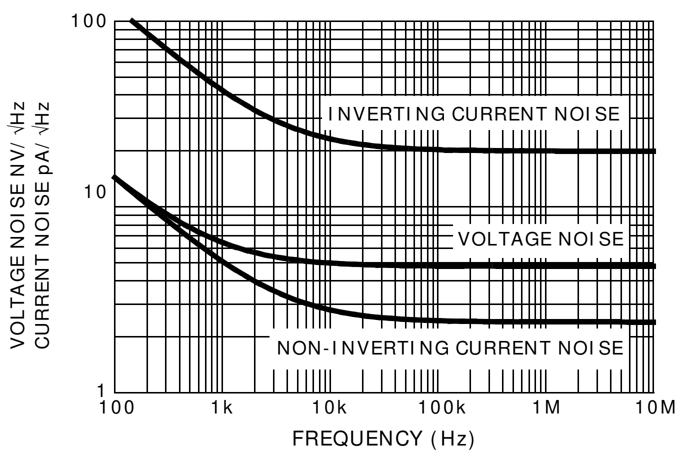


FIGURE 28. INPUT VOLTAGE AND CURRENT NOISE DENSITY

Typical Performance Curves

V_{CC} = ±12V, R_F = 3.2kΩ, G_D = 10V/V (differential), R_{LOAD} = 100Ω, T_A ≈ +25°C, C1 = 3.3V, C0 = I_{ADJ} = 0V (low power), unless otherwise noted.

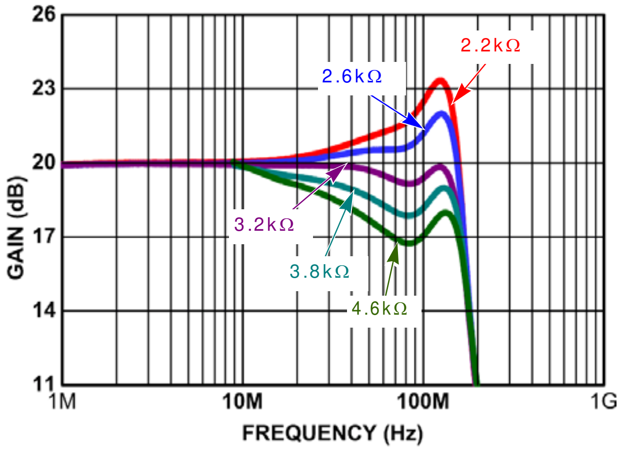


FIGURE 29. SMALL SIGNAL FREQUENCY RESPONSE vs RF

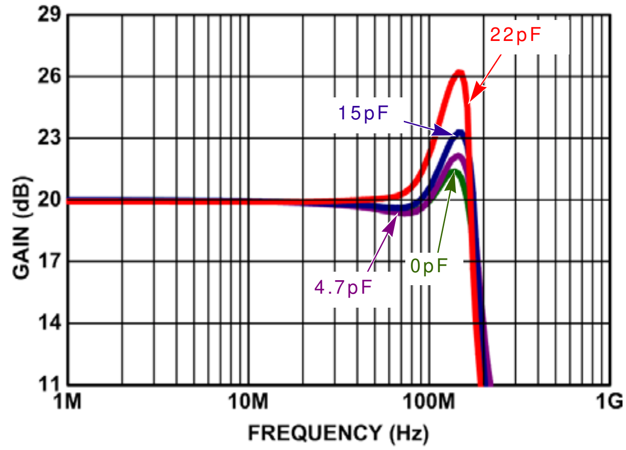


FIGURE 30. SMALL SIGNAL FREQUENCY RESPONSE vs CLOAD

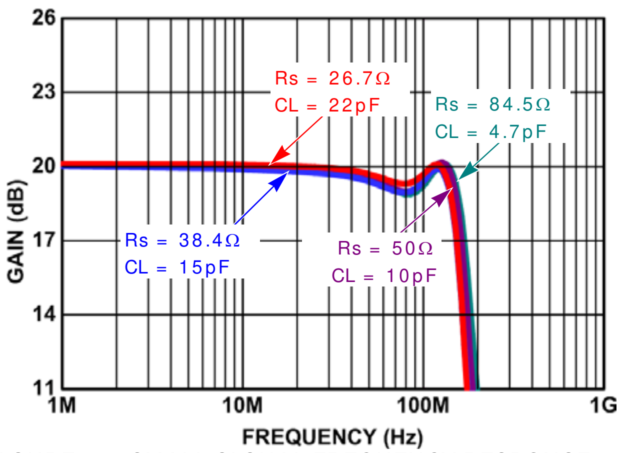


FIGURE 31. SMALL SIGNAL FREQUENCY RESPONSE vs CLOAD WITH Rs

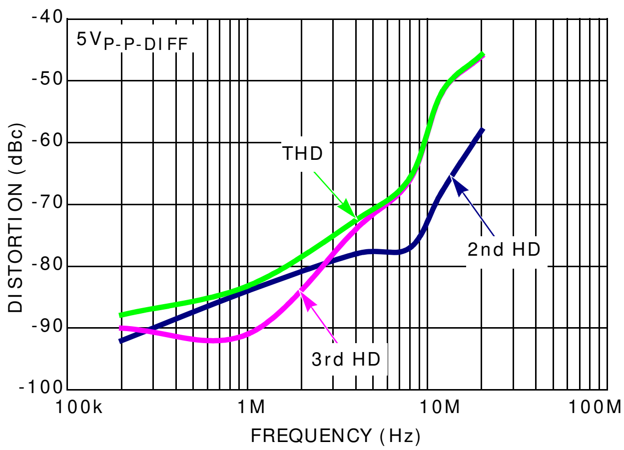


FIGURE 32. DISTORTION vs FREQUENCY

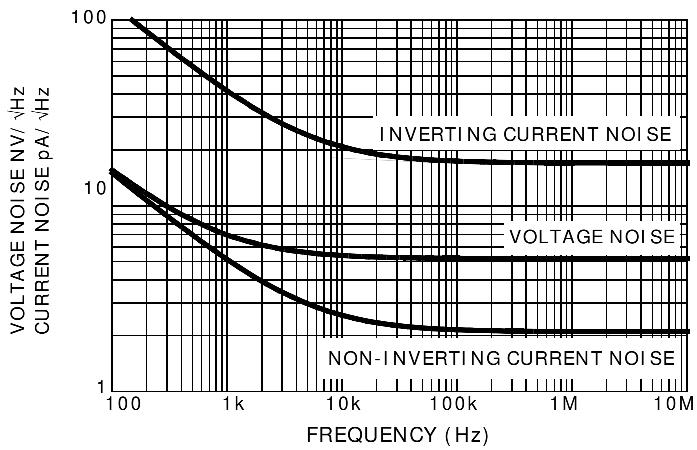


FIGURE 33. INPUT VOLTAGE AND CURRENT NOISE DENSITY

Typical Performance Curves

V_{CC} = ±12V, R_F = 3.2kΩ, G_D = 10V/V (differential), R_{LOAD} = 100Ω, T_A ≈ +25°C, C0 and C1 Parametric, unless otherwise noted.

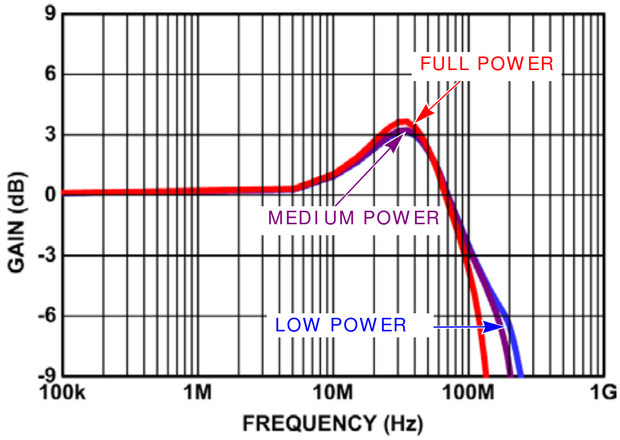


FIGURE 34. COMMON MODE SMALL SIGNAL FREQUENCY RESPONSE

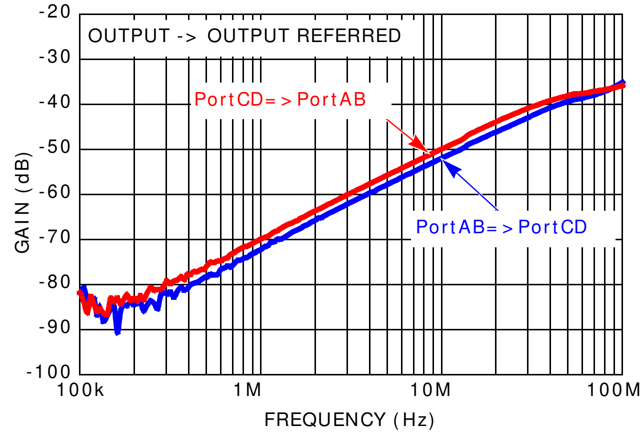


FIGURE 35. CHANNEL TO CHANNEL X-TALK

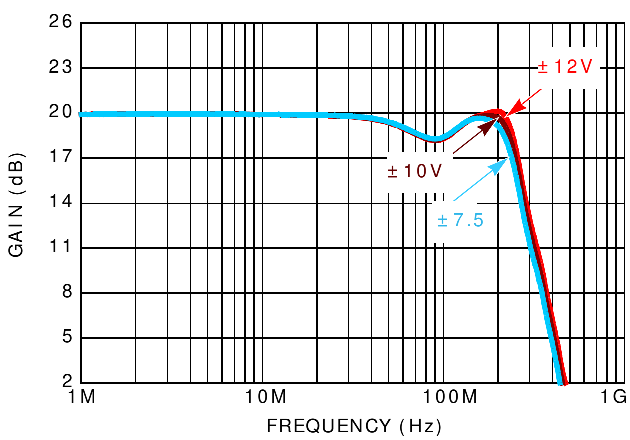


FIGURE 36. SMALL SIGNAL BANDWIDTH vs SUPPLY VOLTAGE

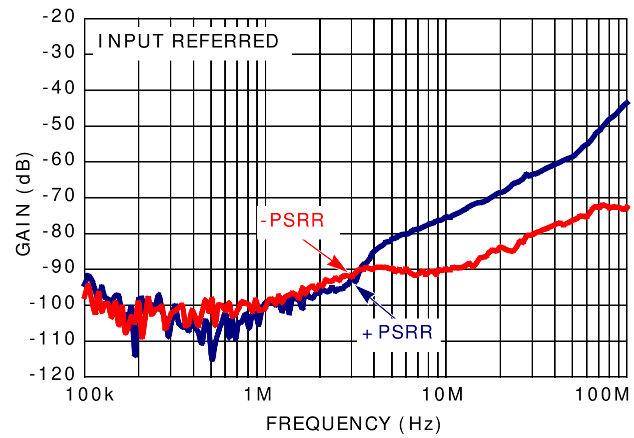


FIGURE 37. +PSRR TO DIFFERENTIAL OUTPUT

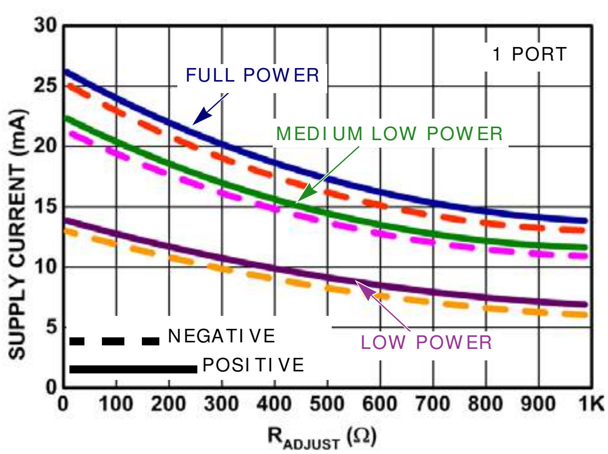


FIGURE 38. SUPPLY CURRENT vs R_{ADJ}

Typical Performance Curves

V_{CC} = ±12V, R_F = 3.2kΩ, G_D = 10V/V (differential), R_{LOAD} = 100Ω, T_A ≈ +25°C, I_{ADJ} = 0V, C0, C1 varied, unless otherwise noted.

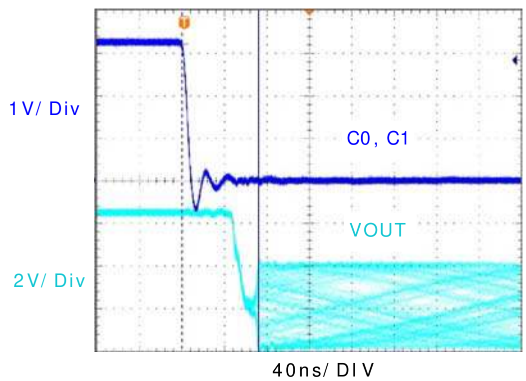


FIGURE 39. POWER-UP TIME

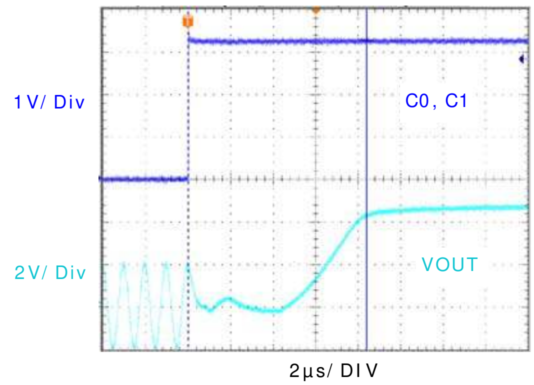


FIGURE 40. POWER-DOWN TIME

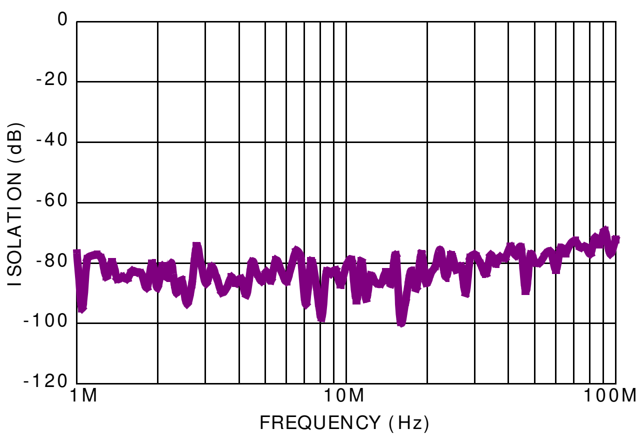


FIGURE 41. OFF-ISOLATION

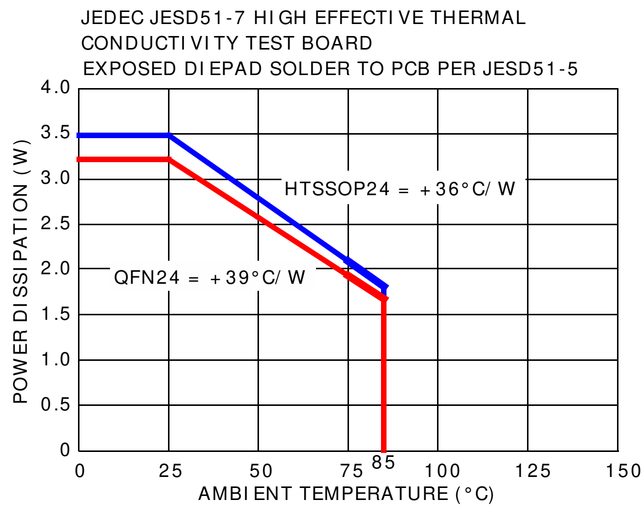


FIGURE 42. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Test Circuit

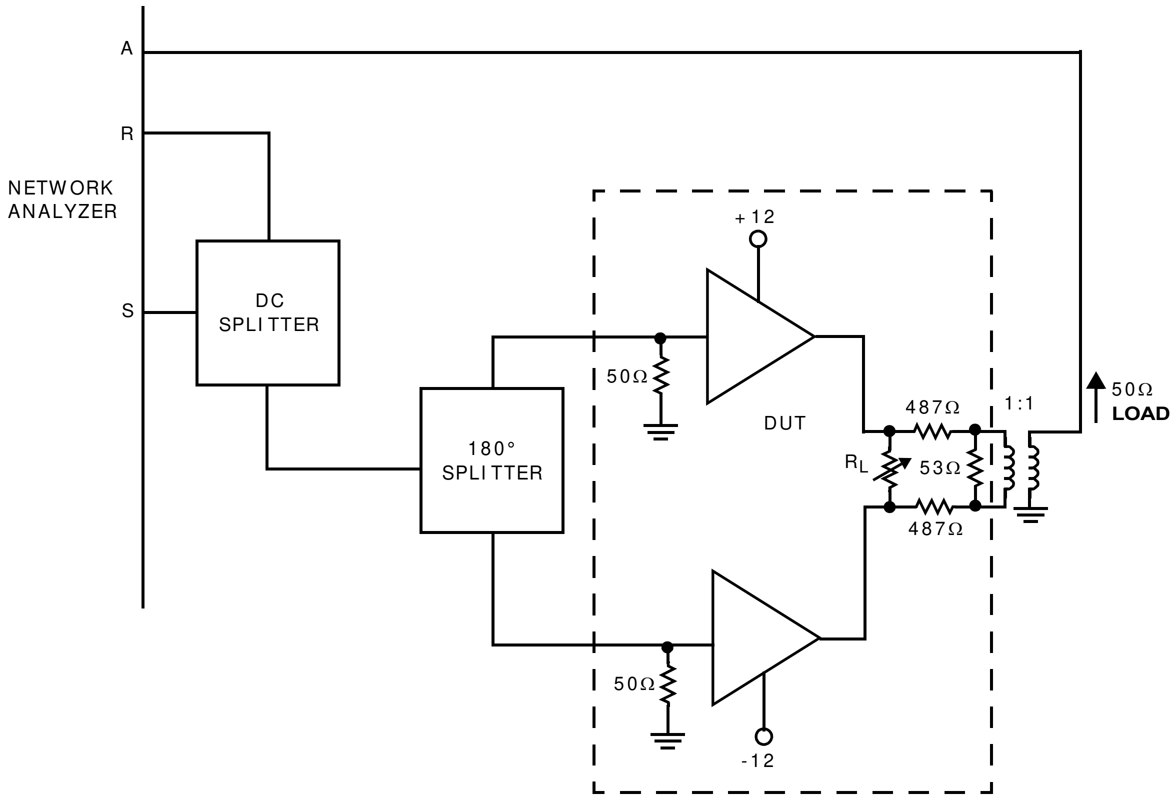


FIGURE 43. FREQUENCY RESPONSE CHARACTERIZATION CIRCUIT

Applications Information

Applying Wideband Current Feedback Op Amps as Differential Drivers

A current feedback amplifier (CFA) like the ISL1539A is particularly suited to the requirements of high output power, high full power bandwidth, differential drivers. This topology offers a very high slew rate on low quiescent power and the ability to hold relatively constant AC characteristics over a wide range of gains. The AC characteristics are principally set by the feedback resistor value in simple differential gain circuits as shown in Figure 44.

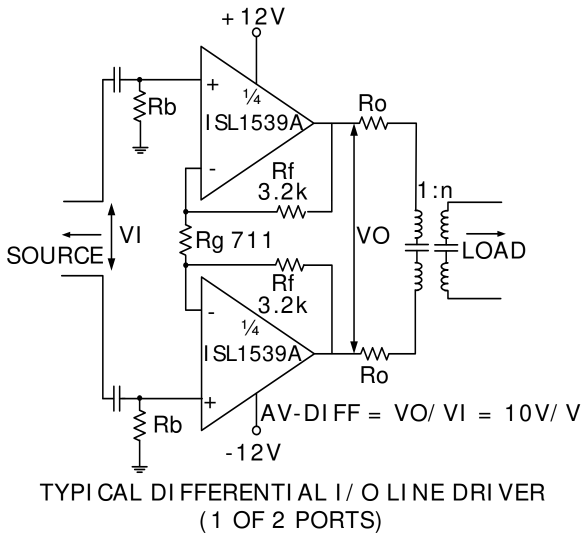


FIGURE 44. PASSIVE TERMINATION CIRCUIT

In this differential gain of 10 V/V circuit, the 3.2k feedback resistors are setting the bandwidth while the 711 gain resistor controls the gain. The Vo/Vi gain for this circuit is set by Equation 1:

$$\frac{V_o}{V_i} = 1 + 2\frac{R_f}{R_g} = 1 + 2\frac{3.2k\Omega}{711\Omega} = 10 \qquad \text{(EQ. 1)}$$

The effect of increasing or decreasing the feedback resistor value is shown in Figures 19, 24 and 29 (at the 3 power settings). Increasing R_F will tend to roll off the response while decreasing it will peak the frequency response up extending the bandwidth. R_G was adjusted in each of these plots to hold a constant gain of 10 (or 20dB). This shows the flexibility offered by the CFA topology - the frequency response can be controlled with the value of the feedback resistor with the R_G resistor then setting the desired gain.

The ISL1539A provides 4 very power efficient, high output current, CFA's. These are intended to be connected as two pairs of differential drivers. The pinout diagrams of page two show that Channels A and B are intended to operate as a pair while Channels C and D comprise the other pair. Power control is also provided through two pairs of control pins which separately set the power for Channels A and B together and then the other pair controls Channels C and D together.

Very low output distortion at low power can be provided by the differential configuration. The high slew rate intrinsic to the CFA topology also contributes to the exceptional performance shown in Figures 22, 27 and 32. These swept frequency distortion plots show extremely low distortion at 200kHz holding to very low levels up through 20MHz. At the lowest operating power (Figure 32, which is at low power, or 6.75mA per amplifier or 13.5mA/port) we still see < -70dBc through 5MHz for a $5V_{P-P}$ differential output swing.

Advanced Configurations - Active Termination

Where the best power efficiency is required in a full duplex DSL line interface application, it is common to apply the circuit shown below to reduce the power loss in the matching element while retaining a higher impedance for the upstream signal coming into this output stage. This circuit acts to provide a higher apparent output impedance (through its cross-coupled positive feedback through the Rp resistors) while physically taking a smaller IR drop through the Rm resistors for the output signal..

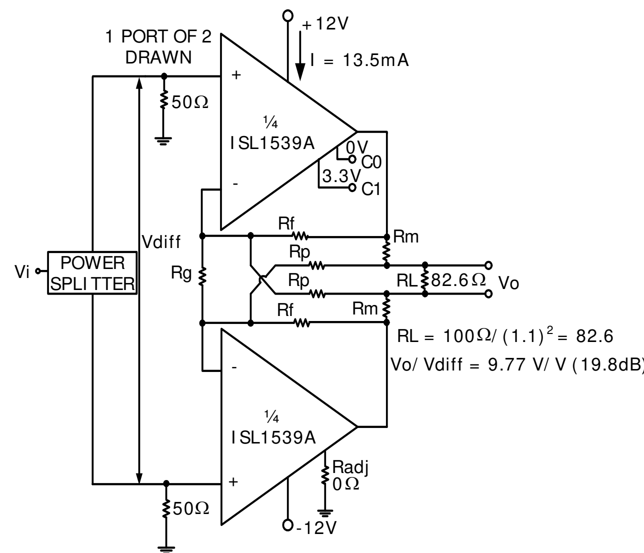


FIGURE 45. ACTIVE TERMINATION TEST CIRCUIT

This circuit is showing one of two ports configured in an active termination circuit used for some of the specification and characterization tests. This is showing the device operating in the low power mode, but data has been shown at the other power settings as well.

The 82.6Ω differential load is intended to emulate a 100Ω line load reflected through a 1:1.1 turns ratio transformer ($100\Omega/(1.1^2) = 82.6\Omega$ load). The gain and output impedance for this circuit can be described by the following equations.

The ideal transfer function is set by the open circuit gain (RL = infinite) and an equivalent output impedance Z_O.

$$\frac{V_o}{V_i} = A_{oc}\frac{R_L}{R_L + Z_o} \quad \text{(EQ. 2)}$$

The goal of the positive feedback resistor, R_P is to provide some "gain" in the apparent output impedance over just the 2* R_M. It also will act to increase the A_{OC} over the simple differential gain equation if a synthesis factor (SF) is defined as shown in Equation 3:

$$SF = \frac{1}{1 - \frac{R_f - R_m}{R_p}} \quad \text{(EQ. 3)}$$

We can see this "gain" is achieved by letting R_P be > R_F The closer R_P is to R_F-R_M, the more "gain" is achieved but at the risk of instability. With this SF defined as shown above, the exact A_{OC} and Z_O will be as shown in Equations 4 and 5:

$$A_{oc} = SF(1 + 2\frac{R_f}{R_g} + \frac{R_f - R_m}{R_p}) \quad \text{(EQ. 4)}$$

$$Z_o = SF(2R_m) \quad \text{(EQ. 5)}$$

For test purposes, the circuit shown in Figure 45 was configured to achieve the following results.

SF = 2.19

A_{OC} = 17.7V/V

Z_O = 66Ω

Putting these together into the gain to an 82.6Ω load gives the following test condition as shown by Equation 6.

$$\frac{V_o}{V_i} = A_{oc}\frac{R_L}{R_L + Z_o} = 17.7\frac{82.6\Omega}{82.6\Omega + 66\Omega} = 9.84\left(\frac{V}{V}\right) \quad \text{(EQ. 6)}$$

The advantage offered by this technique is that for whatever swing we desire at the load, there is less rise through the physical output matching resistor than if we simply inserted two 33Ω R_M resistors to achieve the 66Ω output impedance achieved in this test circuit. Whatever load current is required in R_L will rise to the output pins through 2* R_M. The rise from the load swing to the output pin swing is given by Equation 7:

$$\frac{R_L + 2R_m}{R_L} \quad \text{(EQ. 7)}$$

This was only 1.36 for the test circuit shown above. In differential circuits the ± V_P at the output pins produces a 4V_P for the differential peak-to-peak voltage. Hence a ±10V swing at each output in the above circuit will produce a 40V_{P-P} differential swing which will drop to the load divided by 1.36 - or a 29.41V_{P-P} differential swing.

Distortion and MTPR

The ISL1539A is intended to provide very low distortion levels under the demanding conditions required by the discrete multi-tone (DMT) characteristic of modern DSL modulations. The standard test for linearity is the Multi-Tone Power Ratio (MTPR) test where a specified standard is loaded up with discrete carriers over the specified frequencies in such a way as to produce the maximum rated line power and Peak to Average Ratio (PAR) with some tones missing. The measure of linearity is the separation from the active tones vs. a missing tone. To the extent that the amplifier is slightly non-linear, it will fold a small amount of power into the missing tones through intermodulation products for the active tones. Figure 17 shows the circuit operating at the low power setting used to test ADSL2+ frequency plan and power. For this test the carriers are spaced at 5kHz.

This -60dBc MTPR is exceptional for the very low 13.5mA total quiescent current used in this configuration. Operating at reduced power targets on the line will improve MTPR as will operating the amplifiers at higher quiescent current.

The characteristic curves show the exceptional single tone performance available using the ISL1539A. At the highest quiescent power, operating at a simple differential gain of 10V/V, Figure 22 shows the 5V_{P-P} distortion plot.

Figure 22 shows a better than -80dBc through 8MHz for the 2nd and 3rd harmonics. The rapid rise in the spurious above 10MHz is coming from the onset of fine scale slew limiting effects. By 20MHz, the output signal is requiring a differential slew rate of 300V/µs - a significant portion of the available 3000V/µs slew rate available at full power.

Power Control Function

Figure 46 shows a simplified schematic for the power control features included in the ISL1539A. Each of the 4 differential pairs shown in the drawing are used to steer control currents (I_{BIAS} terms) into additional current mirrors (not shown) that control the quiescent bias current for each of the two ports. This bias control shares the I_{ADJ} pin. When I_{ADJ} is grounded, the typical supply current levels shown in the "Electrical Specifications" tables on page 5 are produced. Inserting an external resistor to ground in the I_{ADJ} pin will scale the quiescent currents down, as shown in Figure 38.

It is also possible to scale the I_{ADJ} currents up by tying the I_{ADJ} pin through a resistor to a negative supply. As long as the resulting voltage divider between this external negative voltage and the internal +0.4V on the other side of the 500Ω resistor stays above the maximum rated negative voltage on the I_{ADJ} pin (-1V). For instance, to double the typical quiescent current levels, the current in the I_{ADJ} pin must be doubled from its nominal 800µA level. Using a -5V supply through an external 2.88kΩ resistor will double the current while leaving the I_{ADJ} pin voltage at approximately -0.4V, which is well within rated minimum. This approach should be used with great caution as very high internal power dissipations can easily be produced. However, it can be a useful approach to extend operation, particularly when operating on lower total supply voltages than the rated typical of ±12V.

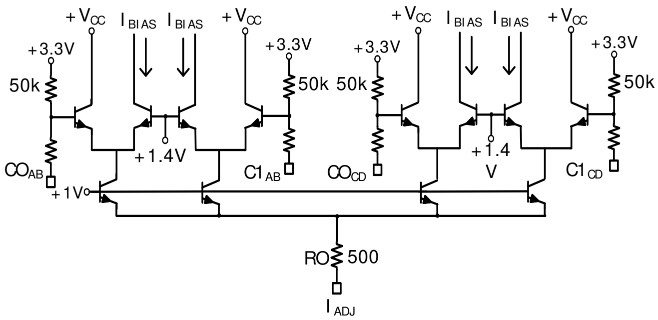


FIGURE 46. BIAS CONTROL CIRCUIT

The current in RO divides in 1/4 levels to form the bias current for the 4 pairs of differential switches. Each pair of switches controls the quiescent current for one port. For instance, $C0_{AB}$ and $C1_{AB}$ control the quiescent current for the port constructed from amplifiers A and B. If both control lines are unconnected externally, the internal 50kΩ pull-up will switch the differential pairs to divert the 100µA tail currents into the supply turning off the amplifiers. Taking both control pins low will pass both I_{BIAS} lines on into scaling current sources. With I_{REF} grounded, this will give the typical 27.2mA total quiescent current for a port shown in the "Electrical Specification" tables on page 5. Taking C_0 high (>2V) while leaving C_1 low (<0.8V) will reduce the current into a port to a typical 23mA. Taking C_1 high, while leaving C_0 low will reduce the current in a port to a typical 13.5mA supply current. Table 2 summarizes the operation modes for ISL1539A for each port.

TABLE 2. POWER MODES OF THE ISL1539A

C_1	C_0	OPERATION
0	0	I_S Full Power Mode
0	1	I_S Medium Power Mode
1	0	I_S Low Power Mode
1	1	Power-Down

Performance Considerations

Driving Capacitive Loads

All closed loop op amps are susceptible to reduced phase margin when driving capacitive loads. This shows up as peaking in the frequency response that can, in extreme situations, lead to oscillations. The ISL1539A is designed to operate successfully with small capacitive loads such as layout parasitics. As the parasitic capacitance increases, it is best consider a small resistor in series with the output to isolate the phase margin effects of the capacitor. Figure 20 on page 10 shows the effect of capacitive load on the differential gain of 10 circuit. With 15pF on each output, we see about 5dB peaking. This will increase quickly at higher C_{loads}. If this degree of peaking is unacceptable, a small series resistor can be used to improve the flatness as shown in Figure 21.

Output DC Error Model

Often, non-inverting bias current (ibn), inverting bias current (ibi), and input offset voltage (Vio) are quite low for typical op amps.

Vio, ibn, ibi can be mapped to output offset both common and differential mode. Consider the circuit in Figure 47.

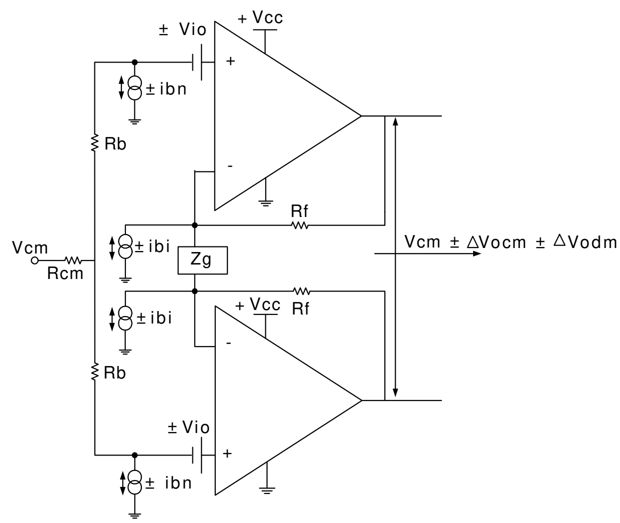


FIGURE 47. DC ERROR MODEL

The output common mode offset voltage (Vo-cm) is derived from the input common mode voltage (Vi-cm), as expressed in Equations 8 and 9:

$$Vicm = \pm 2 \times ibn \times Rcm \pm ibn \times Rb \pm Vio \quad \text{(EQ. 8)}$$

$$Vocm = \pm Vicm \pm Rf \times ibi \quad \text{(EQ. 9)}$$

The output differential mode offset voltage (Vo-dm) is derived from the input differential mode voltage (Vi-dm), as expressed in Equations 10 and 11:

$$Vidm = \pm \Delta ibn \times Rb \pm \Delta Vio \quad \text{(EQ. 10)}$$

$$Vodm = \pm Vidm \times \left(1 + \frac{2Rf}{Rg}\right) \pm \Delta ibi \times Rf \quad \text{(EQ. 11)}$$

Example:

Referring to the "Electrical Specification" tables on page 6:

ibn = 8µA, Δibn = 2µA

ibi = 75µA, Δibi = 35µA

Vio = 8mV, ΔVio = 2mV

Assuming Rf = 3kΩ, Rg = 333Ω, Rb = 7.5kΩ Rcm = 5kΩ, the total output offset voltage derived is expressed in Equation 12:

$$Vcm = Vocm + 0.5 \times Vodm = 434mV \quad \text{(EQ. 12)}$$

Given the worst case DC errors, 434mV of DC shift will be at the output reducing the available output swing slightly. Actual operation should never see this much shift as the error terms are not completely independent.

Output Headroom Model

Driving high voltages into heavy loads will require a careful consideration of the available output swing vs. load. Figure 48 shows a useful model for predicting the available output swing. If the output is modeled as ideal NPN and PNP transistors, the output swing limits can be described as no load headrooms (V_P and V_N) and an equivalent impedance to the supplies (R_P and R_N)

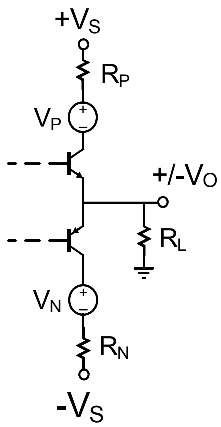


FIGURE 48. HEADROOM MODEL

The no load headrooms can be found in the "Electrical Specifications" table on page 5 as 12V - 10.9V = 1.1V and they are equal to each supply.

The equivalent impedances for this model can be extracted from the reduced swings shown in the specification table for the heavier loads. Looking at the typical 60Ω load swings, we see a +9.8V and -9.7V swing. Solving for the two resistors in the Headroom model shown in Figure 48 gives:

Rp = 6.7Ω and Rn = 7.4Ω

For the differential configuration, Figure 49 shows the Headroom model that can be used to predict the maximum available swing for a given supply voltage and load resistor, R_L.

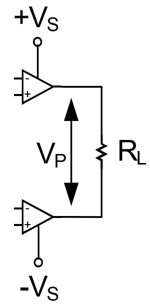


FIGURE 49. HEADROOM MODEL

For equal bipolar supplies, the available peak output swing will be given by Equation 13:

$$V_p = \frac{2(V_s - V_p - V_n)}{1 + \frac{R_p + R_n}{R_L}} \quad \text{(EQ. 13)}$$

For example, to worst case the typical gain of 10 design using ±12V supplies with ±5% supply tolerance and a minimum expected load of 90Ω, a maximum V_P can be calculated as shown in Equation 14:

$$V_p = \frac{2(V_s - V_p - V_n)}{1 + \frac{R_p + R_n}{R_L}} = \frac{2(11.4 - 2.2)}{1 + \frac{6.7\Omega + 7.4\Omega}{90\Omega}} = 15.9V_p \quad \text{(EQ. 14)}$$

The minimum V_{P-P} would be twice this, or 31.8V_{P-P}. While this extreme condition would normally not be encountered, it does show the importance of knowing your minimum expected load for high output swing conditions.

Output Noise Model

The full differential output noise model for the ISL1539A should include the 3 input noise terms for each device as well as the noise contributions due to the external resistors.

This necessarily becomes an involved model due to the number of terms, but if the terms that are the same on each side of the differential circuit can be assumed to be equal, it will simplify considerably. The noise model shown in Figure 50 includes all of the op amp terms and resistor terms. This model is directed at calculating the differential output spot noise for different values of the resistors in the simple differential gain circuit. It is assuming each amplifier term is independent and uncorrelated to the other terms.

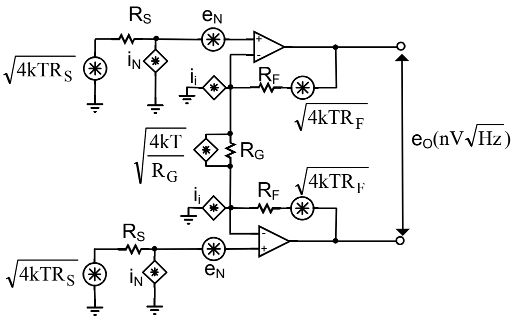


FIGURE 50. OUTPUT NOISE MODEL

In Figure 50, the circle sources are noise voltages while the diamonds are noise currents and 4kT is 1.6E - 20J.

If the op amp terms are assumed to be equal for the two sides of the circuit and two R_F and R_S resistors are also equal, and the differential gain is defined as $Ad = 1+2R_F/R_G$, the differential output noise expression becomes Equation 15.

$$e_o = \sqrt{2\left(A_d^2\right)\left(e_n^2 + (i_nR_s)^2 + 4kTR_s\right) + 2\left(i_iR_f\right)^2 + 2A_d\left(4kTR_f\right)} \quad \text{(EQ. 15)}$$

Putting in numbers for the gain of 10 characterization circuit (with $R_S = 50\Omega$) gives a differential output noise of $e_O = 69nV/\sqrt{Hz}$. Dividing this by the differential gain of 10 gives an input noise of $e_i = 6.9nV/\sqrt{Hz}$ which is only slightly more than the RMS sum of the two 4nV input voltage noise terms for the op amps themselves ($5.7nV/\sqrt{Hz}$).

Board Design Recommendations

The feedback resistors need to be placed as close as possible to the output and inverting input pins to minimize parasitic capacitance in the feedback loop. This includes the R_F and R_P resistors in the active termination configuration. Keep the gain resistor also very close to the inverting inputs for its port and minimize parasitic capacitances to ground or power planes as well.

Close placement of the supply decoupling capacitors will minimize parasitic inductance in the supply path. High frequency load currents are typically pulled through these capacitors so close placement of 0.01µF capacitors on each of the supply pins will improve dynamic performance. Higher valued capacitors, 6.8µF typically, can be placed further from the package as they are providing more of the low frequency decoupling.

The thermal pad for the ISL1539A should be connected to either ground or the $-V_S$ power plane. The choice of which plane depends on which one would have the more accessible thermal area.

While the ISL1539A is relatively robust in driving parasitic capacitive loads, it is always preferred to get into any series output resistor needed in the design as physically close as possible to the output pins. Then trace capacitance on the other side of that resistor will have a much smaller effect on loop phase margin.

Protection devices that are intended to steer large load transients away from the ISL1539A output stage and into the power supplies or ground should have a short trace from their supply connections into the nearest supply capacitor - or should include their own supply capacitors to provide a low impedance path under fast transient conditions.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
9/23/09	FN6916.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL1539A

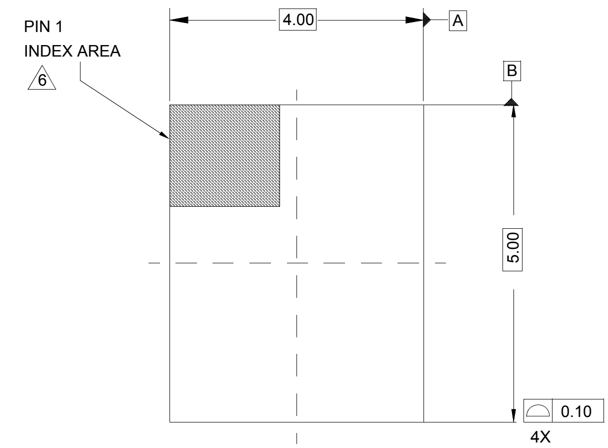
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

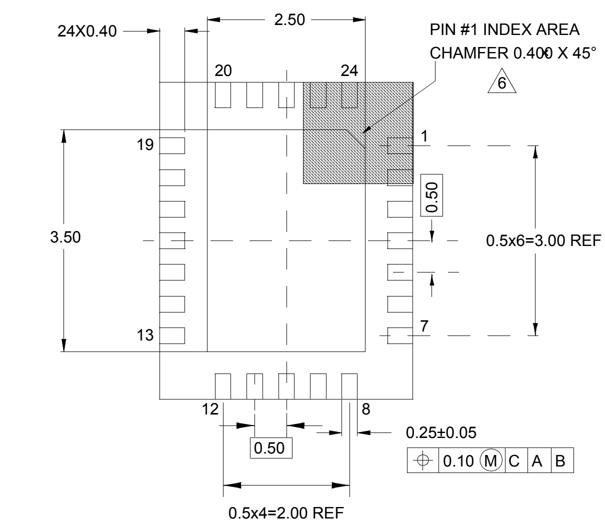
Package Outline Drawing

L24.4x5B

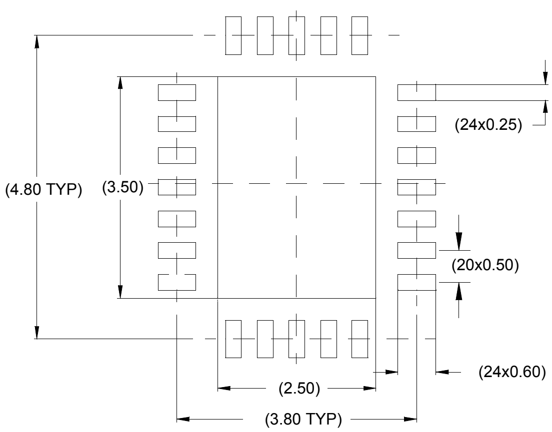
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 10/06



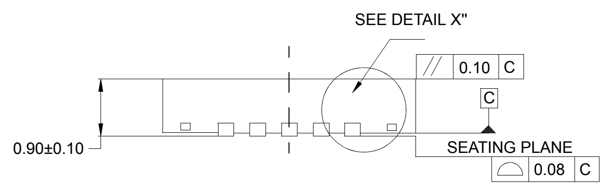
TOP VIEW



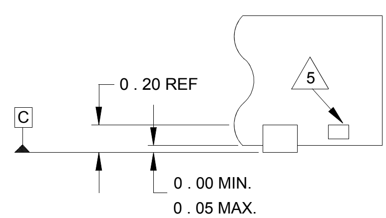
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

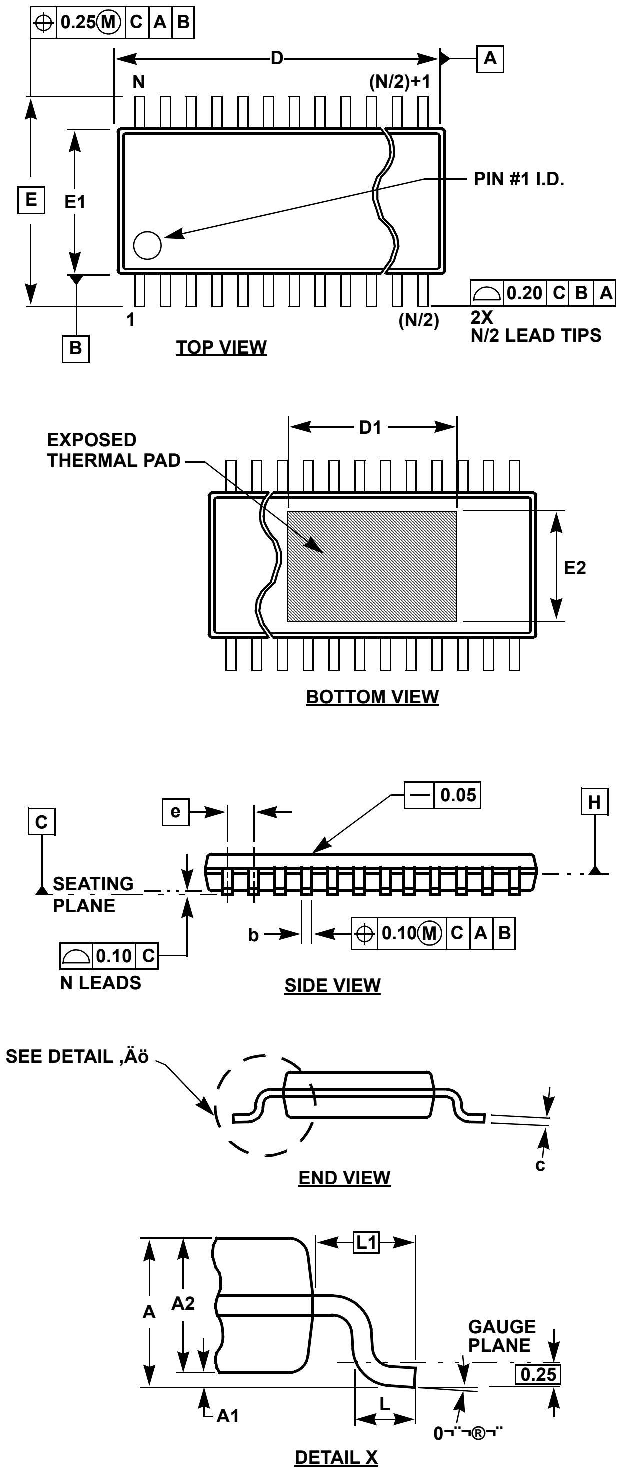


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

HTSSOP (Heat-Sink TSSOP) Family



MDP0048

HTSSOP (HEAT-SINK TSSOP) FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	20 LD	24 LD	28 LD	38 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.075	0.075	0.075	0.075	0.075	±0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	6.50	7.80	9.70	9.70	±0.10
D1	3.2	4.2	4.3	5.0	7.25	Reference
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
E2	3.0	3.0	3.0	3.0	3.0	Reference
e	0.65	0.65	0.65	0.65	0.50	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
N	14	20	24	28	38	Reference

Rev. 3 2/07

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at Datum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.