

Thermally-Enhanced High Power RF LDMOS FETs 60 W, 2110 – 2170 MHz

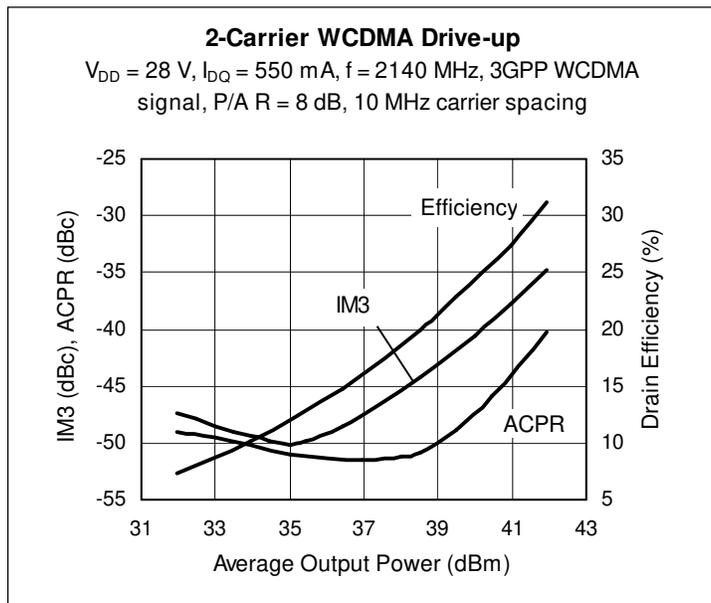
Description

The PTFA210601E and PTFA210601F are 60-watt LDMOS FETs designed for single- and two-carrier WCDMA power amplifier applications in the 2110 to 2170 MHz band. Features include input and output matching, and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA210601E
 Package H-36265-2



PTFA210601F
 Package H-37265-2



Features

- Thermally-enhanced packages, Pb-free and RoHS-compliant
- Broadband internal matching
- Typical two-carrier WCDMA performance at 2140 MHz, 28 V
 - Average output power = 12 W
 - Linear Gain = 16 dB
 - Efficiency = 27.0%
 - Intermodulation distortion = -38 dBc
 - Adjacent channel power = -44 dBc
- Typical CW performance, 2170 MHz, 28 V
 - Output power at P-1dB = 68 W
 - Efficiency = 58.5%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 60 W (CW) output power

RF Characteristics

WCDMA Measurements (tested in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 550\text{ mA}$, $P_{OUT} = 12\text{ W}$ average

$f_1 = 2135\text{ MHz}$, $f_2 = 2145\text{ MHz}$, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15.0	16.0	—	dB
Drain Efficiency	η_D	26.0	27.0	—	%
Intermodulation Distortion	IMD	—	-38	-37	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-tone Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ} = 550\text{ mA}$, $P_{OUT} = 60\text{ W PEP}$, $f = 2140\text{ MHz}$, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	16	—	dB
Drain Efficiency	η_D	—	42	—	%
Intermodulation Distortion	IMD	—	-28	—	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
On-State Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.15	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}$, $I_{DQ} = 550\text{ mA}$	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA

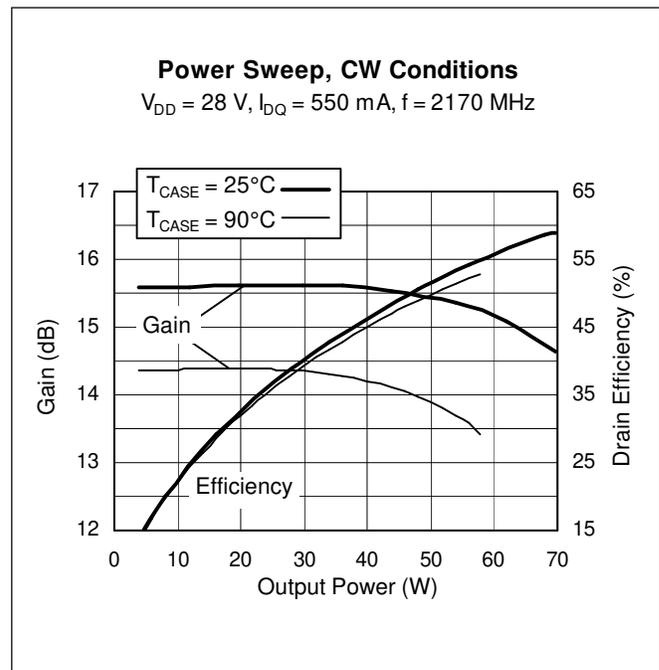
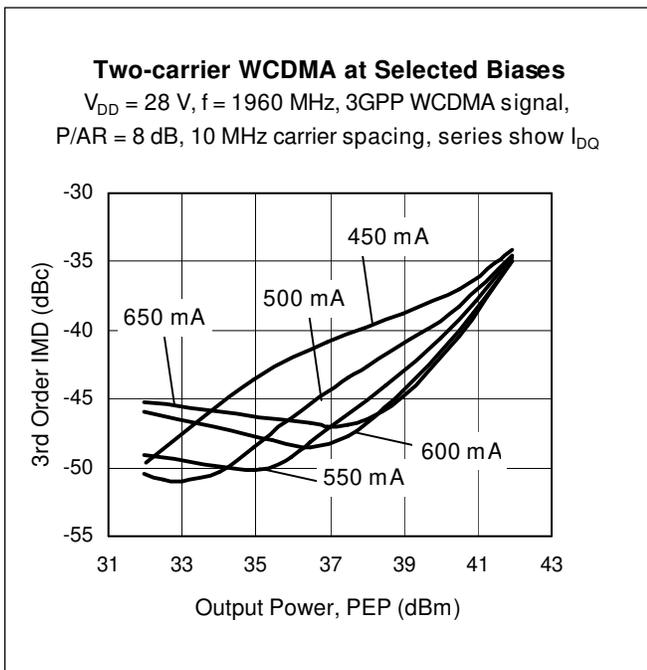
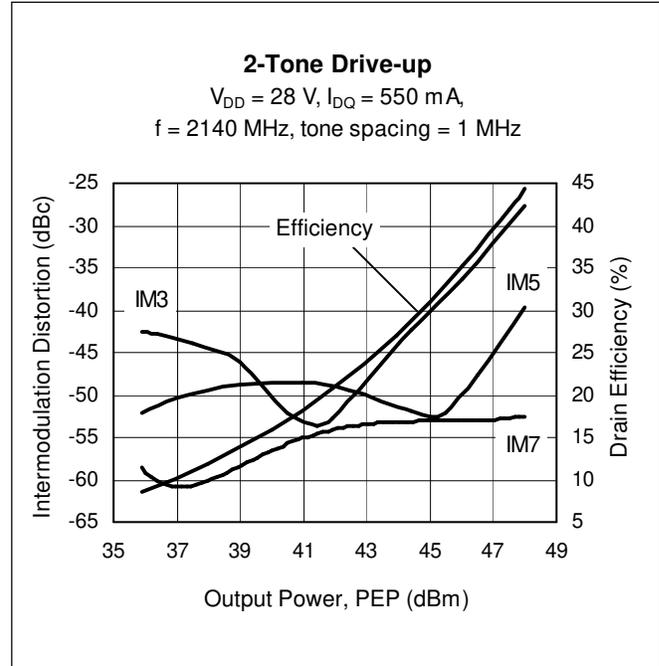
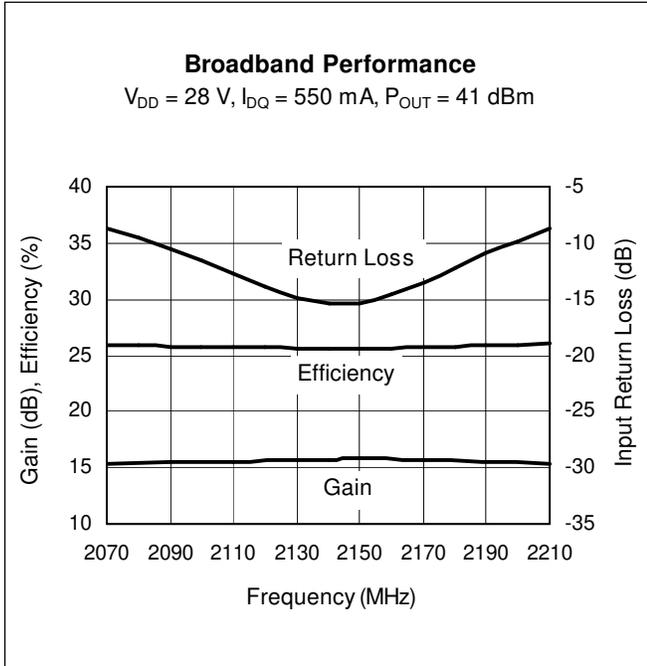
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	-0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Total Device Dissipation	P_D	196	W
		Above 25 $^{\circ}\text{C}$ derate by	1.12
Storage Temperature Range	T_{STG}	-40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$, 60 W CW)	$R_{\theta JC}$	0.89	$^{\circ}\text{C}/\text{W}$

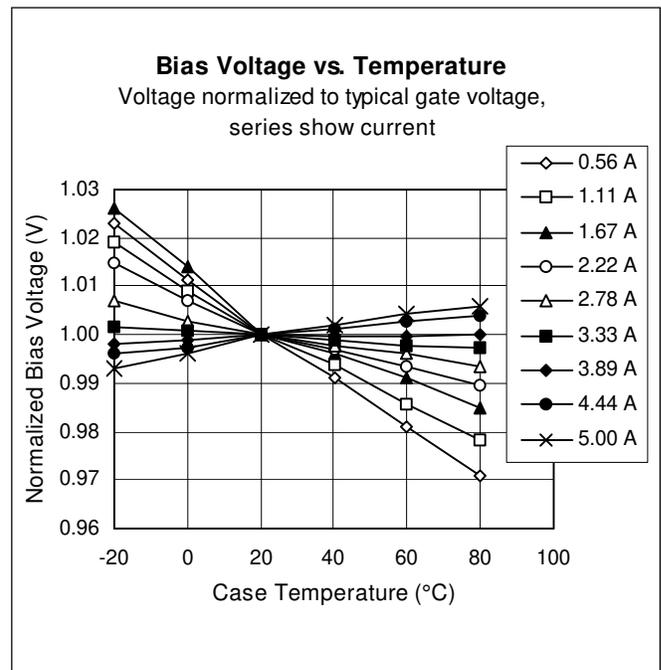
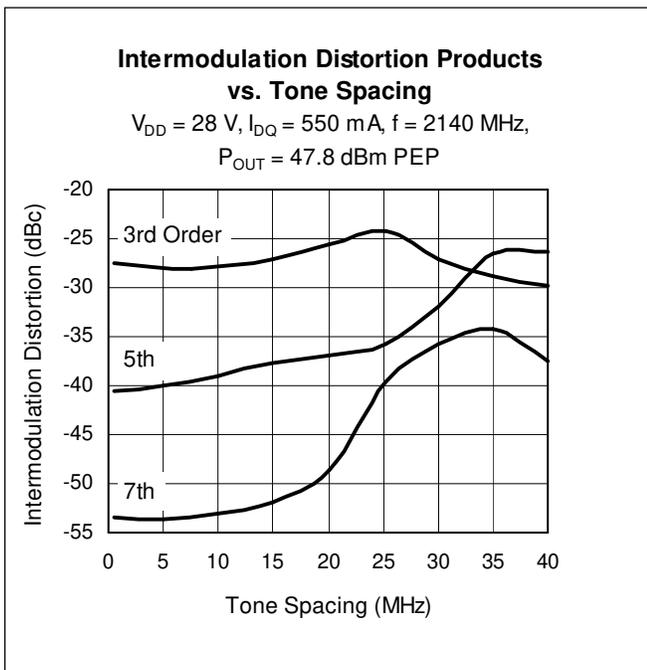
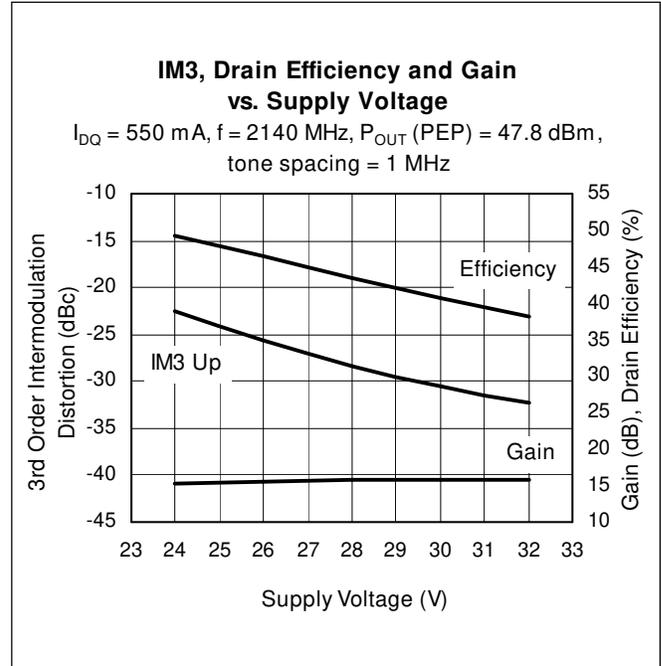
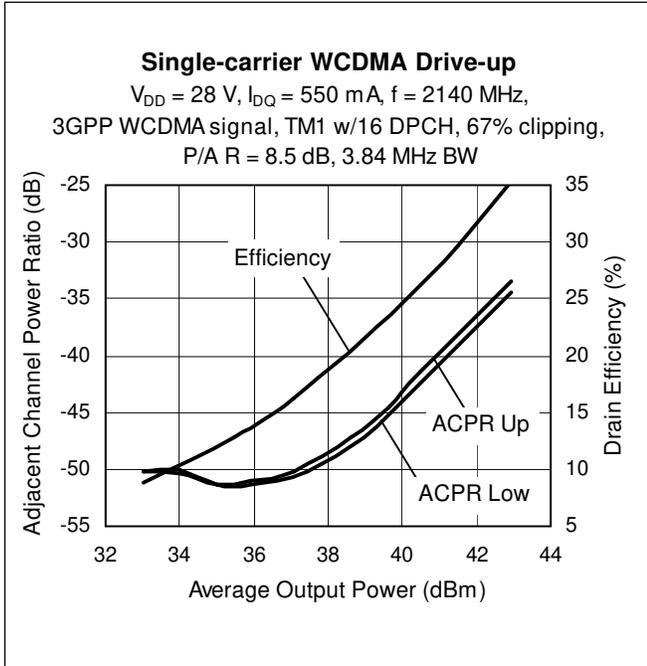
Ordering Information

Type and Version	Package Type	Package Description	Marking
PTFA210601E V4	H-36265-2	Thermally-enhanced slotted flange, single-ended	PTFA210601E
PTFA210601F V4	H-37265-2	Thermally-enhanced earless flange, single-ended	PTFA210601F

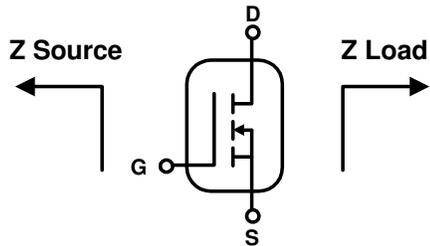
Typical Performance (data taken in a production test fixture)



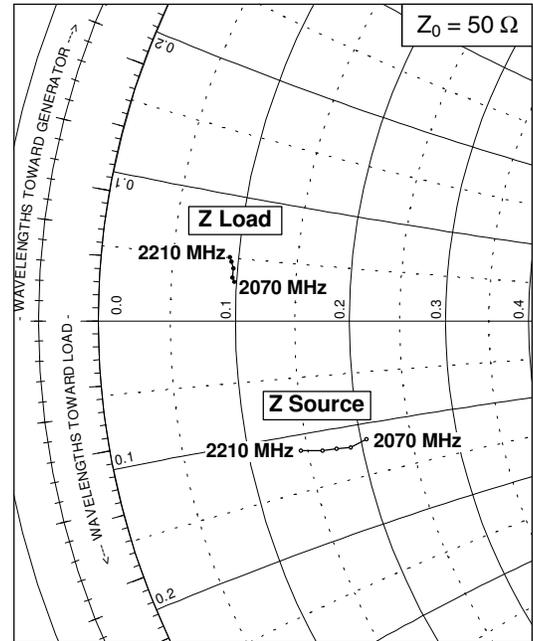
Typical Performance (cont.)



Broadband Circuit Impedance

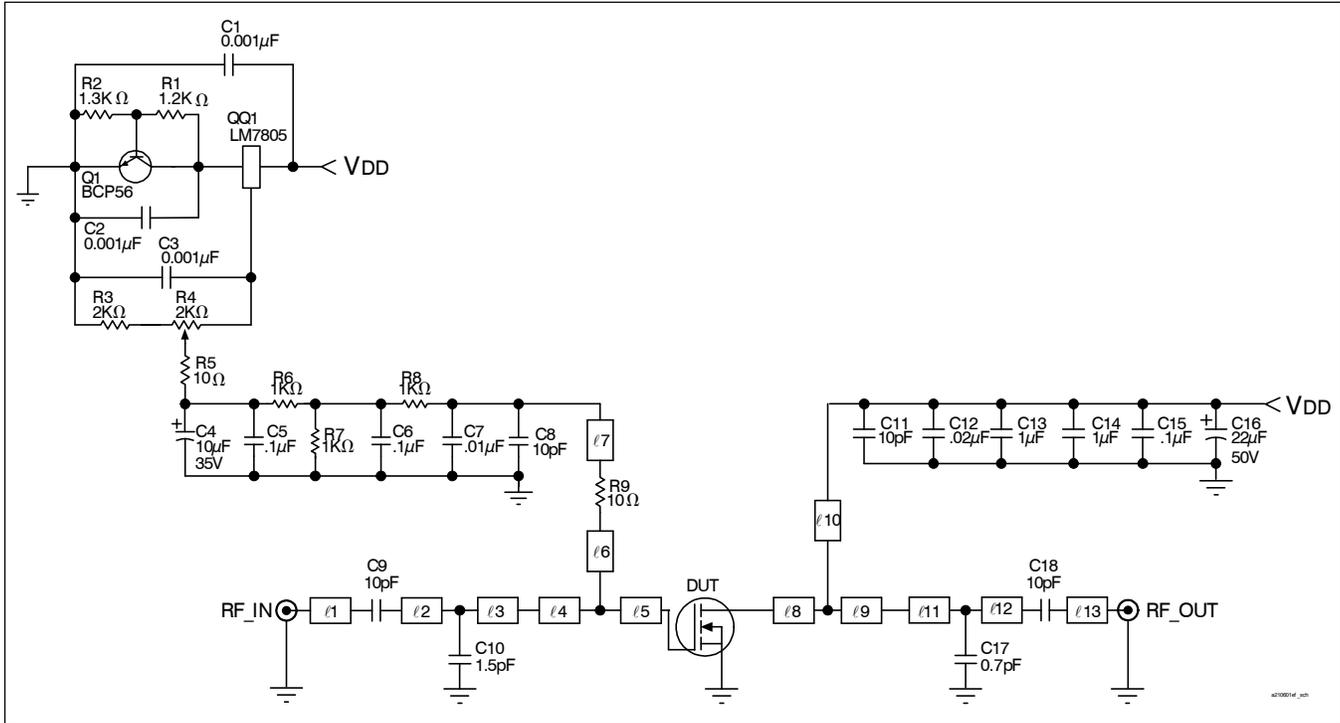


Frequency MHz	Z Source Ω		Z Load Ω	
	R	jX	R	jX
2070	10.29	-5.79	4.91	1.57
2110	9.46	-6.02	4.83	1.75
2140	8.79	-5.95	4.85	2.12
2170	8.14	-5.91	4.76	2.38
2210	7.19	-5.72	4.66	2.55



See next page for reference circuit information

Reference Circuit



Reference circuit schematic for $f = 2140$ MHz

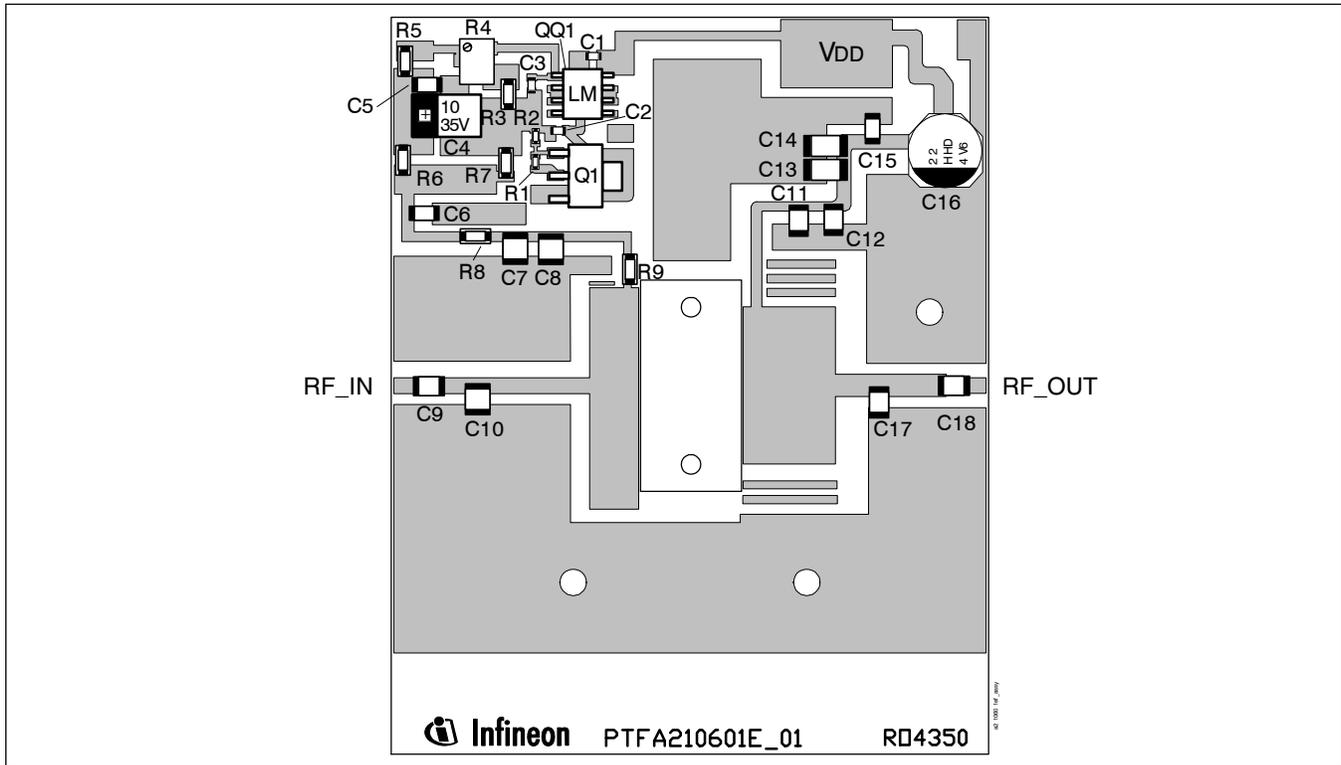
Circuit Assembly Information

DUT	PTFA210601E or PTFA210601F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, $\epsilon_r = 3.48$	Rogers 4350	1 oz. copper

Microstrip	Electrical Characteristics at 2140 MHz ¹	Dimensions: L x W (mm)	Dimensions: L x W (in.)
l_1	0.030λ , 50.0Ω	2.54 x 1.52	0.100 x 0.060
l_2	0.038λ , 50.0Ω	3.15 x 1.52	0.124 x 0.060
l_3	0.146λ , 50.0Ω	12.32 x 1.52	0.485 x 0.060
l_4	0.049λ , 6.2Ω	3.81 x 22.78	0.150 x 0.897
l_5	0.016λ , 6.2Ω	1.17 x 22.78	0.046 x 0.897
l_6	0.009λ , 80.0Ω	0.74 x 0.69	0.029 x 0.027
l_7	0.112λ , 80.0Ω	9.78 x 0.69	0.385 x 0.027
l_8	0.018λ , 8.5Ω	1.35 x 16.26	0.053 x 0.640
l_9	0.105λ , 8.5Ω	8.08 x 16.26	0.318 x 0.640
l_{10}	0.173λ , 67.0Ω	14.83 x 1.02	0.584 x 0.040
l_{11}	0.051λ , 41.0Ω	4.11 x 2.29	0.162 x 0.090
l_{12}	0.077λ , 41.0Ω	6.35 x 2.29	0.250 x 0.090
l_{13}	0.032λ , 50.0Ω	2.79 x 1.52	0.110 x 0.060

¹Electrical characteristics are rounded.

Reference Circuit (cont.)

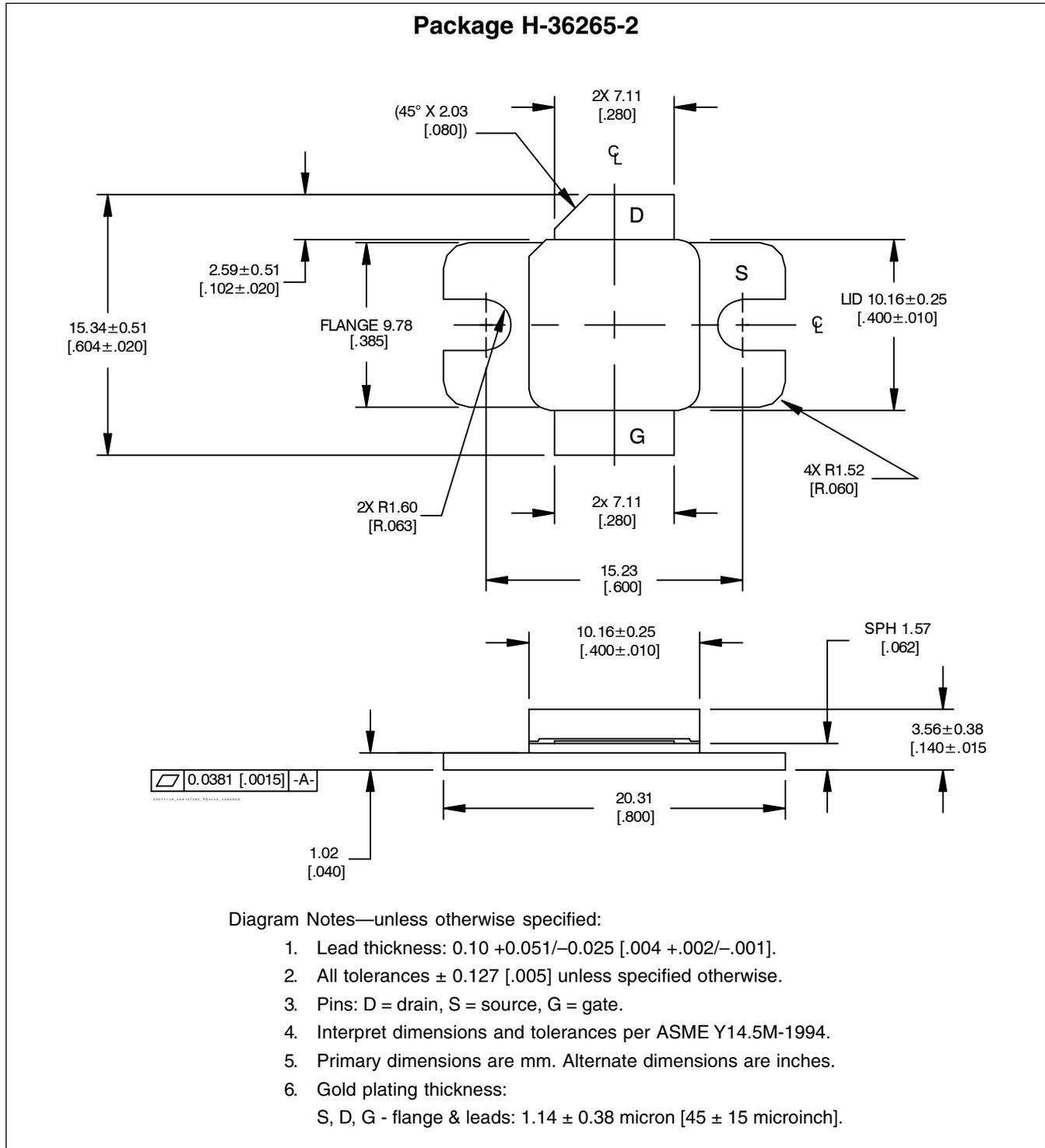


Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 μ F	Digi-Key	PCC1772CT-ND
C4	Tantalum capacitor, 10 μ F, 35 V	Digi-Key	PCS6106TR-ND
C5, C6, C15	Capacitor, 0.1 μ F	Digi-Key	PCC104BCT-ND
C7	Capacitor, 0.01 μ F	ATC	100B 103
C8, C9, C11, C18	Ceramic capacitor, 10 pF	ATC	100B 100
C10	Ceramic capacitor, 1.5 pF	ATC	100B 1R5
C12	Capacitor, 0.02 μ F	ATC	200B 203
C13, C14	Capacitor, 1.0 μ F	Digi-Key	445-1411-1-ND
C16	Electrolytic capacitor, 22 μ F, 50 V	Digi-Key	PCE3374CT-ND
C17	Ceramic capacitor, 0.7 pF	ATC	100B 0R7
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor, 1.2k ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor, 1.3k ohms	Digi-Key	P1.3KGCT-ND
R3	Chip resistor, 2k ohms	Digi-Key	P2KECT-ND
R4	Potentiometer, 2k ohms	Digi-Key	3224W-202ETR-ND
R5, R9	Chip resistor, 10 ohms	Digi-Key	P10ECT-ND
R6, R7, R8	Chip resistor, 1k ohms	Digi-Key	P1KECT-ND

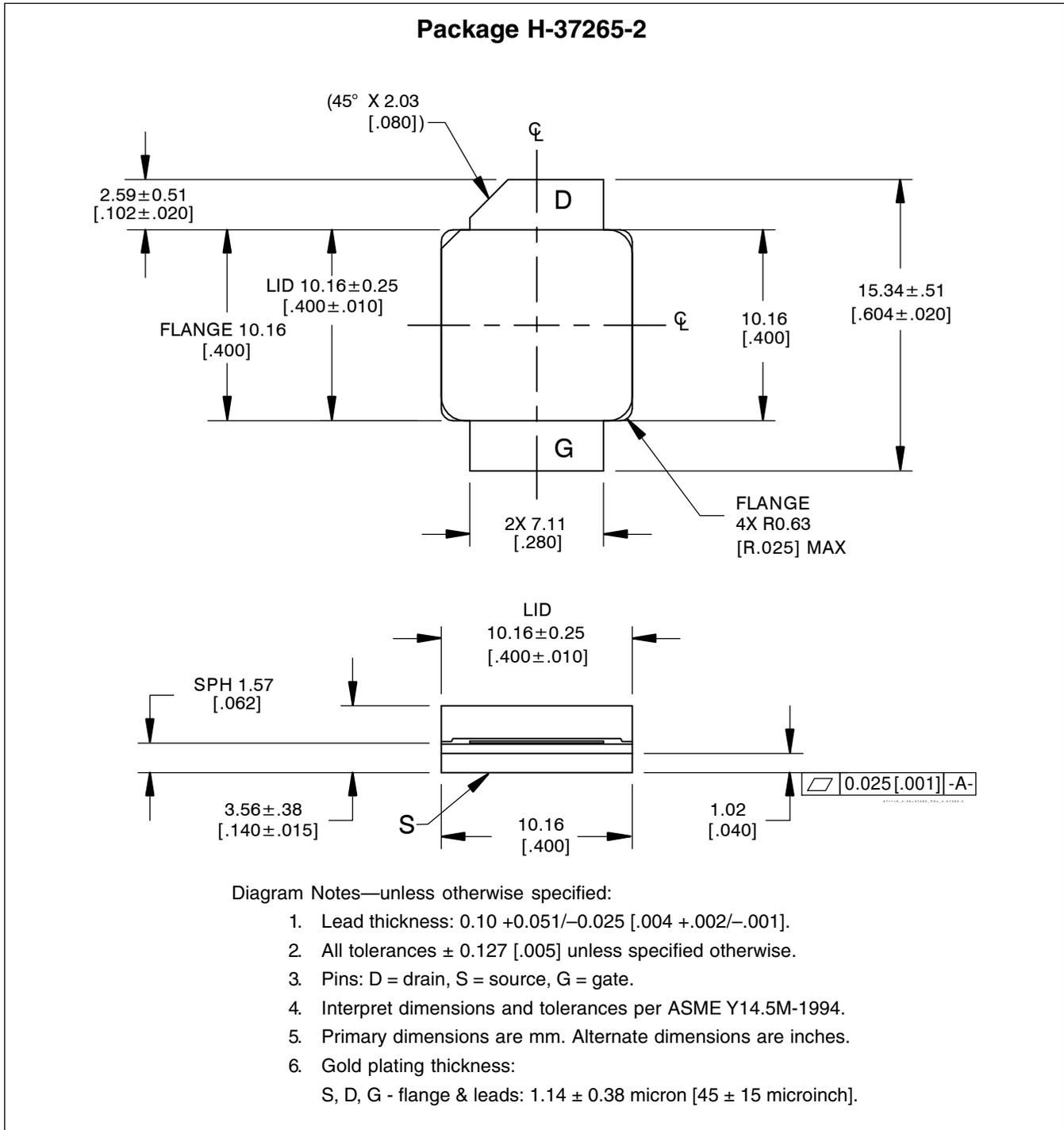
*Gerber Files for this circuit available on request

Package Outline Specifications



Find the latest and most complete information about products and packaging at the Infineon Internet page
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Package Outline Specifications (cont.)



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Revision History: 2007-11-19

Data Sheet

Previous Version: 2007-03-02, Data Sheet

Page	Subjects (major changes since last revision)
1, 2, 8, 9	Update to product V4, with new package technologies. Update package outline diagrams.

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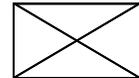
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Edition 2007-11-19

Published by

Infineon Technologies AG

81726 München, Germany

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