



Table of Contents

Table of Contents.....	1
Description.....	2
Features.....	2
Applications.....	2
Required Equipment.....	3
Evaluation Board Overview.....	3
Instructions.....	4
Evaluation Board Schematic.....	5
Bill of Materials.....	6
Typical Performance.....	7

Description

The EN6382QI is a Power System on a Chip (PowerSoC) DC to DC converter with an integrated inductor, PWM controller, MOSFETs and compensation to provide the smallest solution size in an 8x8x3mm 56 pin QFN module. It offers very high efficiency and is able to provide 8A continuous output current with no de-rating. The EN6382QI also provides excellent line and load regulation over temperature. The EN6382QI is specifically designed to meet the precise voltage and fast transient requirements of high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in distributed power architecture.

Other features include precision enable threshold, pre-bias monotonic start-up, and programmable soft-start. The device's advanced circuit techniques, ultra-high switching frequency, and proprietary integrated inductor technology deliver high-quality, ultra-compact DC-DC conversion.

The Altera Enpirion integrated inductor solution significantly helps to reduce noise. The complete power converter solution enhances productivity by offering greatly simplified board design, layout and manufacturing requirements. All Altera Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Features

- High Efficiency (Up to 96%)
- Excellent Ripple and EMI Performance
- Up to 8A Continuous Operating Current
- Input Voltage Range (3.0V to 6.5V)
- 1.5% V_{FB} Accuracy
- Optimized Total Solution Size (170 mm²)
- Precision Enable Threshold for Sequencing
- Programmable Soft-Start
- Thermal, Over-Current, Short Circuit, Reverse Current Limit and Under-Voltage Protections
- RoHS Compliant, MSL Level 3, 260°C Reflow

Applications

- Point of load regulation for FPGAs, ASICs, processors, DSPs, and distributed power architectures.
- Industrial automation, servers, storage, adapter cards, wireless base stations, test and measurement, and embedded computing.
- Space constrained applications that require the highest power density.
- Noise sensitive applications.

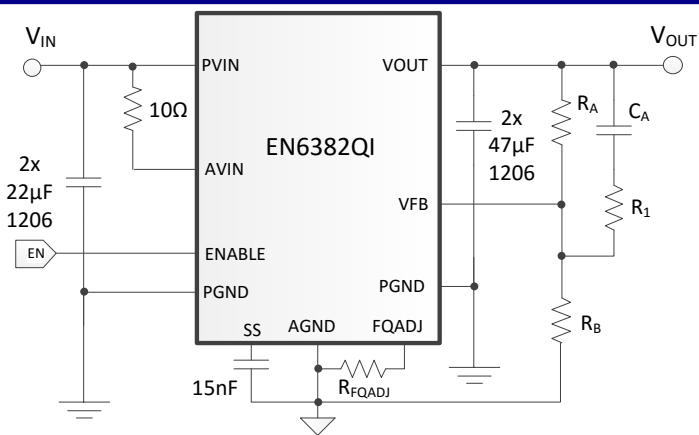


Figure 1: Simplified Applications Circuit

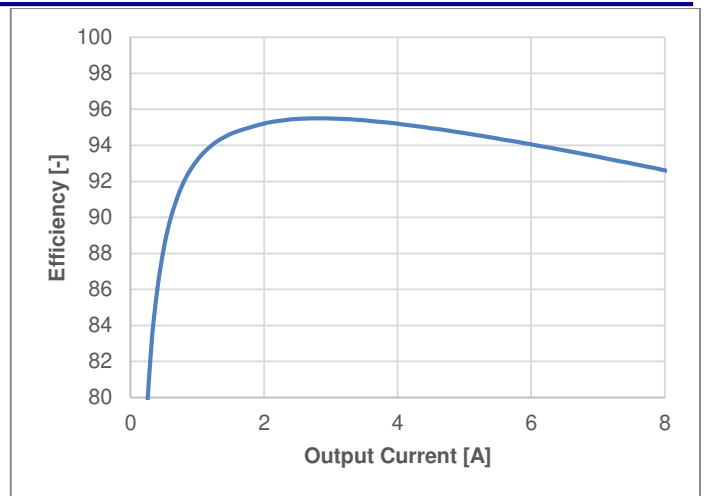


Figure 2: Efficiency at $V_{IN} = 5V$, $V_{OUT} = 3.3V$

Required Equipment

No.#	Equipment	Minimum Spec
1	DC power supply	10V/10A, adjustable
2	Electronic Load	10V/20A with dynamic load capabilities
3	DMM	-
4	Oscilloscope	-
5	Cables	>10A capability, banana terminal

Evaluation Board Overview

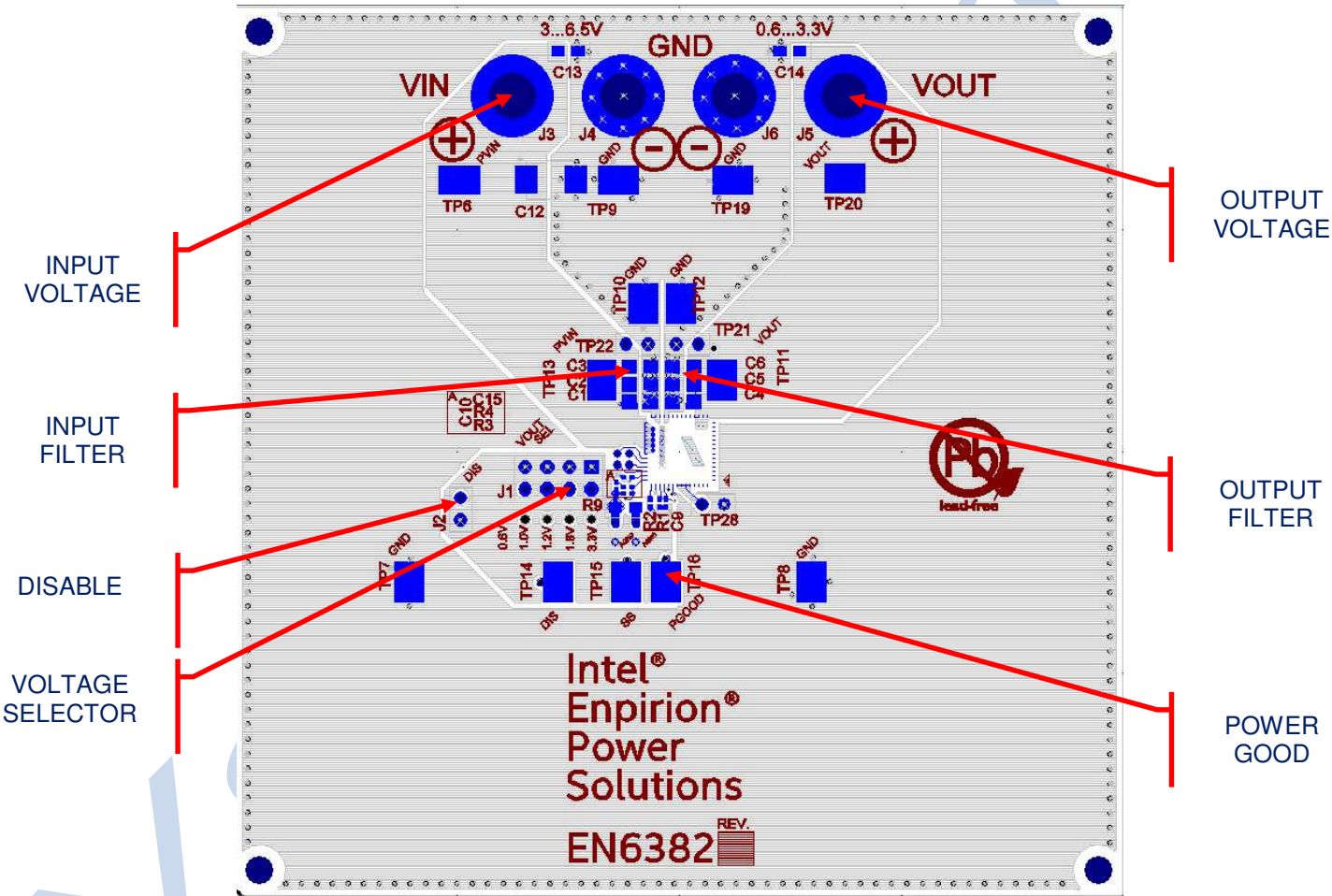


Figure 3: EN6382 Evaluation Board Illustration (Top Layer)

Instructions



Warning:

Incorrect polarity of the power supply may cause permanent damage!



Warning:

Power supply voltage above 7V may cause permanent damage!



1) Connecting the power supply

- Set the Power Supply to 5V/10A
- Connect the power supply to the board (make sure that the power supply is OFF) with two patch cables, not longer than 12 inch (30cm). Using longer wires is possible, provided that additional bulk is added to the board and the input voltage is monitored at the board level. Please use INPUT GROUND and INPUT VOLTAGE jacks to connect the power.

- Please observe the correct polarity.

2) Connecting the load

- Connect the load to the OUTPUT GROUND and OUTPUT voltage with patch cables, no longer than 12 inches (30cm).
- Please observe the correct polarity.

3) Jumper Setting

- The board will arrive with NO jumper on the J2 and one jumper on J1, in the 1V0 position. Connecting more than one jumper on J1 will not damage the board – just drive the output voltage higher.

4) Power-up the board

- After all preparations above, the board should be ready to perform.

Note: To measure the Bode Plot of the DC-DC converter, R9 must be replaced with 50 Ω , while TP1, 2 and 3 should be used to connect the probes of the phase analyzer.

Evaluation Board Schematic

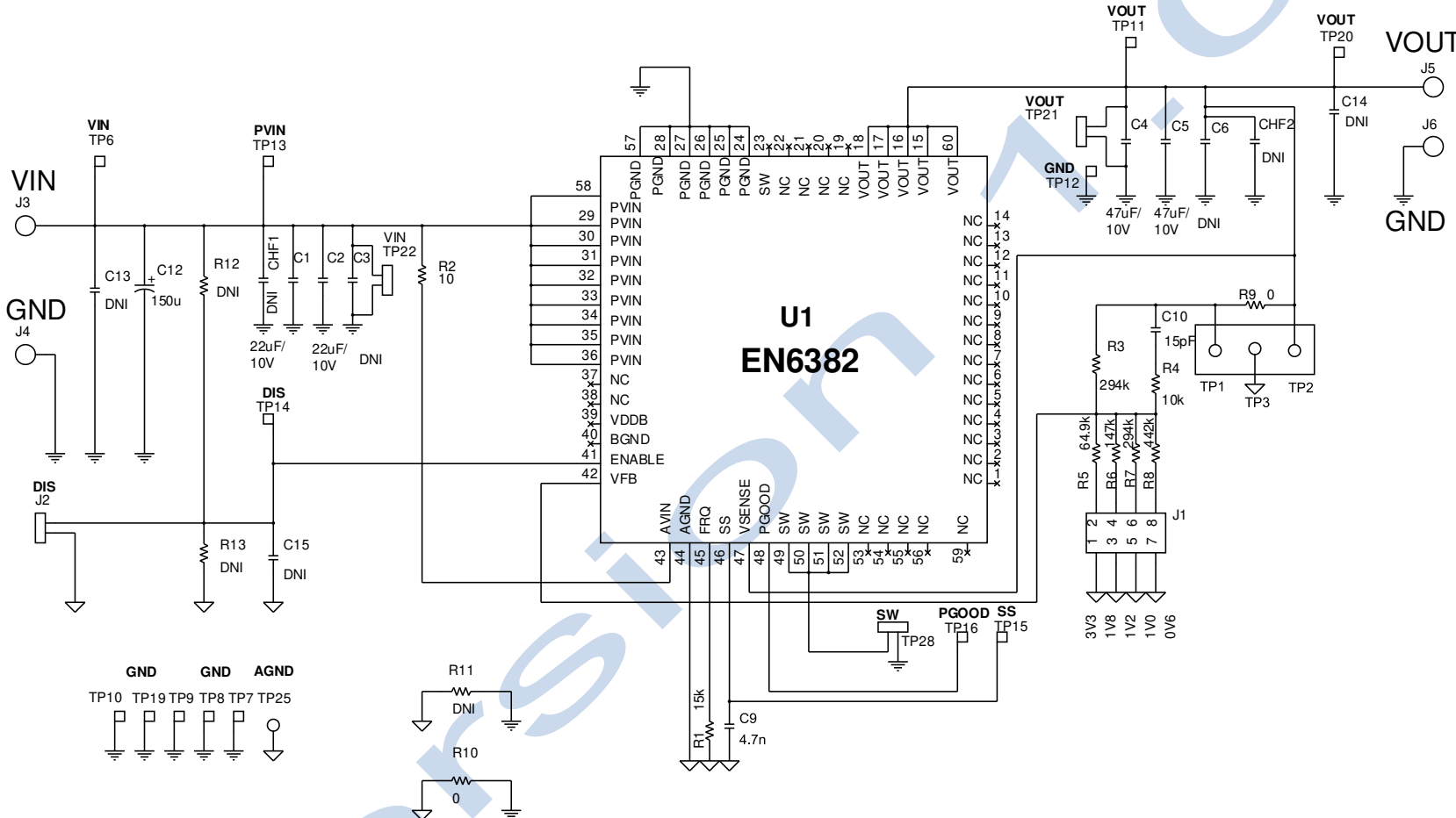


Figure 4: Evaluation Board Schematic

Bill of Materials

Designator	Qty	Description
C1,C2	2	22 μ F/10V
C9	1	4.7nF
C10	1	15pF
C4, C5	1	47 μ F/10V
C12	1	150 μ F
R1	1	15k Ω
R2	1	10 Ω
R3,R7	2	294k Ω
R4	1	10k Ω
R5	1	64.9k Ω
R6	1	147k Ω
R8	1	442k Ω
R9, R10	2	0 Ω
U1	1	EN6382QI

Typical Performance

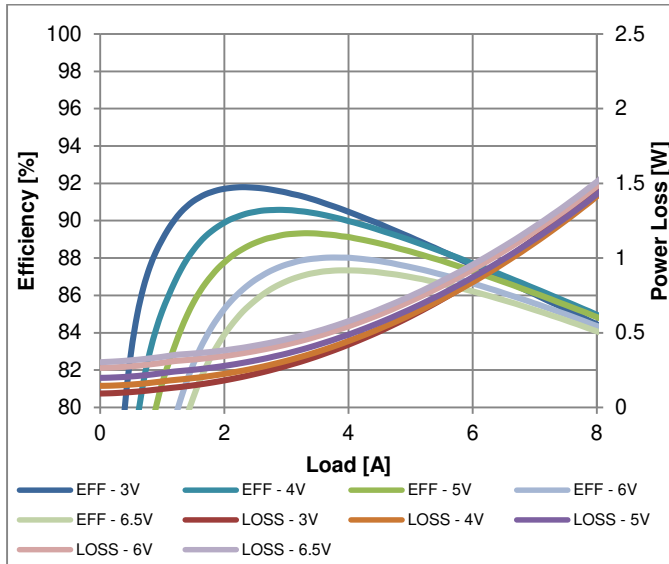


Figure 5: Efficiency – $V_{OUT} = 1V$, various V_{IN} ,
 $f = 1.5MHz$

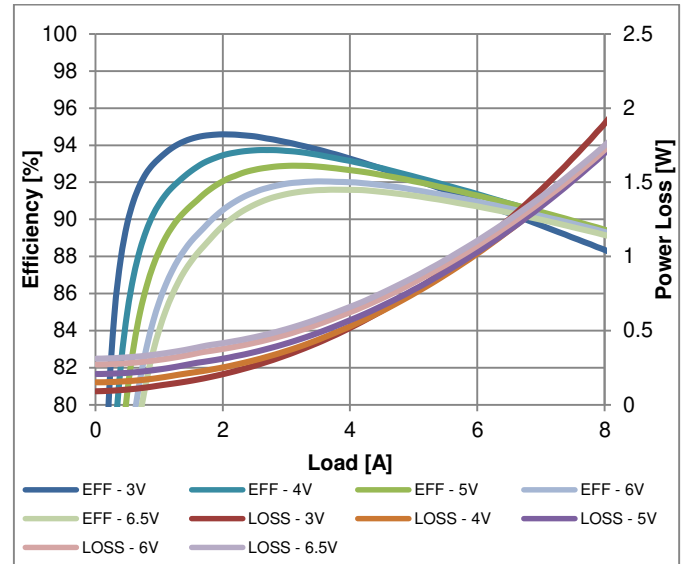


Figure 6: Efficiency – $V_{OUT} = 1.8V$, various V_{IN} ,
 $f = 1.5MHz$

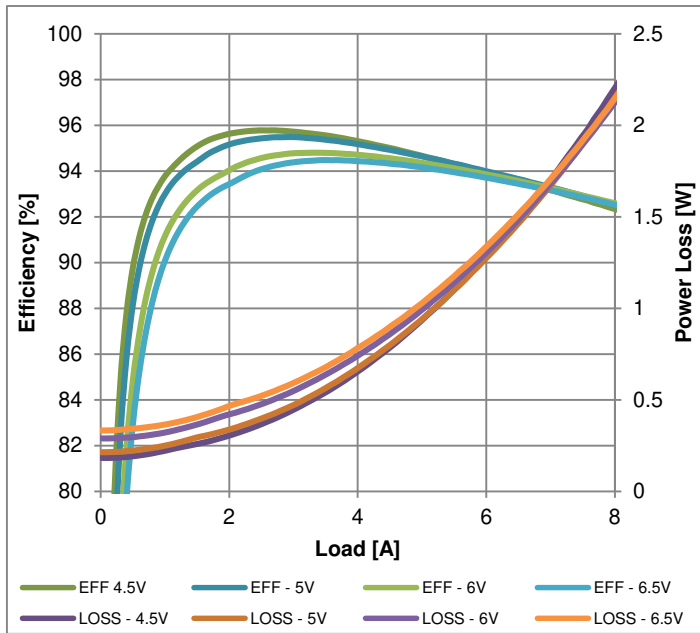


Figure 7: Efficiency – $V_{OUT} = 3.3V$, various V_{OUT} ,
 $f = 1.5MHz$

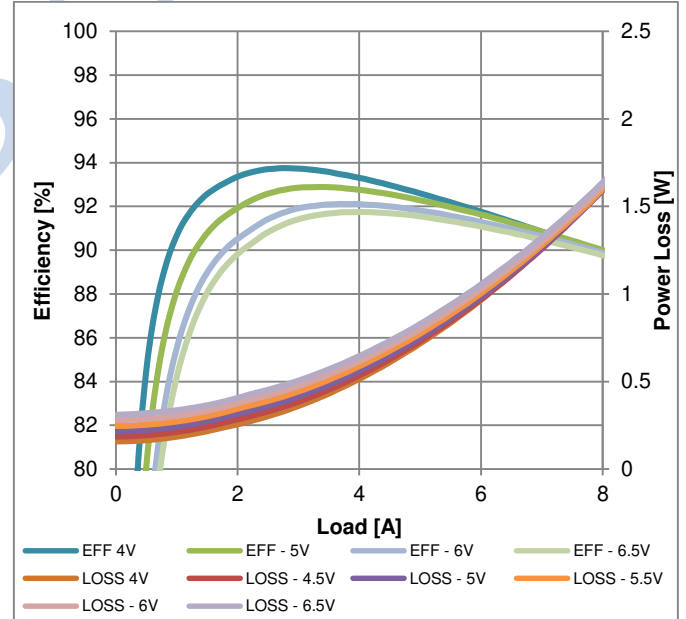


Figure 8: Efficiency – $V_{OUT} = 1.8V$, various V_{OUT} ,
 $T = -40^{\circ}C$

Typical Performance Curves (Continued)

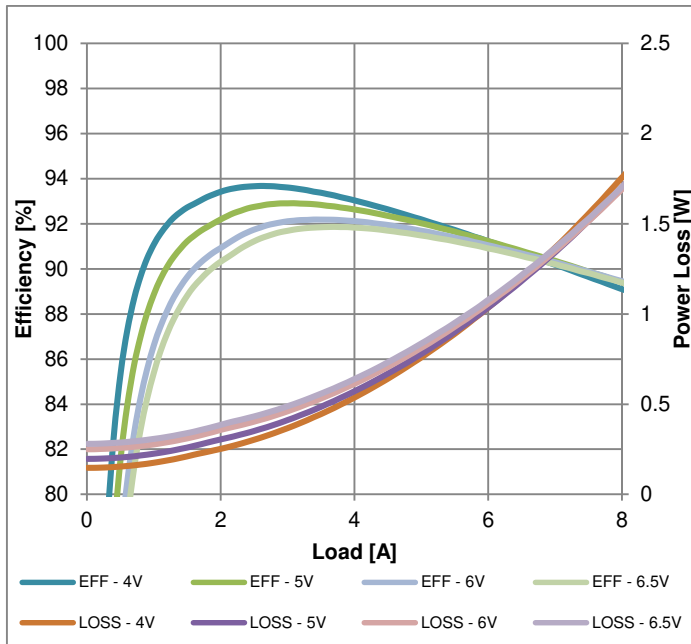


Figure 9: Efficiency – $V_{OUT} = 1.8V$, various V_{OUT} ,
 $T = +25^{\circ}C$

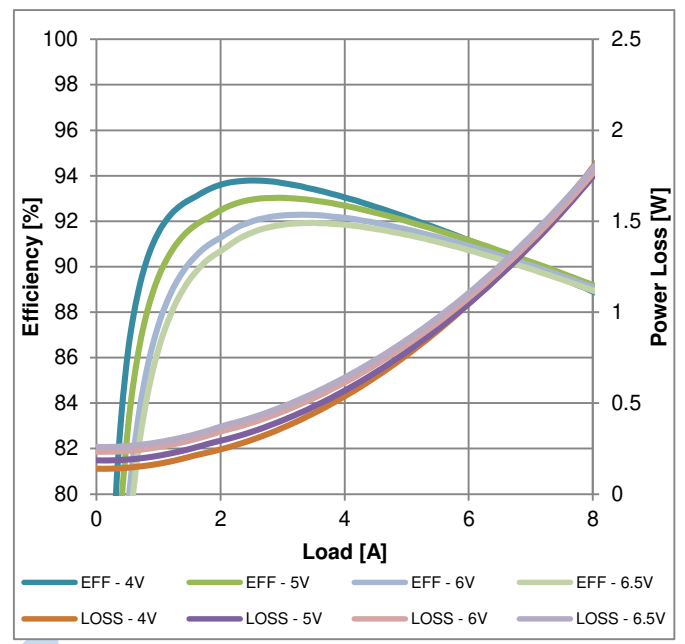


Figure 10: Efficiency – $V_{OUT} = 1.8V$, various V_{OUT} ,
 $T = +85^{\circ}C$

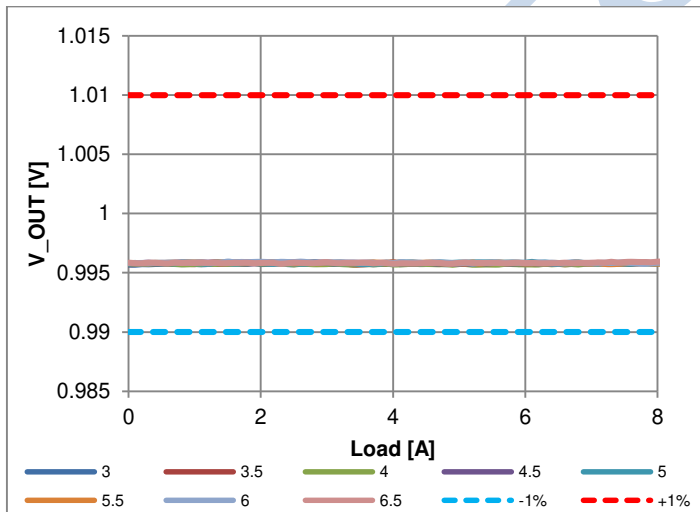


Figure 11: Load and Line regulation, $T = -40^{\circ}C$

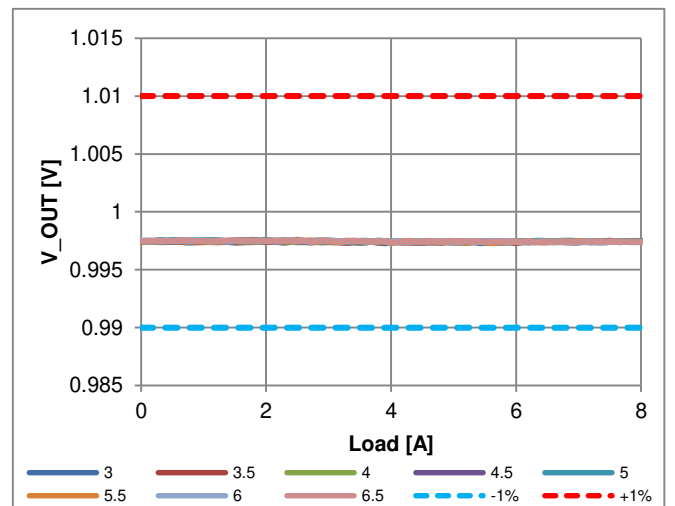


Figure 12: Load and Line regulation, $T = +25^{\circ}C$

Typical Performance Curves (Continued)

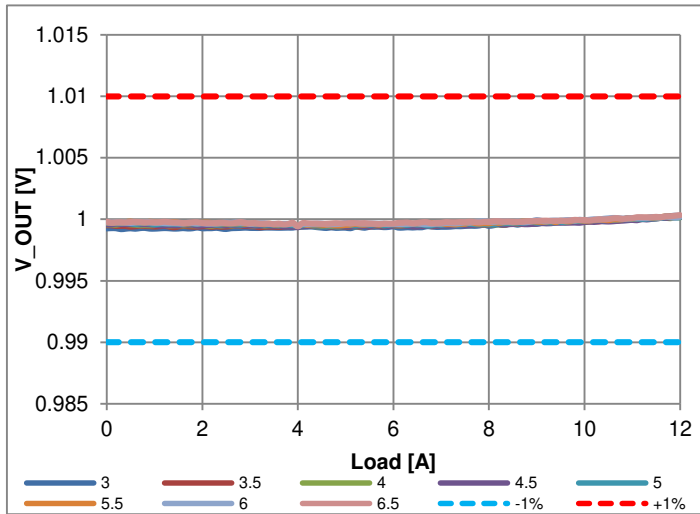


Figure 13: Load and Line regulation, T = +85°C

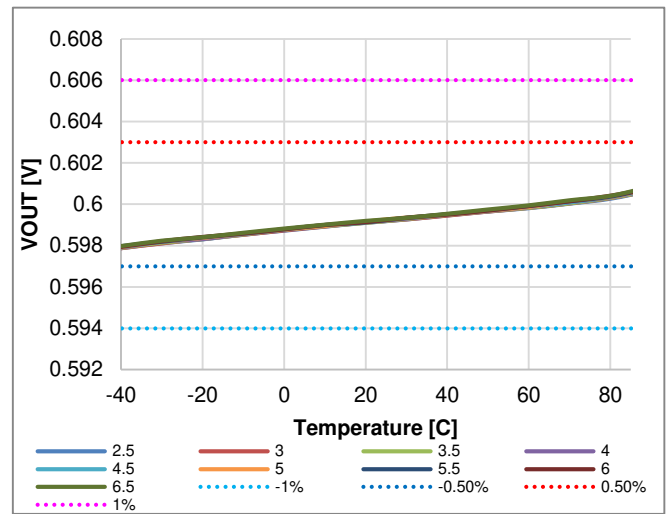


Figure 14: Line regulation over Temperature

Typical Performance Characteristics

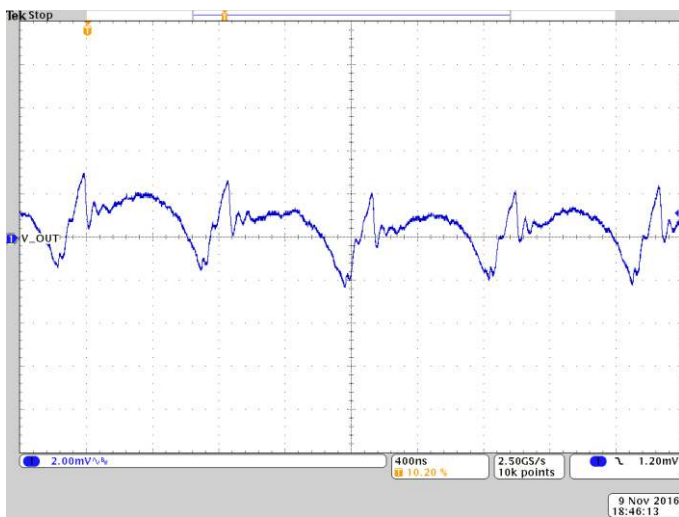


Figure 15: Output ripple $V_{IN} = 5V$, $V_{OUT} = 1V$

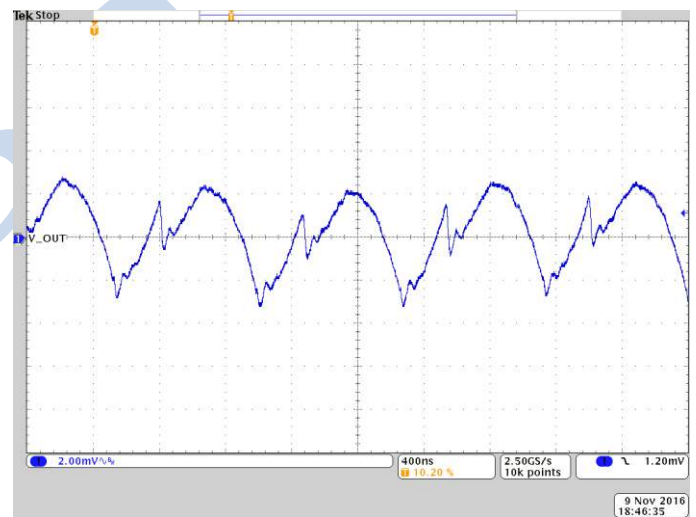


Figure 16: Output ripple $V_{IN} = 5V$, $V_{OUT} = 1.8V$

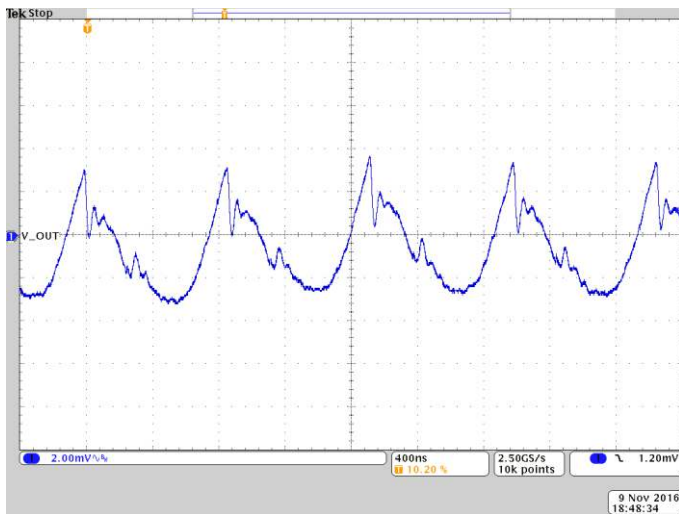


Figure 17: Output ripple $V_{IN} = 5V$, $V_{OUT} = 3.3V$

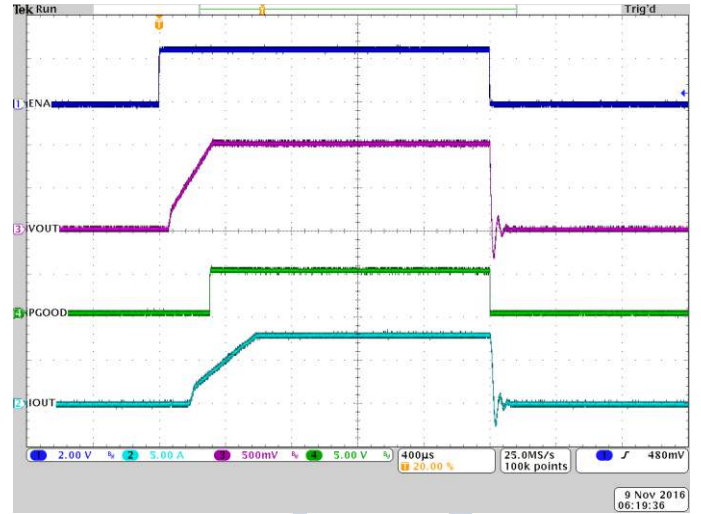


Figure 18: Startup $V_{IN} = 5V$, $V_{OUT} = 1V$, $I_L = 8A$

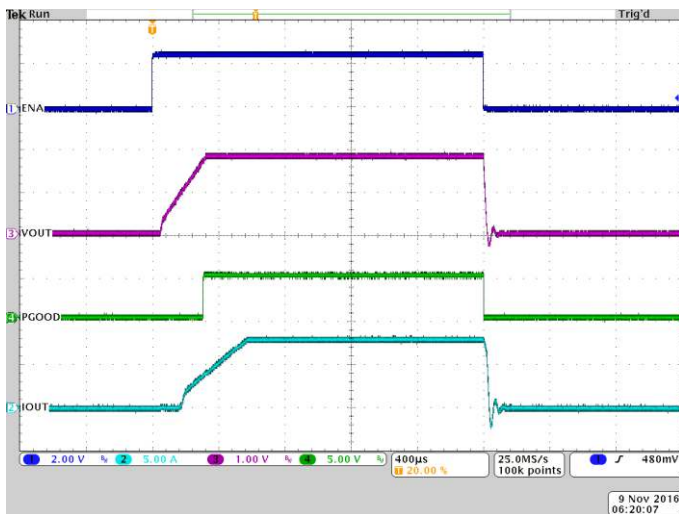


Figure 19: Startup $V_{IN} = 5V$, $V_{OUT} = 1.8V$, $I_{LOAD} = 8A$

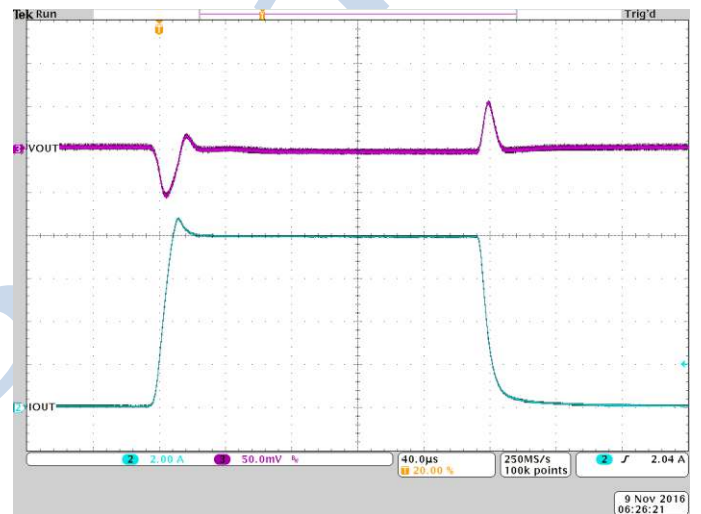


Figure 20: 0/8A load transient

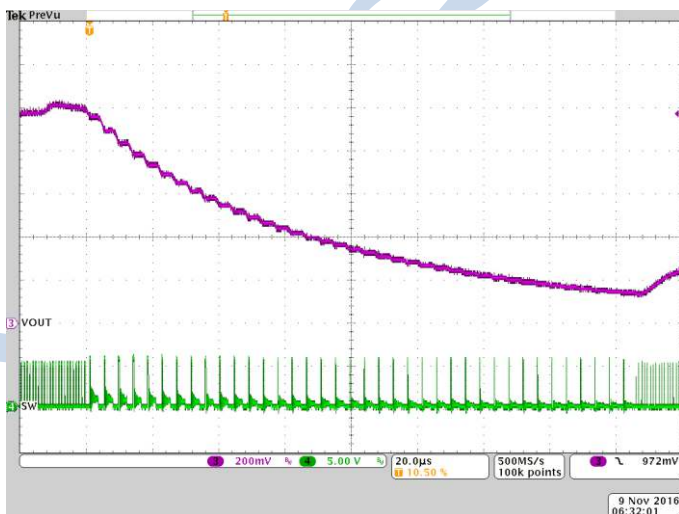


Figure 21: RCL protection activated by forcing the SS pin

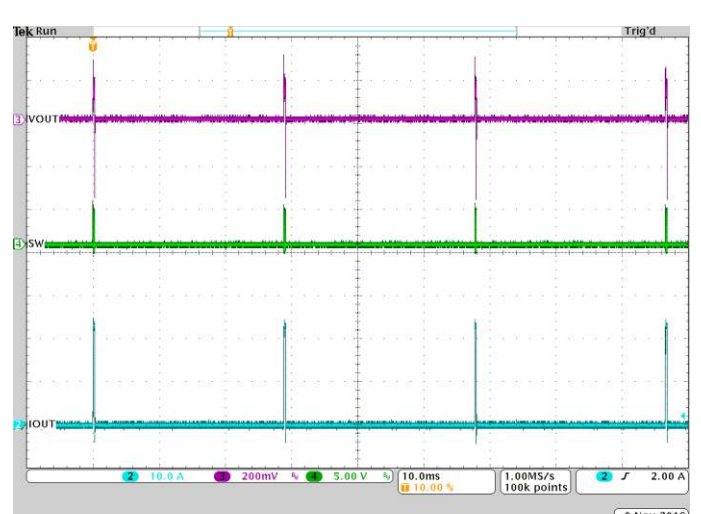
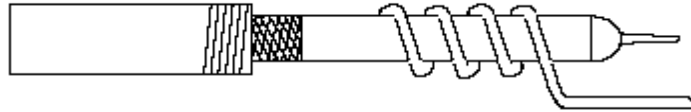


Figure 22: Hiccup mode during short-circuit protection

Test Recommendations

In order to get accurate measurements for sensitive nodes, small loop area (small antennae) are recommended. Besides the built-in low inductance of the ground, the small loop area will collect less EMI than the standard oscilloscope ground cables.



The EVAL board provides **3 test-points suitable** for connecting the oscilloscope probe as described above; these are:

- **TP28** – for the Switch Node (SW)
- **TP21** – for the Output Voltage (V_{OUT})
- **TP22** – for the Input Voltage (V_{IN}).

Contact Information

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