ON Semiconductor

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Configurable Multifunction Gate

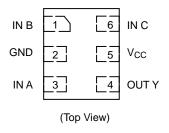
The NLX1G97 MiniGate $^{\text{M}}$ is an advanced high-speed CMOS multifunction gate. The device allows the user to choose logic functions MUX, AND, OR, NAND, NOR, INVERT and BUFFER. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

The NLX1G97 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.3 \text{ ns (Typ)} @ V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu A$ (Maximum) at $T_A = 25^{\circ}C$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- These are Pb-Free Devices

PIN ASSIGNMENTS





ON Semiconductor®

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MARKING DIAGRAMS



UDFN6 1.0 x 1.0 CASE 517BX





UDFN6 1.2 x 1.0 CASE 517AA





UDFN6 1.45 x 1.0 CASE 517AQ



F = Specific Device CodeM = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

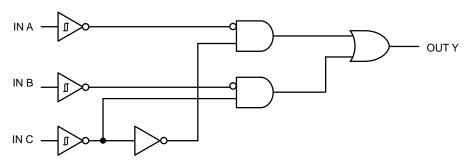


Figure 1. Function Diagram

PIN ASSIGNMENT

1	IN B
2	GND
3	IN A
4	OUT Y
5	V _{CC}
6	IN C

FUNCTION TABLE*

	Output		
А	В	С	Υ
L	L	L	L
L	L	Н	L
L	Н	L	Н
L	Н	Н	L
Н	L	L	L
Н	L	Н	Н
Н	Н	L	Н
Н	Н	Н	Н

^{*}To select a logic function, please refer to "Logic Configurations section".

LOGIC CONFIGURATIONS

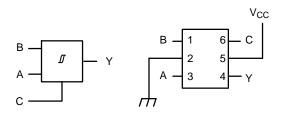


Figure 2. 2-Input MUX

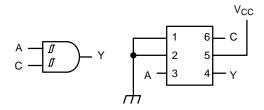
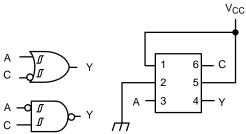
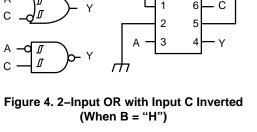


Figure 3. 2-Input AND (When B = "L")





 V_{CC} - C 2

Figure 6. 2-Input OR (When A ="H")

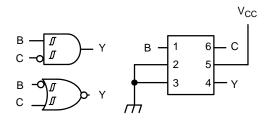


Figure 5. 2-Input AND with Input C Inverted (When A = "L")

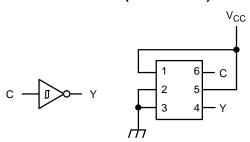


Figure 7. Inverter (When A = "L" and B = `"H")

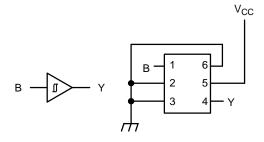


Figure 8. Buffer (When A = C = "L")

MAXIMUM RATINGS

Symbol	Para	ameter	Value	Unit		
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V		
V _{IN}	DC Input Voltage		-0.5 to +7.0	V		
V _{OUT}	DC Output Voltage	DC Output Voltage				
I _{IK}	DC Input Diode Current	V _{IN} < GND	-50	mA		
I _{OK}	DC Output Diode Current	V _{OUT} < GND	-50	mA		
Io	DC Output Source/Sink Current	±50	mA			
Icc	DC Supply Current Per Supply Pin	± 100	mA			
I _{GND}	DC Ground Current per Ground Pin	±100	mA			
T _{STG}	Storage Temperature Range		-65 to +150	°C		
TL	Lead Temperature, 1 mm from Case to	or 10 Seconds	260	°C		
TJ	Junction Temperature Under Bias		150	°C		
MSL	Moisture Sensitivity		Level 1			
F _R	Flammability Rating Oxygen	Index: 28 to 34	UL 94 V-0 @ 0.125 in			
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V		
I _{LATCHUP}	Latchup Performance Above V _{CC} and	Below GND at 125°C (Note 5)	±500	mA		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace no air flow.

- 2. Tested to EIA/JESD22-A114-A.
- 3. Tested to EIA/JESD22-A115-A.
- 4. Tested to JESD22-C101-A.
- 5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Paramo	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage	Positive DC Supply Voltage			
V _{IN}	Digital Input Voltage	0	5.5	V	
V _{OUT}	Output Voltage	0	5.5	V	
T _A	Operating Free–Air Temperature	- 55	+125	°C	
Δt/ΔV	Input Transition Rise or Fall Rate	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0 0 0	No Limit No Llmit No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

			V _{CC}	7	Γ _A = 25°	C	T _A ≤	+85°C		55°C to 25°C	
Symbol	Parameter	Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{T+}	Positive		1.65	0.79		1.16		1.16		1.16	V
	Threshold Voltage		2.3	1.11		1.56		1.56		1.56	1
			3.0	1.5		1.87		1.87		1.87	1
			4.5	2.16		2.74		2.74		2.74	
			5.5	2.61		3.33		3.33		3.33	
V_{T-}	Negative		1.65	0.35		0.62	0.35		0.35		V
	Threshold Voltage		2.3	0.58		0.87	0.58		0.58		1
	voltage		3.0	0.84		1.19	0.84		0.84		
			4.5	1.41		1.9	1.41		1.41		
			5.5	1.78		2.29	1.78		1.78		1
V _H	Hysteresis		1.65	0.30		0.62	0.30	0.62	0.30	0.62	V
	Voltage		2.3	0.40		0.8	0.40	0.8	0.40	0.8	1
			3.0	0.53		0.87	0.53	0.87	0.53	0.87	1
			4.5	0.71		1.04	0.71	1.04	0.71	1.04	1
			5.5	0.8		1.2	0.8	1.2	8.0	1.2	1
V _{OH}	Minimum High-Level	$V_{IN} = V_{T-MIN} \text{ or } V_{T+MAX}$ $I_{OH} = -50 \mu\text{A}$	1.65 – 5.5	V _{CC} - 0.1			V _{CC} - 0.1		V _{CC} - 0.1		V
	Output Voltage	$V_{IN} = V_{T-MIN}$ or V_{T+MAX}									
		$I_{OH} = -4 \text{ mA}$	1.65	1.2			1.2		1.2		
		$I_{OH} = -8 \text{ mA}$	2.3	1.9			1.9		1.9		
		I _{OH} = -16 mA	3.0	2.4			2.4		2.4		
		$I_{OH} = -24 \text{ mA}$	3.0	2.3			2.3		2.3		
		$I_{OH} = -32 \text{ mA}$	4.5	3.8			3.8		3.8		
V _{OL}	Maximum Low-Level	$V_{IN} = V_{T-MIN} \text{ or } V_{T+MAX}$ $I_{OL} = 50 \mu\text{A}$	1.65 – 5.5			0.1		0.1		0.1	V
	Output Voltage	$V_{IN} = V_{T-MIN}$ or V_{T+MAX}									1
		I _{OL} = 4 mA	1.65			0.45		0.45		0.45	
		I _{OL} = 8 mA	2.3			0.3		0.3		0.3	
		I _{OL} = 16 mA	3.0			0.4		0.4		0.4	
		I _{OL} = 24 mA	3.0			0.55		0.55		0.55	1
		I _{OL} = 32 mA	4.5			0.55		0.55		0.55	1
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μΑ
I _{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			1.0		10		10	μΑ

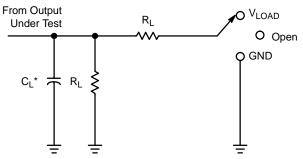
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$)

				٦	Γ _A = 25°(;	T _A ≤	+85°C	T _A = - to +1	-55°C 25°C	
Symbol	Parameter	V _{CC} (V)	Test Condition	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} ,	Propagation Delay,	1.65 – 1.95		3.2	8.6	14.4	3.2	14.4	3.2	14.4	ns
t _{PHL}	Any Input to Output Y (See Test Circuit)	2.3 – 2.7		2.0	5.1	8.3	2.0	8.3	2.0	8.3	
		3.0 – 3.6		1.5	3.9	6.3	1.5	6.3	1.5	6.3	
		4.5 – 5.5		1.1	3.3	5.1	1.1	5.1	1.1	5.1	
C _{IN}	Input Capacitance				3.5						pF
C _{PD}	Power Dissipation Capacitance (Note 6)	5.0	f = 10 MHz		22						pF

^{6.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no–load dynamic power consumption: P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

TEST CIRCUIT AND VOLTAGE WAVEFORMS



Test	S 1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V_{LOAD}
t _{PHZ} /t _{PZH}	GND

Figure 9. Load Circuit

	Inputs						
V _{CC}	VI	t _r /t _f	V _M	V_{LOAD}	CL	R_{L}	V_Δ
1.8 V ± 0.15 V	V _{CC}	≤ 2 ns	V _{CC} /2	2 x V _{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V _{CC}	≤ 2 ns	V _{CC} /2	2 x V _{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5.5 V ± 0.5 V	V _{CC}	≤ 2.5 ns	V _{CC} /2	2 x V _{CC}	50 pF	500 Ω	0.3 V

 $^{^{\}star}C_{L}$ includes probes and jig capacitance.

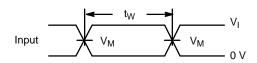


Figure 10. Voltage Waveforms Pulse Duration

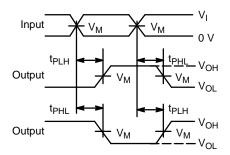


Figure 12. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

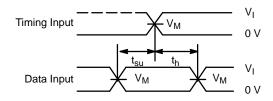


Figure 11. Voltage Waveforms Setup and Hold Times

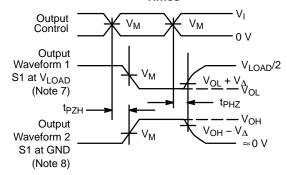


Figure 13. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling

- 7. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
- 8. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
- 9. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$.
- 10. The outputs are measured one at a time, with one transition per measurement.
- 11. All parameters are waveforms are not applicable to all devices.

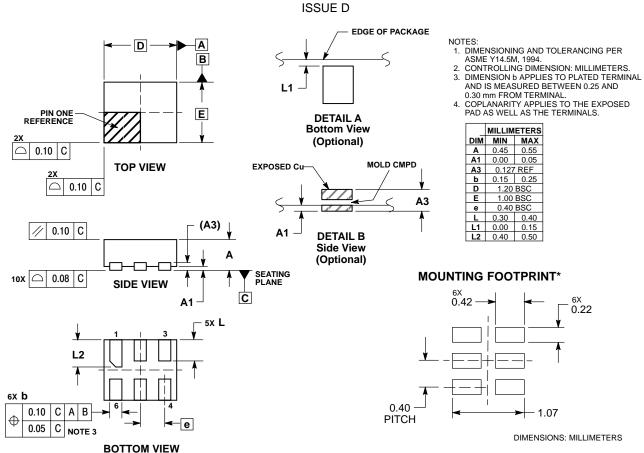
ORDERING INFORMATION

Device	Package	Shipping [†]
NLX1G97MUTCG	UDFN6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G97AMUTCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G97CMUTCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

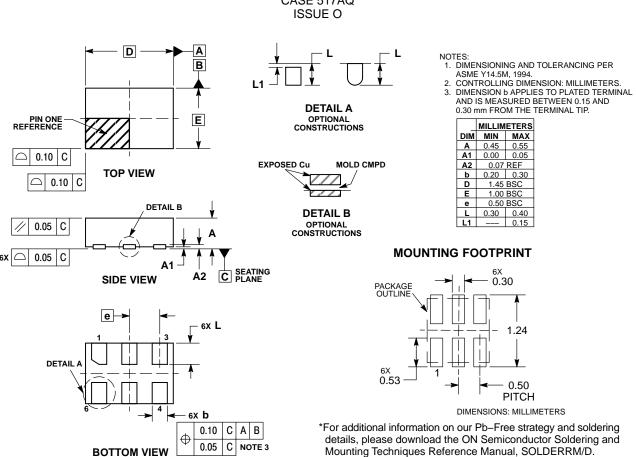
UDFN6, 1.2x1.0, 0.4PCASE 517AA-01



^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

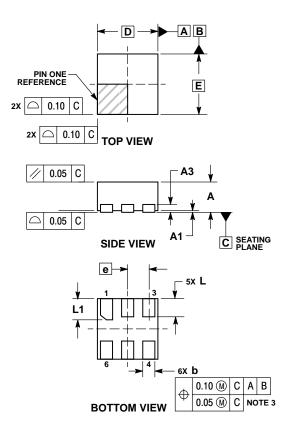
PACKAGE DIMENSIONS

UDFN6 1.45x1.0, 0.5P CASE 517AQ



PACKAGE DIMENSIONS

UDFN6 1.0x1.0. 0.35P CASE 517BX **ISSUE O**

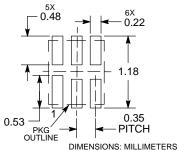


NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP. PACKAGE DIMENSIONS EXCLUSIVE OF
- BURRS AND MOLD FLASH.

	MILLIMETERS						
DIM	MIN	MAX					
Α	0.45	0.55					
A1	0.00	0.05					
A3	0.13 REF						
b	0.12	0.22					
D	1.00 BSC						
E	1.00 BSC						
е	0.35 BSC						
L	0.25	0.35					
11	0.30	0.40					

RECOMMENDED **SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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