PSMN020-100YS

N-channel 100V 20.5mΩ standard level MOSFET in LFPAK

26 March 2014 — Product data sheet

1. General description

Standard level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

4. Quick reference data

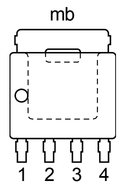
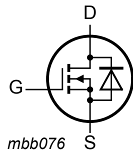
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	100	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; Fig. 2	-	-	43	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 1	-	-	106	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 15$ A; $T_j = 100$ °C; Fig. 13	-	-	37	mΩ
		$V_{GS} = 10$ V; $I_D = 15$ A; $T_j = 25$ °C; Fig. 14	-	15	20.5	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 30$ A; $V_{DS} = 50$ V; Fig. 15; Fig. 16	-	11.8	16.5	nC
$Q_{G(tot)}$	total gate charge		-	41	57.4	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 43 A; V_{sup} ≤ 100 V; unclamped; R_{GS} = 50 Ω; Fig. 4		-	-	103	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN020-100YS	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN020-100YS	20100

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	T_j ≤ 175 °C; T_j ≥ 25 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	106	W

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Symbol	Parameter	Conditions		Min	Max	Unit
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	30	A
		V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	43	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	172	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	43	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	172	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 43 A; V_{sup} ≤ 100 V; unclamped; R_{GS} = 50 Ω; Fig. 4		-	103	mJ

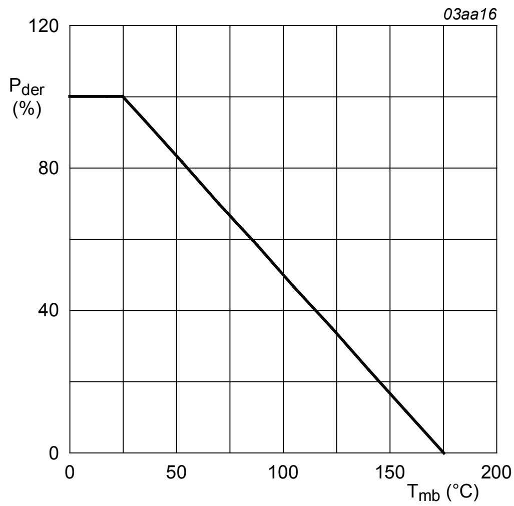

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

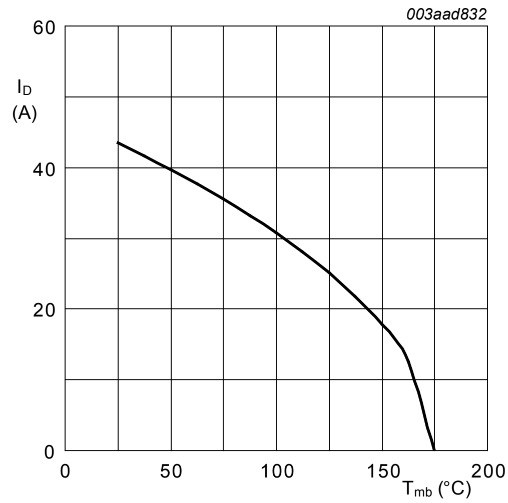

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10\,V$$

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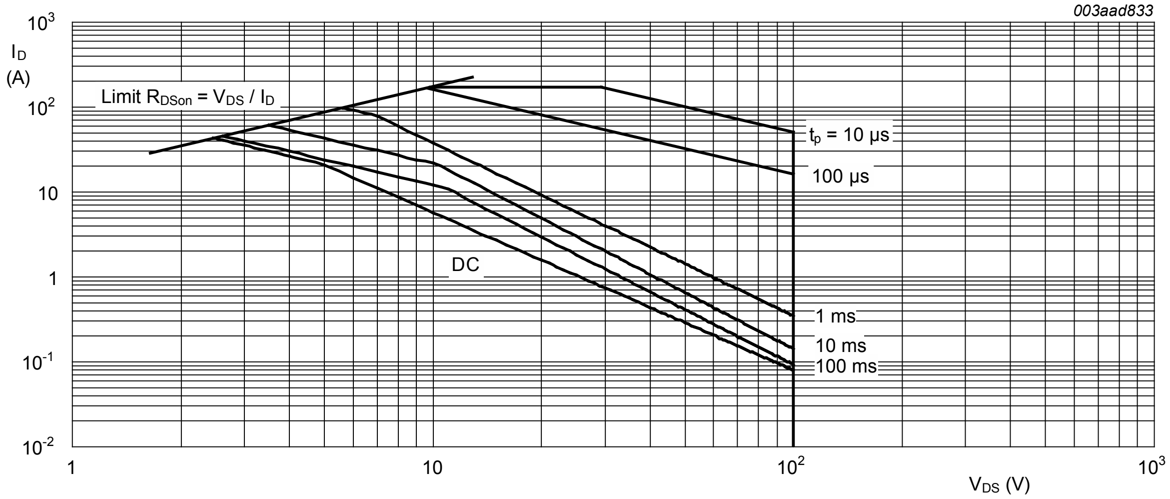
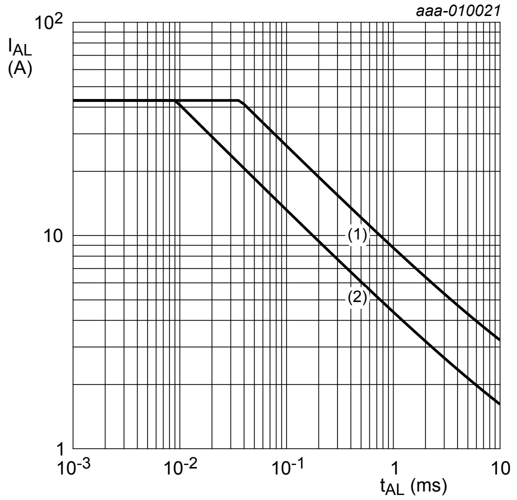


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25\,°C; I_{DM}$ is single pulse



(1) $T_{j(init)}$ = 25 °C; (2) $T_{j(init)}$ = 100 °C

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.63	1.42	K/W

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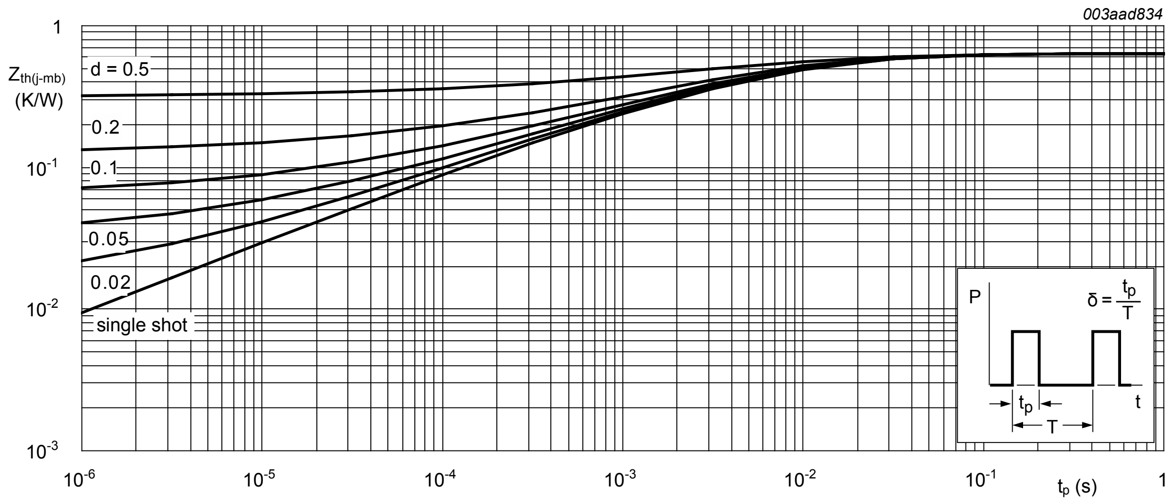

Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 11		0.95	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 12; Fig. 11		2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 11		-	-	4.6	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	-	100	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.06	2	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 100 °C; Fig. 13		-	-	37	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 175 °C; Fig. 13		-	39	57.4	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; Fig. 14		-	15	20.5	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz		-	0.6	1.2	Ω

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 30 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 15; Fig. 16		-	41	57.4	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	34	47.6	nC
Q_{GS}	gate-source charge	I_D = 30 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 15; Fig. 16		-	10.2	14.3	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	I_D = 30 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 15		-	6.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	3.4	-	nC
Q_{GD}	gate-drain charge	I_D = 30 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 15; Fig. 16		-	11.8	16.5	nC
$V_{GS(pl)}$	gate-source plateau voltage	V_{DS} = 50 V; Fig. 15; Fig. 16		-	4.4	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 17		-	2210	2980	pF
C_{oss}	output capacitance			-	167	226	pF
C_{rss}	reverse transfer capacitance			-	103	144	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 1.7 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω; T_j = 25 °C		-	17.4	26.1	ns
t_r	rise time			-	18.1	27.2	ns
$t_{d(off)}$	turn-off delay time			-	37.8	56.7	ns
t_f	fall time			-	15	22.5	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 18		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V		-	52	68	ns
Q_r	recovered charge			-	112	146	nC

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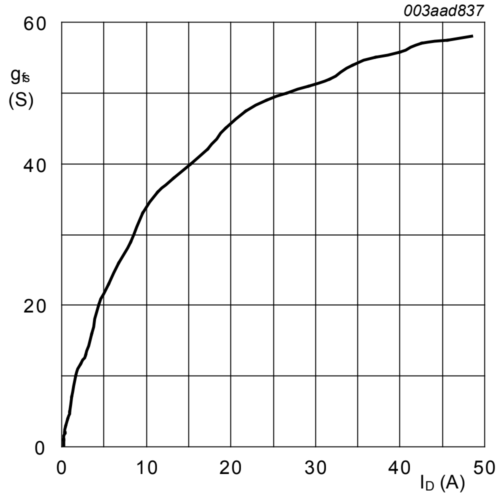

Fig. 6. **Forward transconductance as a function of drain current; typical values**

$T_j = 25\,°C; V_{DS} = 15\,V$

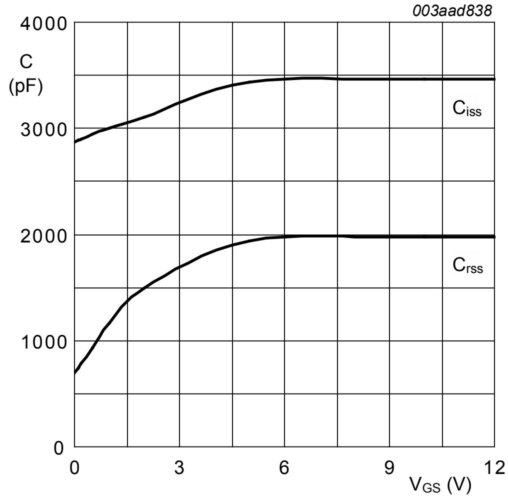

Fig. 7. **Input and reverse transfer capacitances as a function of gate-source voltage; typical values**

$V_{DS} = 0\,V; f = 1\,MHz$

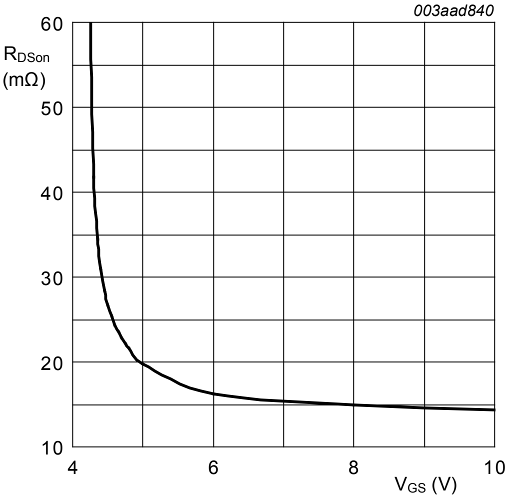

Fig. 8. **Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25\,°C; I_D = 10\,A$

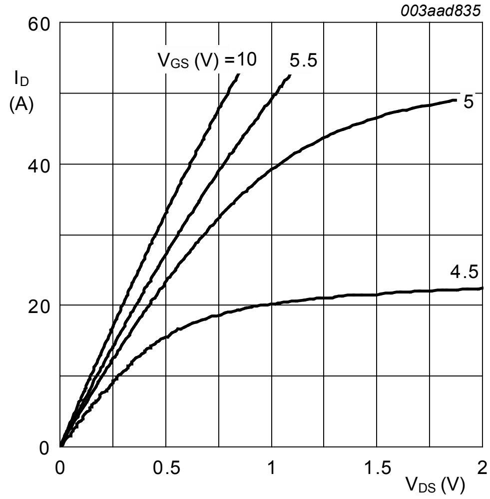

Fig. 9. **Output characteristics: drain current as a function of drain-source voltage; typical values**

$T_j = 25\,°C$

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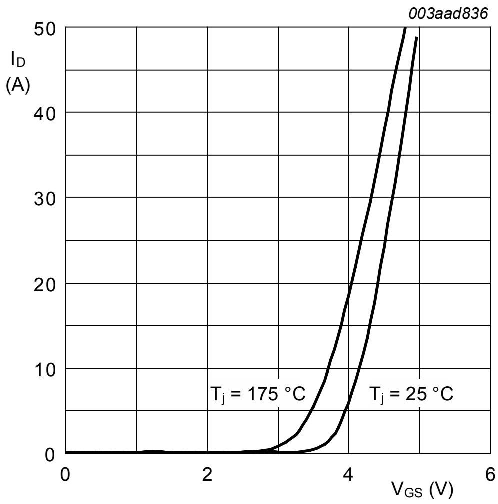

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$$V_{DS} > I_D \times R_{DSon}$$

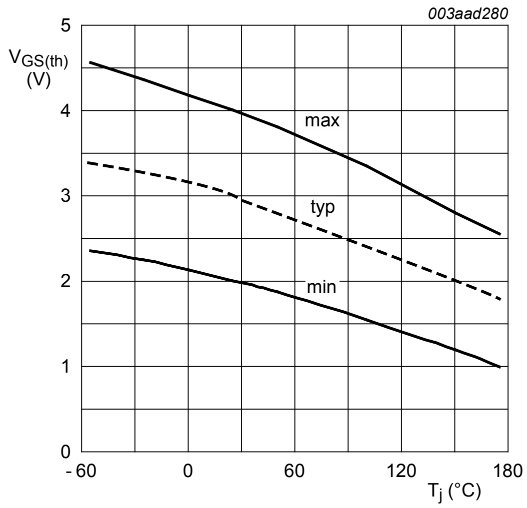

Fig. 11. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1\ \text{mA};\ V_{DS} = V_{GS}$$

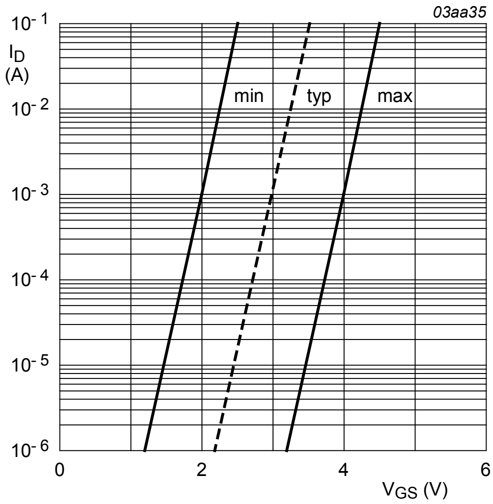

Fig. 12. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25\,°C; V_{DS} = 5V$$

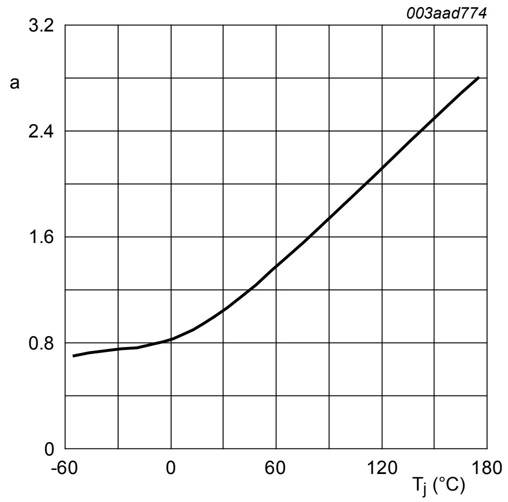

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

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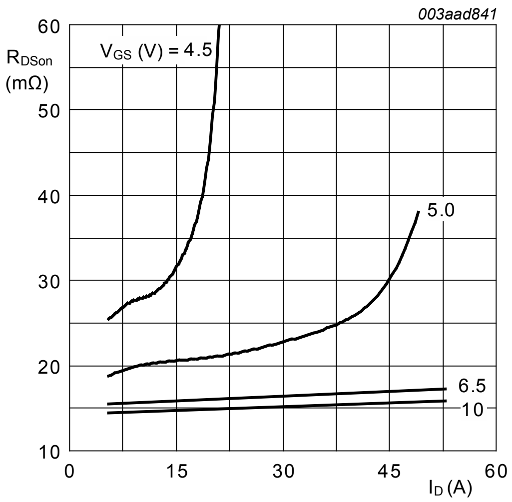

Fig. 14. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

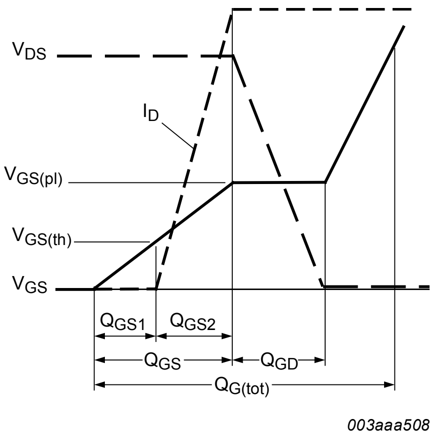

Fig. 15. Gate charge waveform definitions

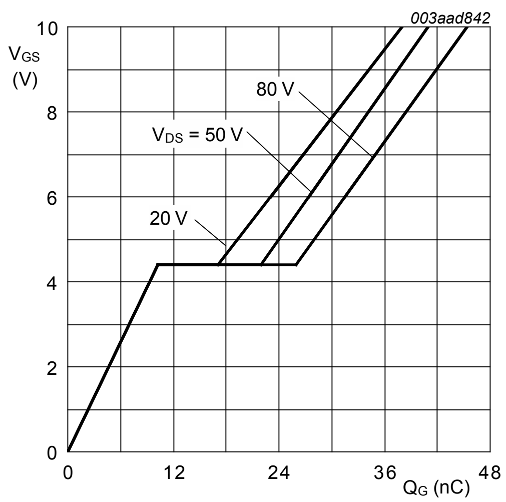

Fig. 16. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C; I_D = 30 A$

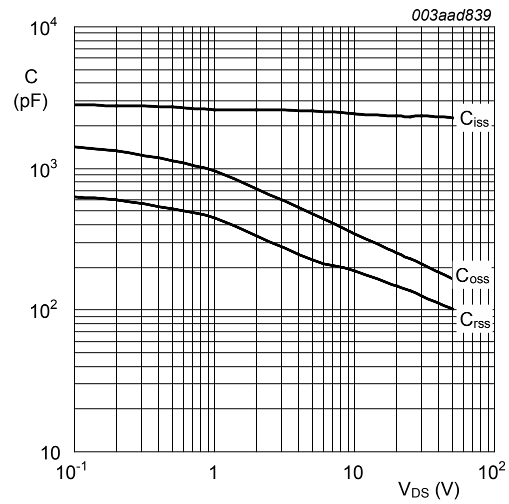

Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0 V; f = 1 MHz$

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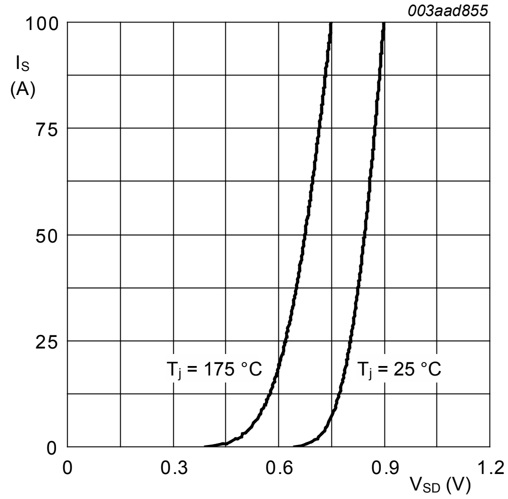

Fig. 18. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0\,V$$

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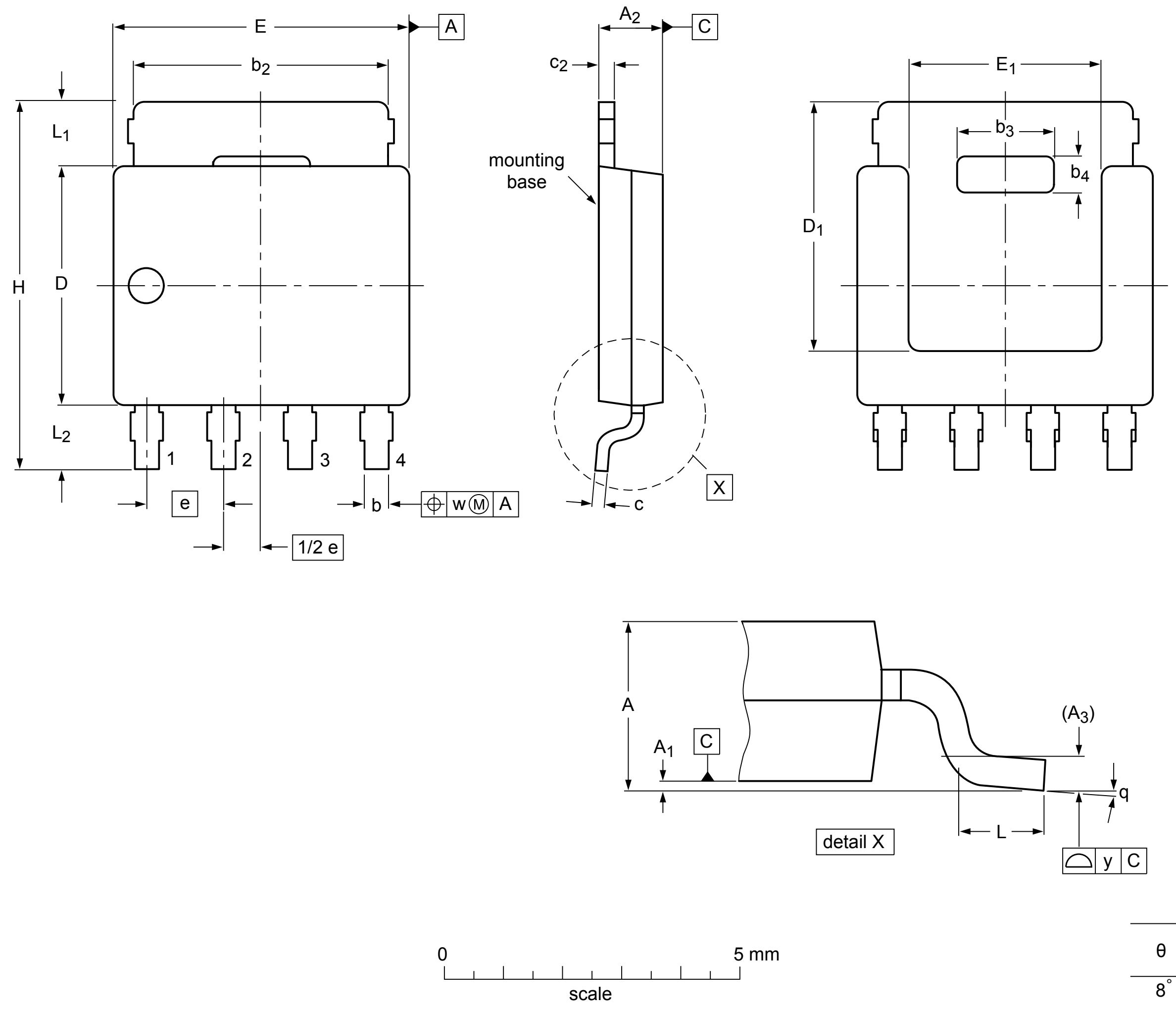
11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



θ
8°
0°

Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
	nom				0.25											1.27					0.25	0.1
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 19. Package outline LFPAK56; Power-SO8 (SOT669)

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12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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