HC5549

Low Power SLIC with Battery Switch

FN4539
Rev 3.00
October 21, 2004

The HC5549 Subscriber line interface circuit is a 100V diellectrically isolated bipolar integrated circuit for use in short loop ISDN, PABX and Pairgain applications. The HC5549 has been optimized for low power as required for battery backed remote terminals or for applications requiring emergency powering from the line such as European ISDN NT1+ designs.

A high and low voltage battery supply may be connected to the HC5549 so that power dissipation can be lowered in the off hook condition in these short loop applications. The high battery supply can be used in the on-hook condition to allow interfacing to fax and answering machines that require 48V to detect end of call status. The HC5549 also has a low power standby state with very low power consumption (35mW) resulting in exceptionally low battery drain while providing continued loop supervision.

The HC5549 provides loop current, ground key and ring trip detect functions as well as an alarm output to indicate thermal overload.

2-wire to 4-wire and 4-wire to 2-wire conversion is provided and impedance matching is achieved using a single external network. The HC5549 is compatible with dual and single supply switched capacitor or DSP codec/filters.

Features

- Dual Battery Operation
- Single Additional +5V Supply
- Low Standby Power Consumption (48V, 35mW)
- On Hook Transmission
- Tip and Ring Disconnect
- Soft or Hard Polarity Reversal
- Supports 12kHz or 16kHz Pulse Metering
- Ring Relay Driver
- On Chip 2-wire AC/DC Loopback
- 0°C to 70°C or -40°C to 85°C Ambient Temp Range
- Low External Component Count
- Pb-Free Available (RoHS Compliant)

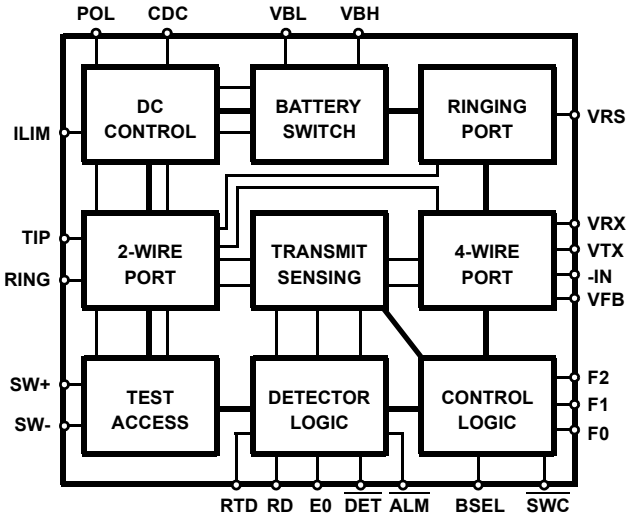
Applications

- ISDN NT1+ Terminals
- Pairgain Remote Termination
- PABX and Key Systems

Related Literature

- AC SPICE Macromodel

Block Diagram



Ordering Information (PLCC Package Only)

PART NUMBER	48V	BAT SW	POL REV	RING DELAY DRIVER	2W LOOP BACK	LB = 53dB	TEMP. RANGE °C	PACKAGE	PKG. DWG. #
HC5549CM	•	•	•	•	•	•	0 to 70	28 Ld PLCC	N28.45
HC5549CMZ (Note)	•	•	•	•	•	•	0 to 70	28 Ld PLCC (Pb-free)	N28.45
HC5549IM	•	•	•	•	•	•	-40 to 85	28 Ld PLCC	N28.45

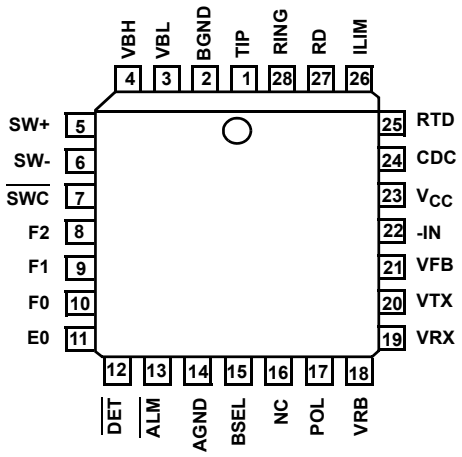
NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Device Operating Modes

OPERATING MODE	F2	F1	F0	E0 = 1	E0 = 0	DESCRIPTION
Low Power Standby	0	0	0	SHD	GKD	MTU compliant standby mode with active loop detector.
Forward Active	0	0	1	SHD	GKD	Forward battery loop feed.
Unused	0	1	0	n/a	n/a	Reserved internal test mode.
Reverse Active	0	1	1	SHD	GKD	Reverse battery loop feed.
Ringing	1	0	0	RTD	RTD	Enabler internal ring trip detector.
Unused	1	0	1	n/a	n/a	Reserved internal test mode.
Unused	1	1	0	n/a	n/a	Reserved internal test mode.
Power Denial	1	1	1	n/a	n/a	Device shutdown.

Pinout

HC5549 (PLCC)
TOP VIEW



Absolute Maximum Ratings $T_A = 25°C$

Maximum Supply Voltages
- V_{CC} . . . . . -0.5V to +7V
- V_{CC} - V_{BAT} 80V

Maximum Tip/Ring Negative Voltage Pulse (Note 2) . . . . . -115V
Maximum Tip/Ring Positive Voltage Pulse (Note 2) 8V
Uncommitted Switch Voltage . . . . . -80V
ESD (Human Body Model) 500V

Operating Conditions

Temperature Range
- Industrial (I suffix) . . . . . -40°C to 85°C
- Commercial (C suffix) . . . . . 0°C to 75°C

Positive Power Supply (V_{CC}) . . . . . +5V ±5%
Negative Power Supply (V_{BH}, V_{BL}) (180, 181, 182) . . -16V to -80V
Uncommitted Switch (loop back or relay driver) . . . . . +5V to -80V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
PLCC Package	53

Maximum Junction Temperature Plastic . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(PLCC - Lead Tips Only)

Die Characteristics

Substrate Potential . . . . . V_{BAT}
Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Characterized with 2 x 10µs, and 10 x 1000µs first level lightning surge waveforms (GR-1089-CORE).
3. These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

Electrical Specifications

Unless Otherwise Specified, T_A = -40°C to 85°C, V_{BL} = -24V, V_{BH} = -48V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC Parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RINGING PARAMETERS					
VRB Input Impedance (Note 3)		480	-	-	kΩ
AC TRANSMISSION PARAMETERS (Forward Active and Reverse Active, BSEL = 0, unless otherwise specified.)					
Receive Input Impedance (Note 3)		160	-	-	kΩ
Transmit Output Impedance (Note 3)		-	-	1	Ω
4-Wire Port Overload Level	THD = 1%	3.1	3.5	-	V_{PK}
2-Wire Port Overload Level	THD = 1%	3.1	3.5	-	V_{PK}
2-Wire Return Loss	300Hz ≤ f < 1kHz	25	32	-	dB
	1kHz ≤ f ≤ 3.4kHz	17	22	-	dB
Longitudinal Current Capability (Per Wire)	Test for False Detect	-	20	-	mA_{RMS}
	Test for False Detect, Low Power Standby, BSEL = 0	-	10	-	mA_{RMS}
2-Wire Longitudinal Balance	Tested per IEEE455-1985, with 368Ω per wire.	53	-	-	dB
4-Wire Longitudinal Balance	Tested per IEEE455-1985, with 368Ω per wire.	59	-	-	dB
4-Wire to 2-Wire Insertion Loss		-0.2	0	+0.3	-
2-Wire to 4-Wire Insertion Loss		-6.22	-6.02	-5.82	-
4-Wire to 4-Wire Insertion Loss		-6.32	-6.02	-5.82	dB
2-Wire to 4-Wire Level Linearity 4-Wire to 2-Wire Level Linearity Referenced to -10dBm	+3 to -40dBm, 1kHz	-	±0.025	-	dB
	-40 to -50dBm, 1kHz	-	±0.050	-	dB
	-50 to -55dBm, 1kHz	-	±0.100	-	dB
Idle Channel Noise 2-Wire	C-Message	-	16	19	dBrnC
	Psophometric	-	-74	-71	dBmp

Electrical Specifications Unless Otherwise Specified, T_A = -40°C to 85°C, V_{BL} = -24V, V_{BH} = -48V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC Parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC PARAMETERS					
Loop Current Limit Programming Range	Max Low Battery = -52V, BSEL = 0	15	-	45	mA
Loop Current Accuracy	I_L = 25mA, BSEL = 0	-	-	± 10	%
Loop Current During Low Power Standby	Forward polarity only.	17	-	26	mA
Open Circuit Voltage (|Tip - Ring|)	BSEL = 0	14	15.5	17	V
	BSEL = 1	37.5	40	42.5	V
Low Power Standby Open Circuit Voltage (Tip - Ring)	BSEL = 1	43	45	47	V
Ring Trip Programming Current Accuracy		-	-	± 10	%
Ring Trip Comparator Threshold		2.3	2.6	2.9	V
Switch Hook Programming Range		5	-	15	mA
Switch Hook Programming Accuracy		-	-	10	%
Dial Pulse Distortion		-	1	-	%
Ground Key Threshold		-	12	-	mA
Thermal Alarm Output	IC junction temperature	-	175	-	°C
RELAY DRIVER					
On Voltage	I_L = 45 mA	-	-	0.60	V
LOGIC INPUTS (F0, F1, F2, E0, SWC)					
Input Low Voltage		-	-	0.8	V
Input High Voltage		2.0	-	-	V
Input Low Current	V_{IL} = 0.4V	-20	-	-	µA
Input High Current	V_{IH} = 2.4V	-	-	5	µA
LOGIC OUTPUTS ($\overline{DET}$, $\overline{ALM}$)					
Output Low Voltage	I_{OL} = 5mA	-	-	0.4	V
Output High Voltage	I_{OH} = 100µA	2.4	-	-	V
SUPPLY CURRENTS (Supply currents not listed are considered negligible and do not contribute significantly to total power dissipation. All measurements made under open circuit load conditions.)					
Low Power Standby	I_{CC}	2.0	3.7	6.0	mA
	I_{BH}, BSEL = 1	-	0.375	0.600	mA
Forward or Reverse (Note 5)	I_{CC}	2.5	4.0	6.0	mA
	I_{BL}, BSEL = 0	-	1.0	2.5	mA
Forward	I_{CC}	3.5	4.5	8.0	mA
	I_{BL}, BSEL = 1	-	0.7	2.0	mA
	I_{BH}, BSEL = 1	-	1.0	2.5	mA
Power Denial	I_{CC}	0.5	3.0	6.0	mA
	I_{BL}, BSEL = 1 or 0	-	0.2	0.5	mA
Forward Lookback	I_{LL}	-	-	10.0	mA
	I_{BL}, V_{BL} = -24V	-	-	25.0	mA

Electrical Specifications Unless Otherwise Specified, T_A = -40°C to 85°C, V_{BL} = -24V, V_{BH} = -48V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC Parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ON HOOK POWER DISSIPATION					
Forward or Reverse	BSEL = 0	-	44	60	mW
Forward or Reverse	BSEL = 1	-	90	150	mW
Low Power Standby	BSEL = 1	-	37	60	mW
OFF HOOK POWER DISSIPATION					
Forward or Reverse	BSEL = 0	-	290	310	mW
POWER SUPPLY REJECTION RATIO					
V_{CC} to 2-Wire	f = 300Hz	-	40	-	dB
	f = 1kHz	-	35	-	dB
	f = 3.4kHz	-	28	-	dB
V_{CC} to 4-Wire	f = 300Hz	-	45	-	dB
	f = 1kHz	-	43	-	dB
	f = 3.4kHz	-	33	-	dB
V_{BL} to 2-Wire	300Hz ≤ f ≤ 3.4kHz	-	30	-	dB
V_{BL} to 4-Wire	300Hz ≤ f ≤ 3.4kHz	-	35	-	dB
V_{BH} to 2-Wire	300Hz ≤ f ≤ 3.4kHz	-	33	-	dB
V_{BH} to 4-Wire	300Hz ≤ f ≤ 1kHz	-	40	-	dB
	1kHz < f ≤ 3.4kHz	-	45	-	dB

Design Equations

Loop Supervision Thresholds

SWITCH HOOK DETECT

The switch hook detect threshold is set by a single external resistor, R_{SH}. Equation 1 is used to calculate the value of R_{SH}.

$$R_{SH} = 600/I_{SH} \quad \text{(EQ. 1)}$$

The term I_{SH} is the desired DC loop current threshold. The loop current threshold programming range is from 5mA to 15mA.

GROUND KEY DETECT

The ground key detector senses a DC current imbalance between the Tip and Ring terminals when the ring terminal is connected to ground. The ground key detect threshold is not externally programmable and is internally fixed to 12mA regardless of the switch hook threshold.

RING TRIP DETECT

The ring trip detect threshold is set by a single external resistor, R_{RT}. I_{RT} should be set between the peak ringing current and the peak off hook current while still ringing.

$$R_{RT} = 1800/I_{RT} \quad \text{(EQ. 2)}$$

The capacitor C_{RT}, in parallel with R_{RT}, will set the ring trip response time.

Loop Current Limit

The loop current limit of the device is programmed by the external resistor R_{IL}. The value of R_{IL} can be calculated using Equation 3.

$$R_{IL} = \frac{1760}{I_{LIM}} \quad \text{(EQ. 3)}$$

The term I_{LIM} is the desired loop current limit. The loop current limit programming range is from 15mA to 45mA.

Impedance Matching

The impedance of the device is programmed with the external component R_S. R_S is the gain setting resistor for the feedback amplifier that provides impedance matching. If complex impedance matching is required, then a complex network can be substituted for R_S.

RESISTIVE IMPEDANCE SYNTHESIS

The source impedance of the device, Z_O, can be calculated in Equation 4.

$$R_S = 400(Z_O) \quad \text{(EQ. 4)}$$

The required impedance is defined by the terminating impedance and protection resistors as shown in Equation 5.

$$Z_O = Z_L - 2R_P \quad \text{(EQ. 5)}$$

4-WIRE TO 2-WIRE GAIN

The 4-wire to 2-wire gain is defined as the receive gain. It is a function of the terminating impedance, synthesized impedance and protection resistors. Equation 6 calculates the receive gain, G_{42}.

$$G_{42} = -2\left(\frac{Z_L}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 6)}$$

When the device source impedance and protection resistors equals the terminating impedance, the receive gain equals unity.

2-WIRE TO 4-WIRE GAIN

The 2-wire to 4-wire gain (G_{24}) is the gain from tip and ring to the VTX output. The transmit gain is calculated in Equation 7.

$$G_{24} = -\left(\frac{Z_O}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 7)}$$

When the protection resistors are set to zero, the transmit gain is -6dB.

TRANSHYBRID GAIN

The transhybrid gain is defined as the 4-wire to 4-wire gain (G_{44}).

$$G_{44} = -\left(\frac{Z_O}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 8)}$$

When the protection resistors are set to zero, the transhybrid gain is -6dB.

COMPLEX IMPEDANCE SYNTHESIS

Substituting the impedance programming resistor, R_S, with a complex programming network provides complex impedance synthesis.

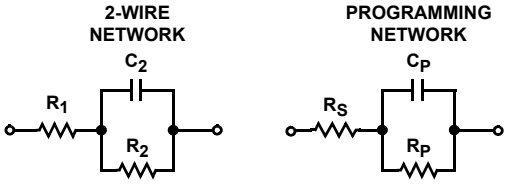


FIGURE 1. COMPLEX PROGRAMMING NETWORK

The reference designators in the programming network match the evaluation board. The component R_S has a different design equation than the R_S used for resistive impedance synthesis. The design equations for each component are provided below.

$$R_S = 400 \times (R_1 - 2(R_P)) \quad \text{(EQ. 9)}$$

$$R_P = 400 \times R_2 \quad \text{(EQ. 10)}$$

$$C_P = C_2/400 \quad \text{(EQ. 11)}$$

Low Power Standby

Overview

The low power standby mode (LPS, 000) should be used during idle line conditions. The device is designed to operate from the high battery during this mode. Most of the internal circuitry is powered down, resulting in low power dissipation. If the 2-wire (tip/ring) DC voltage requirements are not critical during idle line conditions, the device may be operated from the low battery. Operation from the low battery will decrease the standby power dissipation.

TABLE 1. DEVICE INTERFACES DURING LPS

INTERFACE	ON	OFF	NOTES
Receive		x	AC transmission, impedance matching and ringing are disabled during this mode.
Ringing		x	
Transmit		x	
2-Wire	x		Amplifiers disabled.
Loop Detect	x		Switch hook or ground key.

2-WIRE INTERFACE

During LPS, the 2-wire interface is maintained with internal switches and voltage references. The Tip and Ring amplifiers are turned off to conserve power. The device will provide MTU compliance, loop current and loop supervision. Figure 2 represents the internal circuitry providing the 2-wire interface during low power standby.

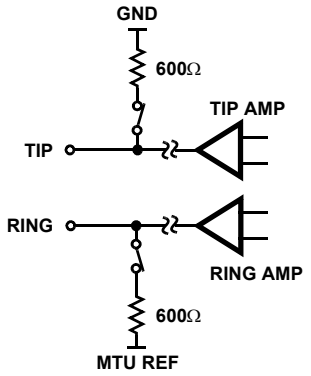


FIGURE 2. LPS 2-WIRE INTERFACE CIRCUIT DIAGRAM

MTU Compliance

Maintenance Termination Unit or MTU compliance places DC voltage requirements on the 2-wire terminals during idle line conditions. The minimum idle voltage is 42.75V. The high side of the MTU range is 56V. The voltage is expressed as the difference between Tip and Ring.

The Tip voltage is held near ground through a 600Ω resistor and switch. The Ring voltage is limited to a maximum of -49V (by MTU REF) when operating from either the high or low battery. A switch and 600Ω resistor connect the MTU reference to the Ring terminal. When the high battery

voltage exceeds the MTU reference of -49V (typically), the Ring terminal will be clamped by the internal reference. The same Ring relationships apply when operating from the low battery voltage. For high battery voltages (VBH) less than or equal to the internal MTU reference threshold:

$$V_{RING} = V_{BH} + 4 \quad \text{(EQ. 12)}$$

Loop Current

During LPS, the device will provide current to a load. The current path is through resistors and switches, and will be function of the off hook loop resistance (R_{LOOP}). This includes the off hook phone resistance and copper loop resistance. The current available during LPS is determined by Equation 13.

$$I_{LOOP} = (-1-(-49))/(600+600+R_{LOOP}) \quad \text{(EQ. 13)}$$

Internal current limiting of the standby switches will limit the maximum current to 20mA.

Another loop current related parameter is longitudinal current capability. The longitudinal current capability is reduced to $10mA_{RMS}$ per pin. The reduction in longitudinal current capability is a result of turning off the Tip and Ring amplifiers.

On Hook Power Dissipation

The on hook power dissipation of the device during LPS is determined by the operating voltages and quiescent currents and is calculated using Equation 14.

$$P_{LPS} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad \text{(EQ. 14)}$$

The quiescent current terms are specified in the electrical tables for each operating mode. Load power dissipation is not a factor since this is an on hook mode. Some applications may specify a standby current. The standby current may be a charging current required for modern telephone electronics.

Standby Current Power dissipation

Any standby line current, I_{SLC}, introduces an additional power dissipation term P_{SLC}. Equation 15 illustrates the power contribution is zero when the standby line current is zero.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| - 49 + 1 + I_{SLC} x 1200) \quad \text{(EQ. 15)}$$

If the battery voltage is less than -49V (the MTU clamp is off), the standby line current power contribution reduces to Equation 16.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| + 1 + I_{SLC} x 1200) \quad \text{(EQ. 16)}$$

Most applications do not specify charging current requirements during standby. When specified, the typical charging current may be as high as 5mA.

Forward Active

Overview

The forward active mode (FA, 001) is the primary AC transmission mode of the device. On hook transmission, DC loop feed and voice transmission are supported during forward active. Loop supervision is provided by either the switch hook detector (E0 = 1) or the ground key detector (E0 = 0). The device may be operated from either high or low battery for on-hook transmission and low battery for loop feed.

On-Hook Transmission

The primary purpose of on hook transmission will be to support caller ID and other advanced signalling features. The transmission over load level while on hook is $3.5V_{PEAK}$.

When operating from the high battery, the DC voltages at Tip and Ring are MTU compliant. The typical Tip voltage is -4V and the Ring voltage is a function of the battery voltage for battery voltages less than -60V as shown in Equation 17.

$$V_{RING} = V_{BH} + 4 \quad \text{(EQ. 17)}$$

Loop supervision is provided by the switch hook detector at the $\overline{DET}$ output. When $\overline{DET}$ goes low, the low battery should be selected for DC loop feed and voice transmission.

Feed Architecture

The design implements a voltage feed current sense architecture. The device controls the voltage across Tip and Ring based on the sensing of load current. Resistors are placed in series with Tip and Ring outputs to provide the current sensing. The diagram below illustrates the concept.

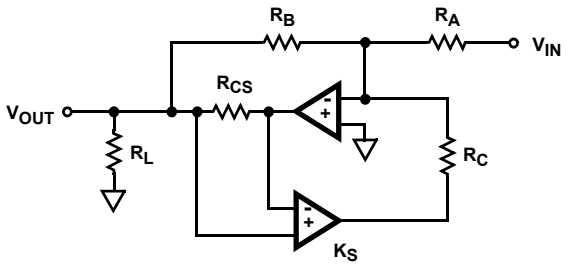


FIGURE 3. VOLTAGE FEED CURRENT SENSE DIAGRAM

By monitoring the current at the amplifier output, a negative feedback mechanism sets the output voltage for a defined load. The amplifier gains are set by resistor ratios (R_A, R_B, R_C) providing all the performance benefits of matched resistors. The internal sense resistor, R_{CS}, is much smaller than the gain resistors and is typically 20Ω for this device. The feedback mechanism, K_S, represents the amplifier configuration providing the negative feedback.

DC Loop Feed

The feedback mechanism for monitoring the DC portion of the loop current is the loop detector. A low pass filter is used in the feedback to block voice band signals from interfering with the loop current limit function. The pole of the low pass filter is set by the external capacitor C_{DC}. The value of the external capacitor should be 4.7µF.

Most applications will operate the device from low battery while off hook. The DC feed characteristic of the device will drive Tip and Ring towards half battery to regulate the DC loop current. For light loads, Tip will be near -4V and Ring will be near V_{VBL} + 4V. The following diagram shows the DC feed characteristic.

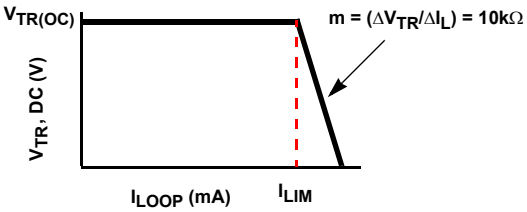


FIGURE 4. DC FEED CHARACTERISTIC

The point on the y-axis labeled $V_{TR(OC)}$ is the open circuit Tip to Ring voltage and is defined by the feed battery voltage.

$$V_{TR(OC)} = |V_{BL}| - 8 \quad \text{(EQ. 18)}$$

The curve of Figure 5 determines the actual loop current for a given set of loop conditions. The loop conditions are determined by the low battery voltage and the DC loop impedance. The DC loop impedance is the sum of the protection resistance, copper resistance (ohms/foot) and the telephone off hook DC resistance.

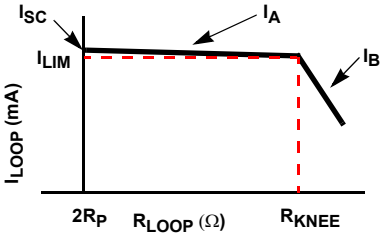


FIGURE 5. I_{LOOP} VERSUS R_{LOOP} LOAD CHARACTERISTIC

The slope of the feed characteristic and the battery voltage define the maximum loop current on the shortest possible loop as the short circuit current I_{SC}.

$$I_{SC} = I_{LIM} + \frac{V_{TR(OC)} - 2R_P I_{LIM}}{10e3} \quad \text{(EQ. 19)}$$

The term I_{LIM} is the programmed current limit, 1760/R_{IL}. The line segment I_A represents the constant current region of the loop current limit function.

$$I_A = I_{LIM} + \frac{V_{TR(OC)} - R_{LOOP} I_{LIM}}{10e3} \quad \text{(EQ. 20)}$$

The maximum loop impedance for a programmed loop current is defined as R_{KNEE}.

$$R_{KNEE} = \frac{V_{TR(OC)}}{I_{LIM}} \quad \text{(EQ. 21)}$$

When R_{KNEE} is exceeded, the device will transition from constant current feed to constant voltage, resistive feed. The line segment I_B represents the resistive feed portion of the load characteristic.

$$I_B = \frac{V_{TR(OC)}}{R_{LOOP}} \quad \text{(EQ. 22)}$$

Voice Transmission

The feedback mechanism for monitoring the AC portion of the loop current consists of two amplifiers, the sense amplifier (SA) and the transmit amplifier (TA). The AC feedback signal is used for impedance synthesis. A detailed model of the AC feed back loop is provided below.

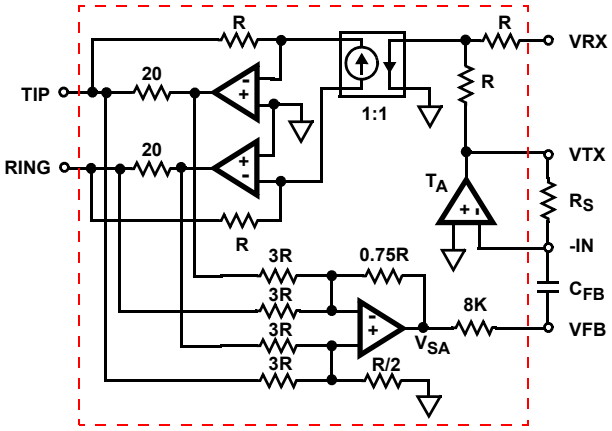


FIGURE 6. AC SIGNAL TRANSMISSION MODEL

The gain of the transmit amplifier, set by R_S, determines the programmed impedance of the device. The capacitor C_{FB} blocks the DC component of the loop current. The ground symbols in the model represent AC grounds, not actual DC potentials.

The sense amp output voltage, V_{SA}, as a function of Tip and Ring voltage and load is calculated using Equation 23.

$$V_{SA} = -(V_T - V_R)\frac{10}{Z_L} \quad \text{(EQ. 23)}$$

The transmit amplifier provides the programmable gain required for impedance synthesis. In addition, the output of this amplifier interfaces to the CODEC transmit input. The output voltage is calculated using Equation 24.

$$V_{VTX} = -V_{SA}\left(\frac{R_S}{8e3}\right) \quad \text{(EQ. 24)}$$

Once the impedance matching components have been selected using the design equations, the above equations provide additional insight as to the expected AC node voltages for a specific Tip and Ring load.

Transhybrid Balance

The final step in completing the impedance synthesis design is calculating the necessary gains for transhybrid balance. The AC feed back loop produces an echo at the V_{TX} output of the signal injected at V_{RX}. The echo must be cancelled to maintain voice quality. Most applications will use a summing amplifier in the CODEC front end as shown below to cancel the echo signal.

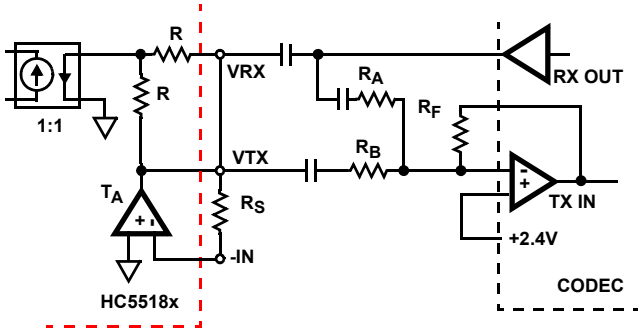


FIGURE 7. TRANSHYBRID BALANCE INTERFACE

The resistor ratio, R_F/R_B, provides the final adjustment for the transmit gain, G_{TX}. The transmit gain is calculated using Equation 25.

$$G_{TX} = -G_{24}\left(\frac{R_F}{R_B}\right) \quad \text{(EQ. 25)}$$

Most applications set $R_F = R_B$, hence the device 2-wire to 4-wire equals the transmit gain. Typically R_B is greater than 20kΩ to prevent loading of the device transmit output.

The resistor ratio, R_F/R_A, is determined by the transhybrid gain of the device, G_{44}. R_F is previously defined by the transmit gain requirement and R_A is calculated using Equation 26.

$$R_A = \frac{R_B}{G_{44}} \quad \text{(EQ. 26)}$$

Power Dissipation

The power dissipated by the device during on hook transmission is strictly a function of the quiescent currents for each supply voltage during Forward Active operation.

$$P_{FAQ} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad \text{(EQ. 27)}$$

Off hook power dissipation is increased above the quiescent power dissipation by the DC load. If the loop length is less than or equal to R_{KNEE}, the device is providing constant current, I_A, and the power dissipation is calculated using Equation 28.

$$P_{FA(IA)} = P_{FA(Q)} + (V_{BL} x I_A) - (R_{LOOP} x I^2_A) \quad \text{(EQ. 28)}$$

If the loop length is greater than R_{KNEE}, the device is operating in the constant voltage, resistive feed region. The power dissipated in this region is calculated using Equation 29.

$$P_{FA(IB)} = P_{FA(Q)} + (V_{BL} x I_B) - (R_{LOOP} x I^2_B) \quad \text{(EQ. 29)}$$

Since the current relationships are different for constant current versus constant voltage, the region of device operation is critical to valid power dissipation calculations.

Reverse Active

Overview

The reverse active mode (RA, 011) provides the same functionality as the forward active mode. On hook transmission, DC loop feed and voice transmission are supported. Loop supervision is provided by either the switch hook detector (E0 = 1) or the ground key detector (E0 = 0). The device may be operated from either high or low battery.

During reverse active the Tip and Ring DC voltage characteristics exchange roles. That is, Ring is typically 4V below ground and Tip is typically 4V more positive than battery. Otherwise, all feed and voice transmission characteristics are identical to forward active.

Silent Polarity Reversal

Changing from forward active to reverse active or vice versa is referred to as polarity reversal. Many applications require slew rate control of the polarity reversal event. Requirements range from minimizing cross talk to protocol signalling.

The device uses an external low voltage capacitor, C_{POL}, to set the reversal time. Once programmed, the reversal time will remain nearly constant over various load conditions. In addition, the reversal timing capacitor is isolated from the AC loop, therefore loop stability is not impacted.

The internal circuitry used to set the polarity reversal time is shown below.

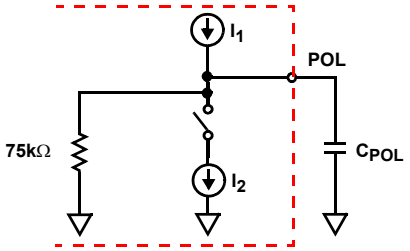


FIGURE 8. REVERSAL TIMING CONTROL

During forward active, the current from source I1 charges the external timing capacitor C_{POL} and the switch is open. The internal resistor provides a clamping function for voltages on the POL node. During reverse active, the switch closes and I2 (roughly twice I1) pulls current from I1 and the timing capacitor. The current at the POL node provides the

drive to a differential pair which controls the reversal time of the Tip and Ring DC voltages.

$$C_{POL} = \frac{\Delta time}{75000} \quad \text{(EQ. 30)}$$

Where Δtime is the required reversal time. Polarized capacitors may be used for C_{POL}. The low voltage at the POL pin and minimal voltage excursion $\pm$0.75V, are well suited to polarized capacitors.

Power Dissipation

The power dissipation equations for forward active operation also apply to the reverse active mode.

Ringing

Overview

The ringing mode (RNG, 100) provides the low side return path for externally supplied battery backed ringing. The ringing signal must be injected through a relay at the ring terminal. The device should be operated from the low battery voltage during this mode to minimize the overall power dissipation during ringing. Current flowing through the Tip terminal will provide the necessary ring trip information.

Ringing Bias Input

The ringing bias input, VRB, is a high impedance input. The VRB input is only selected during the ringing mode. The gain from the VRB input to the Tip output is typically 40V/V. The following equation shows the relationship of the Tip output voltage to the VRB input voltage.

$$V_{TIP} = \frac{VBL}{2} + 40 \times VRB \quad \text{(EQ. 31)}$$

A positive DC voltage at VRB is required to shift the Tip output voltage towards ground to provide the low side ringing return path. Tying the logic input F2 to VRB provides the positive voltage to offset Tip during ringing. A voltage divider is suggested to provide control the actual voltage applied to VRB.

Logic Control

Ringing patterns consist of silent intervals. The ringing to silent pattern is called the ringing cadence. During the silent portion of ringing, the device can be programmed to any other operating mode. The most likely candidates are low power standby or forward active. Depending on system requirements, the low or high battery may be selected.

Loop supervision is provided with the ring trip detector. The ring trip detector senses the change in loop current when the phone is taken off hook. The loop detector full wave rectifies the ringing current, which is then filtered with external components RRT and CRT. The resistor RRT sets the trip threshold and the capacitor CRT sets the trip response time. Most applications will require a trip response time less than 150 milliseconds.

Three very distinct actions occur when the devices detects a ring trip. First, the $\overline{DET}$ output is latched low. The latching mechanism eliminates the need for software filtering of the detector output. The latch is cleared when the operating mode is changed externally. Second, the VRS input is disabled, removing the Tip biasing signal from the line. Third, the device is internally forced to the forward active mode.

Power Dissipation

The power dissipation during ringing is dictated by the load driving requirements and the ringing waveform. The key to valid power calculations is the correct definition of average and rms currents. The average current defines the high battery supply current. The rms current defines the load current.

The cadence provides a time averaging reduction in the peak power. The total power dissipation consists of ringing power, P_r, and the silent interval power, P_s.

$$P_{RNG} = P_r \cdot \frac{t_r}{t_r + t_s} + P_s \cdot \frac{t_s}{t_r + t_s} \quad \text{(EQ. 32)}$$

The terms, tr and ts, represent the cadence. The ringing interval is tr and the silent interval is ts. The typical cadence ratio tr:ts is 1:2.

The quiescent power of the device in the ringing mode is defined in Equation 34.

$$P_{r(Q)} = VBH \cdot IBH_Q + VBL \cdot IBL_Q + VCC \cdot ICC_Q \quad \text{(EQ. 33)}$$

During ringing, the device is operated from the low battery, therefore the VBH power contribution is negligible. The total power during the ringing interval is the sum of the quiescent power and loading power:

$$P_r = P_{r(Q)} + VBL \cdot I_{AVG} - \frac{V_{rms}^2}{Z_{REN} + R_{LOOP}} \quad \text{(EQ. 34)}$$

For sinusoidal waveforms, the average current, I_{AVG}, is defined in equation 36.

$$I_{AVG} = \left(\frac{2}{\pi}\right)\frac{V_{rms} \cdot \sqrt{2}}{Z_{REN} + R_{LOOP}} \quad \text{(EQ. 35)}$$

The only amplifier providing load current during ringing is the Tip amplifier. Therefore the total power contribution from the device is half the average power required by the load.

$$I_{AVG} = \left(\frac{1}{\pi}\right)\frac{V_{rms} \cdot \sqrt{2}}{Z_{REN} + R_{LOOP}} \quad \text{(EQ. 36)}$$

The silent interval power dissipation will be determined by the quiescent power of the selected operating mode.

Power Denial

Overview

The power denial mode (111) will shutdown the entire device except for the logic interface. Loop supervision is not provided. This mode may be used as a sleep mode or to

shutdown in the presence of a persistent thermal alarm. Switching between high and low battery will have no effect during power denial.

Functionality

During power denial, both the Tip and Ring amplifiers are disabled, representing high impedances. The voltages at both outputs are near ground.

Thermal Shutdown

In the event the safe die temperature is exceeded, the $\overline{ALM}$ output will go low and $\overline{DET}$ will go high and the part will automatically shut down. When the device cools, $\overline{ALM}$ will go high and $\overline{DET}$ will reflect the loop status. If the thermal fault persists, $\overline{ALM}$ will go low again and the part will shutdown. Programming power denial will permanently shutdown the device and stop the self cooling cycling.

Battery Switching

Overview

The integrated battery switch selects between the high battery (VBH) and low battery (VBL). The battery switch is controlled with the logic input BSEL. When BSEL is a logic high, the high battery is selected and when a logic low, the low battery is selected. All operating modes of the device will operate from high or low battery except forward loop back.

Functionality

The logic control is independent of the operating mode decode. Independent logic control provides the most flexibility and will support all application configurations.

When changing device operating states, battery switching should occur simultaneously with or prior to changing the operating mode. In most cases, this will minimize overall power dissipation and prevent glitches on the $\overline{DET}$ output.

The only external component required to support the battery switch is a diode in series with the VBH supply lead. In the event that high battery is removed, the diode allows the device to transition to low battery operation.

Low Battery Operation

All off hook operating conditions and ringing should use the low battery. The prime benefit will be reduced power dissipation. The typical low battery for the device is -24V. However this may be increased to support longer loop lengths or high loop current requirements. Standby conditions may also operate from the low battery if MTU compliance is not required, further reducing standby power dissipation.

High Battery Operation

The high battery should be used for standby conditions which must provide MTU compliance. During standby operation the power consumption is typically 40 mW with -48V battery. If standby requirements do not require high battery operation, then a lower battery will result in lower standby power.

Uncommitted Switch

Overview

The uncommitted switch is a three terminal device designed for flexibility. The independent logic control input, $\overline{SWC}$, allows switch operation regardless of device operating mode. The switch is activated by a logic low. The positive and negative terminals of the device are labeled SW+ and SW- respectively.

Relay Driver

The uncommitted switch may be used as a relay driver by connecting SW+ to the relay coil and SW- to ground. The switch is designed to have a maximum on voltage of 0.6V with a load current of 45mA.

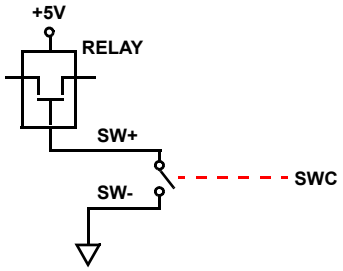


FIGURE 9. EXTERNAL RELAY SWITCHING

Since the device provides the ringing waveform, the relay functions which may be supported include subscriber disconnect, test access or line interface bypass. An external snubber diode is not required when using the uncommitted switch as a relay driver.

Test Load

The switch may be used to connect test loads across Tip and Ring. The test loads can provide external test termination for the device. Proper connection of the uncommitted switch to Tip and Ring is shown below.

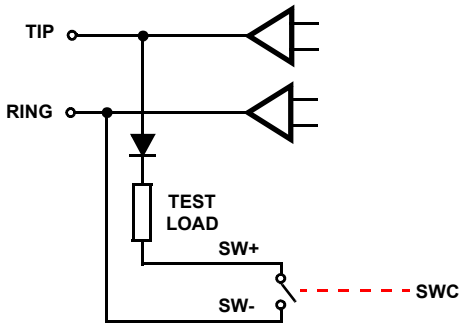


FIGURE 10. TEST LOAD SWITCHING

The diode in series with the test load blocks current from flowing through the uncommitted switch when the polarity of the Tip and Ring terminals are reversed. In addition to the reverse active state, the polarity of Tip and Ring are reversed for half of the ringing cycle. With independent logic control and the blocking diode, the uncommitted switch may be continuously connected to the Tip and Ring terminals.

Basic Application Circuit

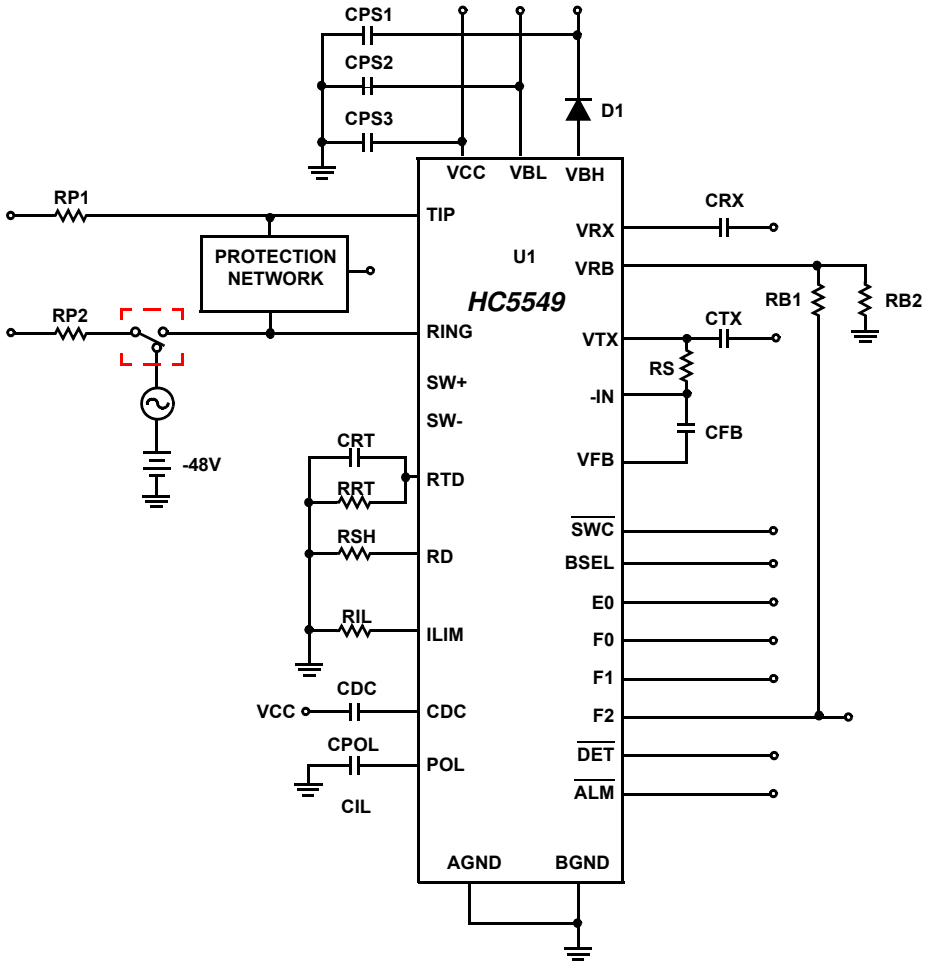


FIGURE 11. HC5549 BASIC APPLICATION CIRCUIT

Basic Application Circuit Component List

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
U1	HC5549	N/A	N/A	n/a	n/a	n/a	n/a
RRT	20kΩ	1%	0.1W	CDC	4.7µF	20%	10V
RSH	49.9kΩ	1%	0.1W	CPS1	0.1µF	20%	>100V
RIL	71.5kΩ	1%	0.1W	CPS2, CPS3	0.1µF	20%	100V
RS	210kΩ	1%	0.1W	D1	1N400X type with breakdown > 100V.		
CRX, CRS, CTX, CRT, CPOL, CFB	0.47µF	20%	10V	RP1, RP2	Protection resistor values are application dependent and will be determined by protection requirements. Standard applications will use ≥ 35Ω per side.		
Design Parameters: Ring Trip Threshold = 90 mA peak., Switch Hook Threshold = 12 mA, Loop Current Limit = 24.6 mA, Synthesize Device Impedance = 210kΩ/400= 525Ω, with 39Ω protection resistors, impedance across Tip and Ring terminals = 603Ω.							

Pin Description

PLCC	SYMBOL	DESCRIPTION
1	TIP	TIP power amplifier output.
2	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
3	VBL	Low battery supply connection.
4	VBH	High battery supply connection.
5	SW+	Uncommitted switch positive terminal.
6	SW-	Uncommitted switch negative terminal.
7	$\overline{SWC}$	Switch control input. This TTL compatible input controls the uncommitted switch, with a logic “0” enabling the switch and logic “1” disabling the switch.
8	F2	Mode control input - MSB. F2-F0 for the TTL compatible parallel control interface for controlling the various modes of operation of the device.
9	F1	Mode control input.
10	F0	Mode control input.
11	E0	Detector Output Selection Input. This TTL input controls the multiplexing of the SHD (E0=1) and GKD (E0 =0) comparator outputs to the $\overline{DET}$ output based upon the state at the F2-F0 pins.
12	$\overline{DET}$	Detector Output - This TTL output provides hook status of the loop based upon the selected operating mode. The detected output will either be switch hook, ground key or ring trip.
13	$\overline{ALM}$	Thermal Shutdown Alarm. This pin signals the internal die temperature has exceeded safe operating temperature and the device has been powered down automatically.
14	AGND	Analog ground reference. This pin should be externally connected to BGND.
15	BSEL	Selects between high and low battery, with a logic “1” selecting the high battery and logic “0” the low battery.
16	NC	This pin is a “no connect” and should remain floating proper device operation.
17	POL	Capacitor connected to this pin sets the polarity reversal slew rate.
18	VRB	Ringing Bias Input - Analog input to offset Tip output towards ground while in Ringing Mode.
19	VRX	Analog Receive Voltage - 4-wire analog audio input voltage. AC couples to codec.
20	VTX	Transmit output voltage - Output of impedance matching amplifier, AC couples to codec.
21	VFB	Feedback voltage for impedance matching. This voltage is scaled to accomplish impedance matching.
22	-IN	Impedance matching amplifier summing node.
23	VCC	Positive voltage power supply.
24	CDC	DC Biasing Filter Capacitor - Connects between this pin and VCC.
25	RTD	Ring trip filter network.
26	ILIM	Loop Current Limit programming resistor.
27	RD	Switch hook detection threshold programming resistor.
28	RING	RING power amplifier output.