6-A, WIDE-INPUT ADJUSTABLE SWITCHING REGULATOR

Check for Samples: PTN78020W, PTN78020H

FEATURES

- **6-A Output Current**
- **Wide-Input Voltage (7 V to 36 V) / (15 V to 36 V)**
- **Wide-Output Voltage Adjust (2.5 V to 12.6 V) / (11.85 V to 22 V)**
- **High Efficiency (Up to 96%)**
- **On/Off Inhibit**
- **Undervoltage Lockout**
- **Output Current Limit**
- **Overtemperature Shutdown**
- **Operating Temperature: -40°C to 85°C**
- **Surface Mount Package Available**

APPLICATIONS

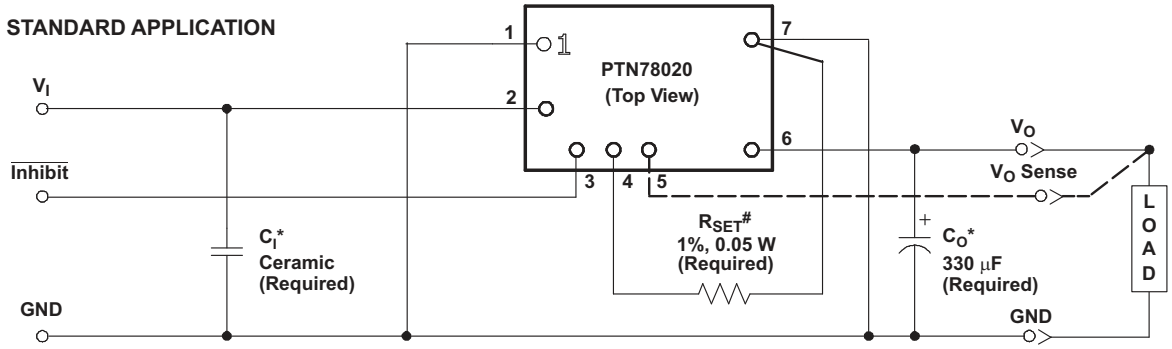
- **General-Purpose, Industrial Controls, HVAC Systems, Test and Measurement, Medical Instrumentation, AC/DC Adaptors, Vehicles, Marine, and Avionics**

DESCRIPTION

The PTN78020 is a series of high-efficiency, step-down integrated switching regulators (ISRs), that represent the third generation in the evolution of high-performance power modules designed for industrial use. The wide-input voltage range makes these modules suitable for a variety of applications that operate off 12–V, 24–V, and 28–V dc power. In new designs they should be considered in place of the PT6620, PT6650, PT6680, and PT6880 series of single in-line pin (SIP) products. The PTN78020 is smaller and lighter than its predecessors, and has either similar or improved electrical performance characteristics. The caseless, double-sided package has excellent thermal characteristics, and is compatible with TI's roadmap for RoHS and lead-free compliance.

Operating from a wide-input voltage range, the PTN78020 provides high-efficiency, step-down voltage conversion for loads of up to 6 A. The output voltage is set using a single, external resistor. The PTN78020W may be set to any value within the range, 2.5 V to 12.6 V, and the PTN78020H from 11.85 V to 22 V. The output voltage of the PTN78020W can be as little as 2 V lower than the input, allowing operation down to 7 V, with an output voltage of 5 V. The output voltage of the PTN78020H can be as little as 3 V lower than the input, allowing operation down to 15 V, with an output voltage of 12 V.

The PTN78020 has undervoltage lockout, an integral on/off inhibit, and includes an output current limit and overtemperature protection.



*See the *Application Information* section for capacitor recommendations. The minimum input capacitance for is 2.2 µF for PTN78020W, and 18.8 µF (4 x 4.7 µF) for PTN78020H

#R_{SET} is required to adjust the output voltage. See the *Application Information* section for values.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range unless otherwise noted
all voltages with respect to GND

				UNIT
T_A	Operating free-air temperature	Over V_I range		–40°C to 85°C
	Wave solder temperature	Surface temperature of module body or pins **(5 seconds)**	Horizontal TH (suffix AH & AD)	260°C
	Solder reflow temperature	Surface temperature of module body or pins	Horizontal SMD (suffix AS)	235°C
			Horizontal SMD (suffix AZ)	260°C
T_S	Storage temperature			–55°C to 125°C
V_I	Input surge voltage, 10 ms maximum			38 V
V_{INH}	Inhibit (pin 3) input voltage			–0.3 V to 5 V
P_O	Output power		$V_I \le 24$ V or $V_O \ge 15$ V	90 W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	Input voltage	PTN78020W	7	36	V
		PTN78020H	15	36	
T_A	Operating free-air temperature		–40	85	°C

PACKAGE SPECIFICATIONS

PTN78020x (Suffix AH, AS, & AZ)			
Weight			7.3 grams
Flammability	Meets UL 94 V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted	Horizontal T/H (suffix AH and AD)	250 G (1)
		Horizontal SMD (suffix AS and AZ)	125 G (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	Horizontal T/H (suffix AH and AD)	20 G (1)
		Horizontal SMD (suffix AS and AZ)	10 G (1)

(1) Qualification limit.

ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 20 V, V_O = 5 V, I_O = I_O (max), C_I = 2.2 µF, C_O = 330 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PTN78020W			
				MIN	TYP	MAX	UNIT
I_O	Output current	T_A = 25°C, natural convection airflow	V_I ≤24 V	0.1		6 (1)	A
			V_I = 32 V	0.1		5 (1)	
			V_I = 36 V	0.1		4.5 (1)	
V_I	Input voltage range	Over I_O range		7 (2)		36 (3)	V
V_O	Set-point voltage tolerance	T_A = 25°C				±2% (4)	
	Temperature variation	–40°C to +85°C			±0.5%		
	Line regulation	Over V_I range			±10		mV
	Load regulation	Over I_O range			±10		mV
	Total output voltage variation	Includes set point, line, load –40 < T_A < 85°C				±3% (4)	
V_O (adj)	Output voltage adjust range		V_I < 12 V	2.5		V_I – 2	V
			12 V ≤ V_I ≤ 15.1 V	2.5		V_I – 2.5	
			15.1 V < V_I ≤ 25 V	2.5		12.6	
			V_I > 25 V	0.1 × V_I		12.6	
η	Efficiency		V_I = 24 V, R_{SET} = 732 Ω, V_O = 12 V		94%		
			V_I = 15 V, R_{SET} = 21 kΩ, V_O = 5 V		88%		
			V_I = 15 V, R_{SET} = 78.7 kΩ, V_O = 3.3 V		85%		
	Output voltage ripple	20-MHz bandwith			1% V_O		$V_{(PP)}$
$I_{O\ (LIM)}$	Current limit threshold	ΔV_O = –50 mV			8.5		A
	Transient response	1 A/µs load step from 50% to 100% $I_O$max					
			Recovery time		200		µs
			V_O over/undershoot		5		$\%V_O$
	Inhibit control (pin 3)	Input high voltage (V_{IH})		1		Open (5)	V
		Input low voltage (V_{IL})		–0.1		0.3	
		Input low current (I_{IL})			0.25		mA
$I_{I(stby)}$	Input standby current	Pin 3 connected to GND			17		mA
UVLO	Undervoltage lockout	V_I increasing			5.5		V
		V_I decreasing			5.2		
F_S	Switching frequency	Over V_I and I_O ranges		440	550	660	kHz
C_I	External input capacitance	Ceramic and nonceramic		2.2 (6)			µF
C_O	External output capacitance	Ceramic				300	µF
		Nonceramic		330 (7)		2,000	
		Equiv. series resistance (nonceramic)		10 (8)			mΩ
MTBF	Calculated reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		5.6			10^6 Hr

(1) Above an input voltage of 24 V, the maximum output current must be derated by 125 mA per volt above 24 V.
(2) For output voltages less than 10 V, the minimum input voltage is 7 V or (V_O + 2) V, whichever is greater. For output voltages of 10 V and higher, the minimum input voltage is (V_O + 2.5 V). See the Application Information section for further guidance.
(3) For output voltages less than 3.6 V, the maximum input voltage is 10 × V_O . See the Application Information section for further guidance.
(4) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with with 100 ppm/°C or better temperature stability.
(5) This control pin has an internal pullup, and if left open-circuit, the module operates when input power is applied. The open-circuit voltage is typically 1.5 V. A small, low-leakage (< 100 nA) MOSFET is recommended for control. See the Application Information section for further guidance.
(6) An external 2.2-µF ceramic capacitor is required across the input (V_I and GND) for proper operation. Locate the capacitor close to the module.
(7) 330 µF of output capacitance is required for proper operation. See the Application Information section for further guidance.
(8) This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 17 mΩ as the minimum when using max-ESR values to calculate.

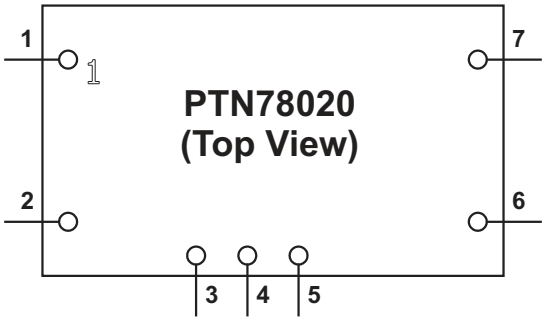
ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature, V_I = 24 V, V_O = 12 V, I_O = I_O (max), C_I = 4× 4.7 µF, C_O = 330 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		PTN78020H			
				MIN	TYP	MAX	UNIT
I_O	Output current	T_A = 25°C, natural convection airflow	V_o =12 V	0.1		6 (1)	A
			V_o =15 V	0.1		6 (1) (2)	
			V_o = 22 V	0.1		4.09 (2)	
V_I	Input voltage range	Over I_O range		15 (3)		36	V
V_O	Set-point voltage tolerance	T_A = 25°C				±2% (4)	
	Temperature variation	–40°C to +85°C			±0.5%		
	Line regulation	Over V_I range			±10		mV
	Load regulation	Over I_O range			±10		mV
	Total output voltage variation	Includes set point, line, load –40 < T_A < 85°C				±3% (4)	
V_O (adj)	Output voltage adjust range		V_I < 19 V	11.85		V_I – 3	V
			19 V ≤ V_I ≤ 25 V	11.85		V_I – 4	
			V_I > 25 V	11.85		22	
η	Efficiency		V_I = 24 V, R_{SET} = 383 k Ω, V_O = 12 V		94%		
			V_I = 24 V, R_{SET} = 15 kΩ, V_O = 15 V		95%		
			V_I = 32 V, R_{SET} = 95.3 Ω, V_O = 22 V		96%		
	Output voltage ripple	20-MHz bandwith			1% V_O		$V_{(PP)}$
$I_{O\ (LIM)}$	Current limit threshold	ΔV_O = –50 mV			8.0		A
	Transient response	1 A/µs load step from 50% to 100% $I_O$max					
			Recovery time		200		µs
			V_O over/undershoot		200		mV
	Inhibit control (pin 3)	Input high voltage (V_{IH})		1		Open (5)	V
		Input low voltage (V_{IL})		–0.1		0.3	
		Input low current (I_{IL})			0.25		mA
$I_{I(stby)}$	Input standby current	Pin 3 connected to GND			17		mA
UVLO	Undervoltage lockout	V_I increasing			12.2		V
		V_I decreasing			12		
F_S	Switching frequency	Over V_I and I_O ranges		440	550	660	kHz
C_I	External input capacitance	Ceramic and nonceramic		18.8 (6)			µF
C_O	External output capacitance	Ceramic		0		300	µF
		Nonceramic		330 (7)		2,000	
		Equiv. series resistance (nonceramic)		10 (8)			mΩ
MTBF	Calculated reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		5.6			10^6 Hr

(1) The maximum output current is 6 A or a maximum output power of 90 W, whichever is less. Above an input voltage of 24 V, the maximum output current must be derated by 125 mA per volt above 24 V. See the Typica lCharacteristics section for further guidance.
(2) Above an output voltage of 15 V, the maximum output current must be derated by 285 mA per volt. The maximum output power is 90 W. See the application information for further guidance.
(3) For output voltages less than 19 V, the minimum input voltage is 15 V or (V_O + 3) V, whichever is greater. For output voltages of 19 V and higher, the minimum input voltage is (V_O + 4 V). See the Application Information section for further guidance.
(4) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with with 100 ppm/°C or better temperature stability.
(5) This control pin has an internal pullup, and if left open-circuit, the module operates when input power is applied. The open-circuit voltage is typically 1.5 V. A small, low-leakage (< 100 nA) MOSFET is recommended for control. See the Application Information section for further guidance.
(6) Four external 4.7-µF ceramic capacitors are required across the input (V_I and GND) for proper operation. Locate the capacitors close to the module.
(7) 330 µF of output capacitance is required for proper operation. See the Application Information section for further guidance.
(8) This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 17 mΩ as the minimum when using max-ESR values to calculate.

PIN ASSIGNMENT



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	1, 7		This is the common ground connection for the V_I and V_O power connections. It is also the 0-V_{dc} reference for the *Inhibit* and V_O *Adjust* control inputs.
V_I	2	I	The positive input voltage power node to the module, which is referenced to common GND.
$\overline{\text{Inhibit}}$	3	I	The Inhibit pin is an open-collector/drain active-low input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied.
V_O Adjust	4	I	A 1% resistor must be connected between this pin and GND (pin 7) to set the output voltage of the module. If left open-circuit, the output voltage is set to its default value. The temperature stability of the resistor should be 100 ppm/°C (or better). The standard resistor value for a number of common output voltages is provided in the application information.
V_O Sense	5	I	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimum voltage accuracy, V_O *Sense* should be connected to V_O . If the sense feature is not used, this pin may be left disconnected.
V_O	6	O	The regulated positive power output with respect to the GND node.

TYPICAL CHARACTERISTICS (7-V INPUT)(1) (2)

EFFICIENCY vs OUTPUT CURRENT

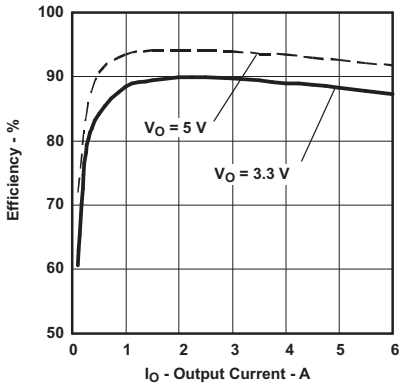


Figure 1.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

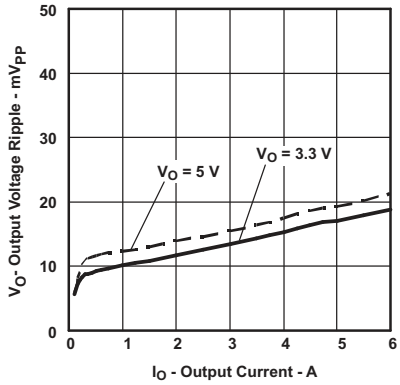


Figure 2.

POWER DISSIPATION vs OUTPUT CURRENT

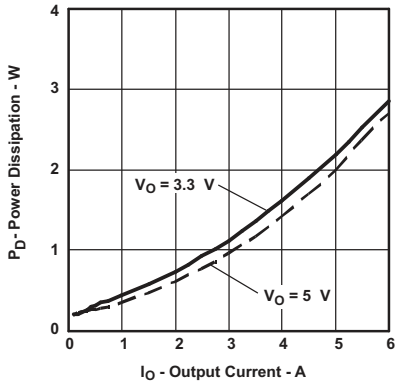


Figure 3.

TEMPERATURE DERATING vs OUTPUT CURRENT

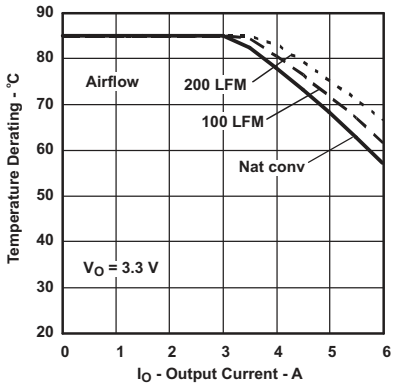


Figure 4.

TEMPERATURE DERATING vs OUTPUT CURRENT

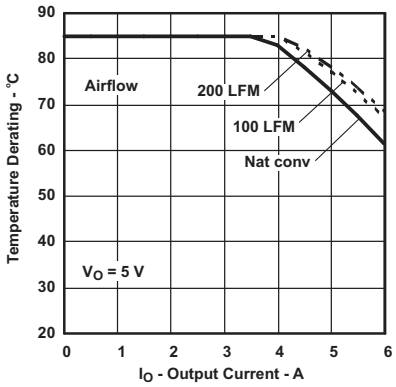


Figure 5.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 4 and Figure 5.

TYPICAL CHARACTERISTICS (15-V INPUT)(1) (2)

EFFICIENCY vs OUTPUT CURRENT

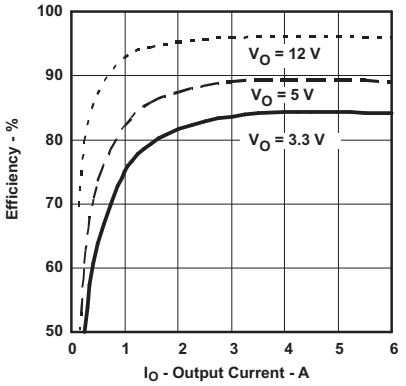


Figure 6.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

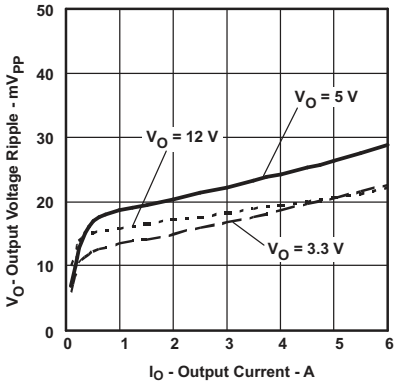


Figure 7.

POWER DISSIPATION vs OUTPUT CURRENT

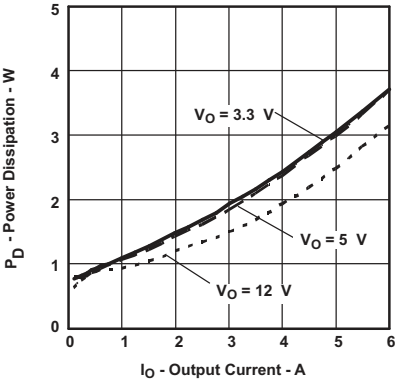


Figure 8.

TEMPERATURE DERATING vs OUTPUT CURRENT

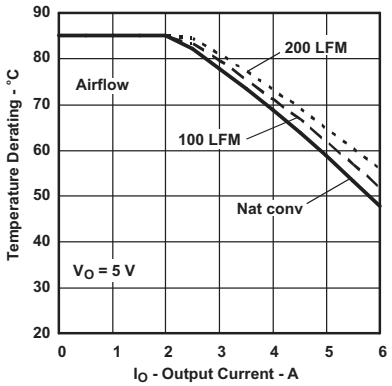


Figure 9.

TEMPERATURE DERATING vs OUTPUT CURRENT

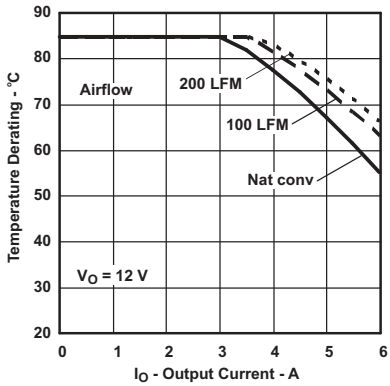


Figure 10.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 6, Figure 7, and Figure 8.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 9 and Figure 10.

TYPICAL CHARACTERISTICS (24-V INPUT)(1) (2)

EFFICIENCY vs OUTPUT CURRENT

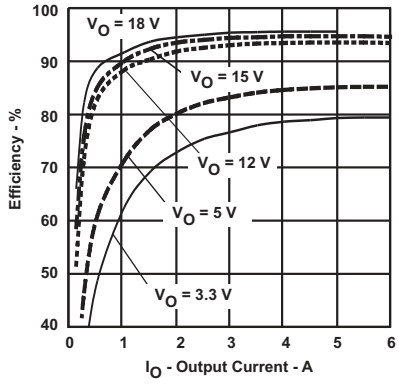


Figure 11.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

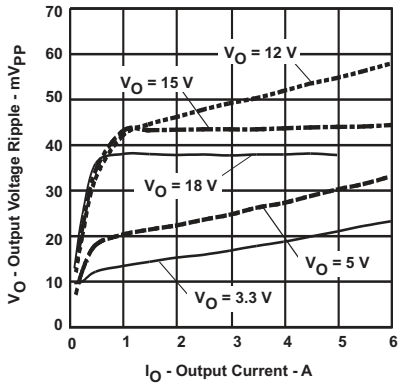


Figure 12.

POWER DISSIPATION vs OUTPUT CURRENT

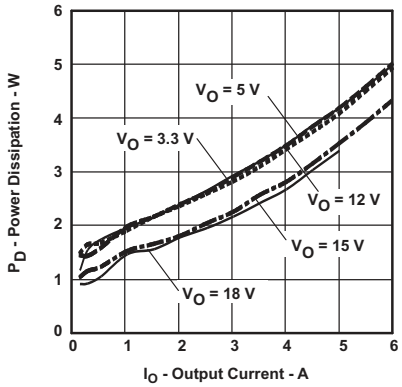


Figure 13.

TEMPERATURE DERATING vs OUTPUT CURRENT

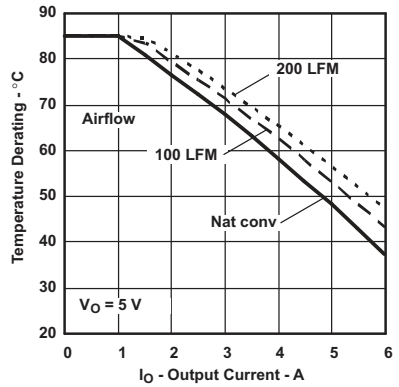


Figure 14.

TEMPERATURE DERATING vs OUTPUT CURRENT

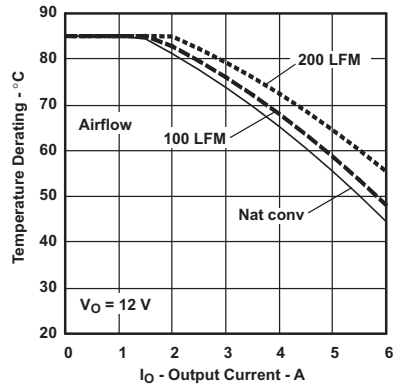


Figure 15.

TEMPERATURE DERATING vs OUTPUT CURRENT

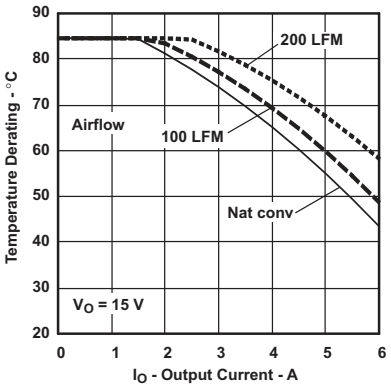


Figure 16.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 11, Figure 12, and Figure 13.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 14 through Figure 16.

TYPICAL CHARACTERISTICS (32-V INPUT)(1) (2)

EFFICIENCY vs OUTPUT CURRENT

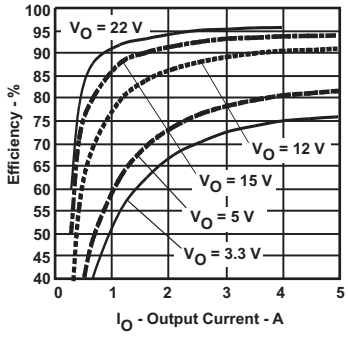


Figure 17.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

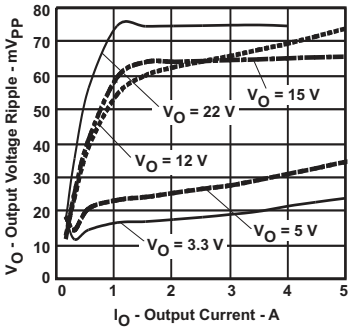


Figure 18.

POWER DISSIPATION vs OUTPUT CURRENT

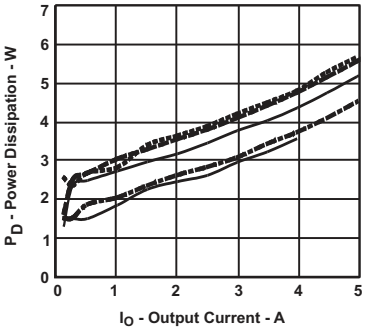


Figure 19.

TEMPERATURE DERATING vs OUTPUT CURRENT

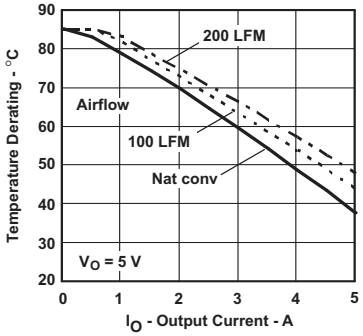


Figure 20.

TEMPERATURE DERATING vs OUTPUT CURRENT

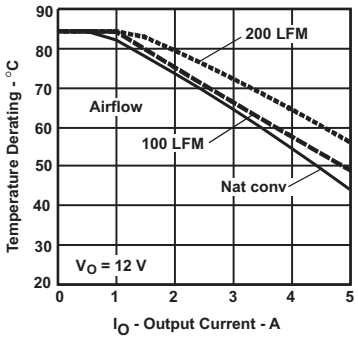


Figure 21.

TEMPERATURE DERATING vs OUTPUT CURRENT

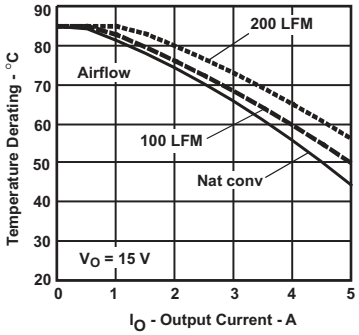


Figure 22.

TEMPERATURE DERATING vs OUTPUT CURRENT

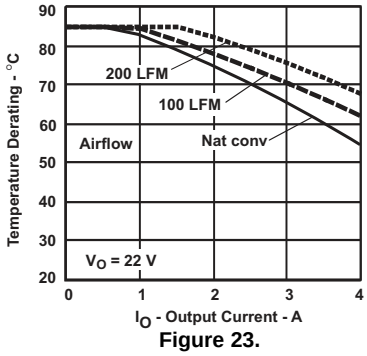


Figure 23.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 17, Figure 18, and Figure 19.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 20 through Figure 23.

APPLICATION INFORMATION

Adjusting the Output Voltage of the PTN78020x Series of Wide-Output Adjust Power Modules

General

A resistor must be connected between the *V_O Adjust* control (pin 4) and *GND* (pin 7) to set the output voltage. The adjustment range is from 2.5 V to 12.6 V for PTN78020W. The adjustment range is from 11.85 V to 22 V for PTN78020H. If pin 4 is left open, the output voltage defaults to the lowest value.

Table 2 gives the preferred value of the external resistor for a number of standard voltages, with the actual output voltage that the value provides. For other output voltages, the value of the required resistor can either be calculated using Equation 1 and the constants for the applicable product in Table 1. Figure 24 shows the placement of the required resistor.

$$R_{SET} = 54.9\ k\Omega \times \frac{1.25\ V}{V_O - V_{min}} - R_P \quad (1)$$

Table 1. R_{SET} Formula Constants

PRODUCT	V_{MIN}	R_P
PTN780x0W	2.5 V	6.49 kΩ
PTN780x0H	11.824 V	6.65 kΩ

Input Voltage Considerations

The PTN78020 is a step-down switching regulator. In order that the output remains in regulation, the input voltage must exceed the output by a minimum differential voltage.

Another consideration is the pulse width modulation (PWM) range of the regulator's internal control circuit. For stable operation, its operating duty cycle should not be lower than some minimum percentage. This defines the maximum advisable ratio between the regulator input and output voltage magnitudes.

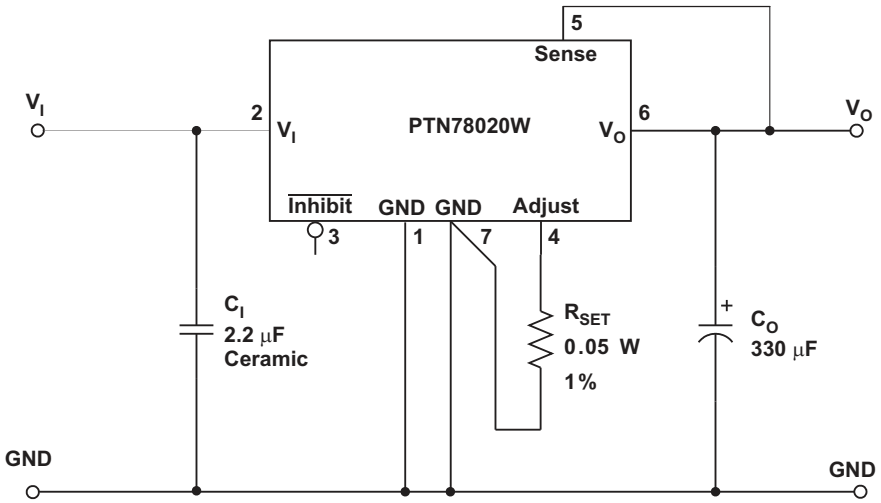
As an example, for satisfactory performance, the operating input voltage range of the PTN78020x must adhere to the following requirements.

1. For PTN78020W output voltages lower than 10 V, the minimum input voltage is (V_O + 2 V) or 7 V, whichever is higher.
2. For PTN78020W output voltages equal to 10 V and higher, the minimum input voltage is (V_O + 2.5 V) .
3. For PTN78020W, the maximum input voltage is (10 × V_O) or 36 V, whichever is less.
4. For PTN78020H output voltages lower than 19 V, the minimum input voltage is (V_O + 3 V) or 15 V, whichever is higher.
5. For PTN78020H output voltages equal to 19 V and higher, the minimum input voltage is (V_O + 4 V) .

Table 2 gives the operating input voltage range for the common output bus voltages. In addition, the Electrical Characteristics table defines the available output voltage adjust range for various input voltages.

Table 2. Standard Values of R_{set} for Common Output Voltages

PRODUCT	V_O (Required)	R_{SET} (Standard Value)	V_O (Actual)	Operating V_I Range
PTN780x0W	2.5 V	Open	2.5 V	7 V to 25 V
	3.3 V	78.7 kΩ	3.306 V	7 V to 33 V
	5 V	21 kΩ	4.996 V	7 V to 36 V
	12 V	732 Ω	12.002 V	14.5 V to 36 V
PTN780x0H	12 V	383 kΩ	12.000 V	15 V to 36 V
	15 V	15 kΩ	14.994 V	18 V to 36 V
	18 V	4.42 kΩ	18.023 V	21 V to 36 V
	22 V	95.3	21.998 V	26 V to 36 V



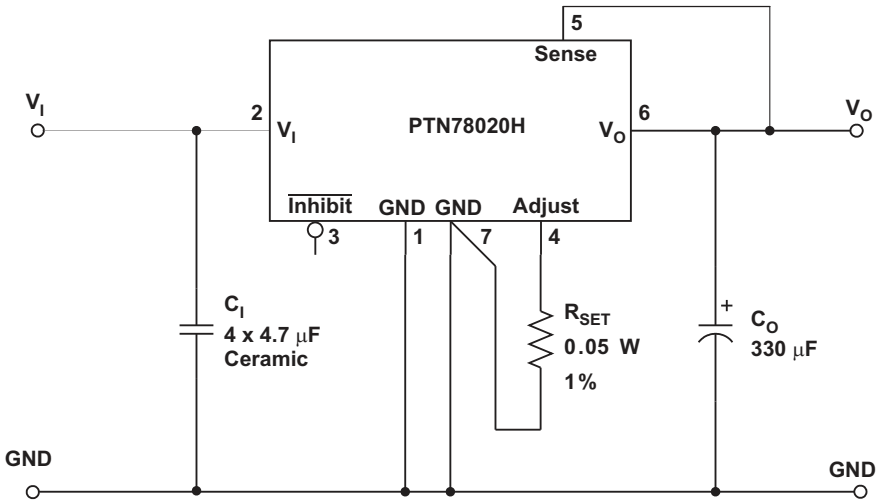
(1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.

(2) Never connect capacitors from V_O *Adjust* to either *GND* or V_O . Any capacitance added to the V_O *Adjust* pin affects the stability of the regulator.

Figure 24. PTN78020W V_O Adjust Resistor Placement

Table 3. PTN78020W Output Voltage Set-Point Resistor Values

V_O (V)	R_{SET} (kΩ)	V_O (V)	R_{SET} (kΩ)	V_O (V)	R_{SET} (kΩ)	V_O (V)	R_{SET} (kΩ)
2.50	Open	3.7 V	50.7	6.1	12.6	9.0	4.07
2.55	1370	3.8 V	46	6.2	12.1	9.2	3.75
2.60	680	3.9 V	42.5	6.3	11.6	9.4	3.46
2.65	451	4.0 V	39.3	6.4	11.1	9.6	3.18
2.70	337	4.1 V	36.4	6.5	10.7	9.8	2.91
2.75	268	4.2 V	33.9	6.6	10.2	10.0	2.66
2.80	222	4.3 V	31.6	6.7	9.85	10.2	2.42
2.85	190	4.4 V	29.6	6.8	9.47	10.4	2.20
2.90	165	4.5 V	27.8	6.9	9.11	10.6	1.98
2.95	146	4.6 V	26.2	7.0	8.76	10.8	1.78
3.00	131	4.7 V	24.7	7.1	8.43	11.0	1.58
3.05	118	4.8 V	23.3	7.2	8.11	11.2	1.40
3.10	108	4.9 V	22.1	7.3	7.81	11.4	1.22
3.15	99.1	5.0 V	21.0	7.4	7.52	11.6	1.05
3.20	91.5	5.1 V	19.9	7.5	7.24	11.8	0.889
3.25	85.0	5.2 V	18.9	7.6	6.97	12.0	0.734
3.30	79.3	5.3 V	18.0	7.7	6.71	12.2	0.585
3.35	74.2	5.4 V	17.2	7.8	6.46	12.4	0.442
3.40	69.8	5.5 V	16.4	7.9	6.22	12.6	0.305
3.45	65.7	5.6 V	15.6	8.0	5.99		
3.50	62.1	5.7 V	15.0	8.2	5.55		
3.55	58.9	5.8 V	14.3	8.4	5.14		
3.60	55.9	5.9 V	13.7	8.6	4.76		
3.65	53.2	6.0 V	13.1	8.8	4.40		



(1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.

(2) Never connect capacitors from V_O *Adjust* to either *GND* or V_O . Any capacitance added to the V_O *Adjust* pin affects the stability of the regulator.

Figure 25. PTN78020H V_O Adjust Resistor Placement

Table 4. PTN78020H Output Voltage Set-Point Resistor Values

V_O	R_{SET}	V_O	R_{SET}	V_O	R_{SET}
11.85 V	2633 kΩ	13.50 V	34.3 kΩ	17.20 V	6.12 kΩ
11.90 V	896 kΩ	13.65 V	30.9 kΩ	17.40 V	5.66 kΩ
11.95 V	538 kΩ	13.80 V	28.1 kΩ	17.60 V	5.23 kΩ
12.00 V	383 kΩ	13.95 V	25.6 kΩ	17.80 V	4.83 kΩ
12.10 V	242 kΩ	14.10 V	23.5 kΩ	18.00 V	4.46 kΩ
12.15 V	204 kΩ	14.25 V	21.6 kΩ	18.20 V	4.11 kΩ
12.20 V	176 kΩ	14.40 V	19.9 kΩ	18.40 V	3.79 kΩ
12.25 V	154 kΩ	14.55 V	18.5 kΩ	18.60 V	3.48 kΩ
12.30 V	138 kΩ	14.70 V	17.2 kΩ	18.80 V	3.19 kΩ
12.35 V	124 kΩ	14.85 V	16.0 kΩ	19.00 V	2.91 kΩ
12.40 V	113 kΩ	15.00 V	14.9 kΩ	19.20 V	2.65 kΩ
12.45 V	103 kΩ	15.15 V	13.9 kΩ	19.40 V	2.41 kΩ
12.50 V	94.9 kΩ	15.30 V	13.1 kΩ	19.60 V	2.18 kΩ
12.55 V	87.9 kΩ	15.45 V	12.3 kΩ	19.80 V	1.95 kΩ
12.60 V	81.8 kΩ	15.60 V	11.5 kΩ	20.00 V	1.74 kΩ
12.65 V	76.4 kΩ	15.75 V	10.8 kΩ	20.20 V	1.54 kΩ
12.70 V	71.7 kΩ	15.90 V	10.2 kΩ	20.40 V	1.35 kΩ
12.75 V	67.5 kΩ	16.05 V	9.59 kΩ	20.60 V	1.17 kΩ
12.80 V	63.7 kΩ	16.20 V	9.03 kΩ	20.80 V	995 Ω
12.85 V	60.2 kΩ	16.35 V	8.51 kΩ	21.00 V	829 kΩ
12.90 V	57.1 kΩ	16.50 V	8.03 kΩ	21.20 V	669 Ω
12.95 V	54.3 kΩ	16.65 V	7.57 kΩ	21.40 V	516 Ω
13.00 V	51.7 kΩ	16.80 V	7.14 kΩ	21.80 V	229 Ω
13.05 V	49.3 kΩ	17.10 V	6.36 kΩ	22.00 V	94 Ω

CAPACITOR RECOMMENDATIONS for the PTN78020 WIDE-OUTPUT ADJUST POWER MODULES

PTN78020W Input Capacitor

The minimum requirement for the input capacitance is a 2.2-µF ceramic capacitor for PTN78020W, in either a X5R or X7R temperature characteristic. Ceramic capacitors should be located within 0.5 inch (1,27 cm) of the regulator's input pins. Electrolytic capacitors can be used at the input, but only in addition to the required ceramic capacitance. The minimum ripple current rating for any nonceramic capacitance must be at least 500 mA rms for $V_O \leq 5.5$. For $V_O > 5.5$ V, the minimum ripple current rating is 750 mA rms. The ripple current rating of electrolytic capacitors is a major consideration when they are used at the input. This ripple current requirement can be reduced by placing more ceramic capacitors at the input, in addition to the minimum required 2.2 µF.

Tantalum capacitors are not recommended for use at the input bus, as none were found to meet the minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This voltage derating is standard practice for regular tantalum capacitors to ensure reliability. Polymer-tantalum capacitors are more reliable, and are available with a maximum rating of typically 20 V. These can be used with input voltages up to 16 V.

PTN78020H Input Capacitor

The minimum requirement for PTN78020H the input capacitance is 18.8 µF (4x 4.7-µF) or equivalent . Ceramic capacitors should be located within 0.5 inch (1,27 cm) of the regulator's input pins. Electrolytic capacitors can be used at the input, but only in addition to the required ceramic capacitance. The minimum ripple current rating for any nonceramic capacitance must be at least 500 mA rms for $V_O \leq 5.5$. For $V_O > 5.5$ V, the minimum ripple current rating is 750 mA rms. The ripple current rating of electrolytic capacitors is a major consideration when they are used at the input.

Tantalum capacitors are not recommended for use at the input bus, as none meet the minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This voltage derating is standard practice for regular tantalum capacitors to ensure reliability. Polymer-tantalum capacitors are more reliable, and are available with a maximum rating of typically 20 V. These can be used with input voltages up to 16 V.

PTN78020W/PTN78020H Output Capacitor

The minimum capacitance required to ensure stability is a 330 µF. Either ceramic or electrolytic-type capacitors can be used. The minimum ripple current rating for the nonceramic capacitance must be at least 250 mA rms. The stability of the module and voltage tolerances are compromised if the capacitor is not placed near the output bus pins. A high-quality, computer-grade electrolytic capacitor should be adequate. A ceramic capacitor can be also be located within 0.5 inch (1,27 cm) of the output pin.

For applications with load transients (sudden changes in load current), the regulator response improves with additional capacitance. Additional electrolytic capacitors should be located close to the load circuit. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz. Aluminum electrolytic capacitors are suitable for ambient temperatures above 0°C. For operation below 0°C, tantalum or Os-Con type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 10 m Ω (17 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of capacitors and vendors are identified in Table 5 and Table 6, the recommended capacitor tables.

Ceramic Capacitors

Above 150 kHz, the performance of aluminum electrolytic capacitors becomes less effective. To further reduce the reflected input ripple current, or the output transient response, multilayer ceramic capacitors must be added. Ceramic capacitors have low ESR and their resonant frequency is higher than the bandwidth of the regulator. When placed at the output, their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 µF. Also, to prevent the formation of local resonances, do not place more than three identical ceramic capacitors with values of 10 µF or greater in parallel.

Tantalum Capacitors

Tantalum-type capacitors may be used at the output, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595, and Kemet T495/T510/T520 capacitors series are suggested over many other tantalum types due to their rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications. When specifying Os-Con and polymer-tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

Capacitor Table

The capacitor tables, Table 5 and Table 6, identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type. This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The rms rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

Designing for Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation of any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

Table 5. Recommended Input/Output Capacitors (PTN78020W)

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE (µF)	EQUIVALENT SERIES RESISTANCE (ESR) (Ω)	85°C MAXIMUM RIPPLE CURRENT (mArms)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
Panasonic FC(Radial)	35	330	0.068	1050	10 × 16	1	1	EEUFC1V331 (V_I < 30 V)
FK (SMD)	50	330	0.12	900	12,5 × 13,5	1 (1)	1	EEVFK1H331Q
United Chemi-Con PXA (SMD)	16	330	0.014	4360	10 × 12,2	1 (1)	≤1	PXA16VC331MJ12TP (V_I < 14 V)
PS	16	330	0.014	5500	10 × 12,5	1 (1)	≤ 1	16PS330M J12 (V_I < 14 V)
LXZ	35	220	0.090	760	10 × 12,5	1(1)	2	LXZ35VB221M10X12LL (V_I < 30 V)
MVZ(SMD)	25	470	0.09	670	10 × 10	1	1	MVZ25VC471MJ10TP (V_I < 24 V) (V_O ≤ 5.5 V)
Nichicon UWG (SMD)	35	330	0.15	670	10 × 10	1	1	UWG1V331MNR1GS
SP	20	180	0.032	4280	10 ×10.5	2 (1)	≤ 2	20SP180M (V_I ~V_O ≤ 16 V)
Sanyo Os-Con SVP (SMD)	16	330	0.020	4700	10 × 12,7	1 (1)	≤ 1	16SVP330M (V_I ≤ 14 V)
SP	20	180	0.032	4280	10 ×10.5	2 (1)	≤ 2	20SP180M (V_I ≤ 16 V)
AVX Tantalum TPS (SMD)	20	100	0.085	1543	7,3 L × 4,3 W × 4,1 H	N/R (2)	≤ 3	TPSV107M020R0085 (V_O ≤ 10 V)
	20	100	0.200	> 817	3225	N/R (2)	≤ 3	TPSE107M020R0200 (V_O ≤ 10 V)

(1) The voltage rating of the input capacitor must be selected for the desired operating input voltage range of the regulator. To operate the regulator at a higher input voltage, select a capacitor with the next higher voltage rating.
(2) Not recommended (N/R). The voltage rating does not meet the minimum operating limits in most applications.

Table 5. Recommended Input/Output Capacitors (PTN78020W) (continued)

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE (µF)	EQUIVALENT SERIES RESISTANCE (ESR) (Ω)	85°C MAXIMUM RIPPLE CURRENT (mArms)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
Kemet X5R Ceramic	6.3	47	0.002	>1000	3225	N/R (3)	≤ 4	C1210C476K9PAC (V_O ≤ 5.5 V)
TDK X5R Ceramic	6.3	47	0.002	>1000	3225	N/R (3)	≤ 4	C3225X5R0J476MT (V_O ≤ 5.5 V)
Murata X5R Ceramic	6.3	47	0.002	>1000	3225	N/R (3)	≤ 4	GRM42-2X5R476M6.3 (V_O ≤ 5.5 V)
Murata X7R Ceramic	50	4.7	0.002	>1000	3225	≥ 1	1	GRM32ER71H475KA88L
TDK X7R Ceramic	50	2.2	0.002	>1000	3225	≥ 1	1	C3225X7R1H225KT
TDK X7R Ceramic	25	2.2	0.002	>1000	3225	≥ 1 (4)	1	C3225X7R1E225KT/MT (V_I~V_O ≤ 20 V)
Kemet X7R Ceramic	25	2.2	0.002	>1000	3225	≥ 1 (4)	1	C1210C225K3RAC (V_O ≤ 20 V)
AVX X7R Ceramic	25	2.2	0.002	>1000	3225	≥ 1 (4)	1	C12103C225KAT2A (V_O ≤ 20 V)
TDK X7R Ceramic	50	1.0	0.002	>1000	3225	≥ 2 (5)	1	C3225X7R1H105KT
Kemet X7R Ceramic	50	1.0	0.002	>1000	3225	≥ 2 (5)	1	C1210C105K5RAC
Kemet Radial Through-hole	50	1.0	0.002	>1000	5,08 × 7,62 × 9,14 H	≥ 2 (5)	1	C330C105K5R5CA
Murata Radial Through-hole	50	2.2	0.004	>1000	10 H × 10 W × 4 D	≥ 1	1	RPER71H2R2KK6F03

(3) The voltage rating of the input capacitor must be selected for the desired operating input voltage range of the regulator. To operate the regulator at a higher input voltage, select a capacitor with the next higher voltage rating.
(4) The maximum rating of the ceramic capacitor limits the regulator operating input voltage to 20 V. Select a alternative ceramic component to operate at a higher input voltage.
(5) A total capacitance of 2 µF is an acceptable replacement value for a single 2.2-µF ceramic capacitor

Table 6. Recommended Input/Output Capacitors (PTN78020H)

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE (µF)	EQUIVALENT SERIES RESISTANCE (ESR) (Ω)	85°C MAXIMUM RIPPLE CURRENT (mArms)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
Panasonic FC(Radial)	35	330	0.068	1050	10 × 16	1	1	EEUFC1V331 (V_I < 30 V)
FK (SMD)	50	330	0.12	900	12,5 × 13,5	1 (1)	1	EEVFK1H331Q
LXZ	35	220	0.09	760	10 × 12,5	1(1)	2	LXZ35VB2231M10X12LL (V_I < 30 V)
MVY(SMD)	35	220	0.15	670	10 × 10	1	2	MVY35VC221M10X10TP (V_I < 30 V)
Nichicon UWG (SMD)	35	330	0.15	670	10 × 10	1	1	UWG1V331MNR1GS (V_I < 30 V)
Sanyo Os-Con SP (SMD	20	180	0.032	4280	10 ×10.5	2 (1)	≤ 2	20SP180M (V_I~ V_O ≤ 16 V)
TDK X7R Ceramic	25	2.2	0.002	>1000	3225	≥ 8 (2)	1	C3225X7R1E225KT/MT (V_O ≤ 20 V)
Murata X7R Ceramic	25	2.2	0.002	>1000	3225	≥ 8 (2)	1	GRM32RR71E225K (V_O ≤ 20 V)
Kemet X7R Ceramic	25	2.2	0.002	>1000	3225	≥ 8 (2)	1	C1210C225K3RAC (V_O ≤ 20 V)
AVX X7R Ceramic	25	2.2	0.002	>1000	32225	≥ 8 (2)	1	C12103C225KAT2A (V_O ≤ 20 V)
Murata X7R Ceramic	50	4.7	0.002	>1000	3225	≥ 4	1	GRM32ER71H475KA88L
TDK X7R Ceramic	50	3.3	0.002	>1000	3225	≥ 6	1	CKG45NX7R1H335M
Murata Radial Through-hole	50	3.3	0.004	>1000	12,5 H x 12,5 W x 4 D	≥ 6	1	RPER71H3R3KK6F03
Kemet Radial Through-hole	50	4.7	0.002	>1000	5,08 × 7,62 × 9,14 H	≥ 4 (3)	1	C350C475K5R5CA

(1) The voltage rating of the input capacitor must be selected for the desired operating input voltage range of the regulator. To operate the regulator at a higher input voltage, select a capacitor with the next higher voltage rating.
(2) The maximum rating of the ceramic capacitor limits the regulator operating input voltage to 20 V. Select a alternative ceramic component to operate at a higher input voltage.
(3) A total capacitance of 2 µF is an acceptable replacement value for a single 2.2-µF ceramic capacitor

Output Voltage Sense

An external output voltage sense improves the load regulation performance of the module by enabling it to compensate for any IR-voltage drop between the module and the load circuit. This voltage drop is caused by the flow of current through the resistance in the printed-circuit board connections.

To use the output voltage sense feature, simply connect the V_O Sense input (pin 5) to V_O, close to the device that draws the most supply current. If an external voltage sense is not desired, the V_O Sense input may be left open circuit. An internal resistor (15 Ω or less), connected between this input and V_O, ensures that the output remains in regulation.

With V_O Sense connected, the difference between the voltage measured directly between the V_O and GND, and that measured from V_O Sense to GND, represents the amount of IR-voltage drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: *The external voltage sense is not designed to compensate for the forward drop of nonlinear or frequency-dependent components that may be placed in series with the regulator's output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the external sense connection, they are effectively placed inside the regulation control loop. This can adversely affect the stability of the module.*

Undervoltage Lockout

The undervoltage lockout (UVLO) circuit prevents the module from attempting to power up until the input voltage is above the UVLO threshold. This is to prevent the module from drawing excessive current from the input source at power up. Below the UVLO threshold, the module is held off.

Power-Up Characteristics

When configured per the standard application, the PTN78020 power module produces a regulated output voltage following the application of a valid input source voltage. During power up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay (typically 5 ms – 10 ms) into the power-up characteristic. This is from the point that a valid input source is recognized. Figure 26 shows the power-up waveforms for a PTN78020W, operating from a 12-V input and with the output voltage adjusted to 5 V. The waveforms were measured with a 1.5-A resistive load.

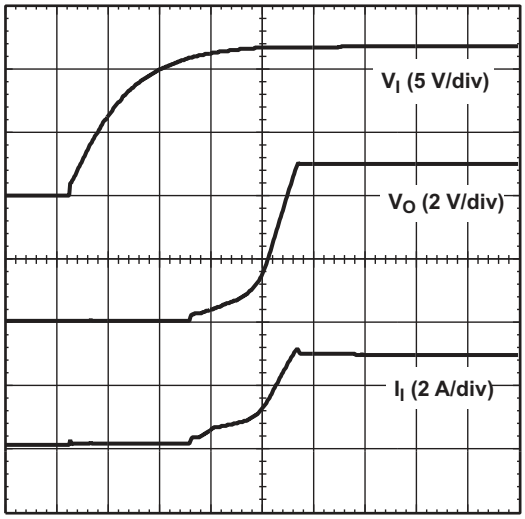


Figure 26. Power-Up Waveforms

Current-Limit Protection

The PTN78020 modules protect against load faults with a continuous current limit characteristic. Under a load fault condition, the output current cannot exceed the current limit value. Attempting to draw current that exceeds the current-limit value causes the module to progressively reduce its output voltage. Current is continuously supplied to the fault until it is removed. On removal of the fault, the output voltage promptly recovers. When limiting output current, the regulator experiences higher power dissipation, which increases its temperature. If the temperature increase is excessive, the module overtemperature protection begins to periodically turn the output voltage completely off.

Overtemperature Protection

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in temperature may be the result of a drop in airflow, a high ambient temperature, or a sustained current limit condition. If the junction temperature of the internal control IC rises excessively, the module turns itself off, reducing the output voltage to zero. The module instantly restarts when the sensed temperature decreases by a few degrees.

Overtemperature protection is a last resort mechanism to prevent damage to the module. It should not be relied on as permanent protection against thermal stress. Always operate the module within its temperature derated limits, for the worst-case operating conditions of output current, ambient temperature, and airflow. Operating the module above these limits, albeit below the thermal shutdown temperature, reduces the long-term reliability of the module.

Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTN78020 power module incorporates an output on/off Inhibit control (pin 3). The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power module functions normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND. Figure 27 shows the the circuit used to demonstrate the inhibit function. Note the discrete transistor (Q1). Turning Q1 on applies a low voltage to the *Inhibit* control pin and turns the module off. The output voltage decays as the load circuit discharges the capacitance. The current drawn at the input is reduced to typically 17 mA. If Q1 is then turned off, the module executes a soft-start power up. A regulated output voltage is produced within 20 ms. Figure 28 shows the typical rise in the output voltage, following the turn off of Q1. The turn off of Q1 corresponds to the fall in the waveform, Q1 Vgs. The waveforms were measured with a 1.5-A resistive load.

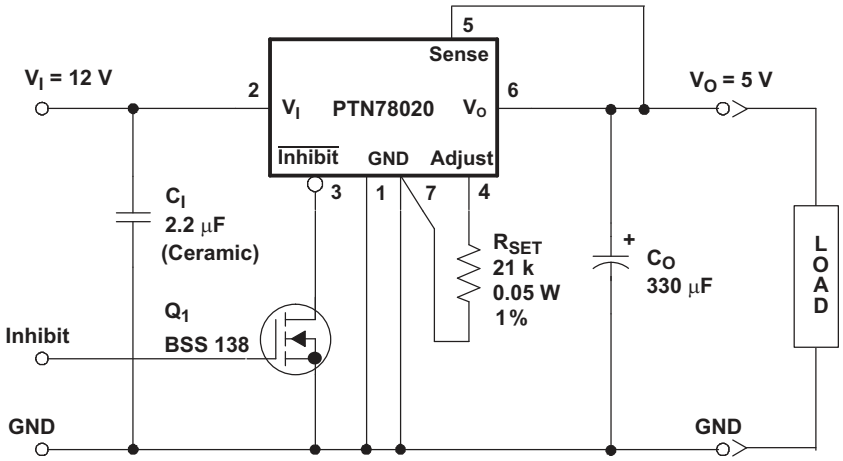


Figure 27. On/Off Inhibit Control Circuit

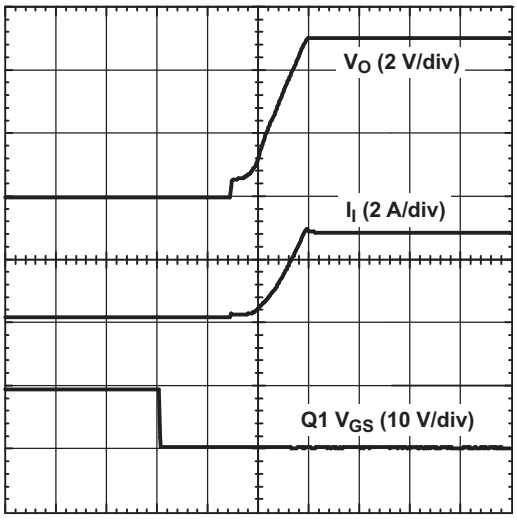


Figure 28. Power Up Response From Inhibit Control

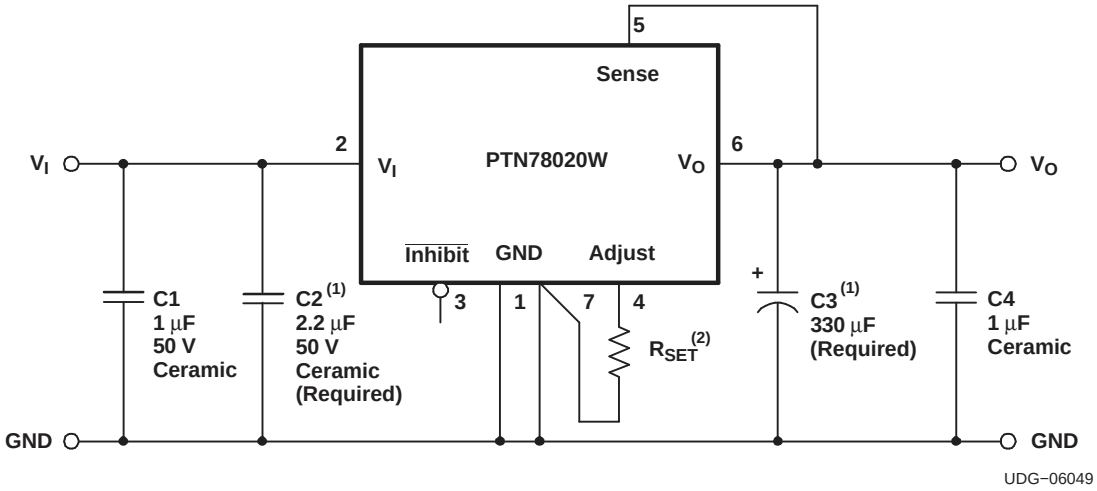
Optional Input/Output Filters

Power modules include internal input and output ceramic capacitors in all of their designs. However, some applications require much lower levels of either input reflected or output ripple/noise. This application describes various filters and design techniques found to be successful in reducing both input and output ripple/noise.

Input/Output Capacitors

The easiest way to reduce output ripple and noise is to add one or more 1-µF ceramic capacitors, such as C4 shown in Figure 29. Ceramic capacitors should be placed close to the output power terminals. A single 1-µF capacitor reduces the output ripple/noise by 10% to 30% for modules with a rated output current of less than 3 A. (Note: C3 is required to improve the regulator transient response, and does not reduce output ripple and noise.)

Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple/noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of C1, minimum 2.2-µF ceramic capacitor, near the input power pins, reduces reflected conducted ripple/noise by 30% to 50%.



(1) See the specifications for required value and type. For the PTN78020H, C2 = 4 × 4.7 µF.

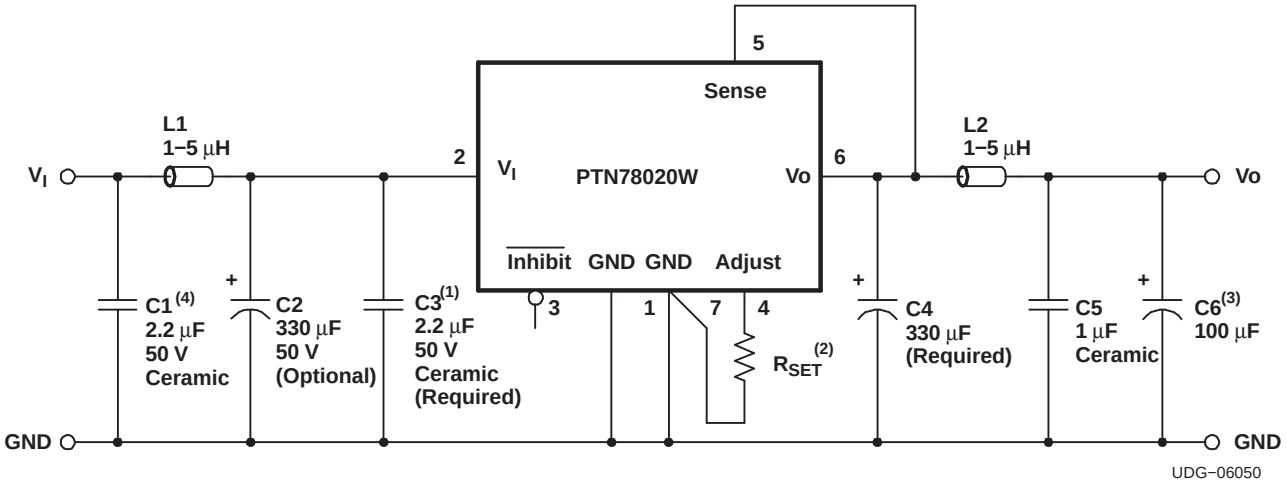
(2) See the *Application Information* section for suggeted value and type.

Figure 29. Adding High-Frequency Bypass Capacitors To The Input and Output

π Filters

If a further reduction in ripple/noise level is required for an application, higher order filters must be used. A π (pi) filter, employing a ferrite bead (Fair-Rite part number 2773021447 or equivalent) in series with the input or output terminals of the regulator reduces the ripple/noise by at least 20 db (see Figure 30 and Figure 31). In order for the inductor to be effective in reduction of ripple and noise, ceramic capacitors are required. (Note: see Capacitor Recommendations for the PTN78020W for addtional information on vendors and component suggestions.)

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency (650 kHz - 1 MHz). The placement of this filter is critical. It must be located as close as possible to the input or output pins to be efffective. The ferrite bead is small (12.5 mm × 3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite also manufactures a surface mount bead (part number 2773021447), through hole (part number 2673000701) rated to 5 A, but in this application, it is effective to 6 A on the output bus. 1-µH to 5-µH inductors can be used in place of the ferrite inductor bead.



(1) See the specifications for required value and type. For the PTN78020H, C3 = 4 × 4.7 µF.

(2) See the *Application Information* section for suggeted value and type.

(3) Recommended whenever I_O > 2A.

(4) For PTN78020H, C1 ≤ 4.7 µF.

Figure 30. Adding π Filters (I_O ≤ 3 A)

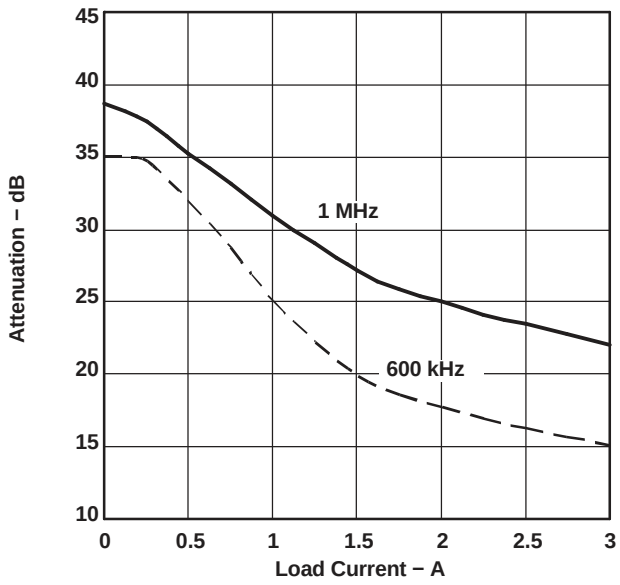
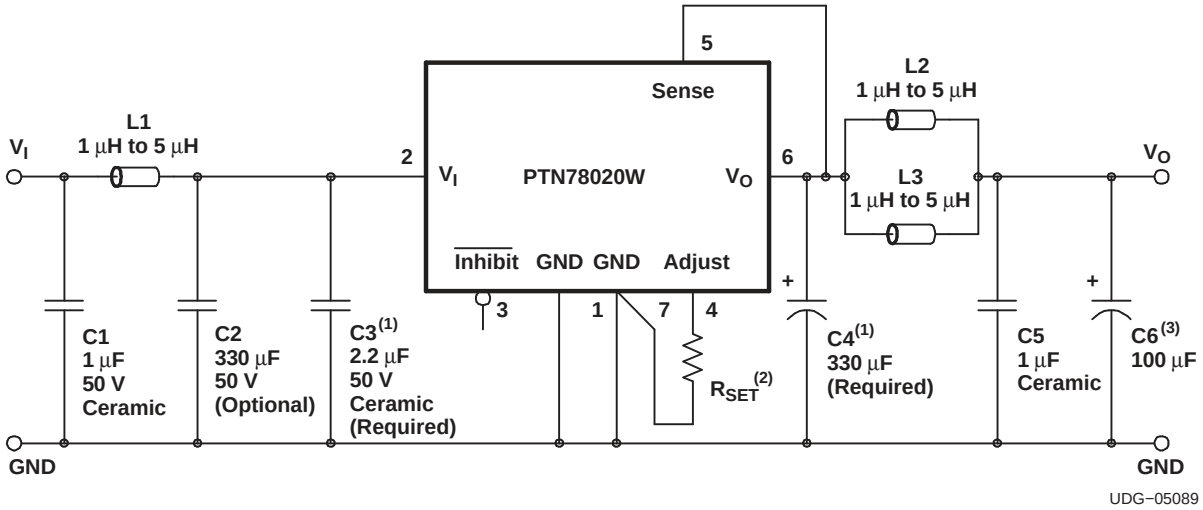


Figure 31. π-Filter Attenuation vs. Load Current



(1) See the specifications for required value and type. For the PTN78020H, C2 = 4 × 4.7 µF.

(2) See the *Application Information* section for suggeted value and type.

(3) Recommended whenever I_O > 2A.

(4) For PTN78020H, C1 ≥ 4.7 µF.

Figure 32. Adding π Filters (I_O = 3 A to 6 A)

REVISION HISTORY

Changes from Revision B (APRIL 2008) to Revision C	Page
• Added **Output Voltage Sense** section	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTN78020HAH	ACTIVE	Through-Hole Module	EUK	7	20	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		Samples
PTN78020HAS	ACTIVE	Surface Mount Module	EUL	7	20	TBD	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTN78020HAZ	ACTIVE	Surface Mount Module	EUL	7	20	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTN78020WAD	ACTIVE	Through-Hole Module	EUK	7	20	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		Samples
PTN78020WAH	ACTIVE	Through-Hole Module	EUK	7	20	Pb-Free (RoHS)	SN	N / A for Pkg Type	-40 to 85		Samples
PTN78020WAS	ACTIVE	Surface Mount Module	EUL	7	20	TBD	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTN78020WAZ	ACTIVE	Surface Mount Module	EUL	7	20	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTN78020WAZT	ACTIVE	Surface Mount Module	EUL	7	200	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

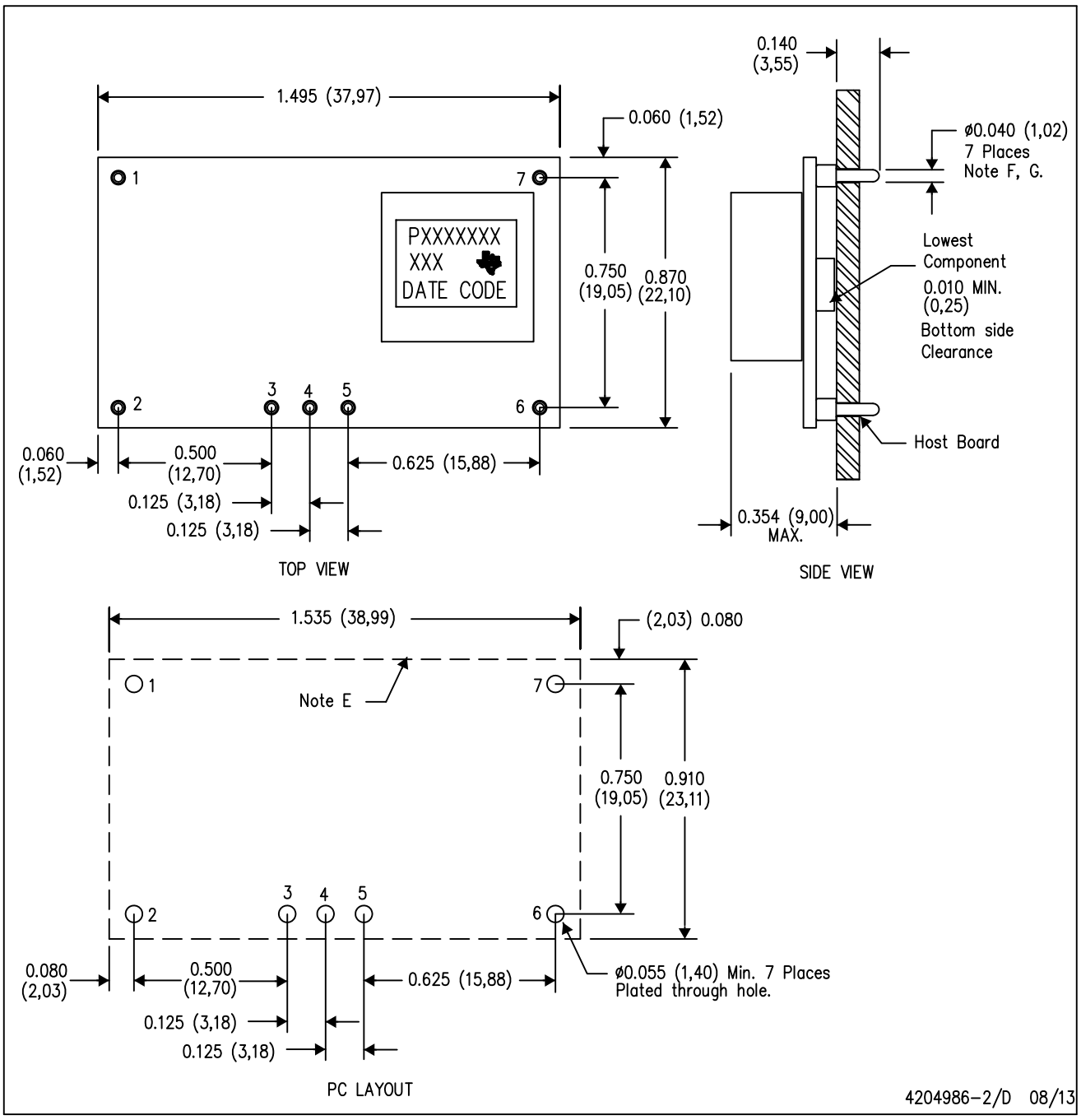
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

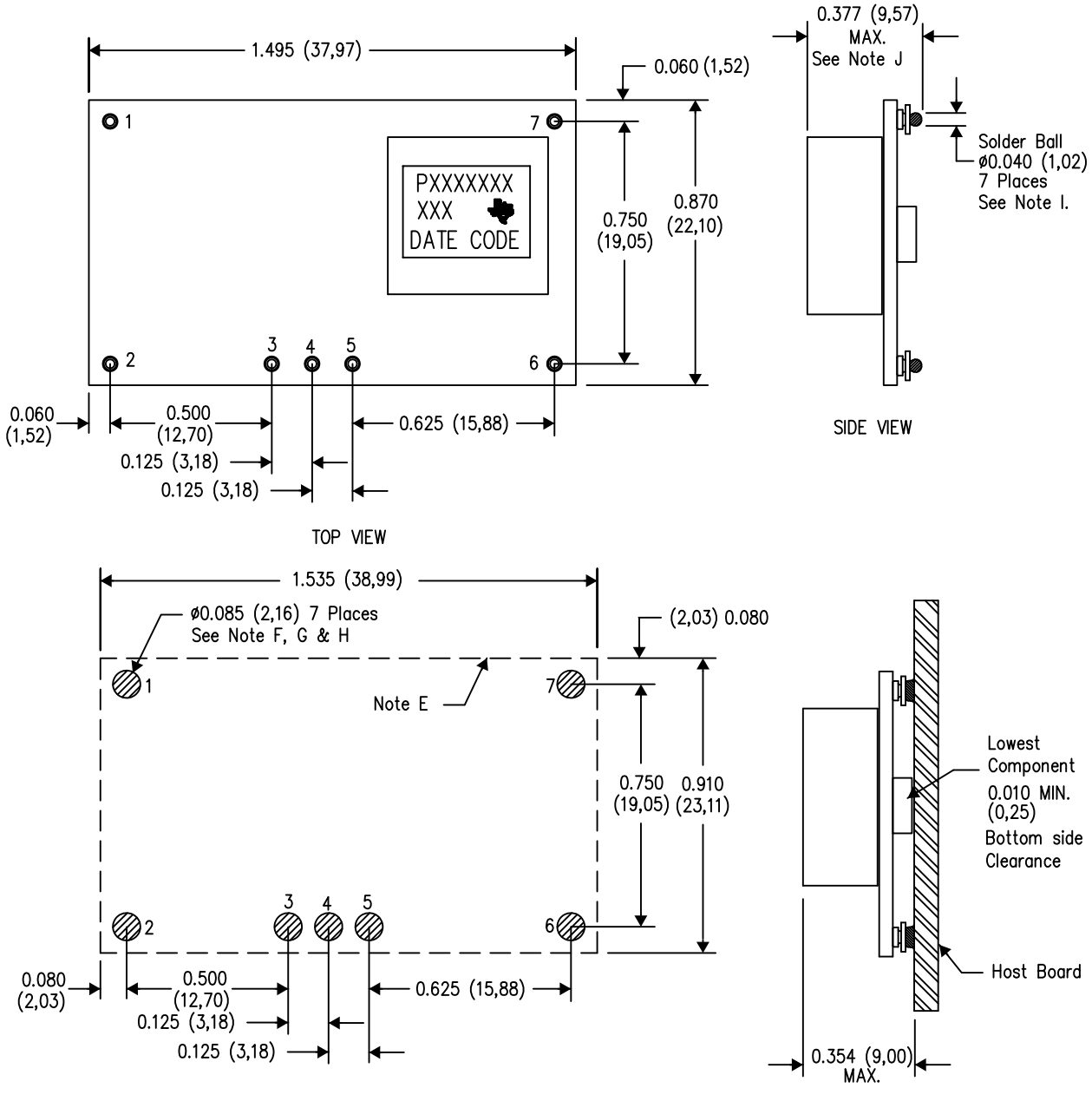
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

EUK (R–PDSS–T7) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
E. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
F. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EUL (R–PDSS–B7) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

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