CY7C1049BN

512K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **Low active power**
  - **— 1320 mW (max.)**
- **Low CMOS standby power (Commercial L version)**
  - **— 2.75 mW (max.)**
- **2.0V Data Retention (400 μW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**

Functional Description[1]

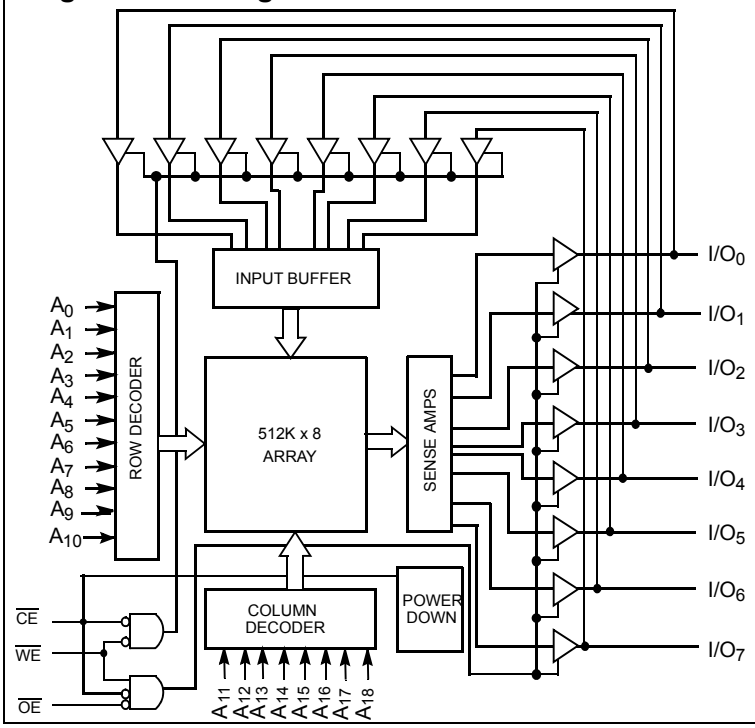
The CY7C1049BN is a high-performance CMOS static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

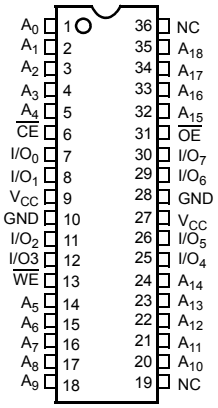
The CY7C1049BN is available in a standard 400-mil-wide 36-pin SOJ package with center power and ground (revolutionary) pinout.

Logic Block Diagram



Pin Configuration

SOJ
Top View



Selection Guide

			7C1049BN-12	7C1049BN-15	7C1049BN-17	7C1049BN-20	7C1049BN-25
Maximum Access Time (ns)			12	15	17	20	25
Maximum Operating Current (mA)			240	220	195	185	180
Maximum CMOS Standby Current (mA)	Com'l		8	8	8	8	8
	Com'l/Ind'l	L	-	-	0.5	0.5	0.5
	Ind'l		-	-	-	9	9

Note:
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	4.5V–5.5V
Industrial	–40°C to +85°C	

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			7C1049B-12		7C1049B-15		7C1049B-17		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA			2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage[2]				–0.3	0.8	–0.3	0.8	–0.3	0.3	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled			–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. f = f_{MAX} = $1/t_{RC}$				240		220		195	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				40		40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l			8		8		8	mA
			Com'l	L		-		-		0.5	mA
			Ind'l			-		-		8	mA
			Ind'l	L		-		-		0.5	mA

Note:
2. Minimum voltage is–2.0V for pulse durations of less than 20 ns.

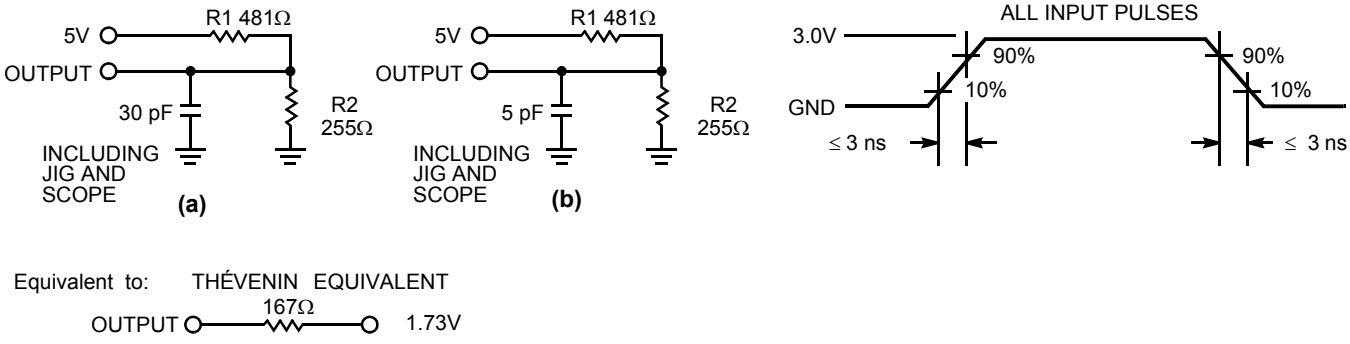
Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions			7C1049B-20 Min.	7C1049B-20 Max.	7C1049B-25 Min.	7C1049B-25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]				–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled			–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$				185		180	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}				40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l			8		8	mA
			Com'l	L		0.5		0.5	mA
			Ind'l			8		8	mA
			Ind'l	L		0.5		0.5	mA

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	I/O Capacitance		8	pF

AC Test Loads and Waveforms



Note:
3. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics[4] Over the Operating Range

Parameter	Description	7C1049B-12		7C1049B-15		7C1049B-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{power}	V_{CC}(typical) to the First Access[5]	1		1		1		ms
t_{RC}	Read Cycle Time	12		15		17		ns
t_{AA}	Address to Data Valid		12		15		17	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		17	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		6		7		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		6		7		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		17	ns
Write Cycle[8, 9]								
t_{WC}	Write Cycle Time	12		15		17		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		12		ns
t_{AW}	Address Set-Up to Write End	10		12		12		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		12		ns
t_{SD}	Data Set-Up to Write End	7		8		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		6		7		8	ns

Notes:

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. t_{power} time has to be provided initially before a read/write operation is started.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics[4] Over the Operating Range (continued)

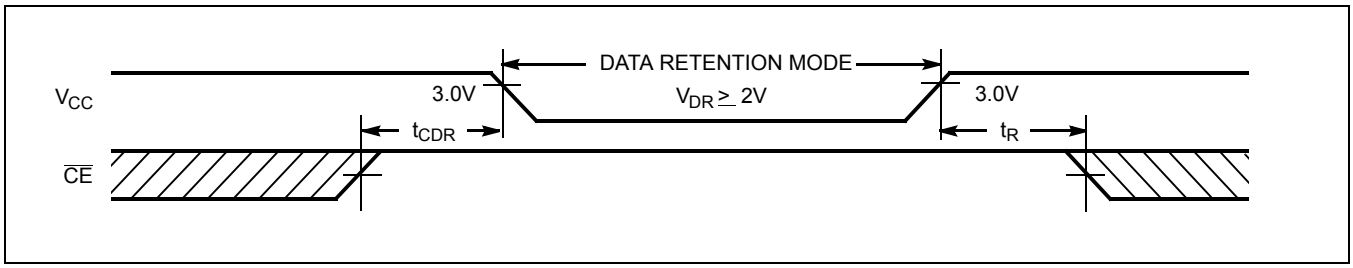
Parameter	Description	7C1049B-20		7C1049B-25		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{power}	V_{CC}(typical) to the First Access[5]	1		1		1
t_{RC}	Read Cycle Time	20		25		ns
t_{AA}	Address to Data Valid		20		25	ns
t_{OHA}	Data Hold from Address Change	3		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		25	ns
Write Cycle[8]						
t_{WC}	Write Cycle Time	20		25		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	13		15		ns
t_{AW}	Address Set-Up to Write End	13		15		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	13		15		ns
t_{SD}	Data Set-Up to Write End	9		10		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		8		10	ns

Data Retention Characteristics Over the Operating Range

Parameter	Description			Conditions[11]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention				2.0		V
I_{CCDR}	Data Retention Current	Com'l	L	$\overline{V_{CC}} = V_{DR} = 3.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		200	µA
		Ind'l				1	mA
t_{CDR}[3]	Chip Deselect to Data Retention Time				0		ns
t_R[10]	Operation Recovery Time				t_{RC}		ns

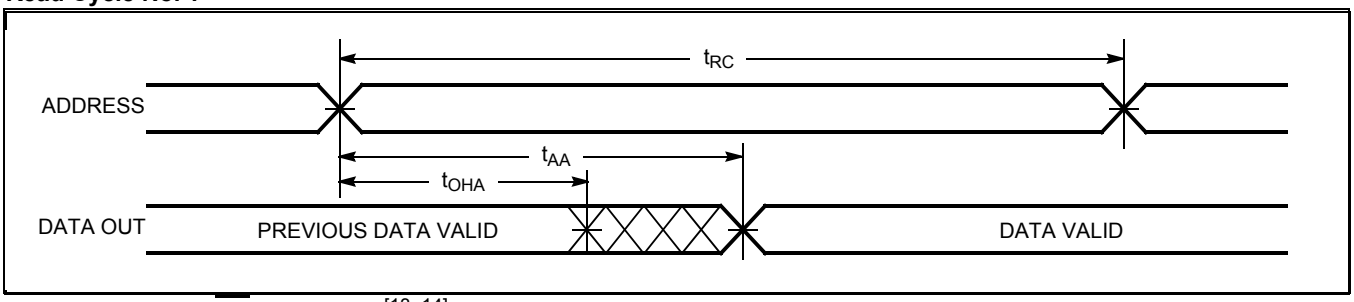
Notes:
10. $t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 and slower speeds.
11. No input may exceed V_{CC} + 0.5V.

Data Retention Waveform

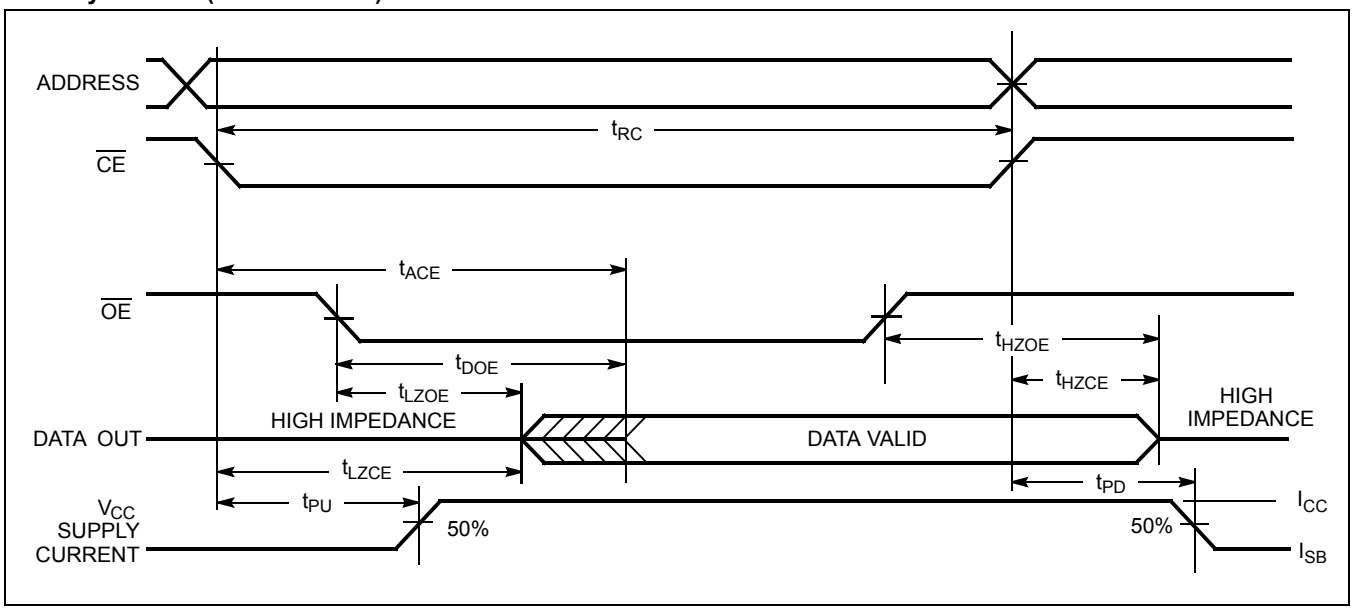


Switching Waveforms

Read Cycle No. 1[12, 13]



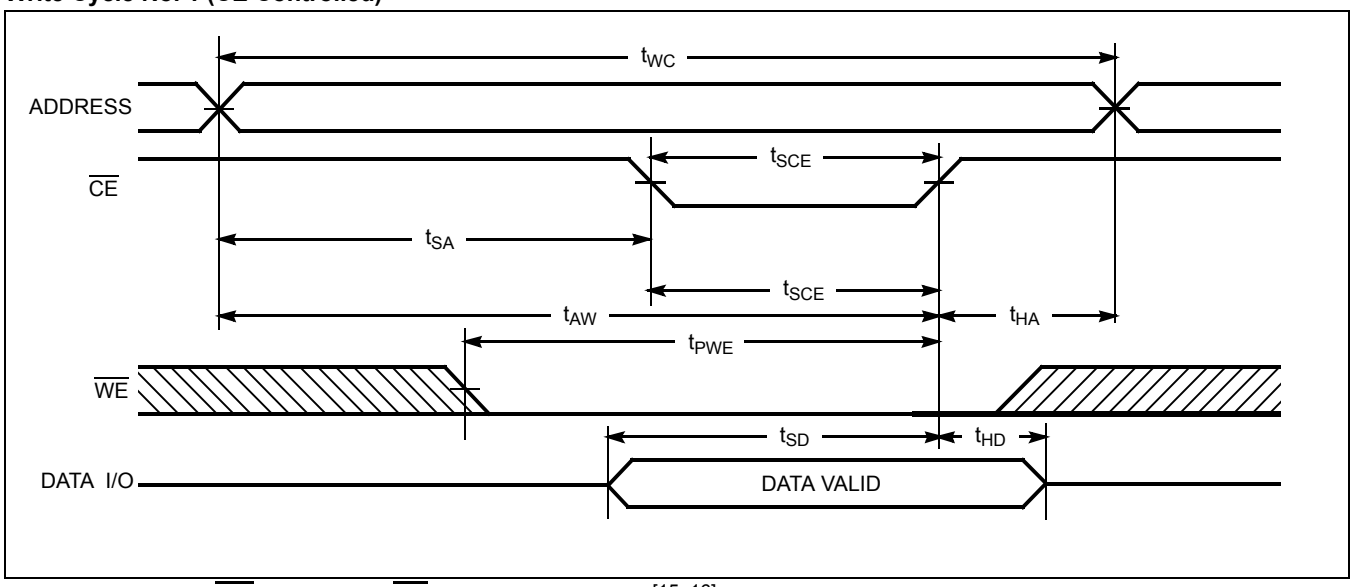
Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



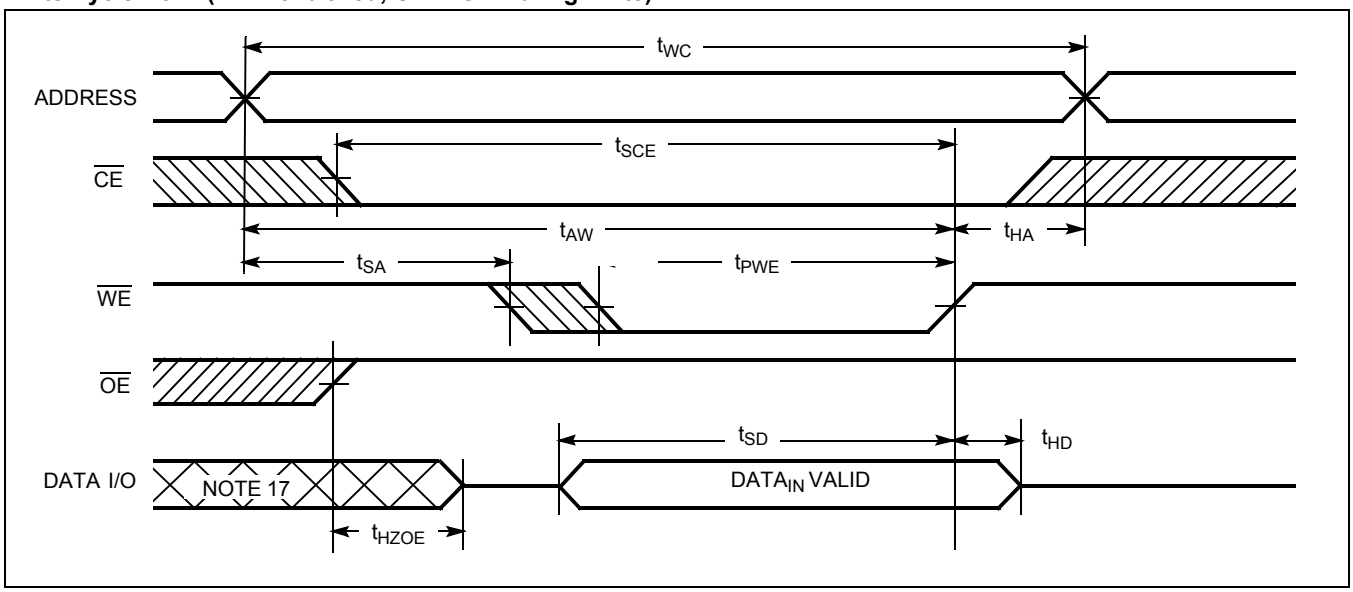
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[15, 16]



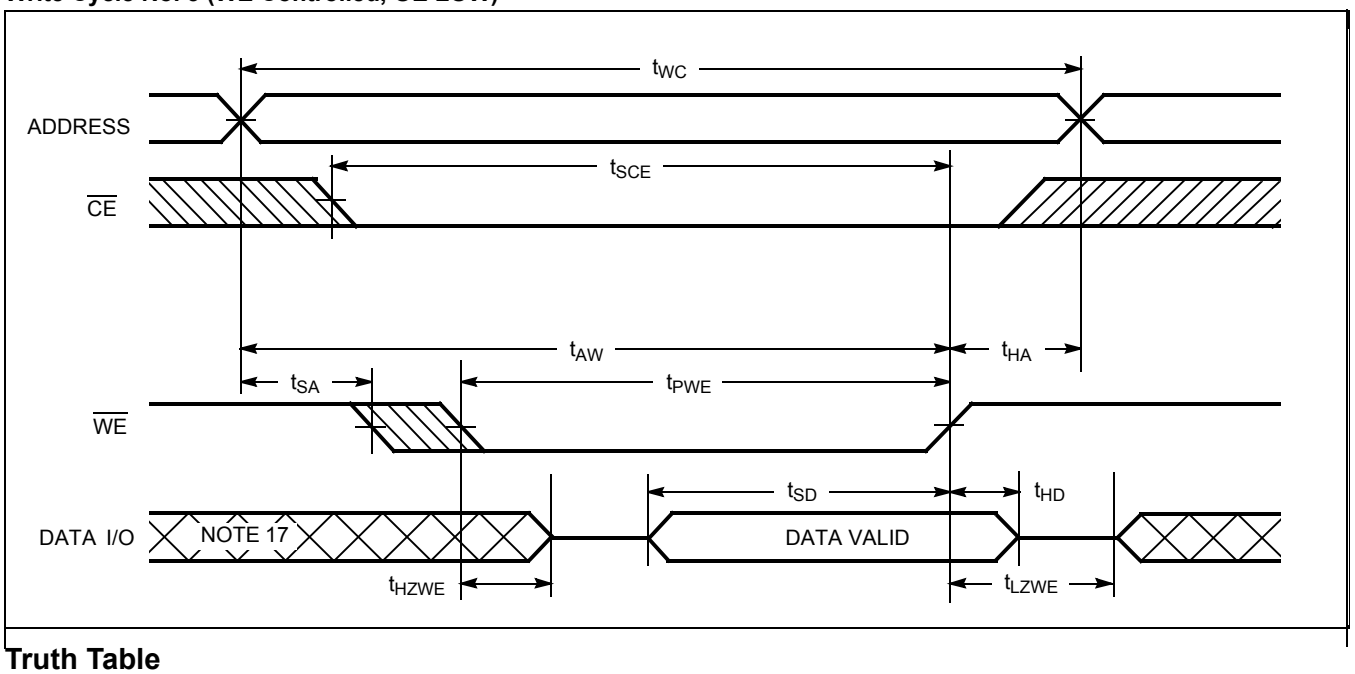
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]



Notes:
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
17. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Power-down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Output disabled	Active (I_{CC})

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available.For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.

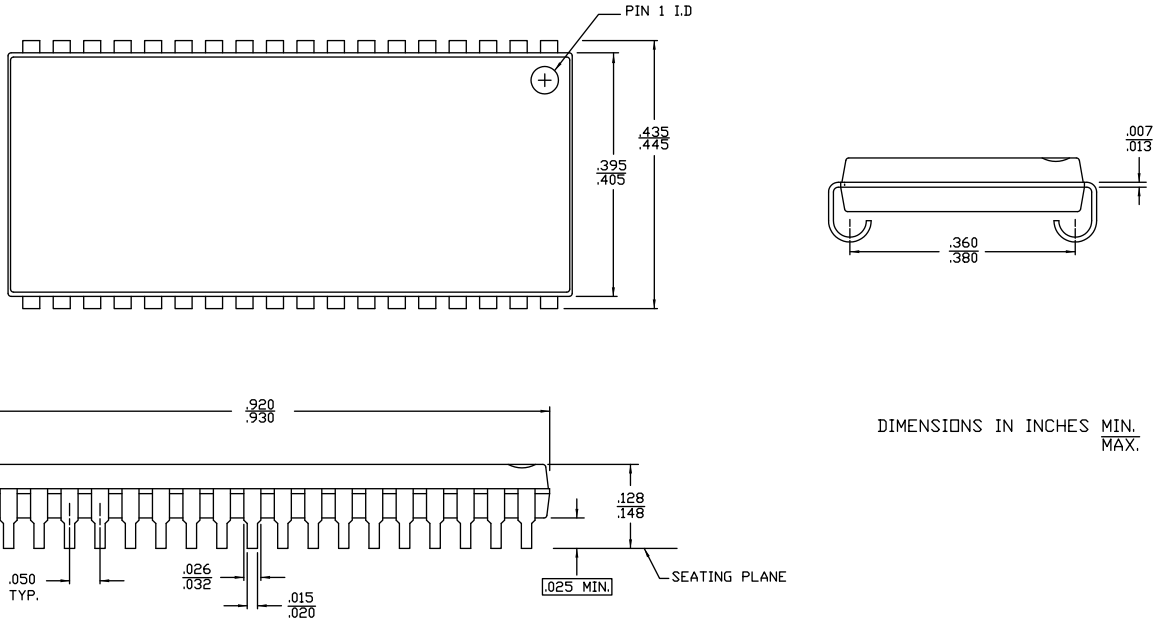
Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1049BN-15VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	Industrial

Please contact local sales representative regarding availability of these parts.

Package Diagram

36 Lead (400 MIL) Molded SOJ V36



51-85090 *D

Document History Page

Document Title: CY7C1049BN 512K x 8 Static RAM Document Number: 001-06501				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	424111	See ECN	NXR	New Data Sheet
*A	2897141	03/22/10	AJU/VKN	Removed inactive parts from the ordering information table. Updated package diagram.