

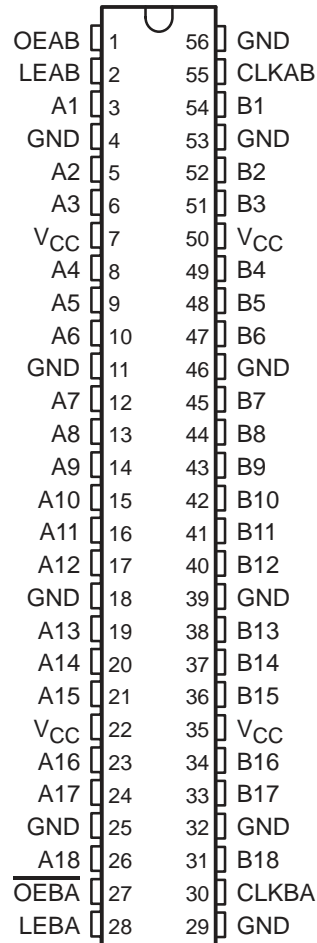
SN74ALVCH16501

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES024C – JULY 1995 – REVISED FEBRUARY 1999

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **UBT™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

**DGG OR DL PACKAGE
(TOP VIEW)**



description

This 18-bit universal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When \overline{OEAB} is high, the outputs are active. When \overline{OEAB} is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , LEBA, and CLKBA. The output enables are complementary (\overline{OEAB} is active high and \overline{OEBA} is active low).

To ensure the high-impedance state during power up or power down, \overline{OEBA} should be tied to V_{CC} through a pullup resistor and \overline{OEAB} should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH16501 is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC, UBT, and Widebus are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

SN74ALVCH16501 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES024C – JULY 1995 – REVISED FEBRUARY 1999

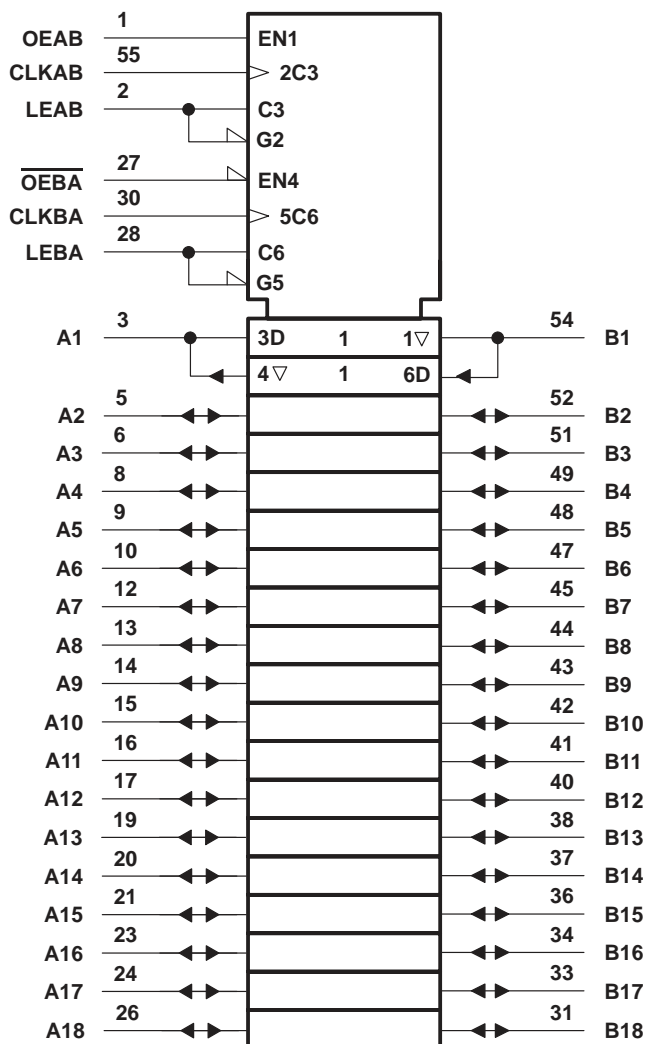
FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L or H	X	B ₀ ‡

† A-to-B data flow is shown; B-to-A flow is similar, but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB is high before LEAB goes low

logic symbols§

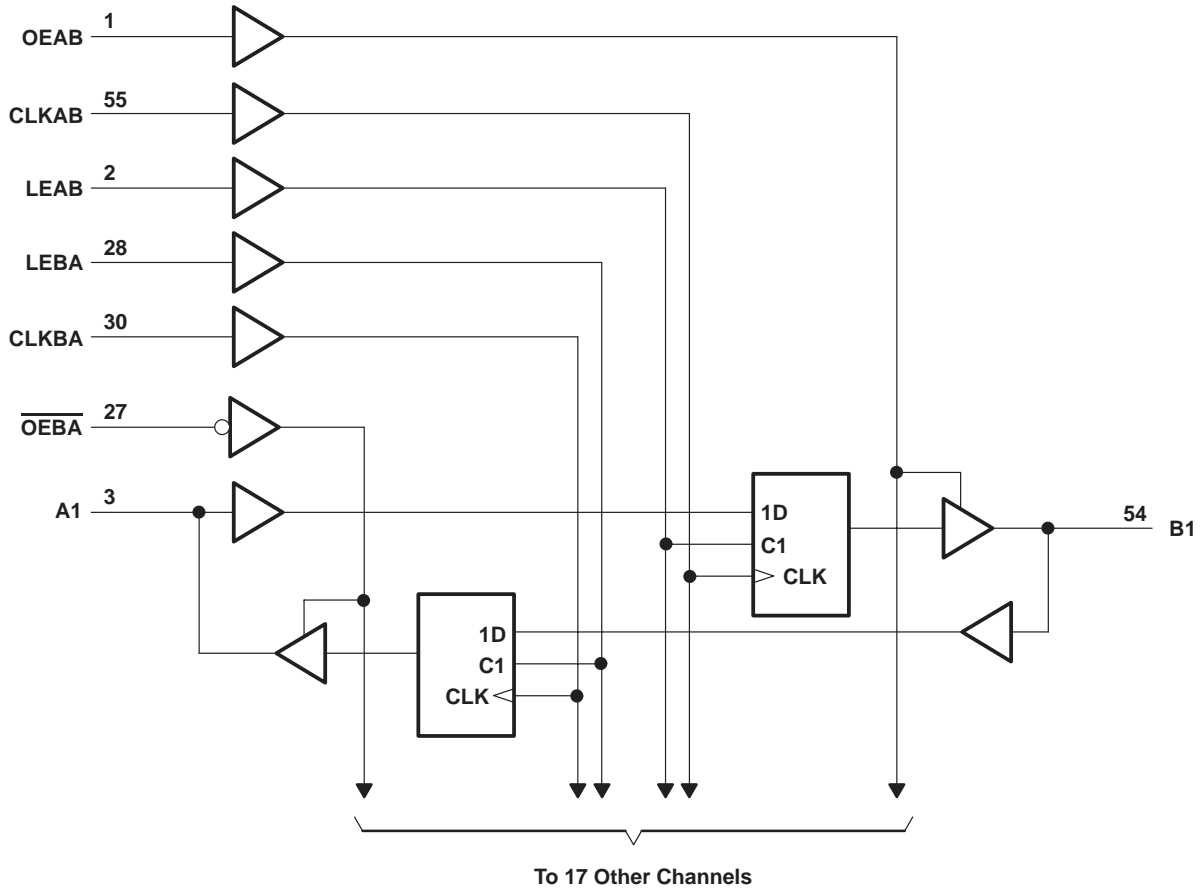


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN74ALVCH16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES024C – JULY 1995 – REVISED FEBRUARY 1999

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	-0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through each V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.



SN74ALVCH16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES024C – JULY 1995 – REVISED FEBRUARY 1999

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	1.7	
		V _{CC} = 2.7 V to 3.6 V	2	
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	0.7	
		V _{CC} = 2.7 V to 3.6 V	0.8	
V _I	Input voltage	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V	-4	mA
		V _{CC} = 2.3 V	-12	
		V _{CC} = 2.7 V	-12	
		V _{CC} = 3 V	-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4	mA
		V _{CC} = 2.3 V	12	
		V _{CC} = 2.7 V	12	
		V _{CC} = 3 V	24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T _A	Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74ALVCH16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES024C – JULY 1995 – REVISED FEBRUARY 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT	
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} -0.2			V	
	I _{OH} = -4 mA	1.65 V	1.2				
	I _{OH} = -6 mA	2.3 V	2				
	I _{OH} = -12 mA	2.3 V	1.7				
		2.7 V	2.2				
		3 V	2.4				
I _{OH} = -24 mA	3 V	2					
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V	0.2			V	
	I _{OL} = 4 mA	1.65 V	0.45				
	I _{OL} = 6 mA	2.3 V	0.4				
	I _{OL} = 12 mA	2.3 V	0.7				
		2.7 V	0.4				
	I _{OL} = 24 mA	3 V	0.55				
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA	
I _I (hold)	V _I = 0.58 V	1.65 V	25			μA	
	V _I = 1.07 V	1.65 V	-25				
	V _I = 0.7 V	2.3 V	45				
	V _I = 1.7 V	2.3 V	-45				
	V _I = 0.8 V	3 V	75				
	V _I = 2 V	3 V	-75				
	V _I = 0 to 3.6 V‡	3.6 V	±500				
I _{OZ} §	V _O = V _{CC} or GND	3.6 V	±10			μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	40			μA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V	750			μA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	4			pF
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	8			pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

		V _{CC} = 1.8 V		V _{CC} = 2.5 V ±0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ±0.3 V		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency	¶		150		150		150		MHz	
t _w	Pulse duration	LE high		¶		3.3		3.3		ns	
		CLK high or low		¶		3.3		3.3			
t _{su}	Setup time	Data before CLK↑		¶		2.2		2.1		ns	
		Data before LE↓	CLK high		¶		1.9		1.6		
			CLK low		¶		1.3		1.1		
t _h	Hold time	Data after CLK↑		¶		0.6		0.6		ns	
		Data after LE↓	CLK high or low		¶		1.4		1.7		

¶ This information was not available at the time of publication.



SN74ALVCH16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES024C – JULY 1995 – REVISED FEBRUARY 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		150		150		150		MHz
t _{pd}	A or B	B or A	†		1	4.8	4.5	1	3.9		ns
	LE	A or B	†		1.1	5.7	5.3	1.3	4.6		
	CLK		†		1.2	6.1	5.6	1.4	4.9		
t _{en}	OEAB	B	†		1	5.8	5.3	1	4.6	ns	
t _{dis}	OEAB	B	†		1.5	6.2	5.7	1.4	5	ns	
t _{en}	<u>OEBA</u>	A	†		1.3	6.3	6	1.1	5	ns	
t _{dis}	<u>OEBA</u>	A	†		1.3	5.3	4.6	1.3	4.2	ns	

† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

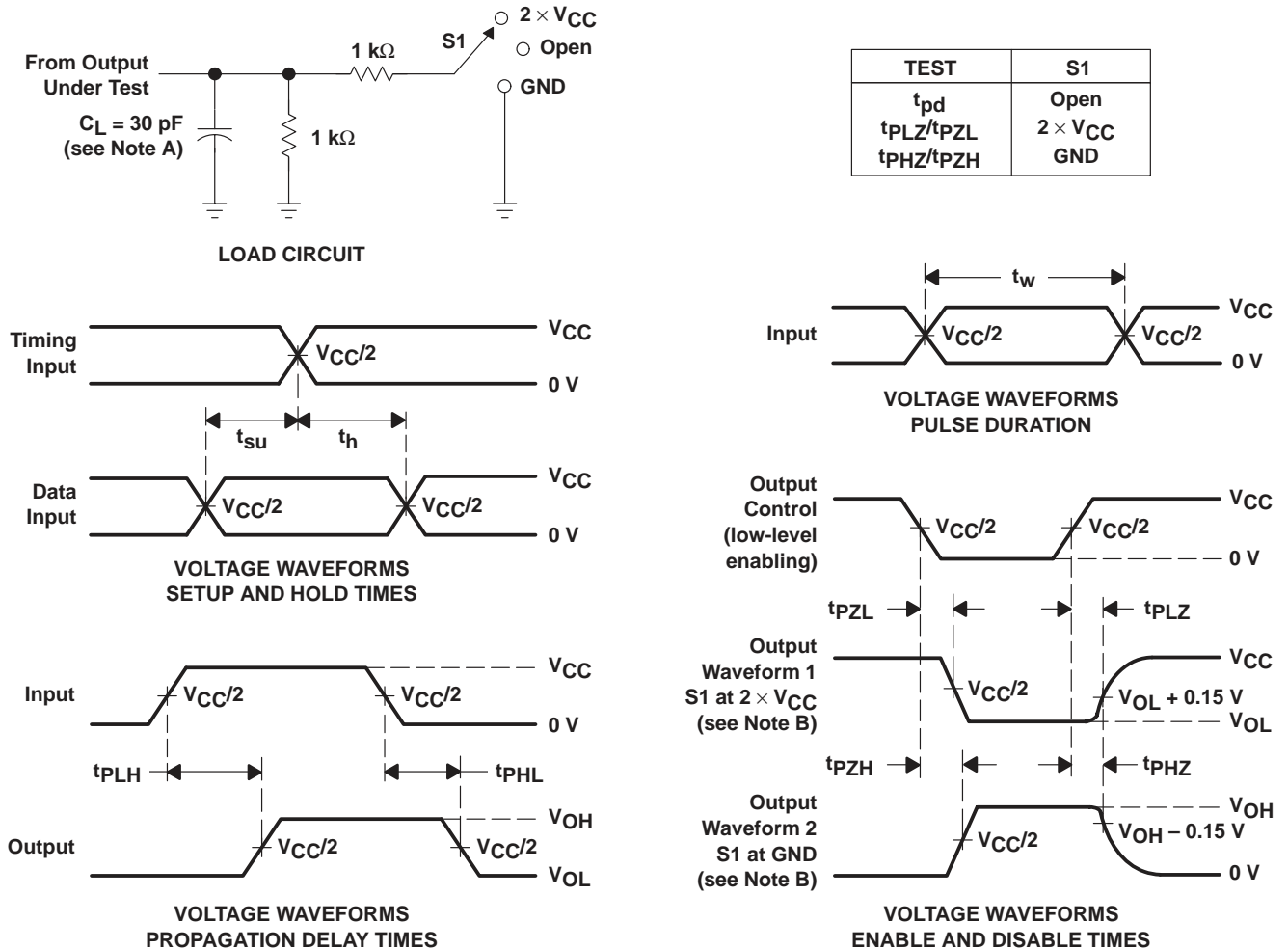
PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	Outputs enabled	†	44	54	pF
		Outputs disabled	†	6	6	

† This information was not available at the time of publication.



PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

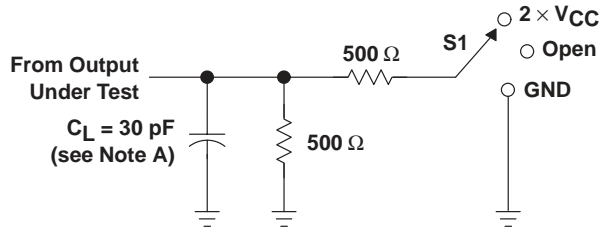
Figure 1. Load Circuit and Voltage Waveforms

SN74ALVCH16501
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

SCES024C – JULY 1995 – REVISED FEBRUARY 1999

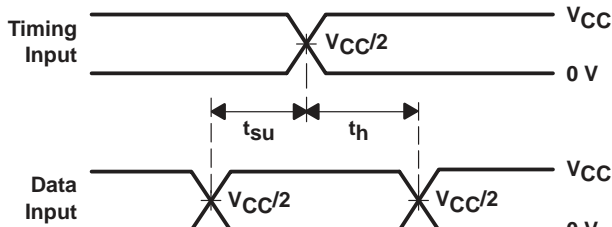
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 V \pm 0.2 V$

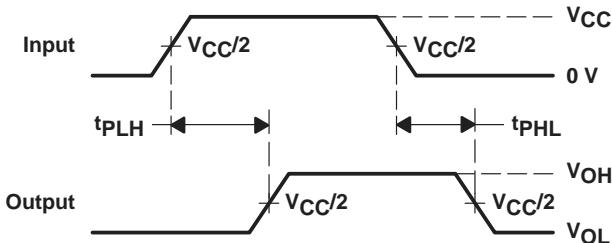


LOAD CIRCUIT

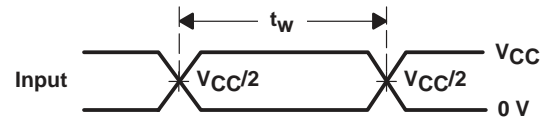
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	GND



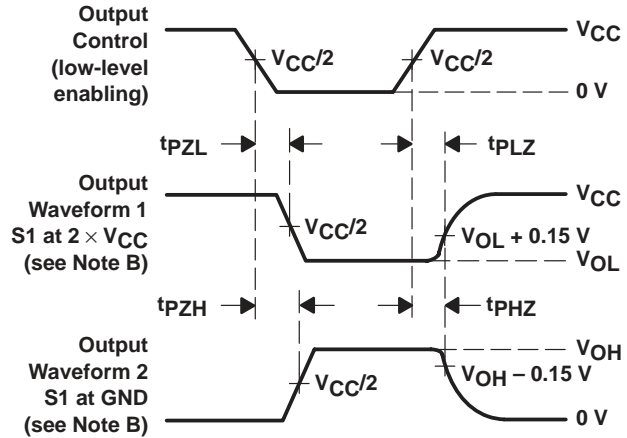
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**

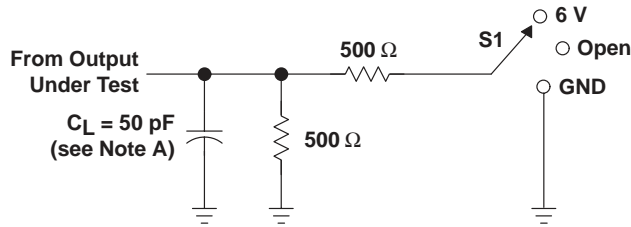


**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

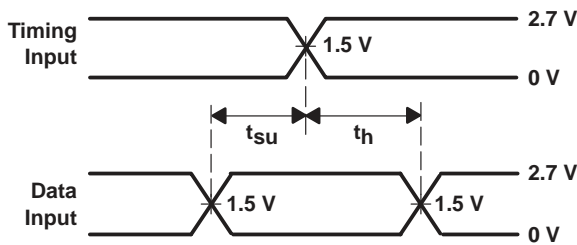
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
 $V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

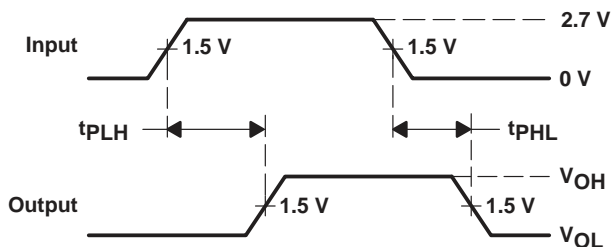


LOAD CIRCUIT

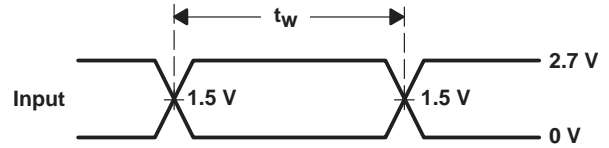
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



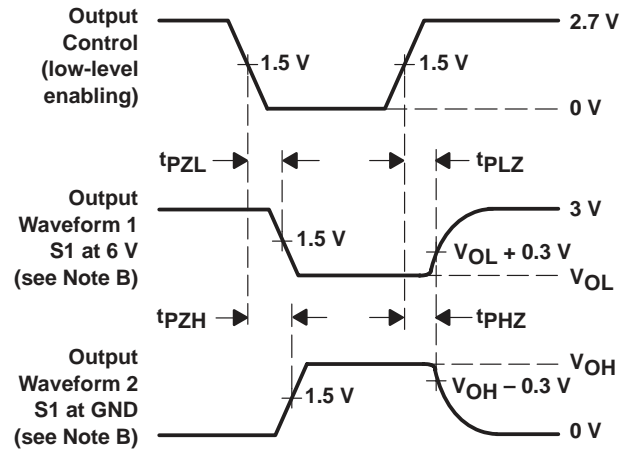
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.